WIB update, 01/16/2020

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WIB Meeting
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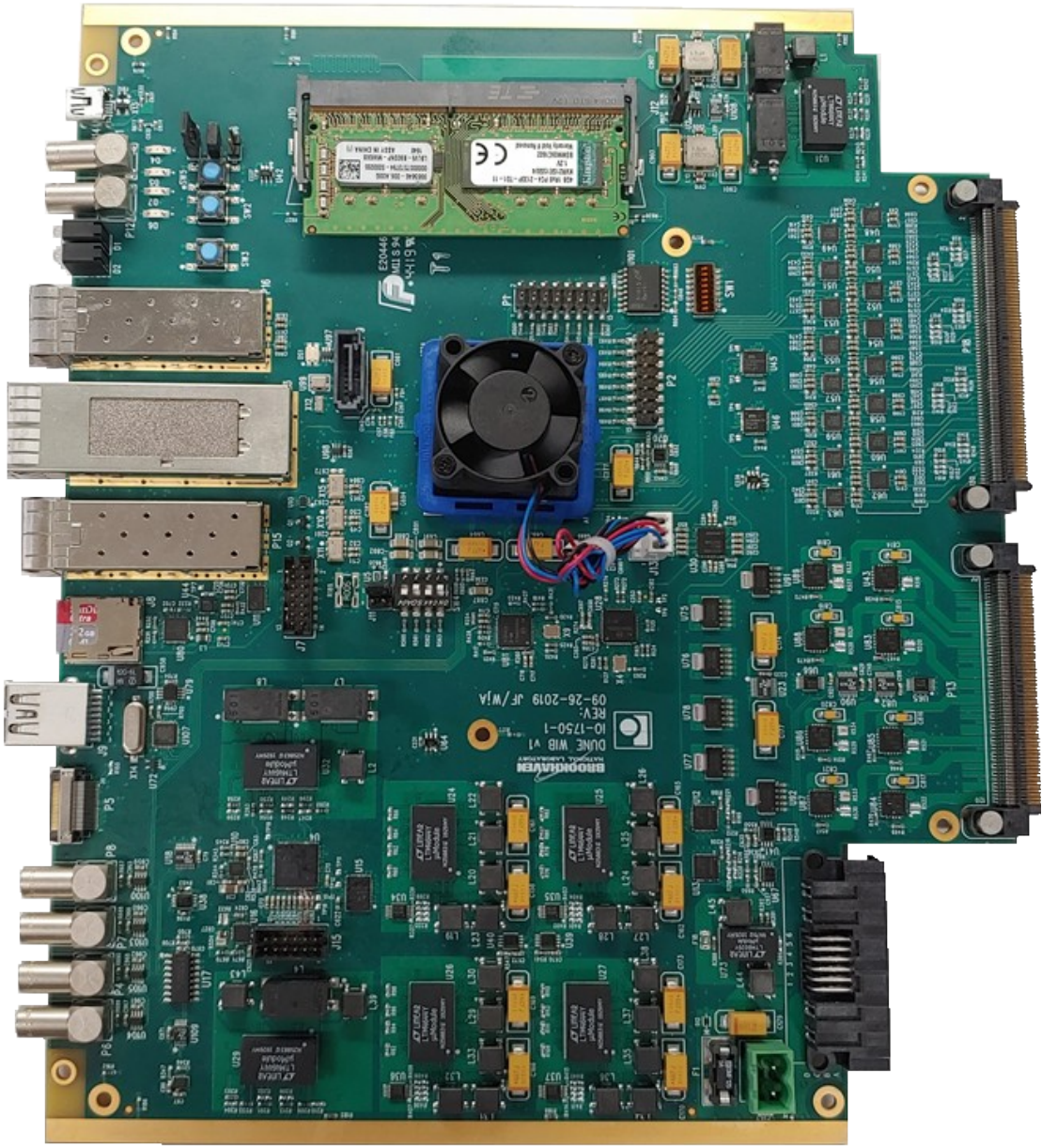
WIB Zynq Ultrascale+ Status

- WIB SocFPGA power management
  - Sequencing control --PASS/DONE
  - Fault management --PASS/DONE
  - Voltage output auto trim --PASS/DONE
- Zynq SocFPGA PL & PS configuration
  - JTAG --PASS/DONE
  - SD CARD --PASS/DONE
  - QSPI --PASS/DONE
- Zynq
  - Functional Testing & validation --PASS/DONE
- ZYNQ PS GIG-E sgmii interface
  - Functional Testing --PASS/DONE
- WIB FEMB communication
  - FEMB clock and data IO -- PASS/DONE
    - Functionality test
- WIB QSFP 10Gb DAQ link
  - Functional Testing & validation test -- PASS/DONE
- WIB FEMB power management
  - Functional Testing --in progress
- WIB timing system
  - SI5344 PLL --in progress
  - SI5342 PLL --in progress
  - Front panel auxiliary SFP port --not started
  - Bristol timing system AD2814 --not started
- WIB FEMB monitors
  - FEMB monitor ADC's --not started



Summary

- Two WIB boards have been assembled and tested.
- There are few remaining features that have not been tested. Testing of these features is ongoing.
- As of now, the WIB functions that are required to communicate with DAQ and FEMBs have been validated. Firmware development can now proceed.