Qpix Frontend Prototype *first* Technical Review

MITCH NEWCOMER PENN INSTRUMENTATION GROUP

Purpose

- Provide the community with a technical update.
- Review of techniques, approaches, methodologies, qualifications.
- Benefit from Expert Designer's suggestions & recommendations, tests.
- Learn from others about process behavior at LAr temperature.

Qpix ASIC design Team at Penn

Design Team:

Instrumentation Staff: Mitch Newcomer, Nandor Dressnandt and Paul Keener

MSEE's provide design help and primary source of development labor:

Seniors: Xinyi Tang, Archmishman Datta,

First Year: Xinyi Jiao, Weilun Li

Historically there has been some overlap in seniors and first year students over the Spring semester and to a lesser extent over the summer.

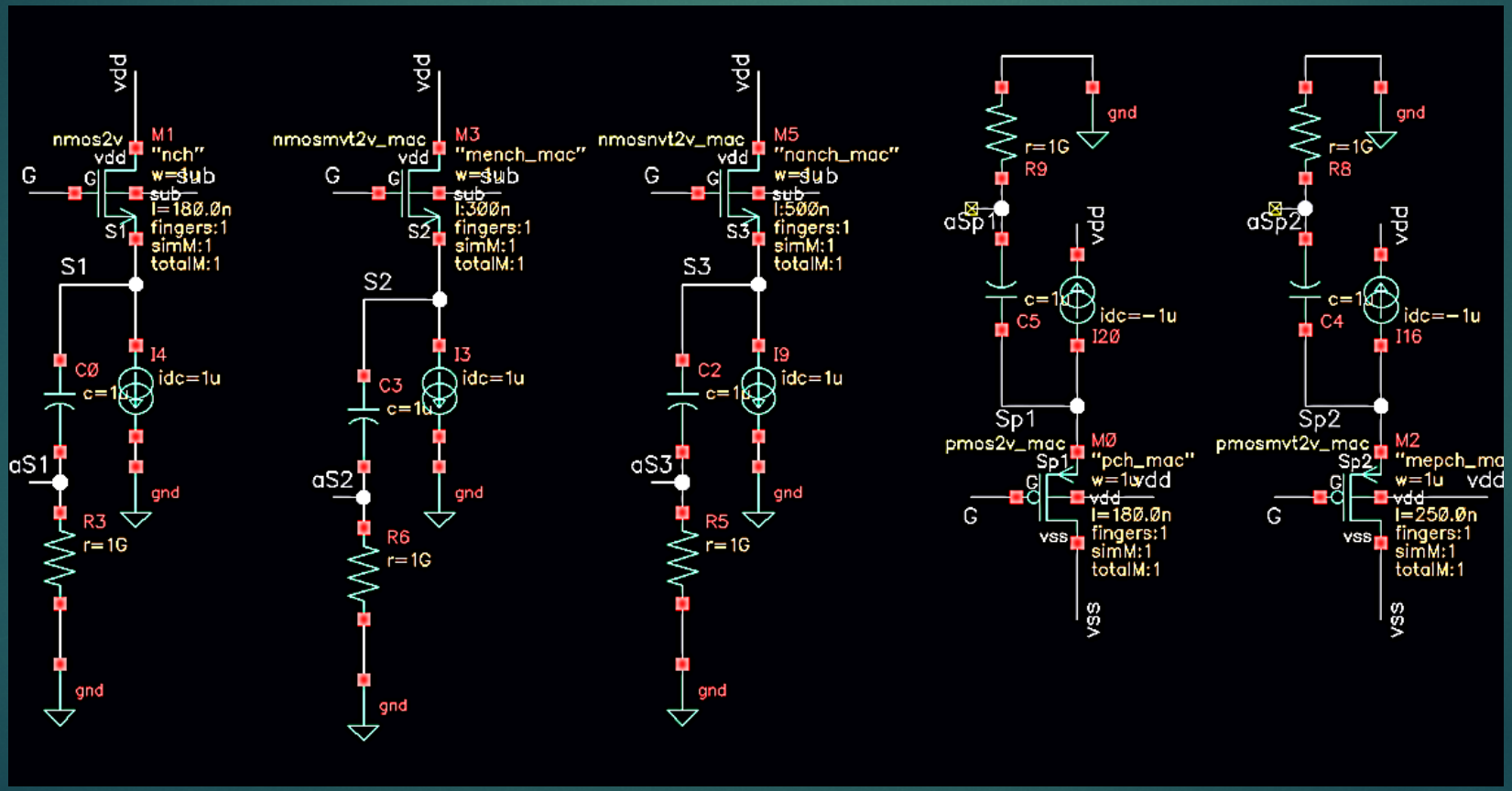
Process Choice 180nm 2v CMOS transistors

We have NO cold measurements or Cold Qualified Models but a wealth of community experience and transistor level studies suggests this choice.

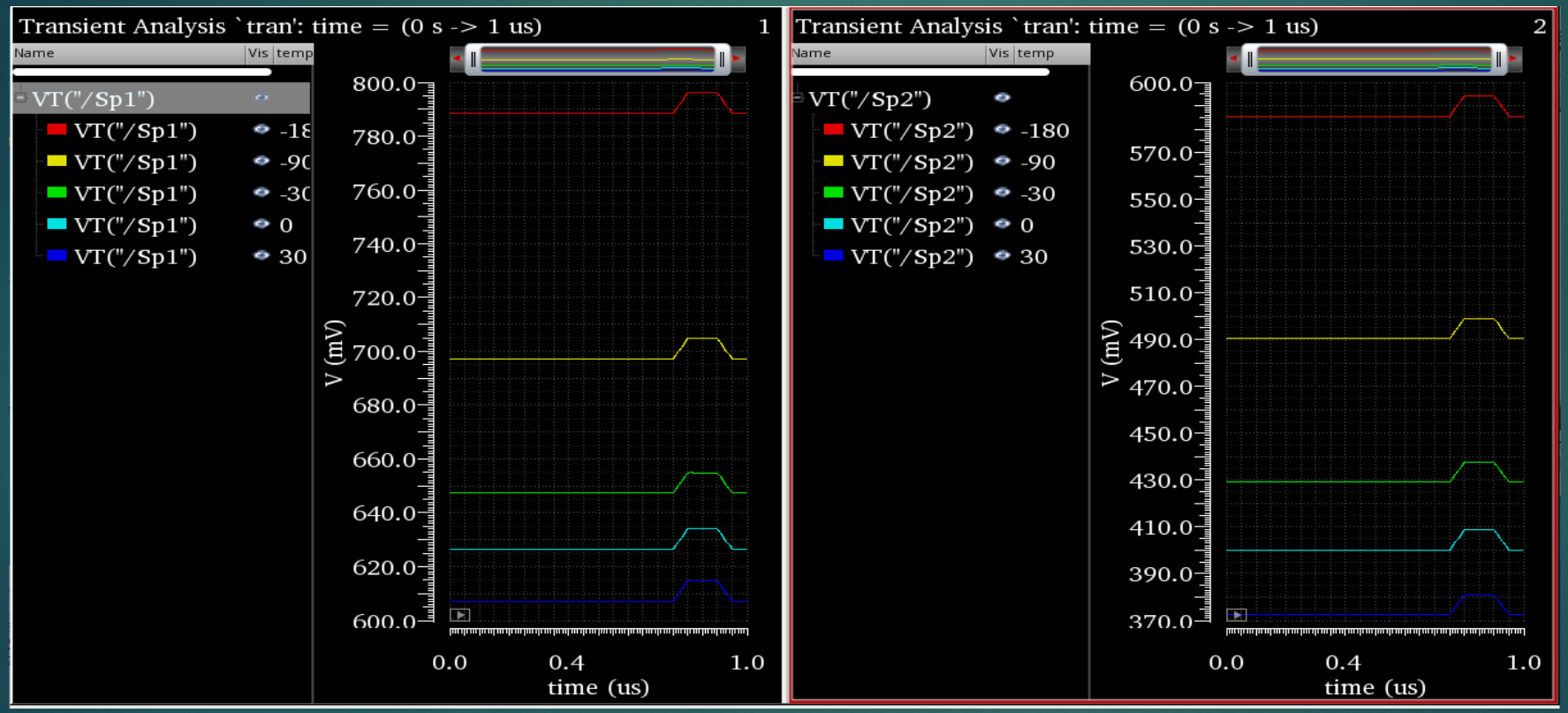
- Process Studies: Cold performance studies Veljko Radeka, Sharorui Li
- Silicon proven ASIC experience from:
  - Dan Dwyer's LAr Pix group (Carl Grace and Dario Gnani designers)
  - BNL FEASIC (Initial Design: Gianluigi, current Lead: Narasimha Manyam)
    - Nara Recently reported finding performance issues in previous design(s) using newly available BSIM 4 (4.5) models extrapolated to LA temperatures.
    - No gain change observed over 1 year of cold operation.

Process Studies: enhance design capability

- The choice of 180nm CMOS was recent. Access to the process PDK's was granted through IMEC and Europractice. Results using tt, BSIM 4.5 models
- Source Follower Vgs and gain at 1µA Min L & W = 1µm over temperature.



PMOS SF simulations

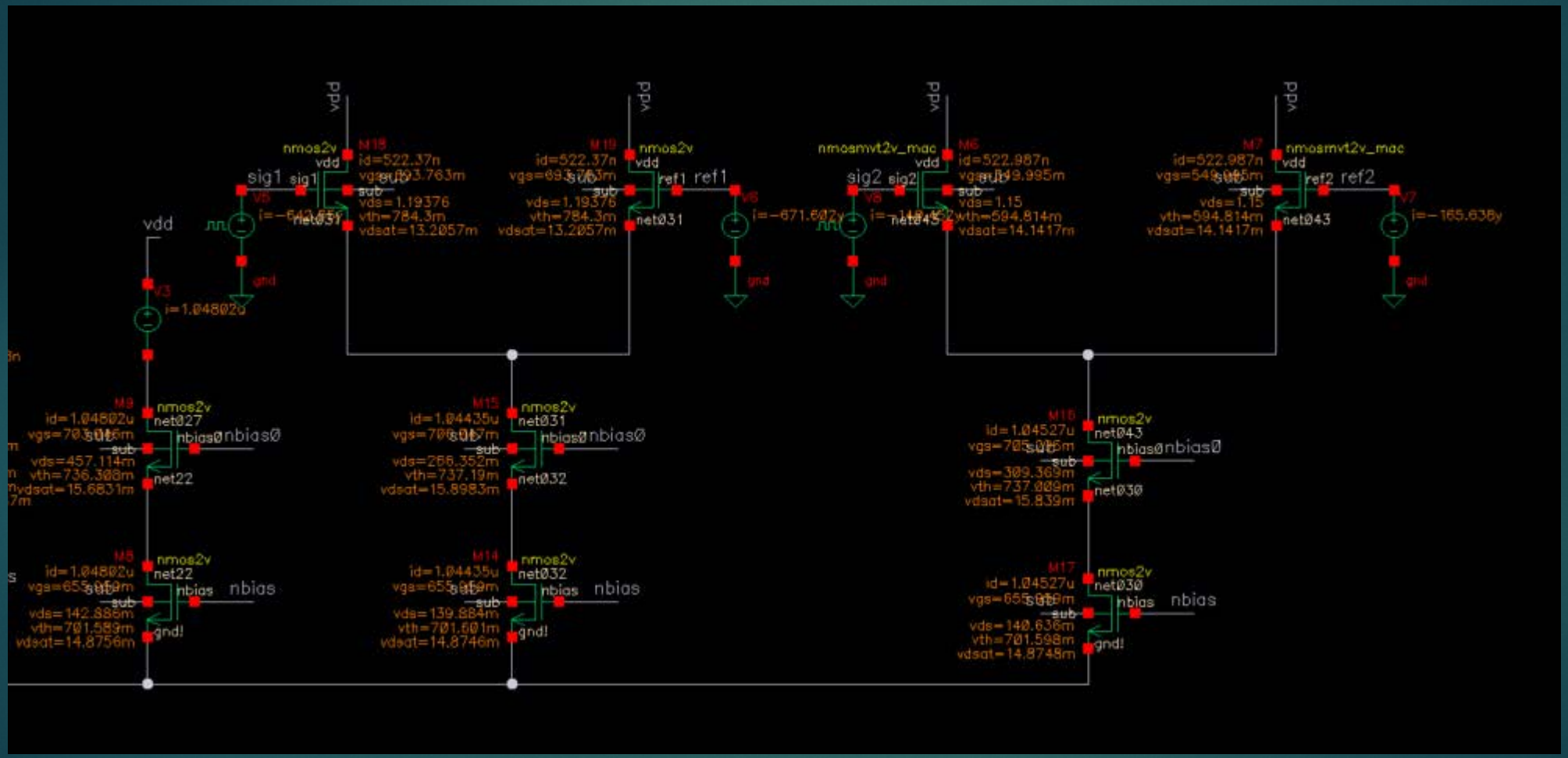


Results NMOS & PMOS...

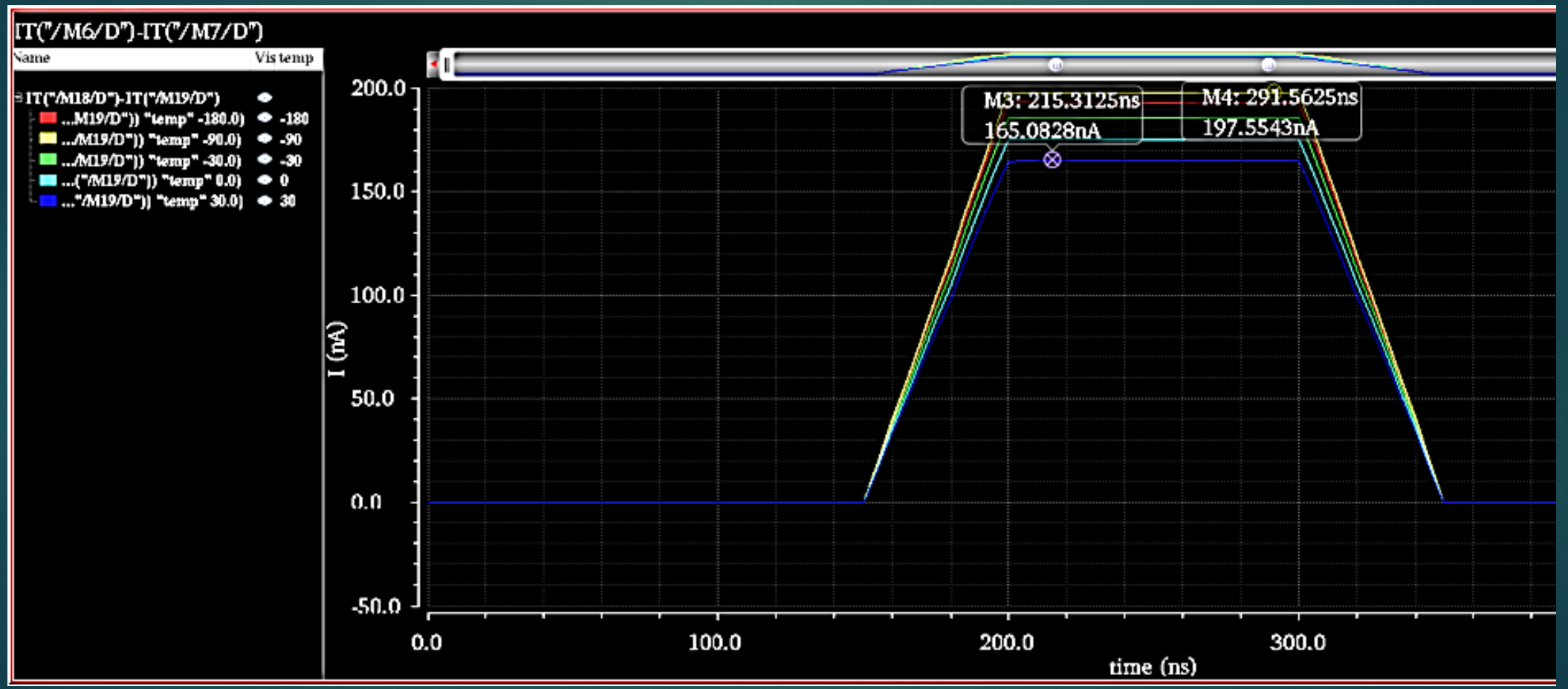
	source follower Vgs @ 1uA (mV)					
	Temp	std	mvt	nvt	P_mac	p_nvt
	30	-326	-224	-104	607	373
	0	-344	-245	-123	626	400
	-30	-362	-266	-143	648	430
	-90	-401	-312	-184	698	491
	-180	-487	-396	-259	789	586
delta	210	161	172	155	-182	-213

SF Gain		
p_std	p_nvt	n_std
0.695	0.826	0.751
0.689	0.825	0.749
0.685	0.825	0.749
0.673	0.823	0.734
0.65	0.822	0.706

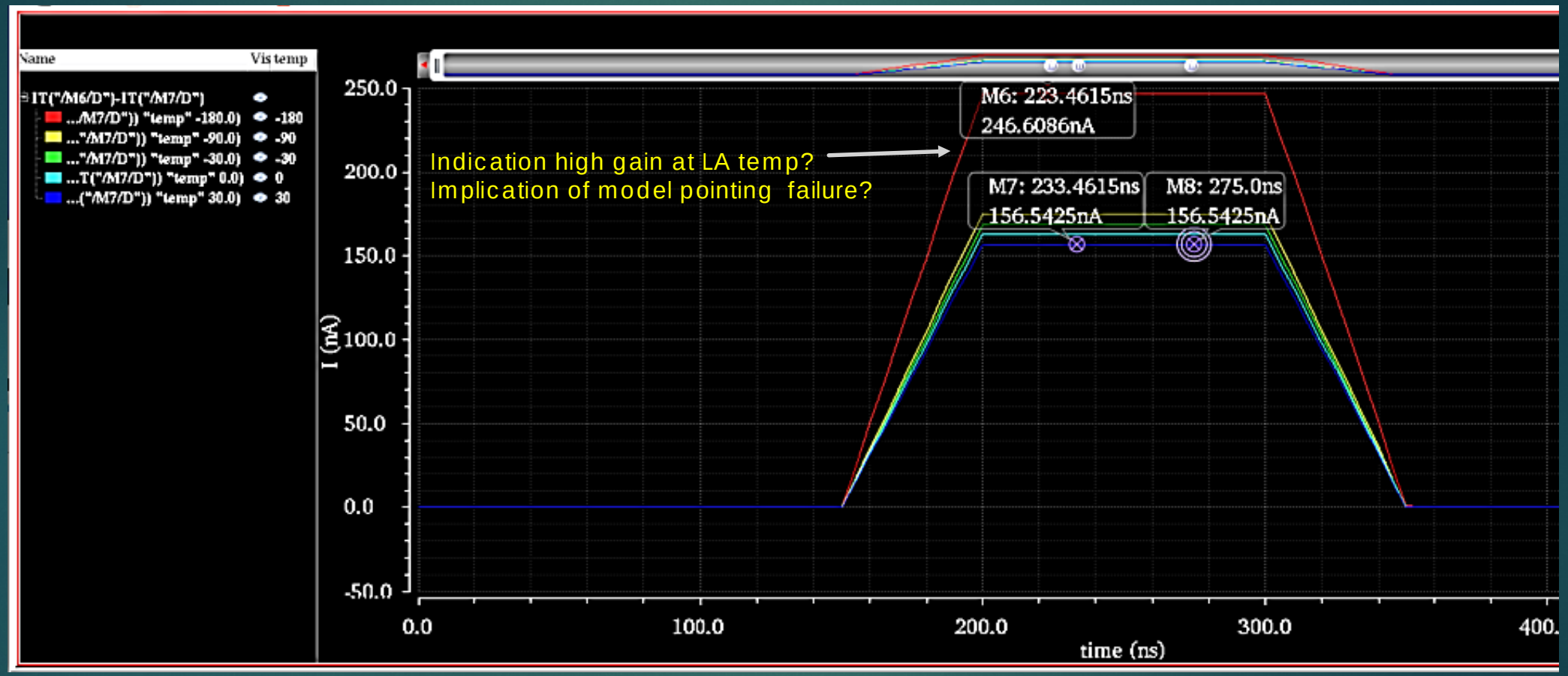
Similar Studies of NMOS Diff pair Gain



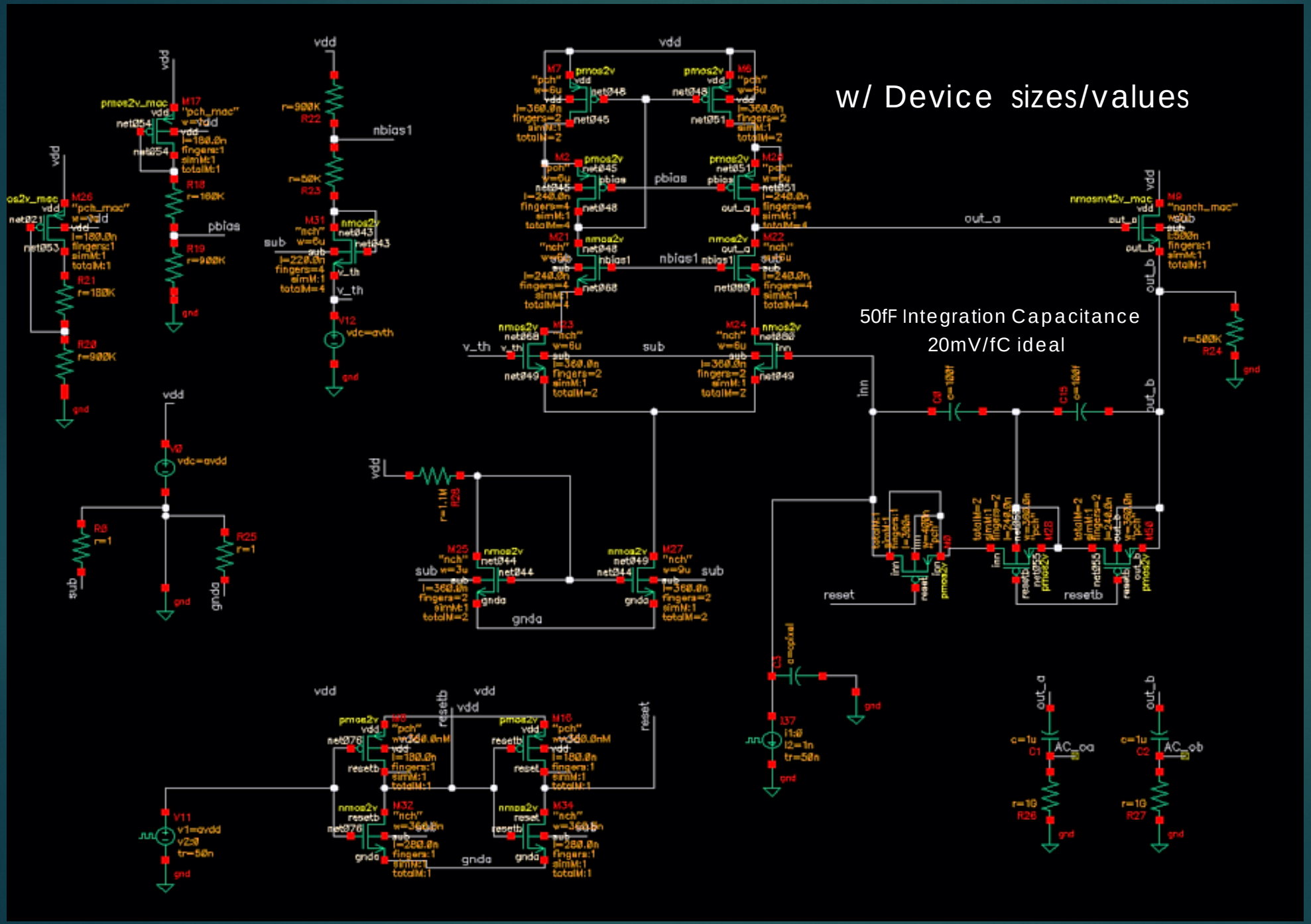
Standard NMOS Dif pair over Temp



mvt NMOS Dif pair over Temp

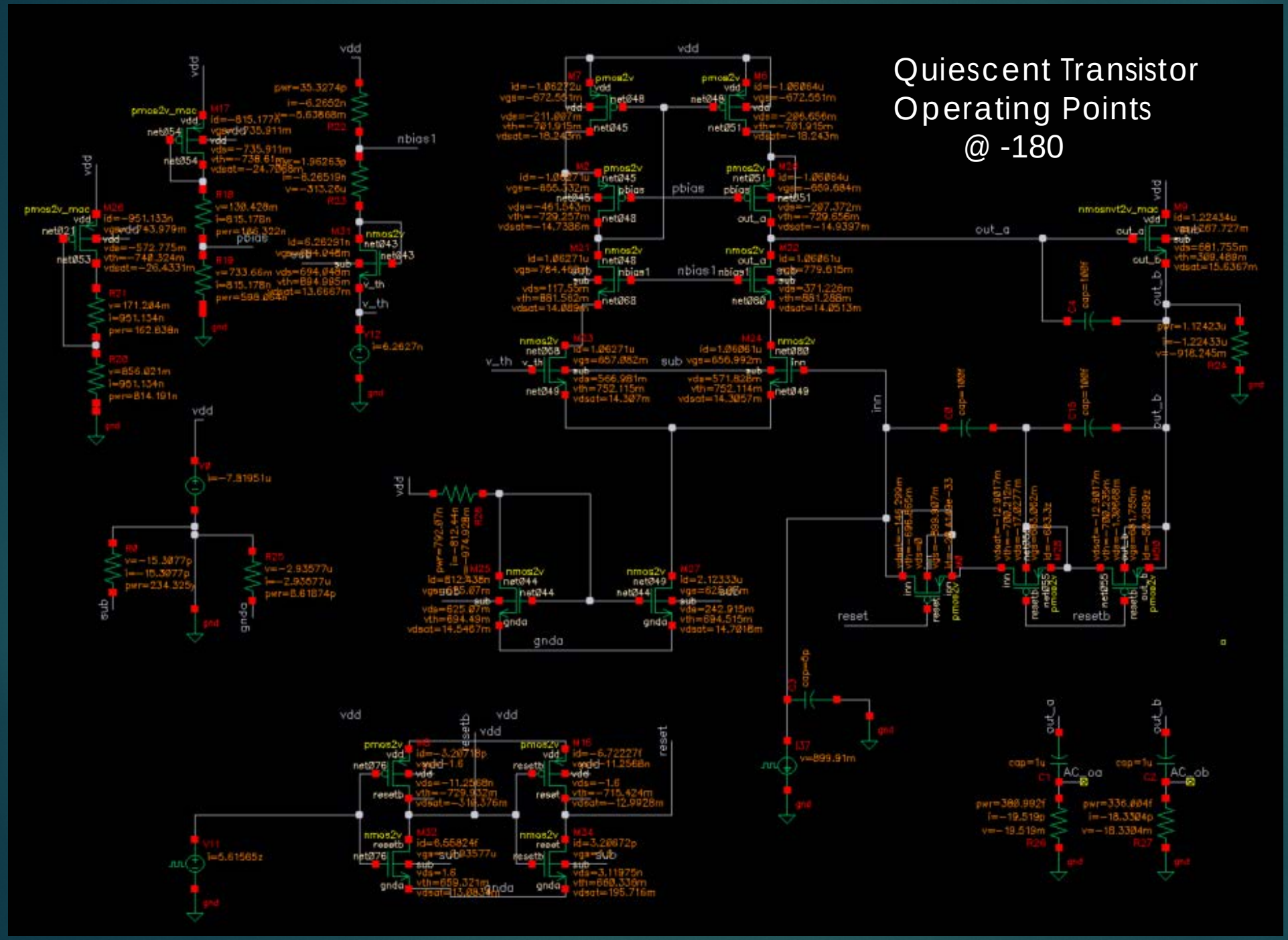


NMOS Integrator Study



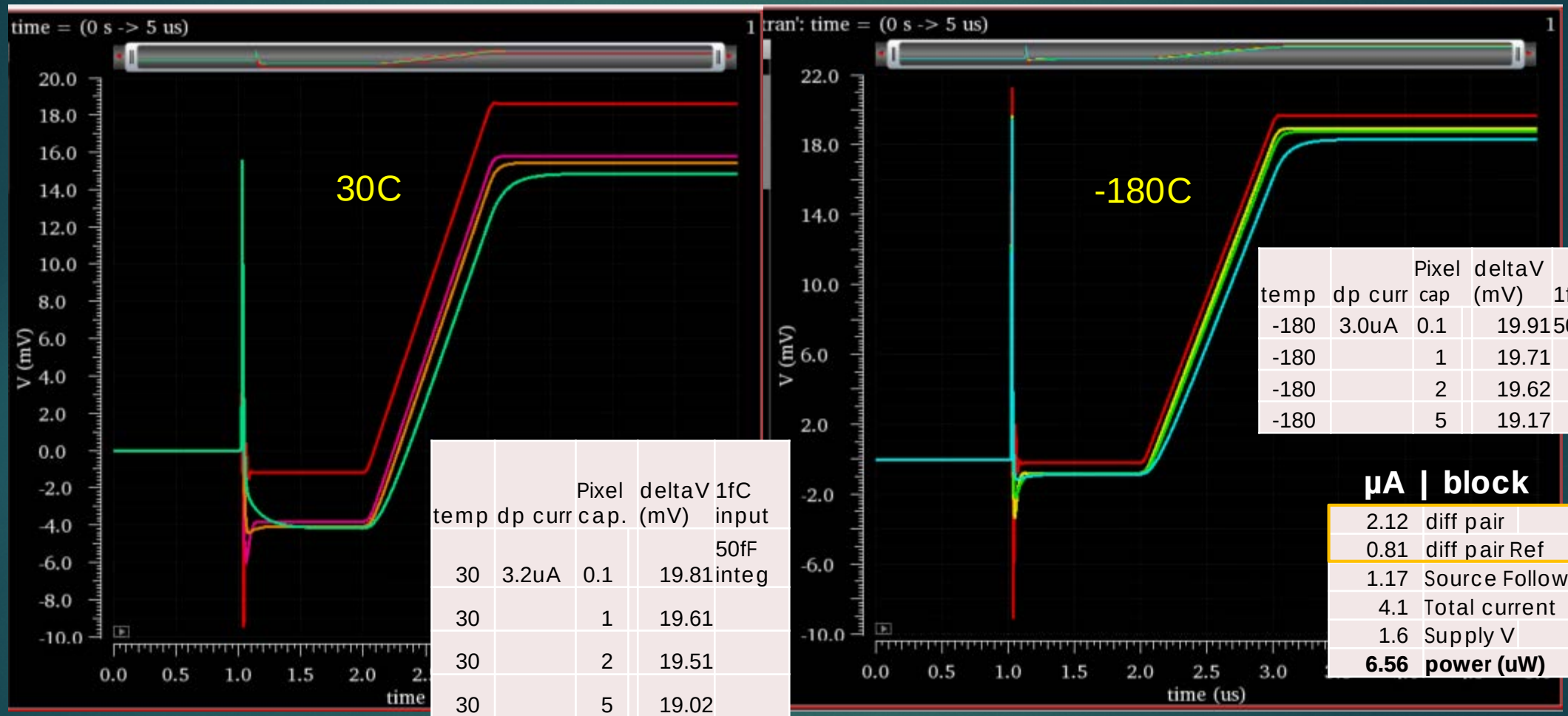
NMOS Integrator

Pixel Capacitance study



Pixel Capacitance Effects of Loading the input

Integrator Stage Output Response for ***50fF Integration cap 1fC input*** *vs* Pixel cap.



temp	dp curr	Pixel cap.	deltaV (mV)	1fC input
30	3.2uA	0.1	19.81	50fF integ
30		1	19.61	
30		2	19.51	
30		5	19.02	

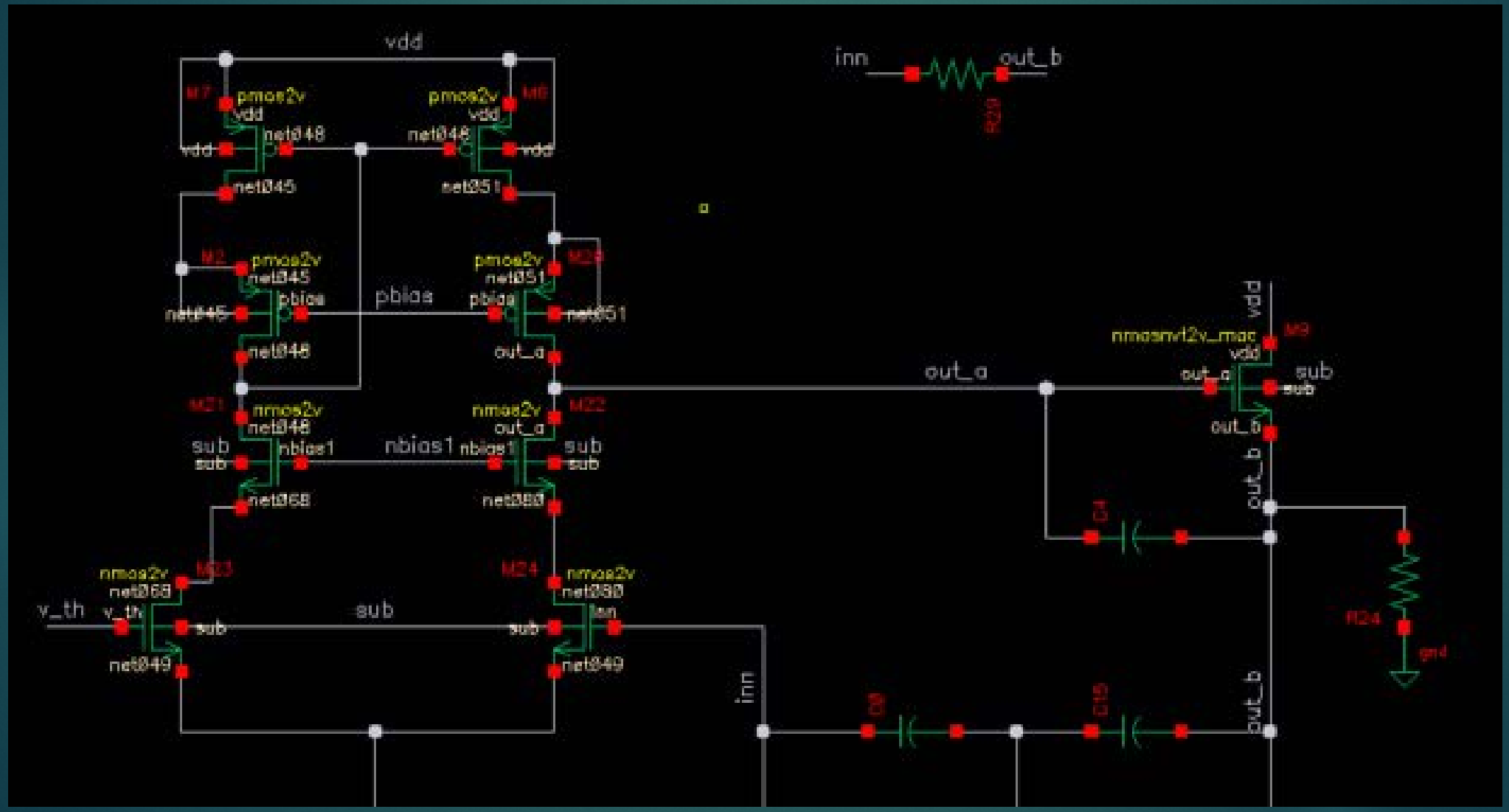
temp	dp curr	Pixel cap	deltaV (mV)	1fC input
-180	3.0uA	0.1	19.91	50fF integ
-180		1	19.71	
-180		2	19.62	
-180		5	19.17	

µA	block
2.12	diff pair
0.81	diff pair Ref
1.17	Source Follower
4.1	Total current
1.6	Supply V
6.56	**power (uW)**

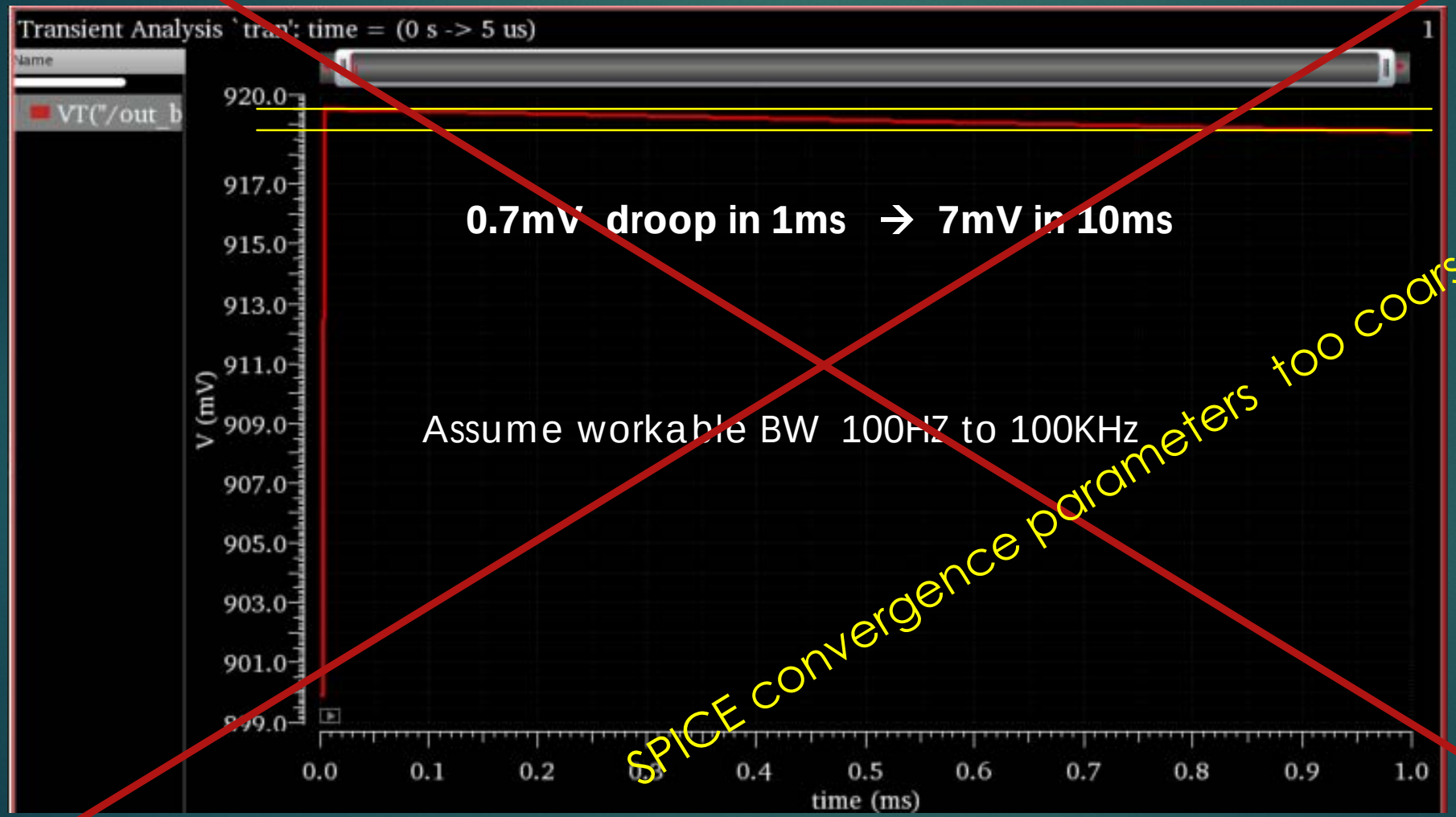
3µA

* No adjustments of bias or reference required.

Setup for Noise simulation: First studies
Apply Noiseless 1000G resistor across integration

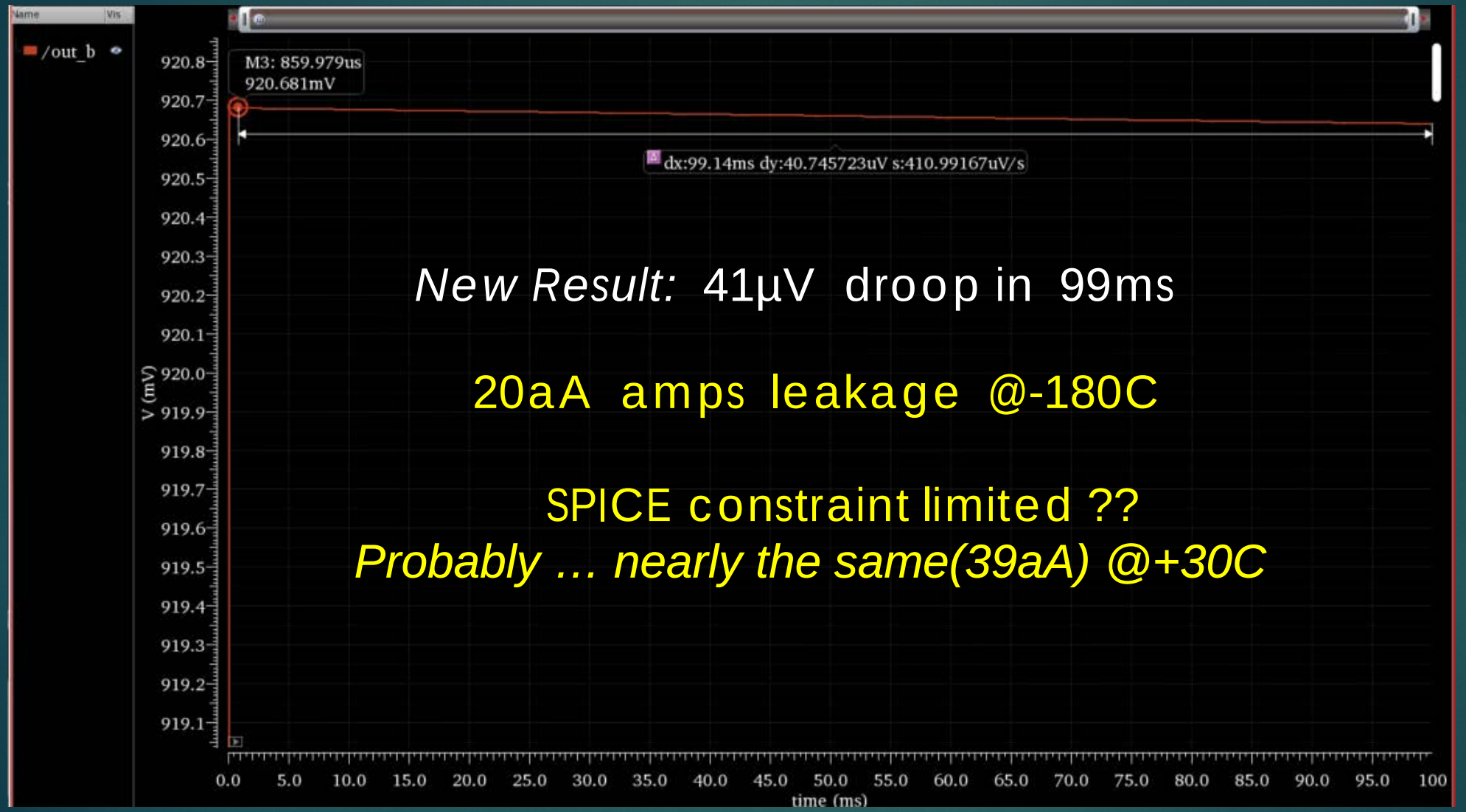


Noise Survey .. Drop in 1mS after 1fC input



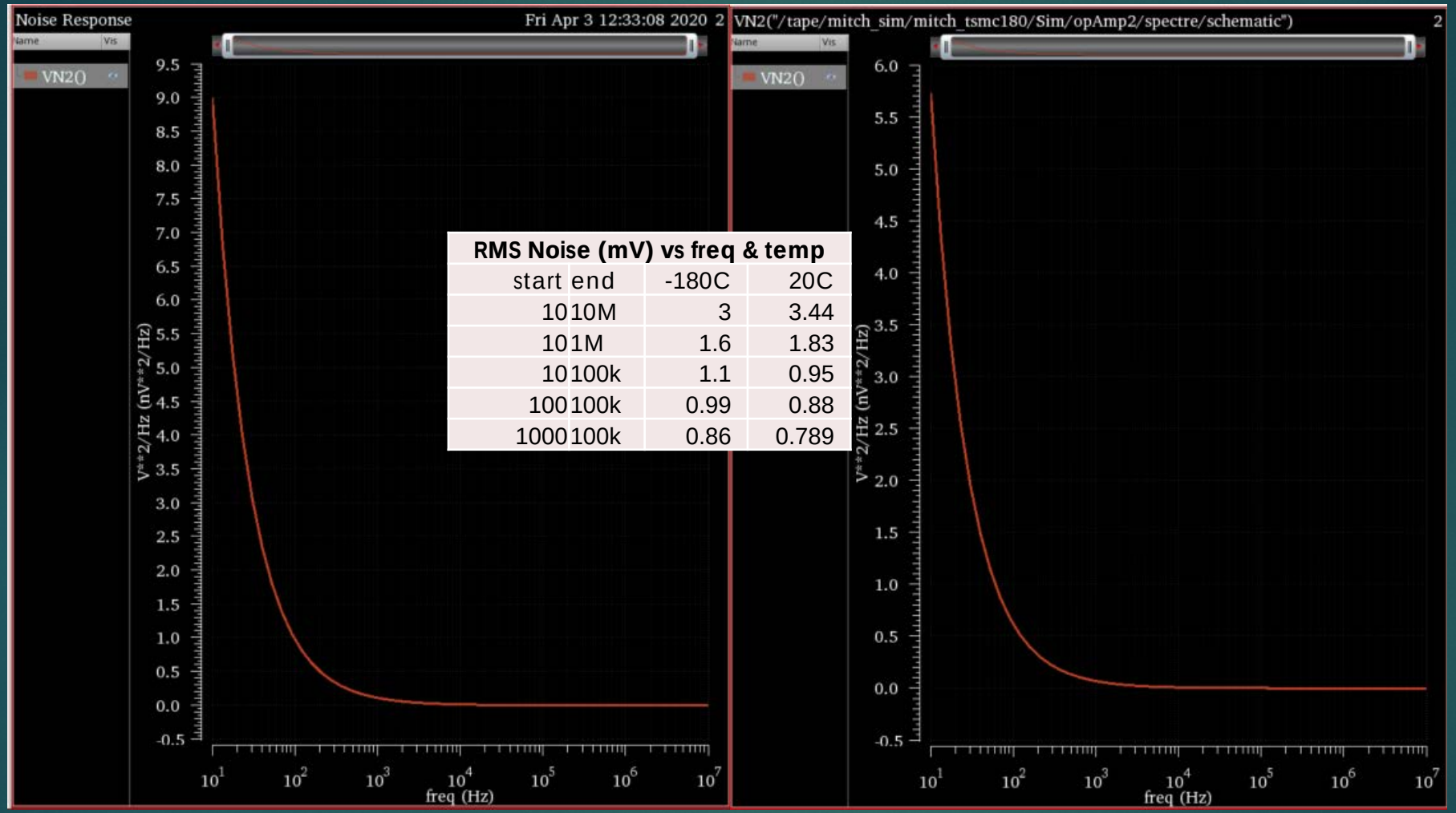
**Update 4/2/20… *actually this is consistent with simulated integrator leakage*

Noise Survey .. Droop in 100mS after 1fC input



** SPICE parameter precision adjusted gmin 1e-15, vabstol 1e-8, iabstol 1e-16

Noise Spectrum (V^2/Hz) and RMS noise (mV)

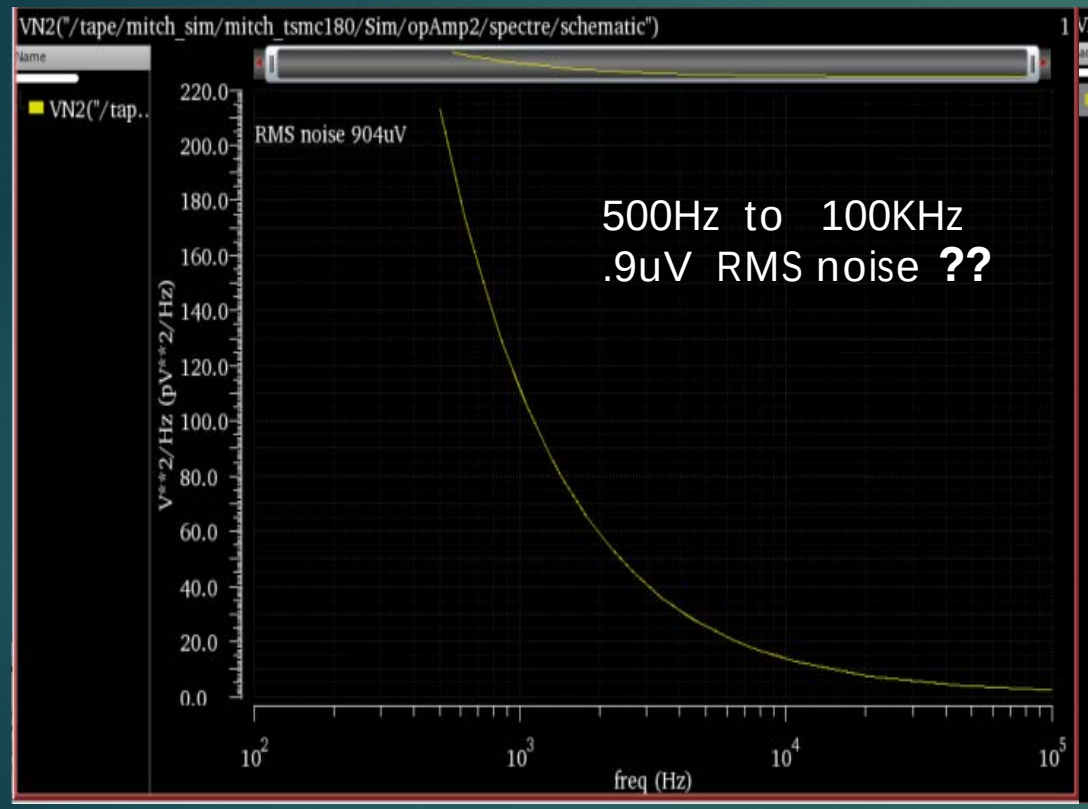


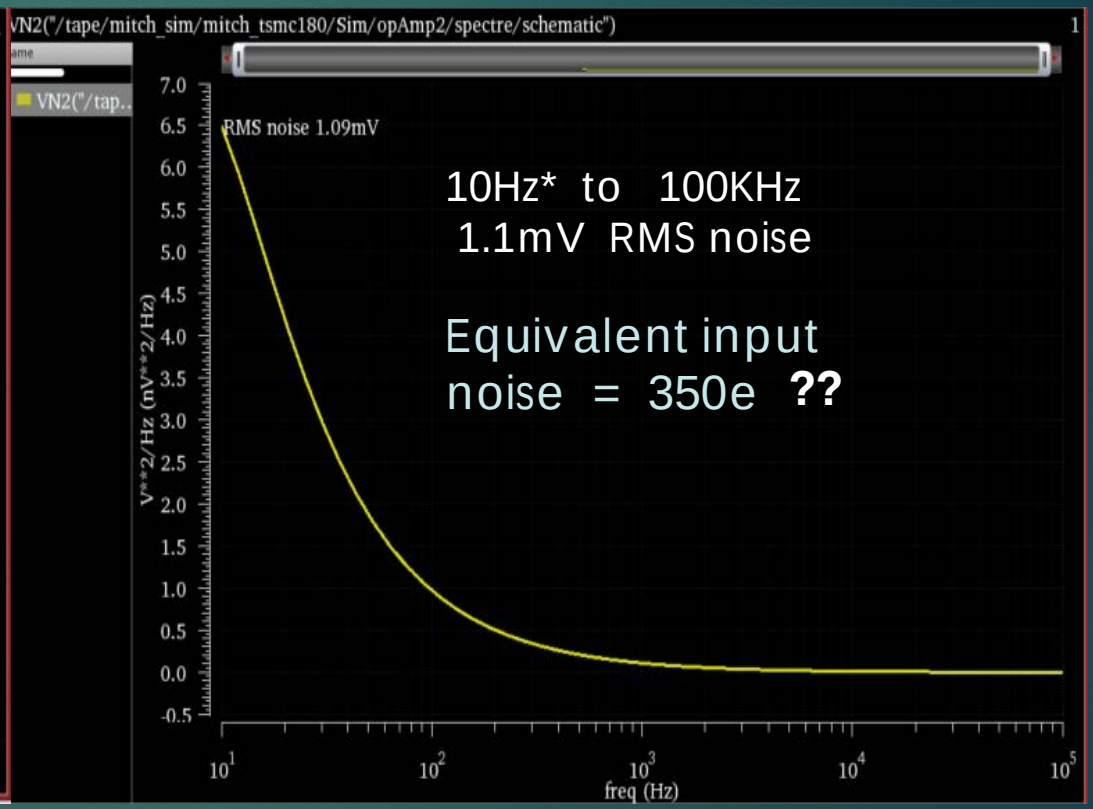
RMS Noise (mV) vs freq & temp			
start	end	-180C	20C
10	10M	3	3.44
10	1M	1.6	1.83
10	100k	1.1	0.95
100	100k	0.99	0.88
1000	100k	0.86	0.789

April 3, Results with finer settings of SPICE convergence options
**1PΩ noisless resistor holds across integrator

Integrator NOISE NMOS 2pF Pixel Cap

Simulation at -180C



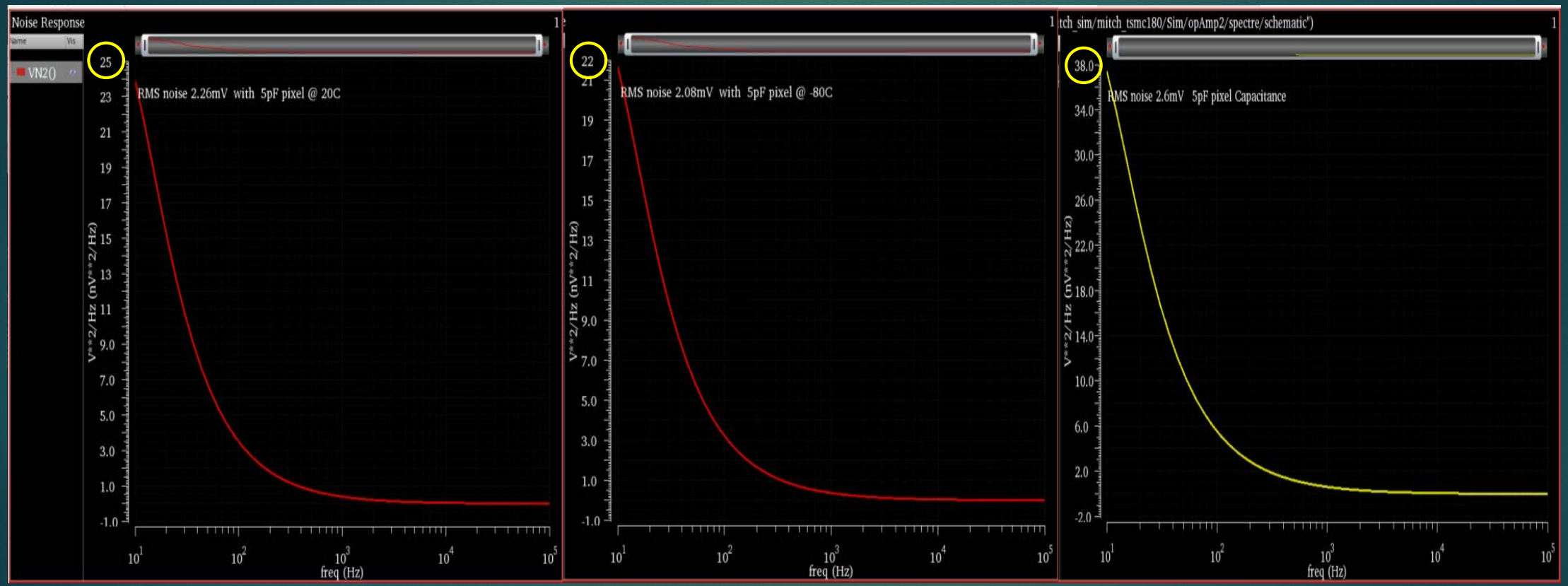


* Note 10Hz has significant attenuation with this test bench

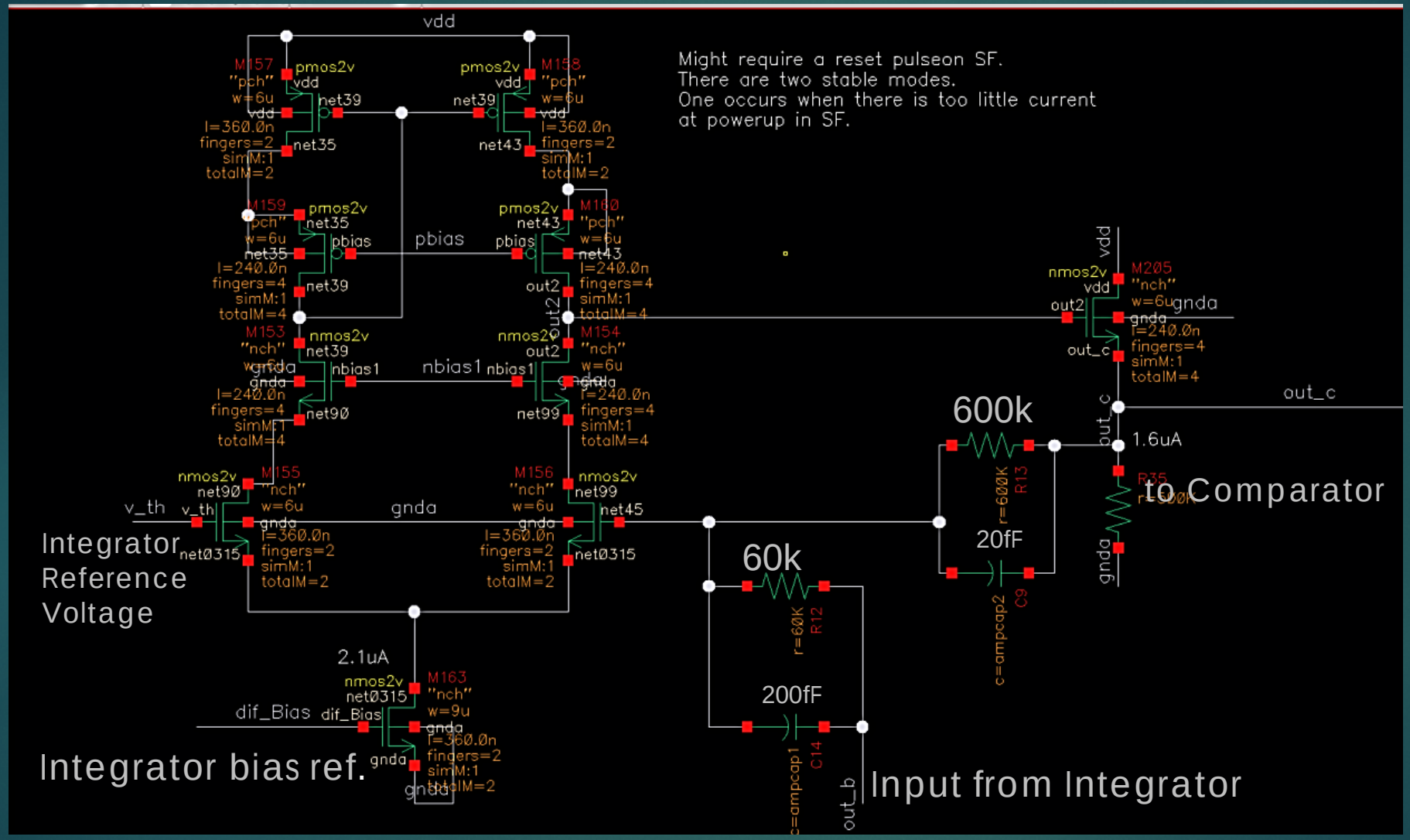
Noise vs temperature with 5pF Pixel Capacitance

RMS values: 2.26mV@ +20C, 2.08mV@ -80C, 2.6mV@ -180

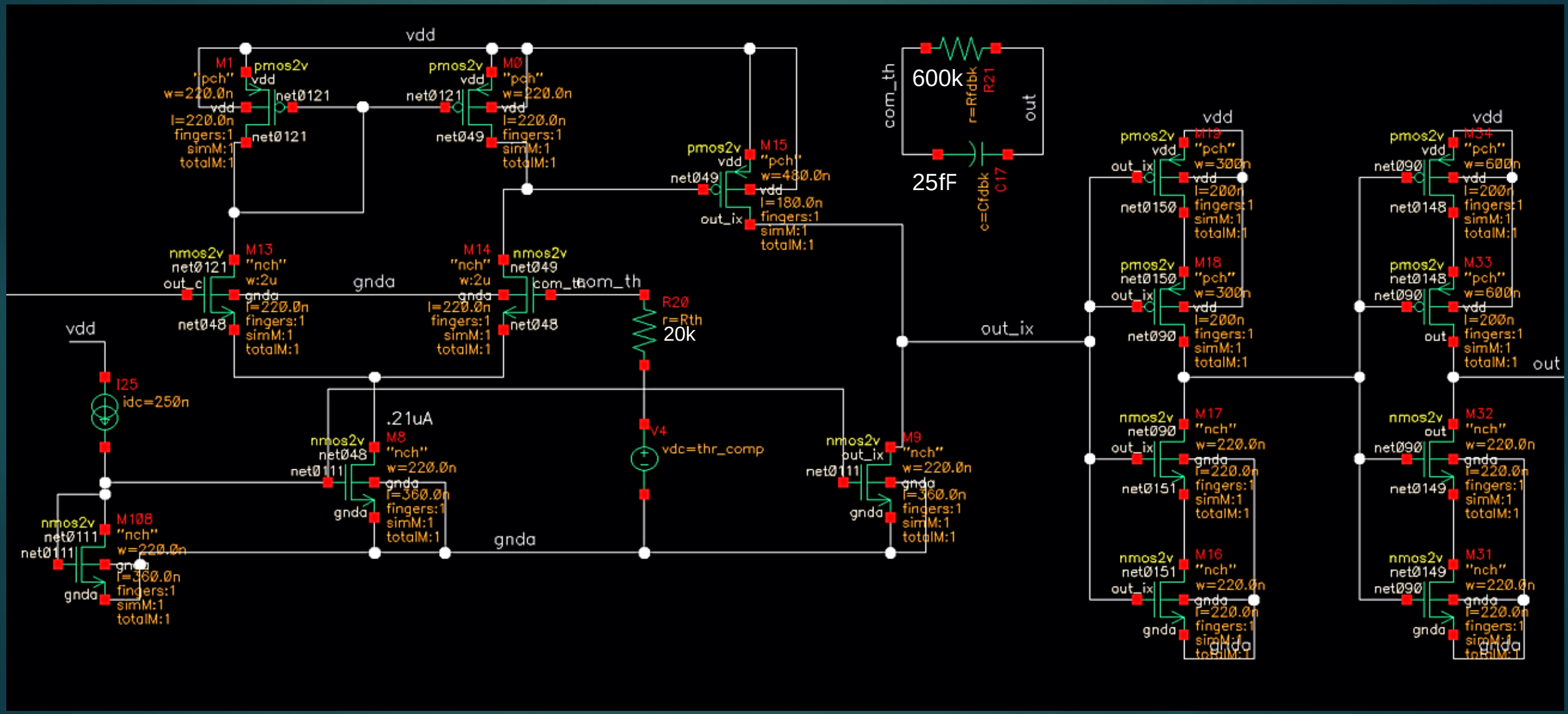
Larger noise at -180C ?? subtle test bench issue ?? Model issue ??



Qpix 10X AMP same opAmp as Integrator

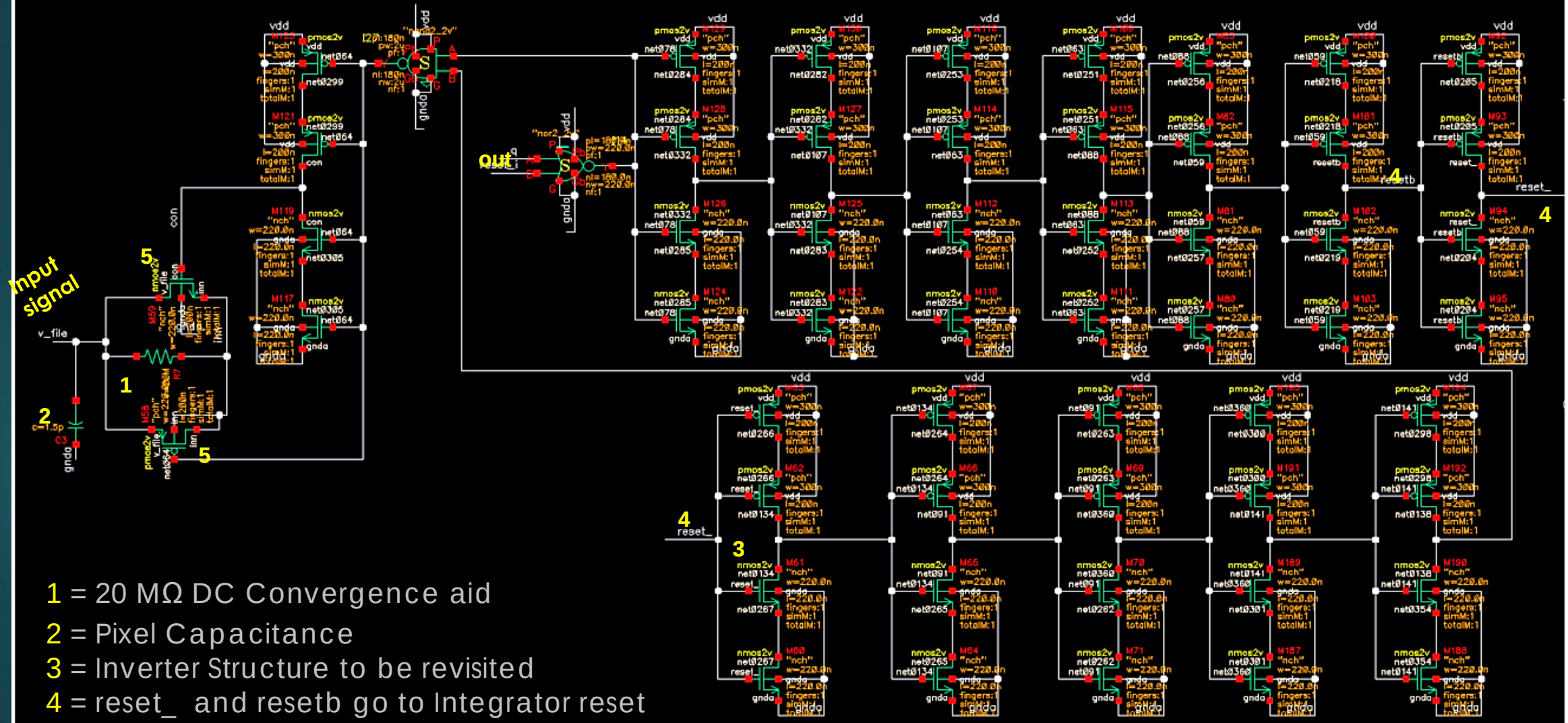


Comparator with short Hysteresis Delay



Pixel Disconnect & Reset related Delays

Delays for Pixel Connect & reset delay control



1 = 20 MΩ DC Convergence aid

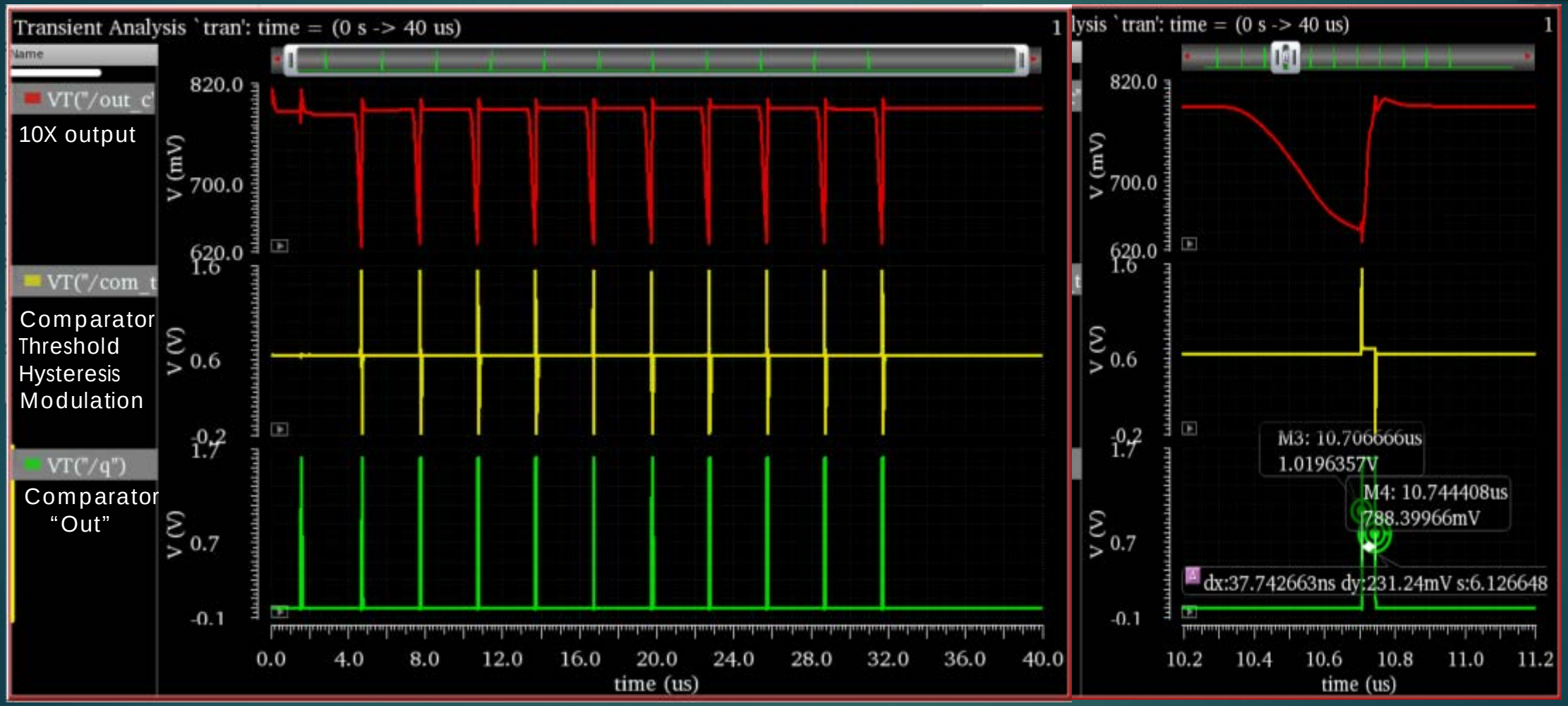
2 = Pixel Capacitance

3 = Inverter Structure to be revisited

4 = reset_ and resetb go to Integrator reset

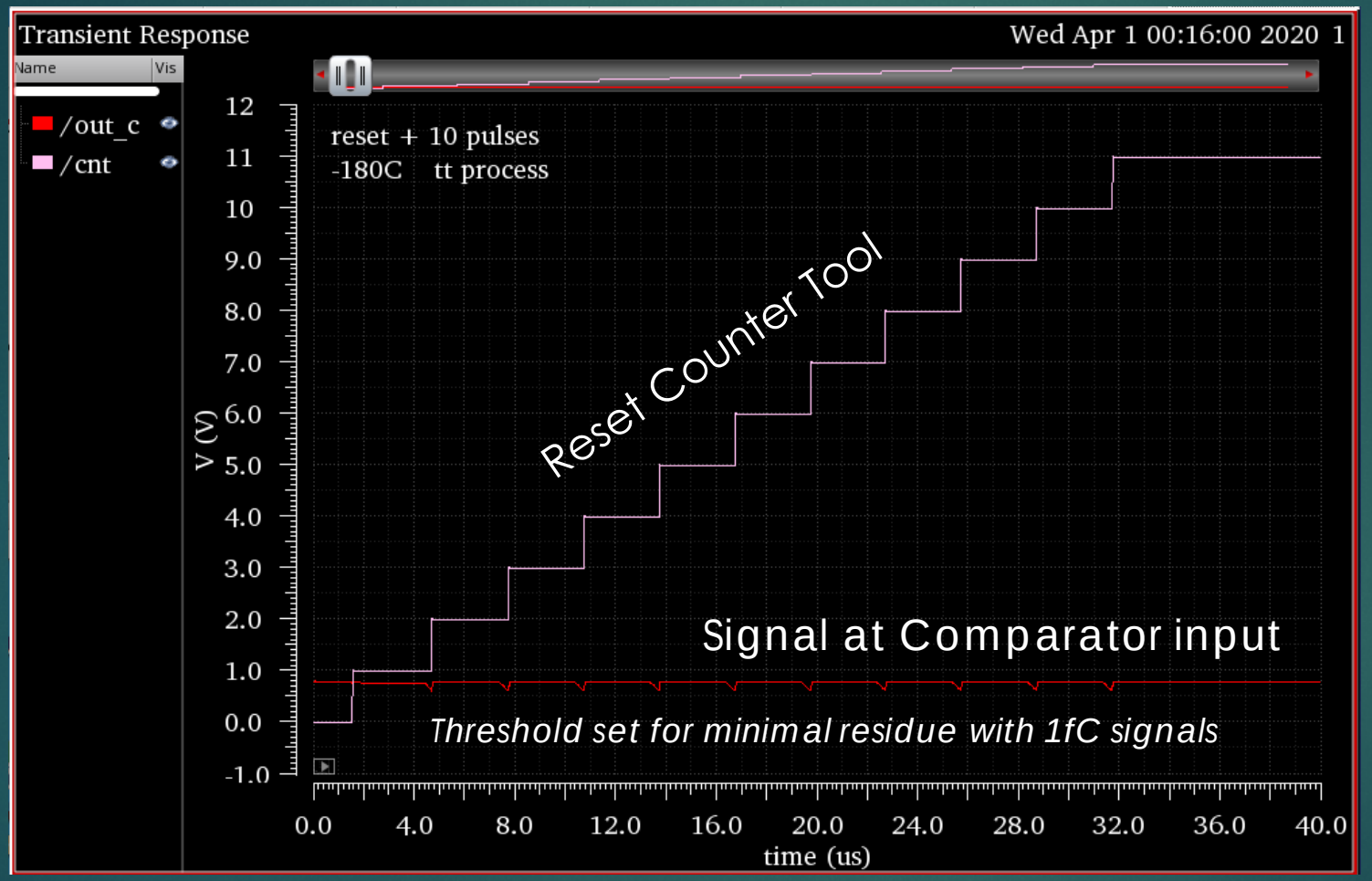
5= pixel connect switches

Signals from 10X output, Hysteresis positive feedback & reset



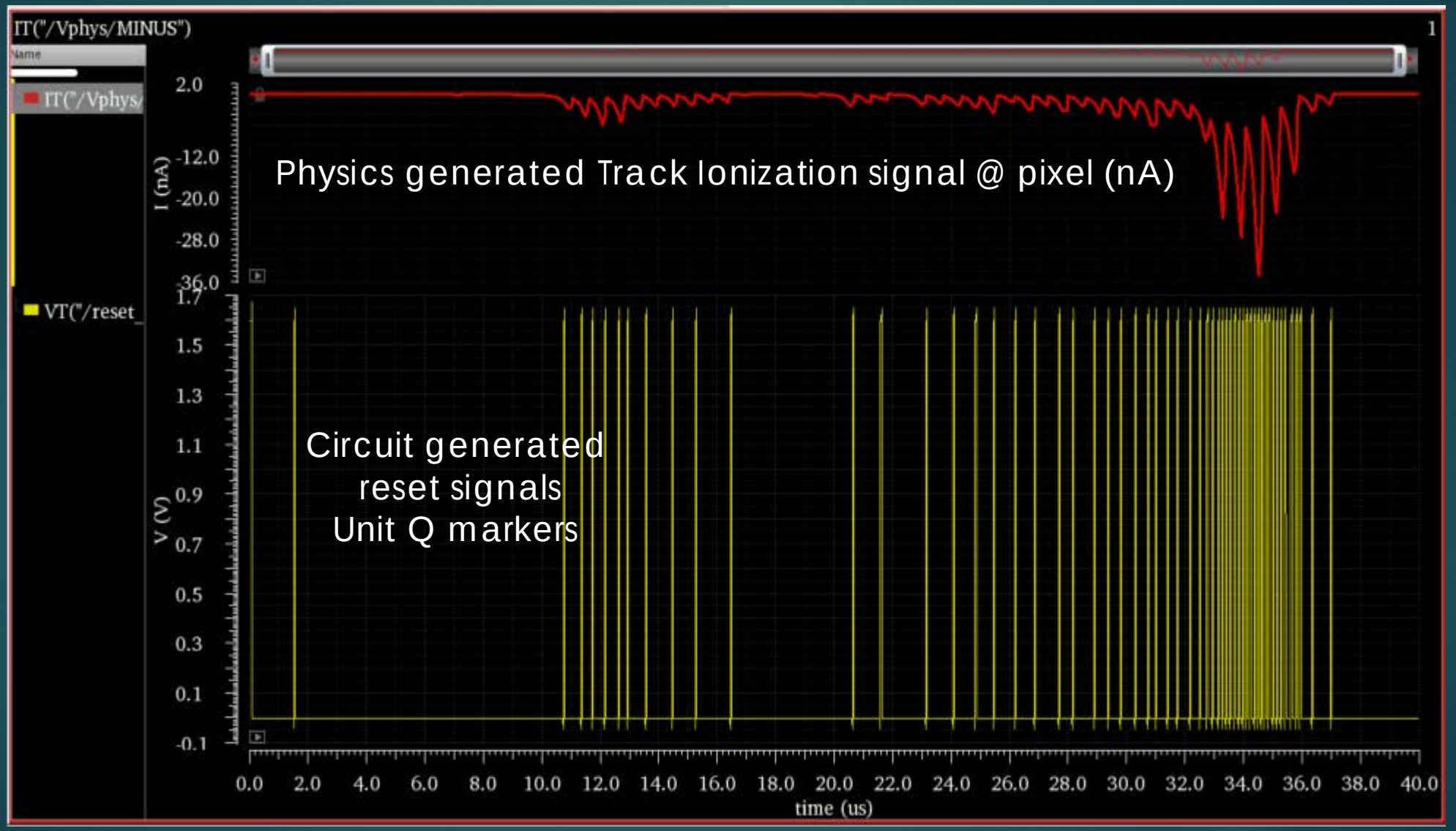
Response to initialization reset & 10, 1fC pulses

@ -180 C , tt models

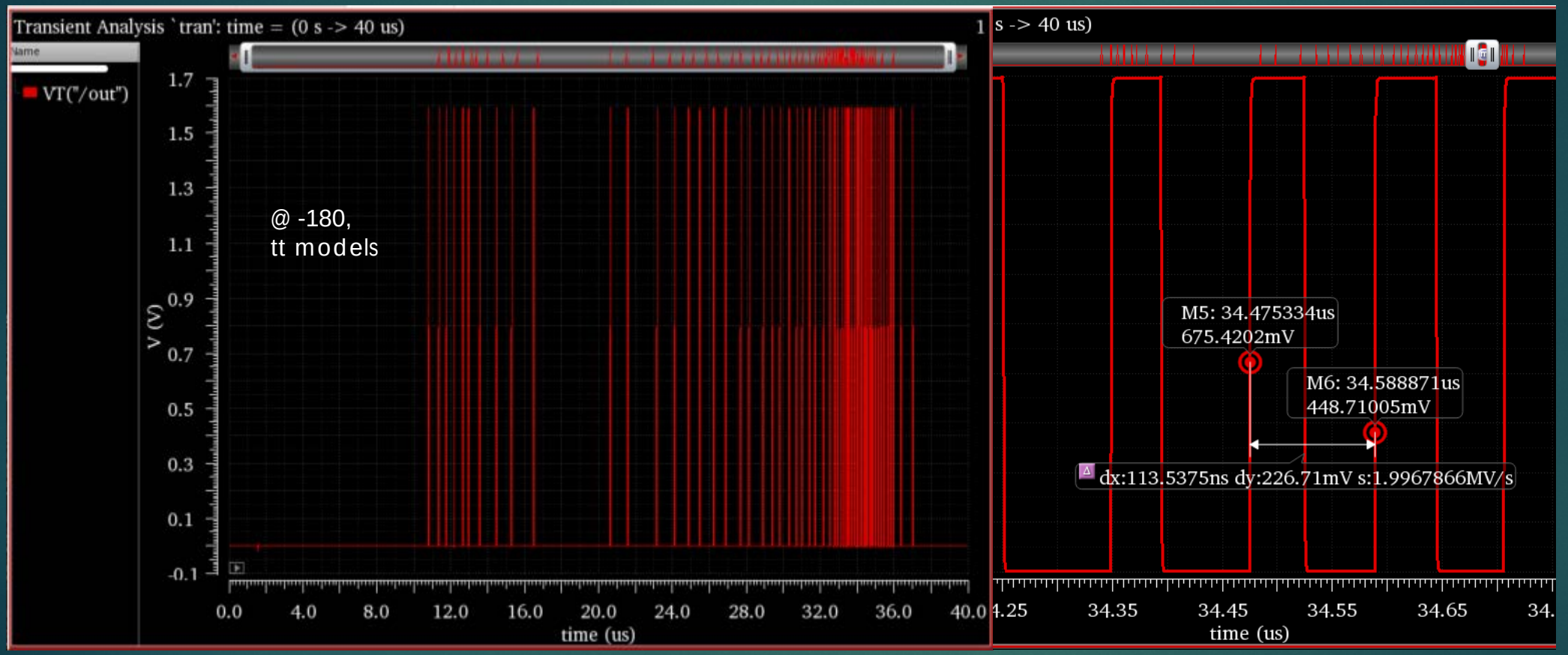


Circuit response to Physics Generated signals.

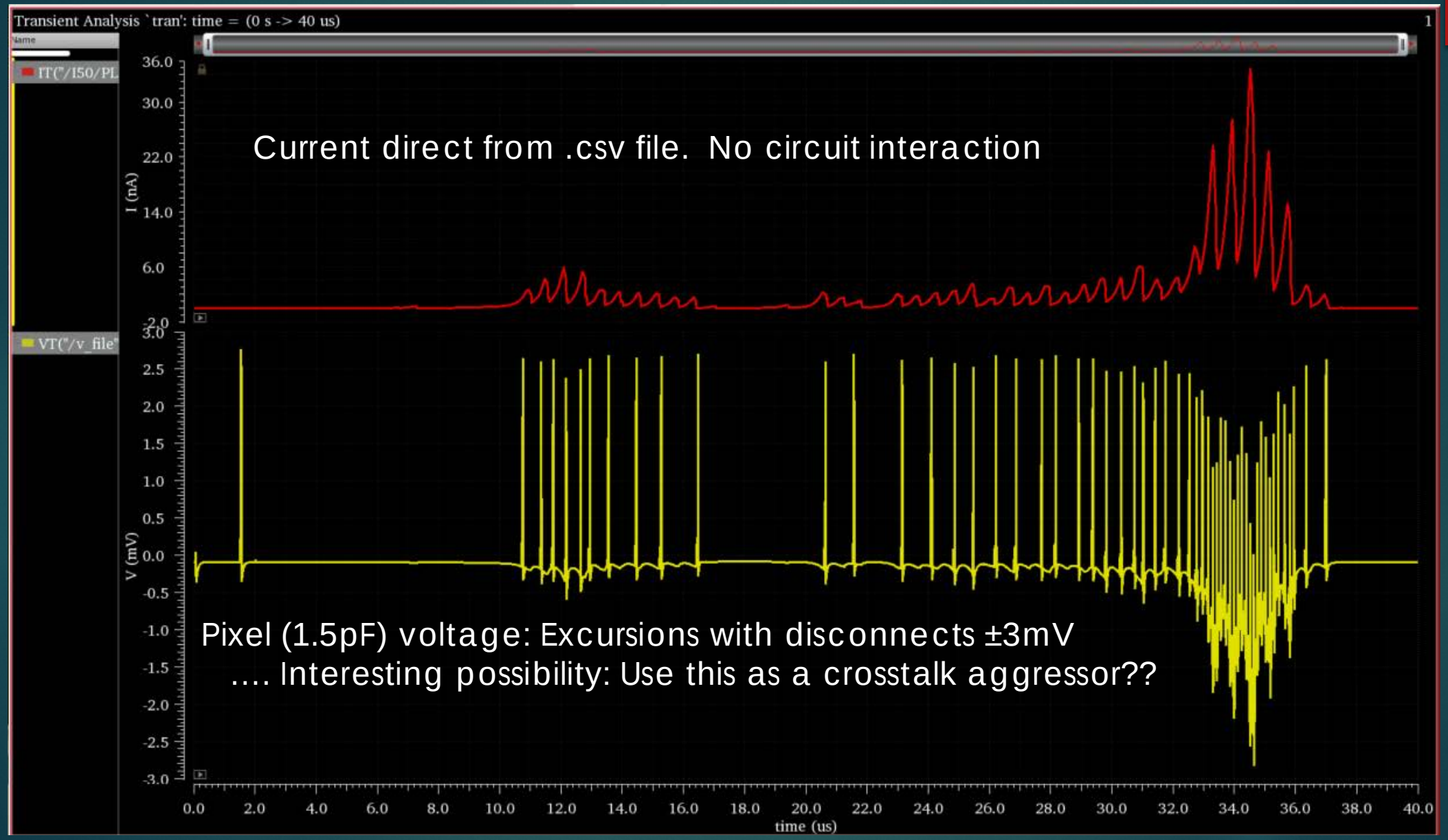
Physics Signal credit to: Hunter Sullivan UTA



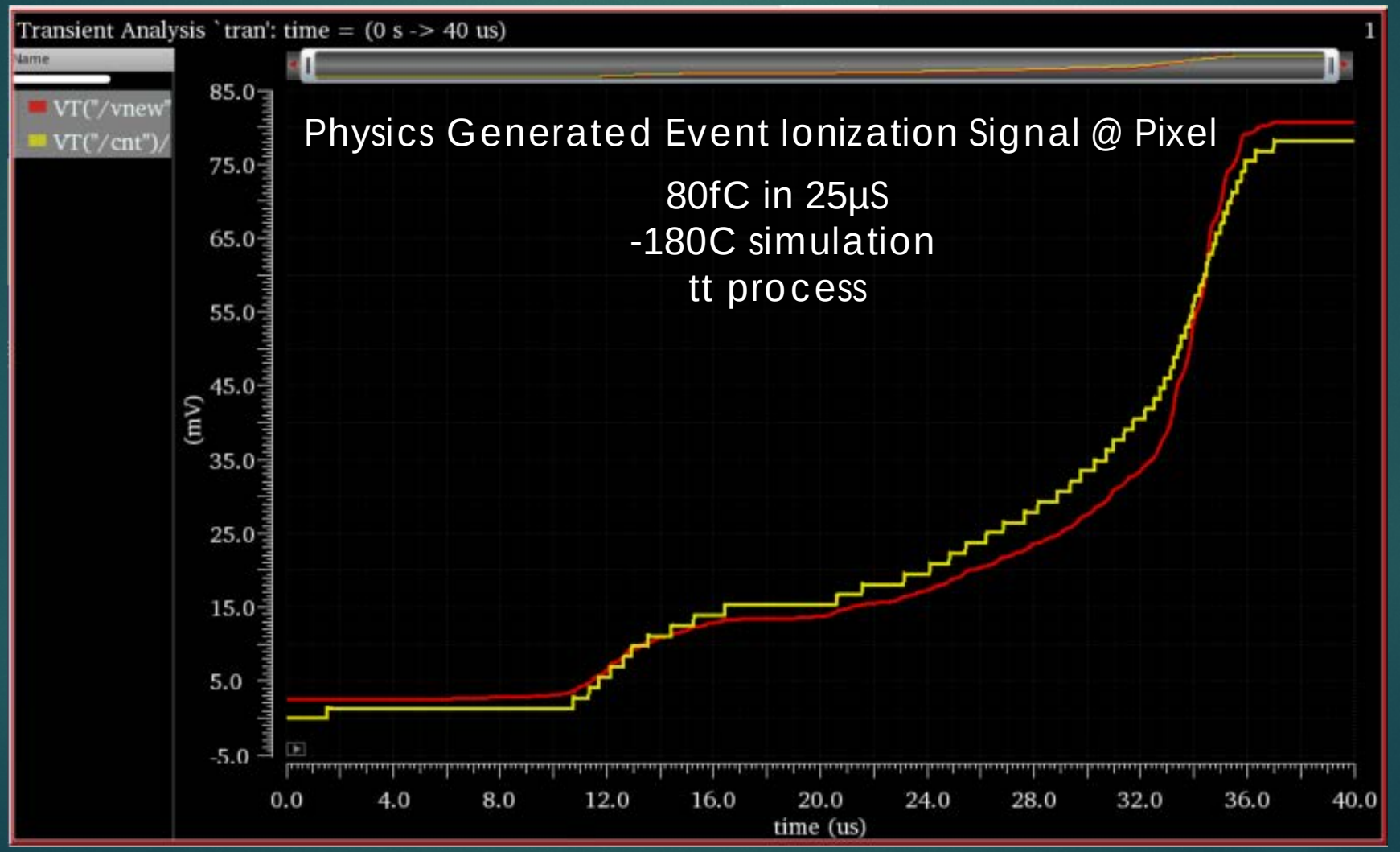
Highest Reset rate: 113.5ns



Large Physics Signal: Current & Voltage on pixel



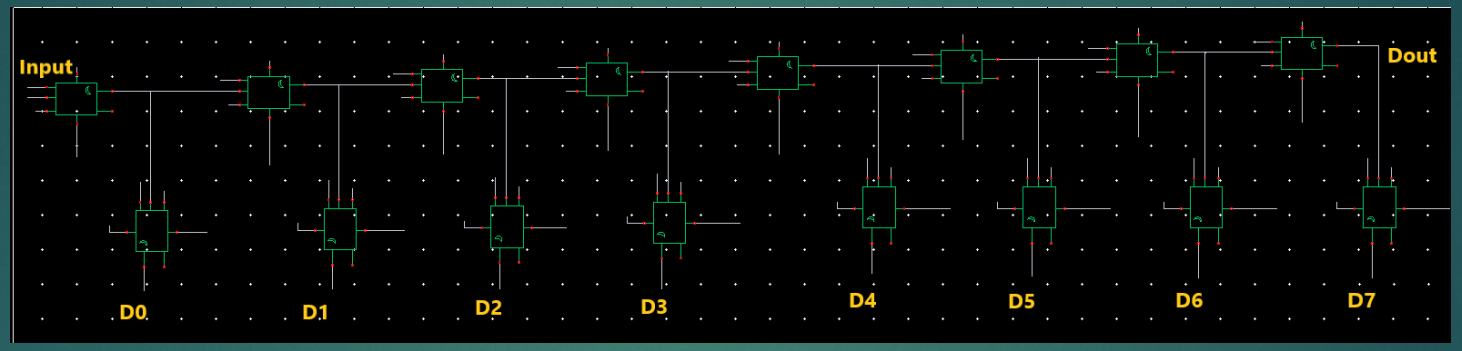
Integrated Pixel event Signal on 1pF Cap
vs
Integrated Reset count at 1mV / Reset



Simple SPI Interface for slow control

- The SPI Module is designed to work as a serial to parallel data converted having the ability to process a 8 bit word at an instance. The Module consists of D Flip Flops connected as shown in figure 1.

signals
Serial Clock
Serial In
Serial Out
Load
D0… D7



Data are shifted into and out of the 8 bit/register words and may be looped back to the output

Noteable Work TBD ahead of LAYOUT

- Develop master Biasing scheme requiring fewer high value resistors. Current design explores reasonable techniques but can be simplified.

The following were studied/partially implemented in blocks studied by MSEE's but now need to be carried to the full design:

- Apply process resistors to current design
- Validate current design over process.
- Validate device mis-match performance.

- Develop suitable Threshold DAC
- Develop / Implement LVDS driver & receiver.

- SPI interface implementation

Summary

- Significant progress has been made over the past 2 years. The design has been implemented in 3 ASIC processes and the circuit has matured along the way lowering power, defining and simplifying circuit elements. It appears to be reasonably responsive to physics generated signals. Higher fidelity is likely available at the cost of an increase in power.
- The most challenging blocks are understood and ready for or close to ready for layout in a prototype design.

- Progress will continue to be made on the design during our unplanned sequestration.
- Parts from other groups could be incorporated leading to a more complete prototype.
- MSEE help really can not be effective until the Lab is re-opened.
- Other implementations could be explored such as the Q replacement approached suggested by David Nygren.

Backup

Sanity Check Noise calculations

- 16.189av * 10^5 = 1.62E-12 sqrt = 1.27236E-06