UH_Q-Pix_OSC_Review

Gang Liu

University of Hawaii

Oscillator Overview

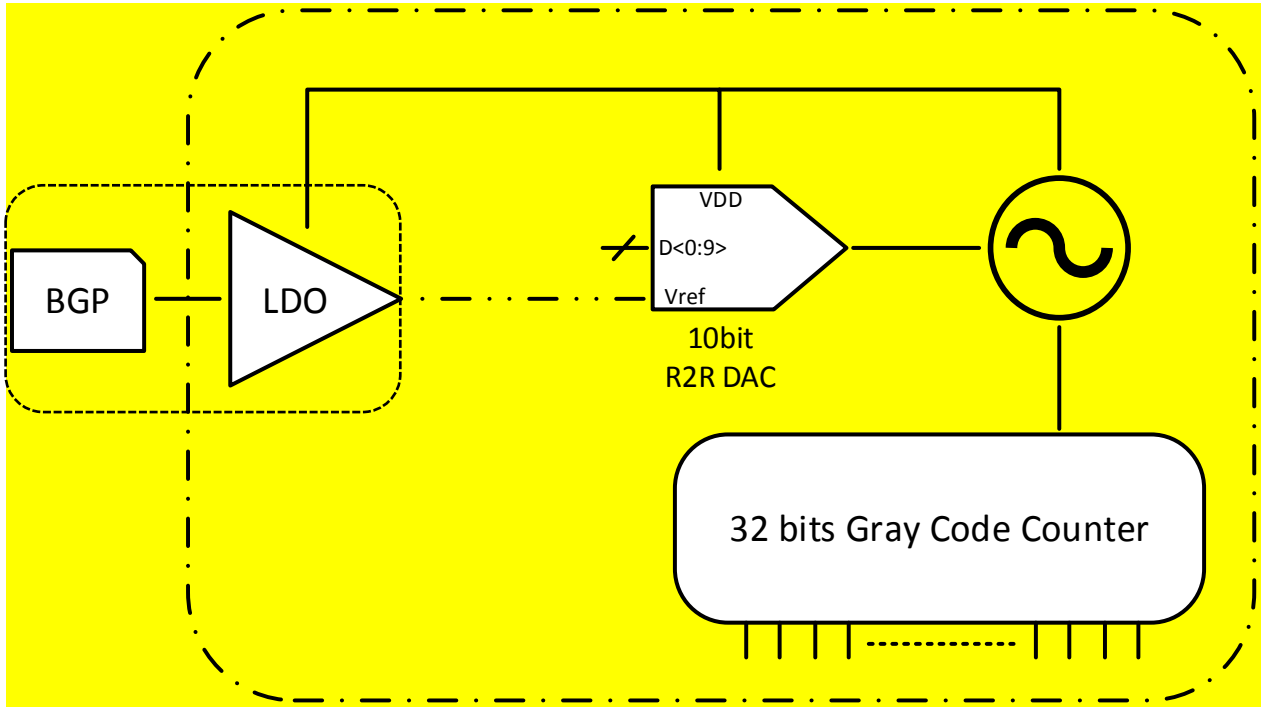
- **Ring oscillator:**

  Tune range, Resolution, Power
- **10-bit DAC:**

  Resolution, Power
- **Bandgap & Regulator**

  Power
- **32-bit Gray Code Counter**

  Power

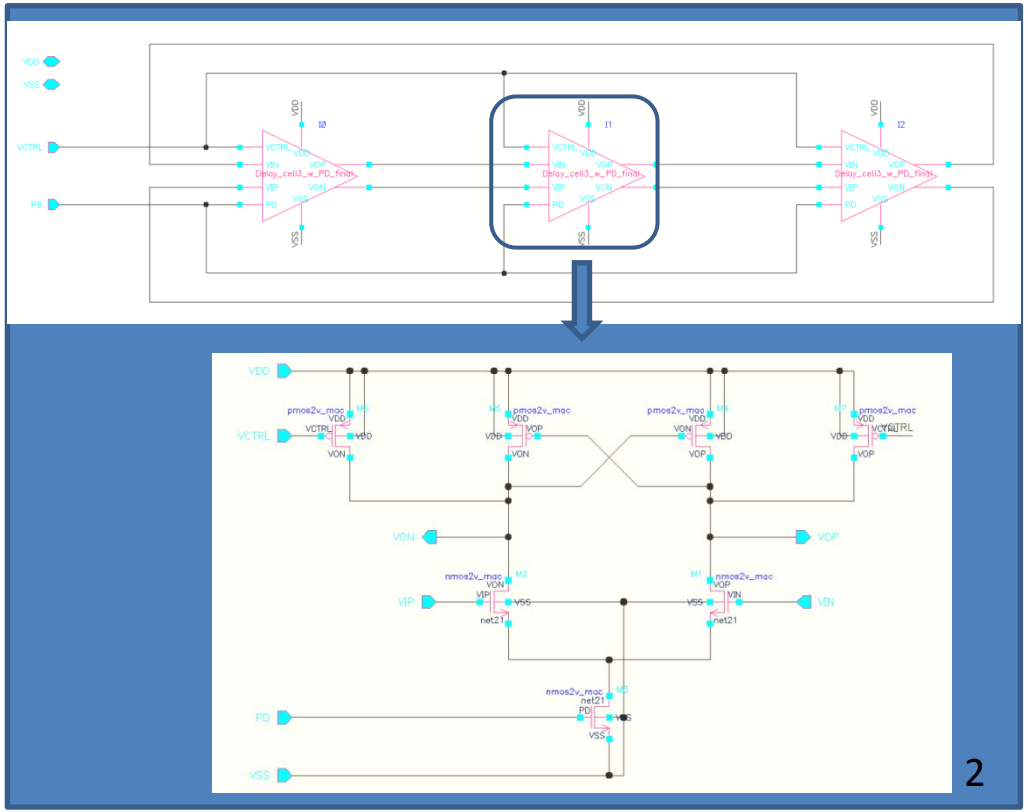


Ring Oscillator

- Tune range: 50MHz ~ 100MHz
- Target resolution: 1%
  - Large transistor
  - Limited range and gain
  - Simple structure and less component
- Differential and no bias delay cell

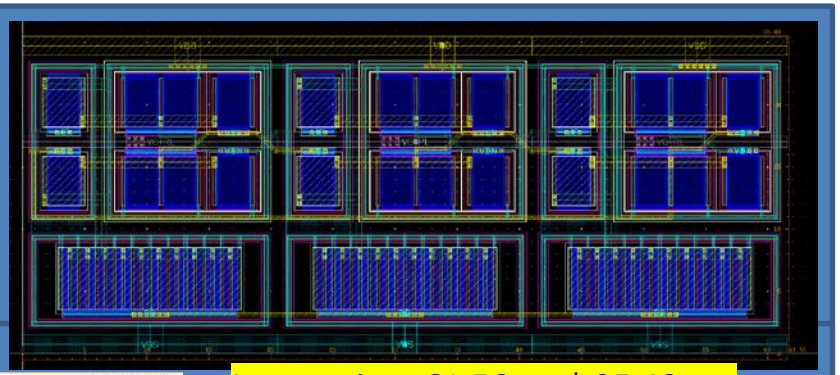
  simple, good common mode noise rejection
- Power-down mode

  Turn off to test the analog performance

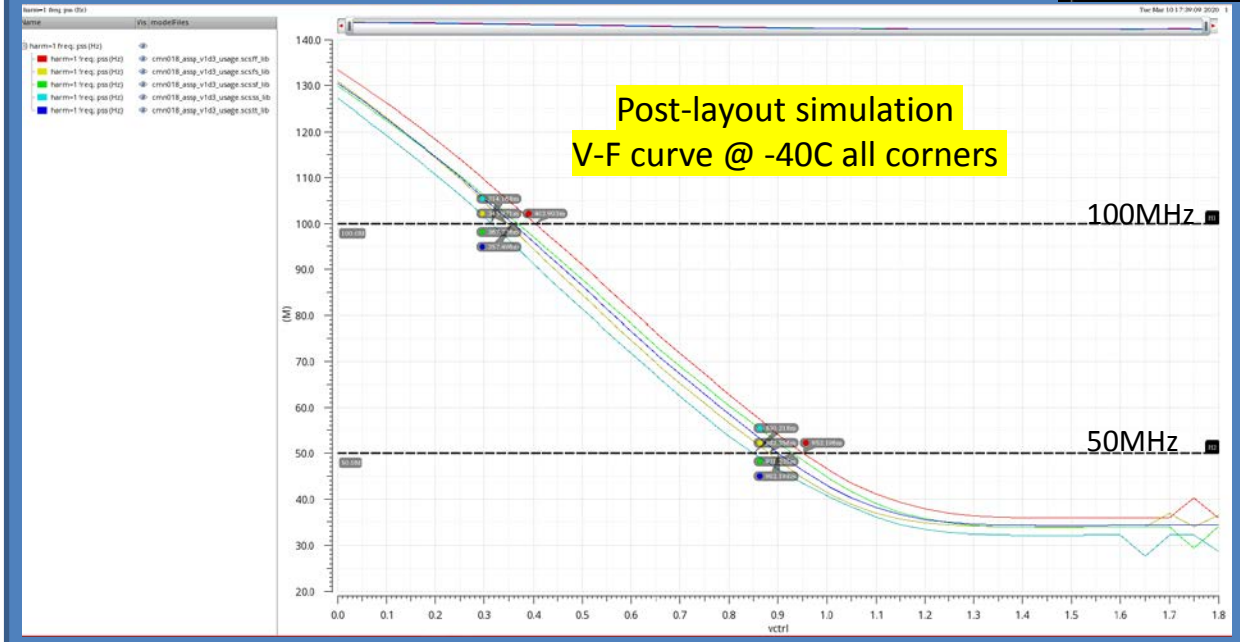


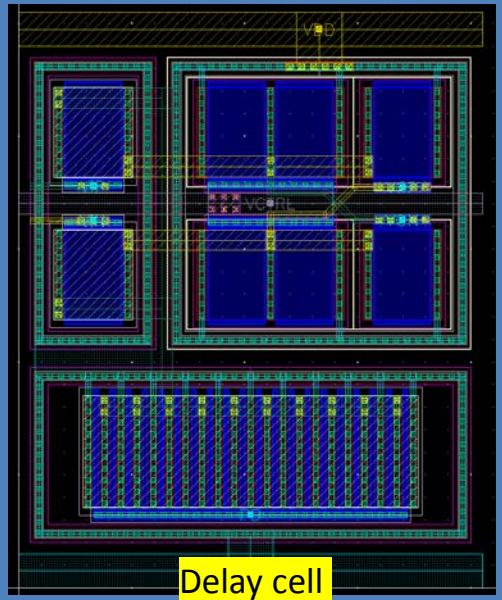
Ring Oscillator

Power: 201.3uA (0.36mW) @ 50MHz -40C typical



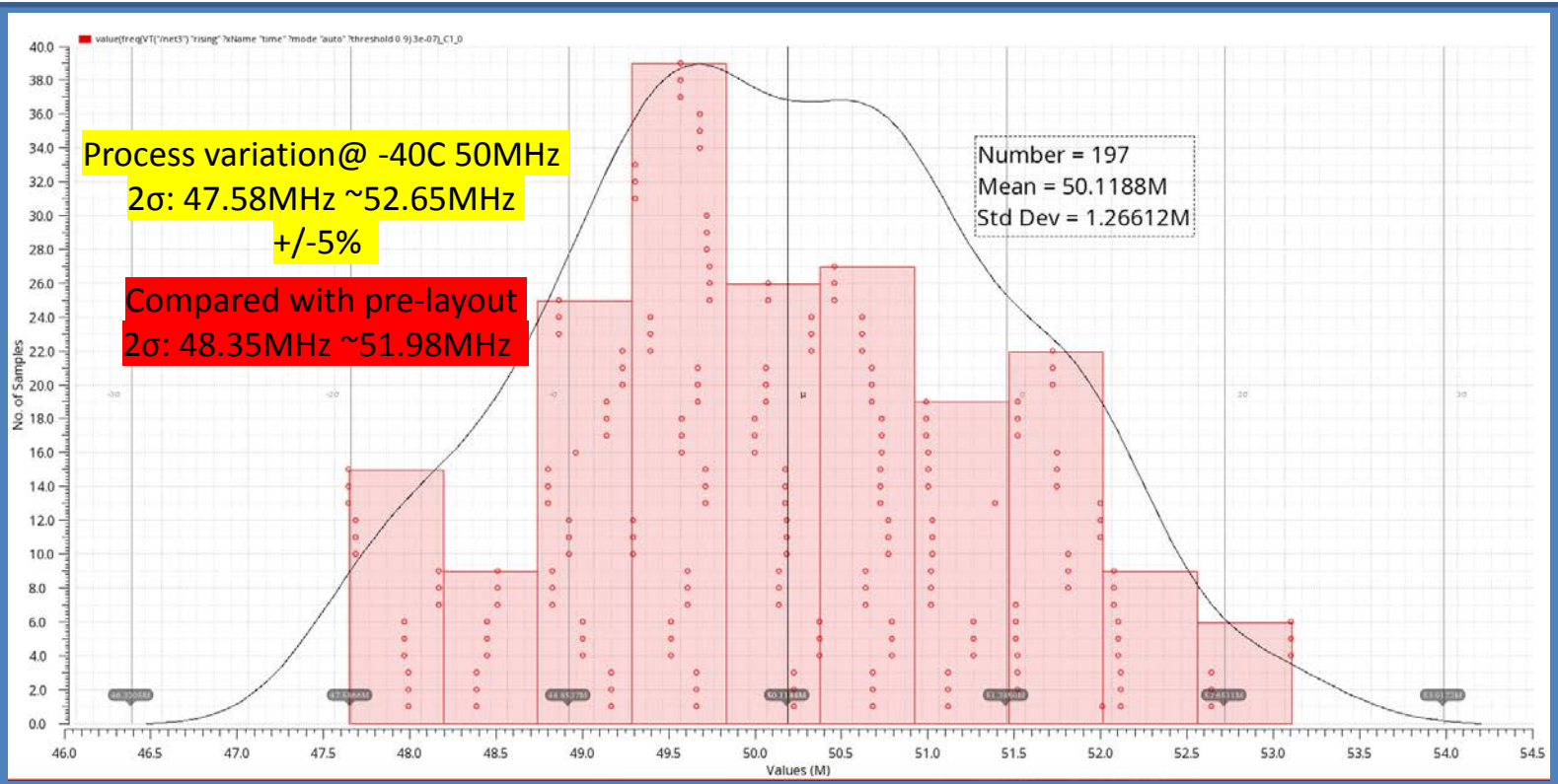
Layout size: 61.56um * 25.48um



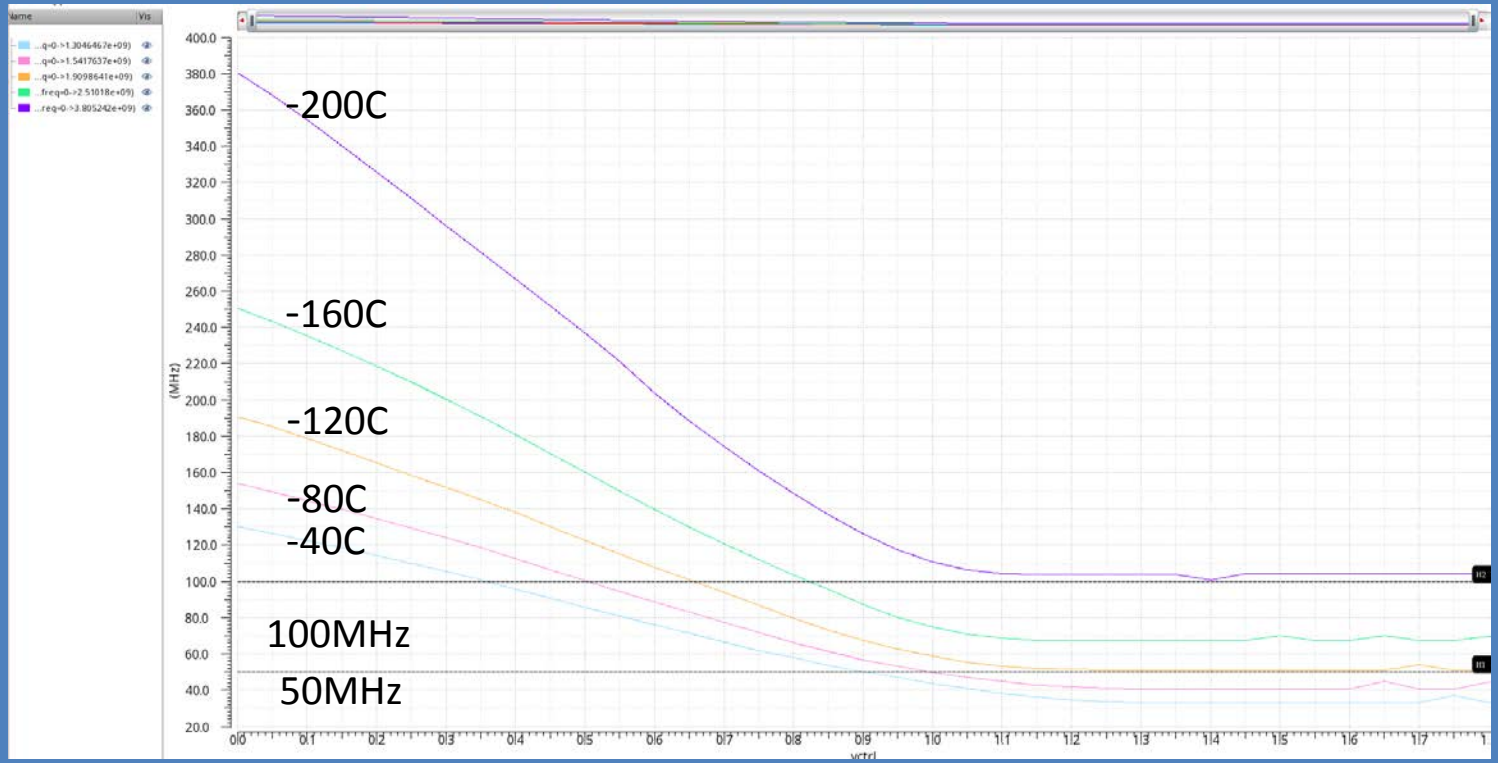


Delay cell

Ring Oscillator



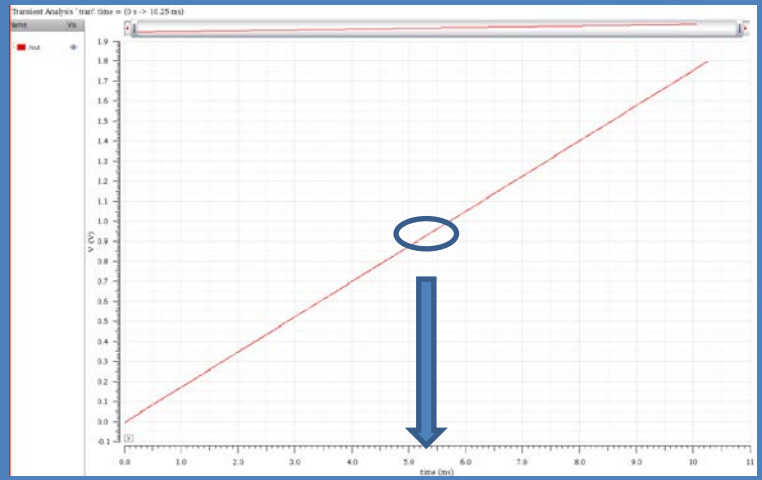
Ring Oscillator

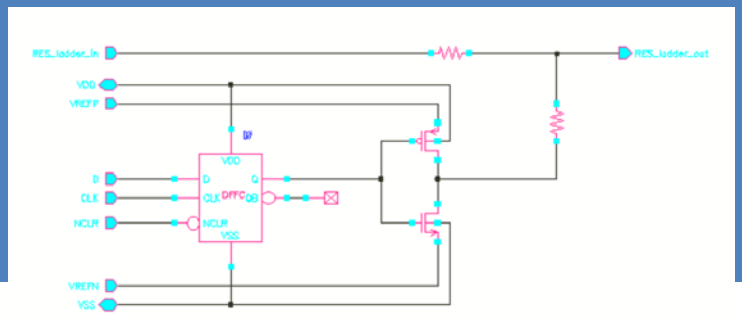


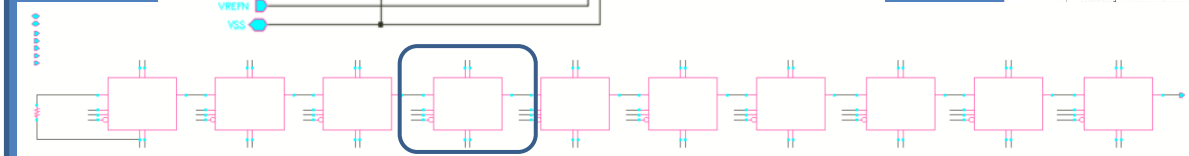
10-bit R2R DAC

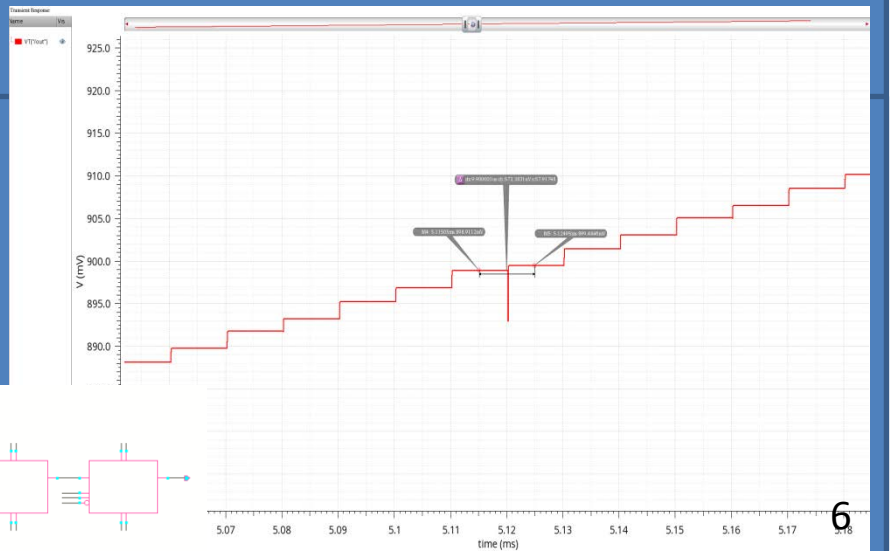
- R2R structure, low power consumption
- Based on 1-bit DAC, cascade to 10 bit
- Worst case happens in the middle of the range, when all the input digits flip.

Quiescent power: 123uA (0.22mW) @ -40C

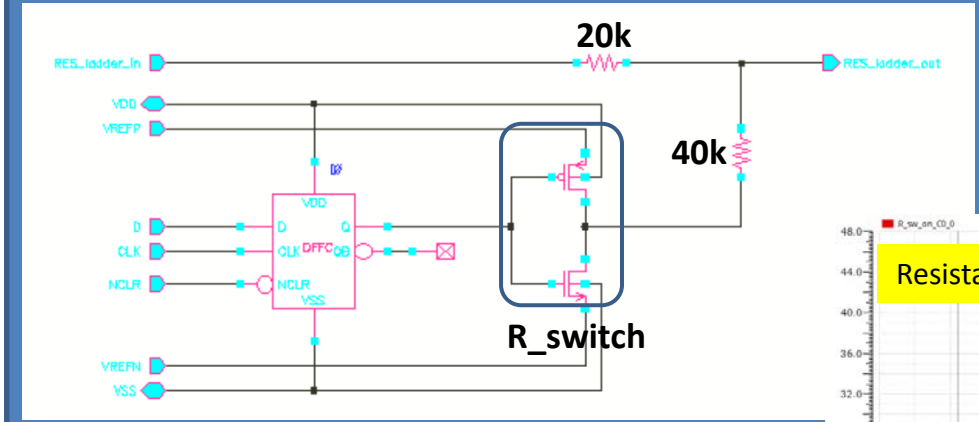


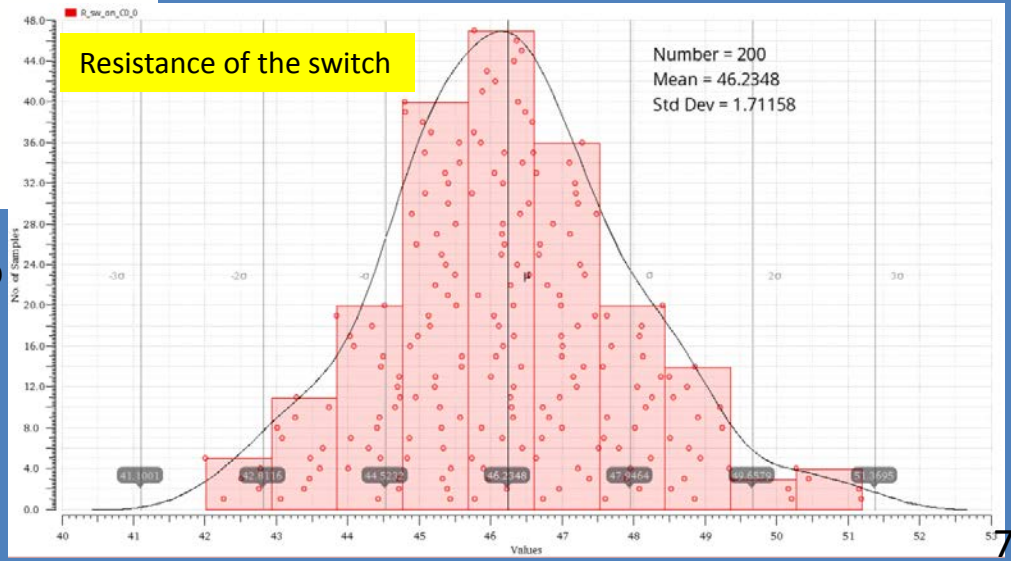






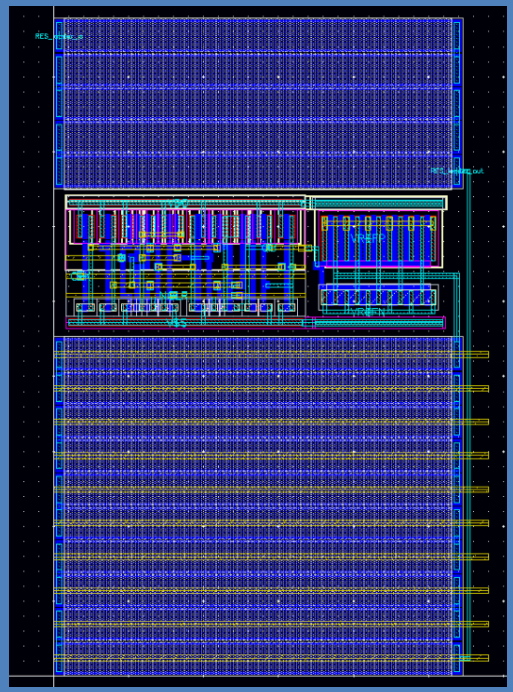
1-bit R2R DAC

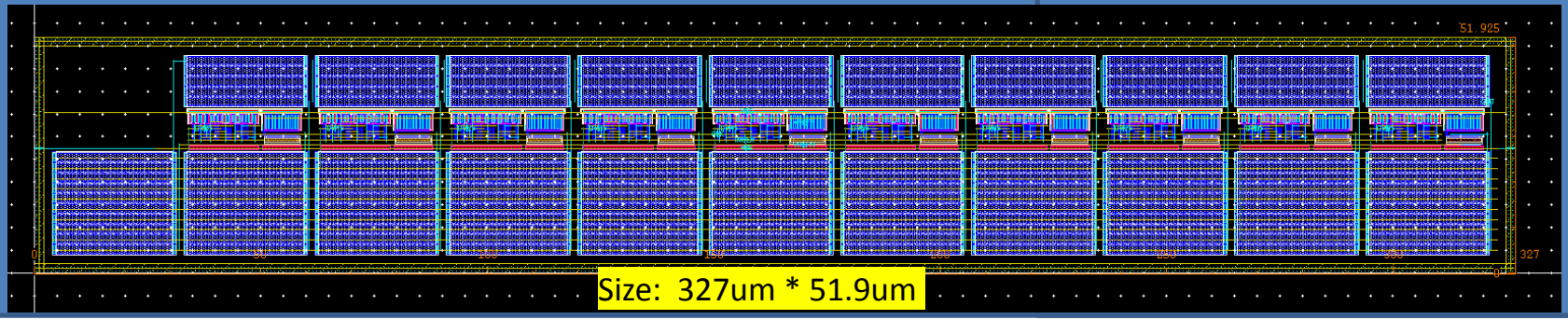




- Two relatively large resistors are chosen to ignore the resistance of the switch.
- R_switch= 46.2ohm, only 0.12% of 40k, could be ignored.

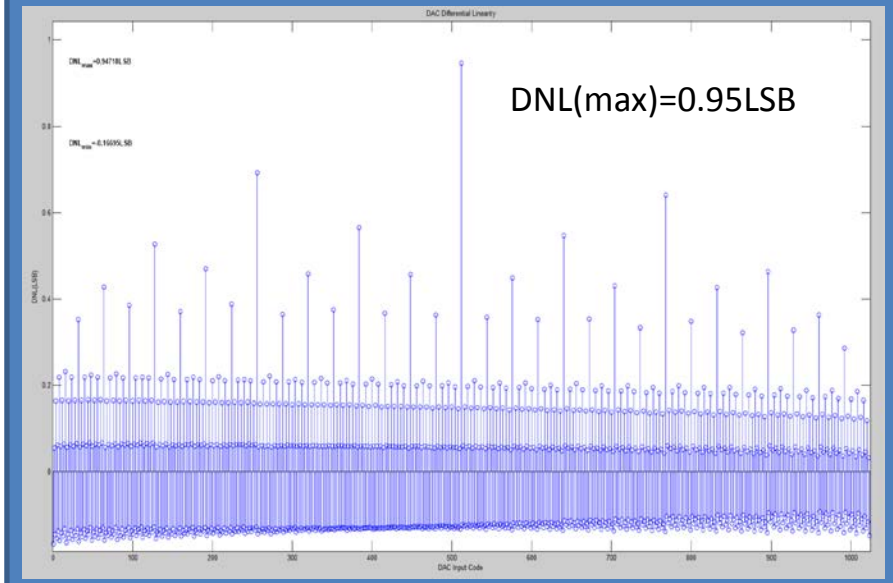
10-bit R2R DAC



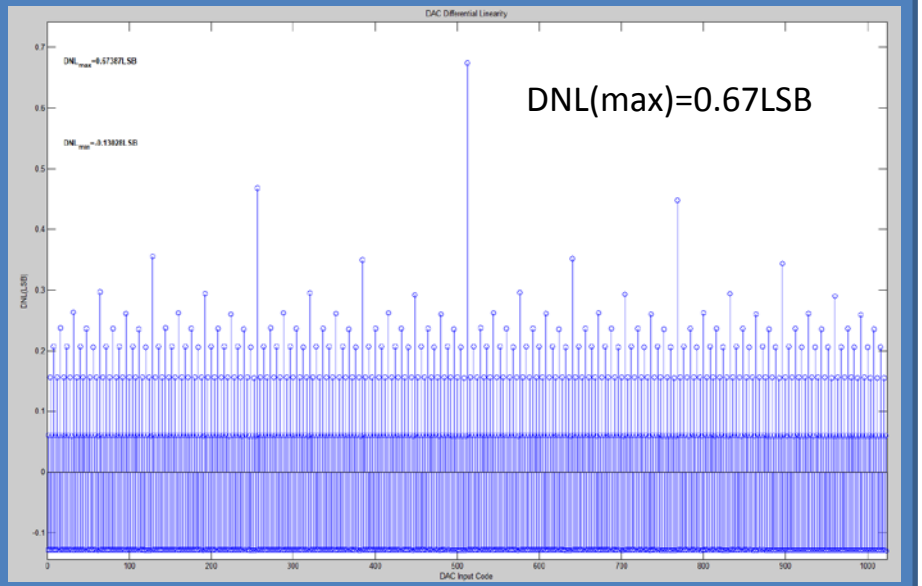


Size: 327um * 51.9um

10-bit R2R DAC

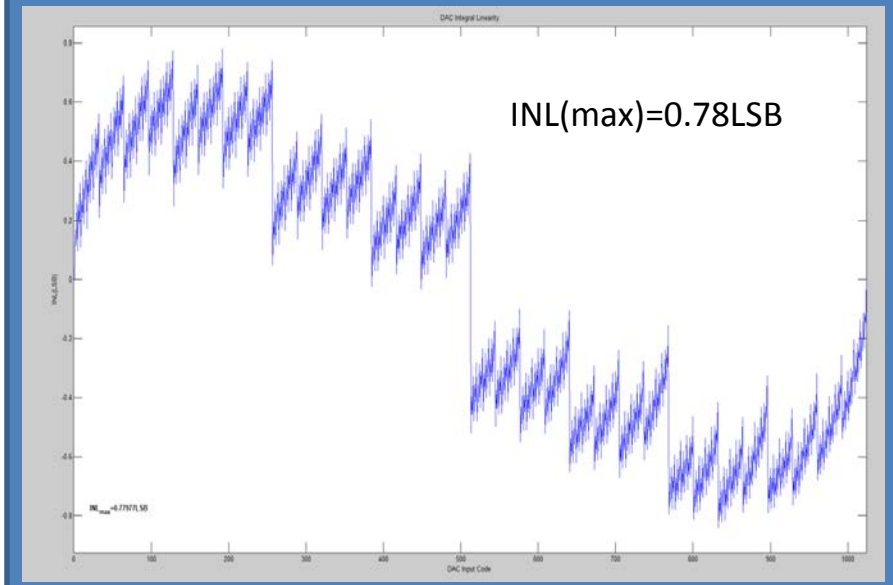


Post-layout

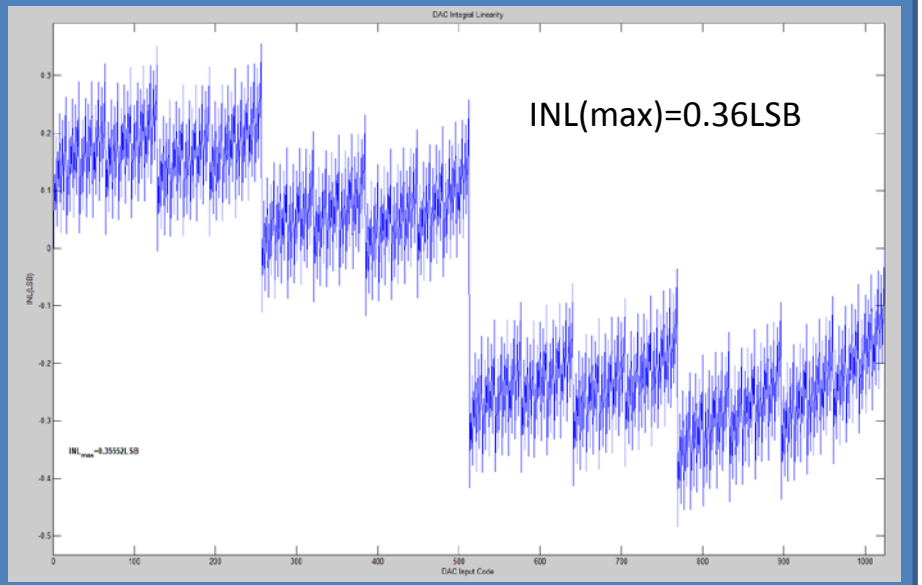


Pre-layout

10-bit R2R DAC



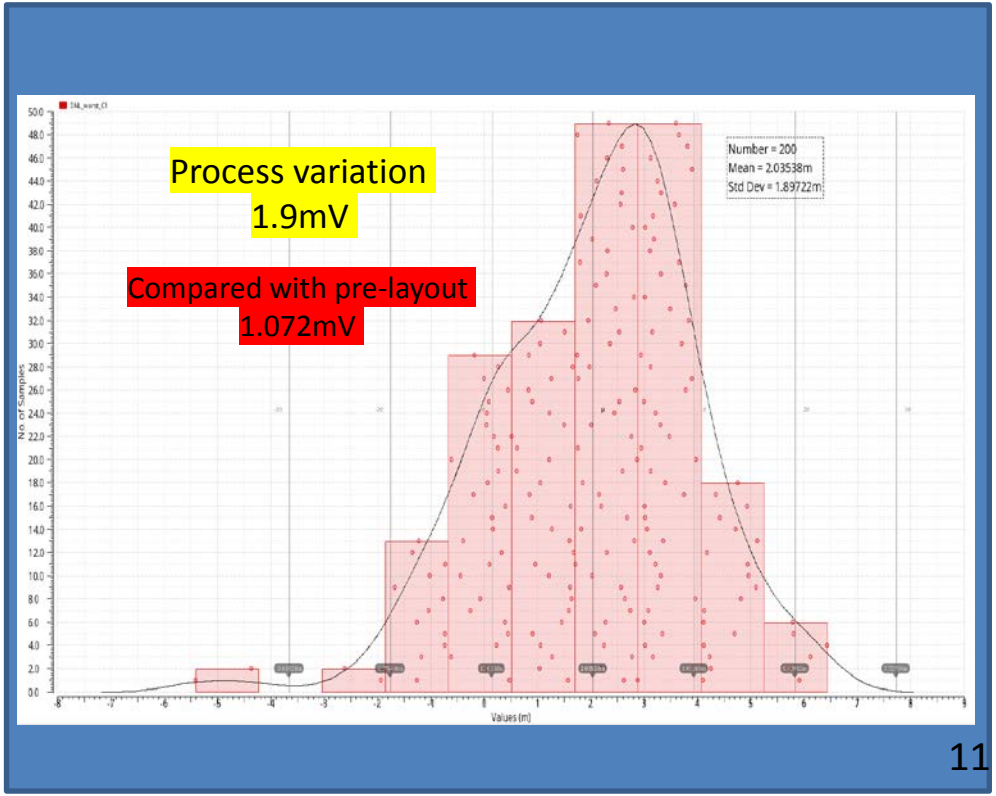
Post-layout



Pre-layout

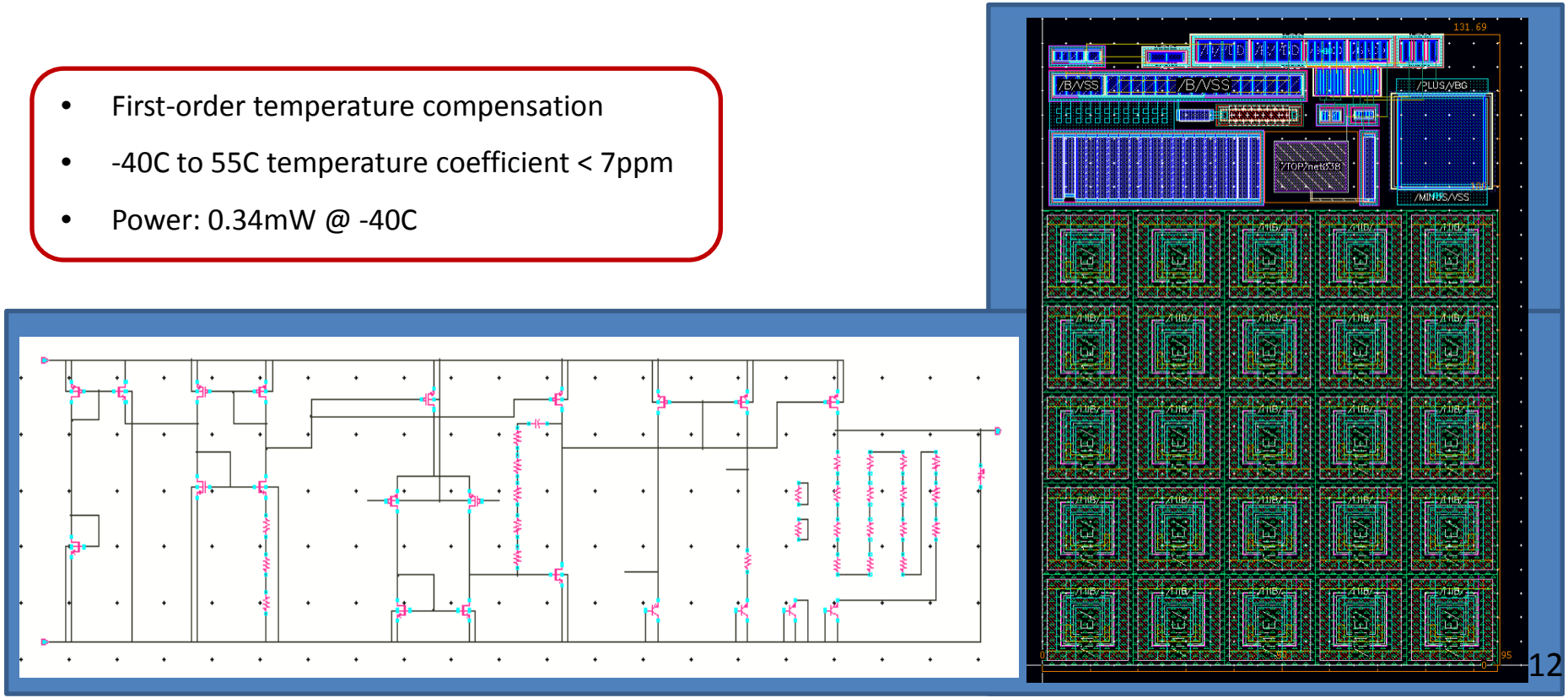
Process variation

- Run monte carlo simulation for the worst case. input=0111111111, 1000000000, 1000000001
- Measure the two steps difference
- The Std Dev is 1.90mV.
- For a 10-bit 1.8V DAC, 1LSB=1.8/1024=1.76mV
- In the worse case 1.90mV could be added to the worst case of DNL
- That's 1.90mV + 1.67mV(0.95LSB)=3.57mV
- 9-bit DAC, 1LSB=3.52mV 8-bit DAC,1LSB=7.03mV
- Worst case 3.52mV<3.57mV<7.03mV, so we still have a 8-bit DAC

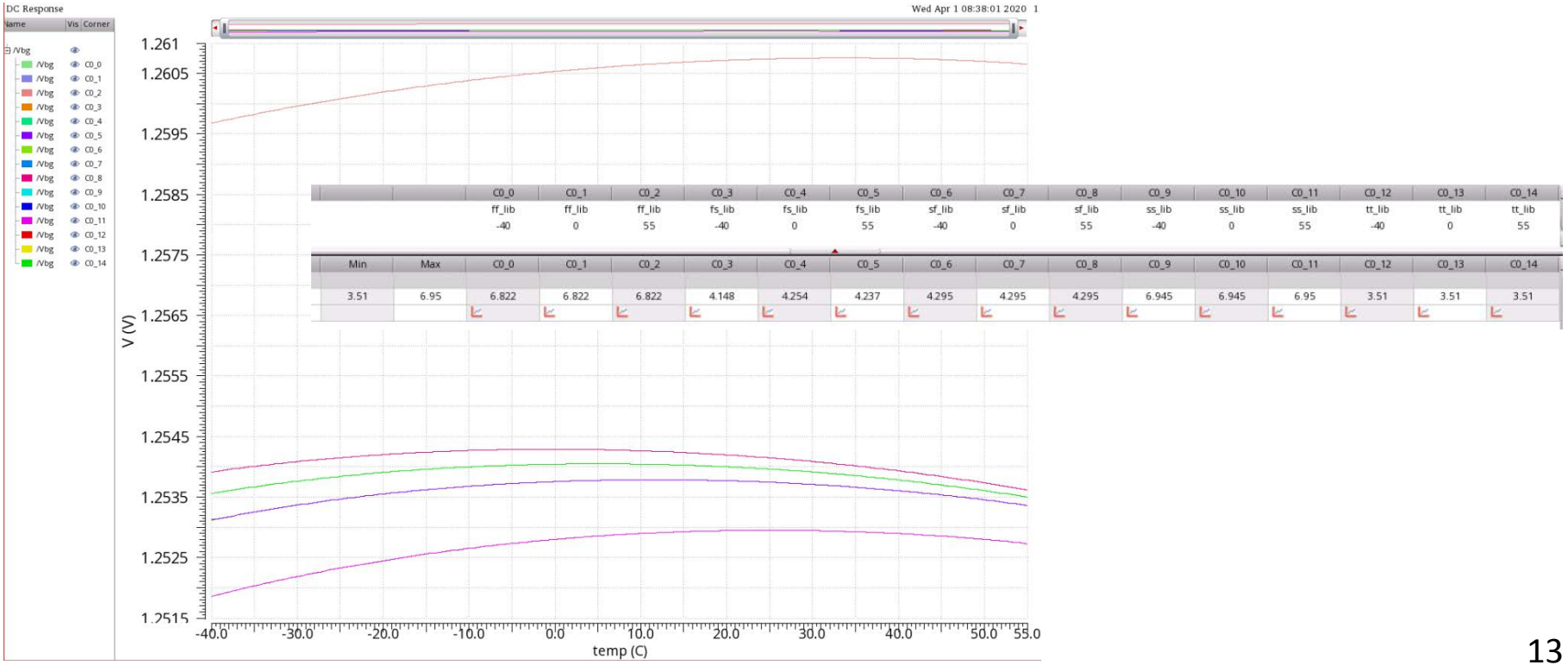


Bandgap

- First-order temperature compensation
- -40C to 55C temperature coefficient < 7ppm
- Power: 0.34mW @ -40C

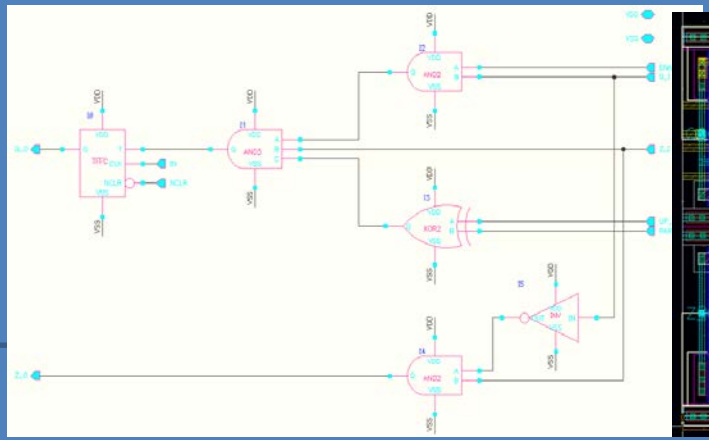


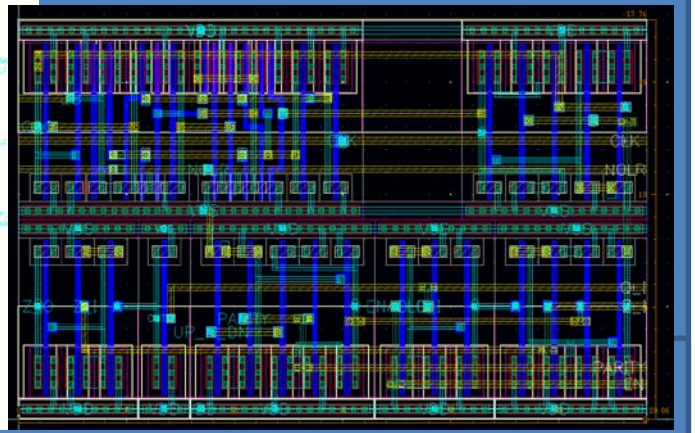
Bandgap

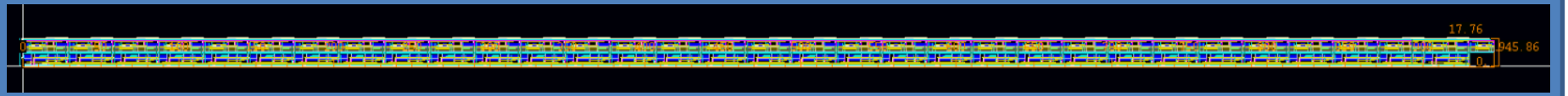

DC Response
Wed Apr 1 08:38:01 2020 1
V (V)
temp (C)
1.261
1.2605
1.2595
1.2585
1.2575
1.2565
1.2555
1.2545
1.2535
1.2525
1.2515
-40.0
-30.0
-20.0
-10.0
0.0
10.0
20.0
30.0
40.0
50.0
55.0
C0_0 ff_lib -40
C0_1 ff_lib 0
C0_2 ff_lib 55
C0_3 fs_lib -40
C0_4 fs_lib 0
C0_5 fs_lib 55
C0_6 sf_lib -40
C0_7 sf_lib 0
C0_8 sf_lib 55
C0_9 ss_lib -40
C0_10 ss_lib 0
C0_11 ss_lib 55
C0_12 tt_lib -40
C0_13 tt_lib 0
C0_14 tt_lib 55
Min 3.51
Max 6.95
C0_0 6.822
C0_1 6.822
C0_2 6.822
C0_3 4.148
C0_4 4.254
C0_5 4.237
C0_6 4.295
C0_7 4.295
C0_8 4.295
C0_9 6.945
C0_10 6.945
C0_11 6.95
C0_12 3.51
C0_13 3.51
C0_14 3.51

32-bit Gray Code Counter

- 1-bit GCC schematic & layout
- Could be cascaded to 32 bit
- Need a reset signal after one counting cycle
- Custom designed std cell



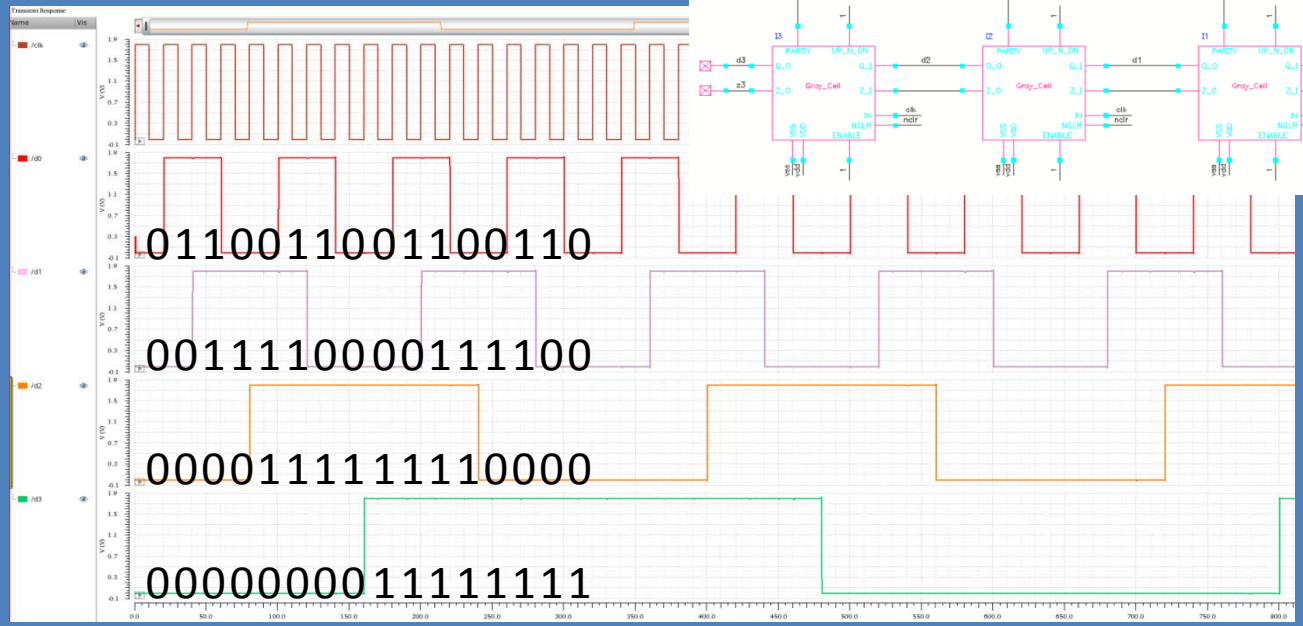


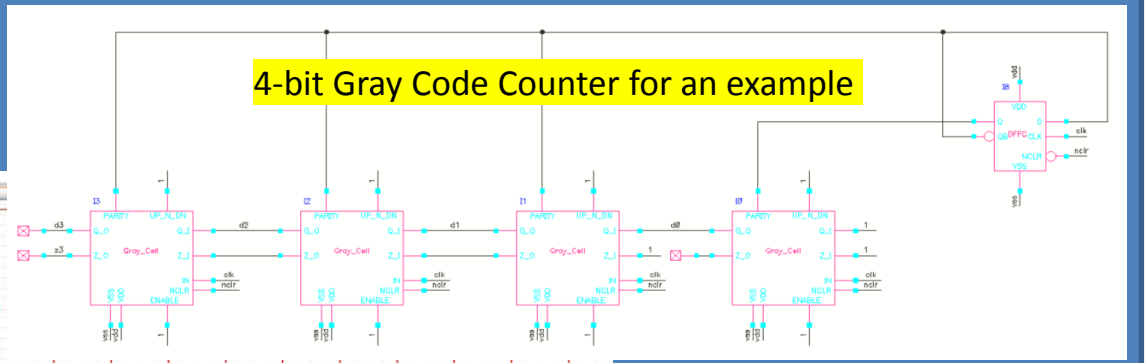


Cascaded 32-bit GCC

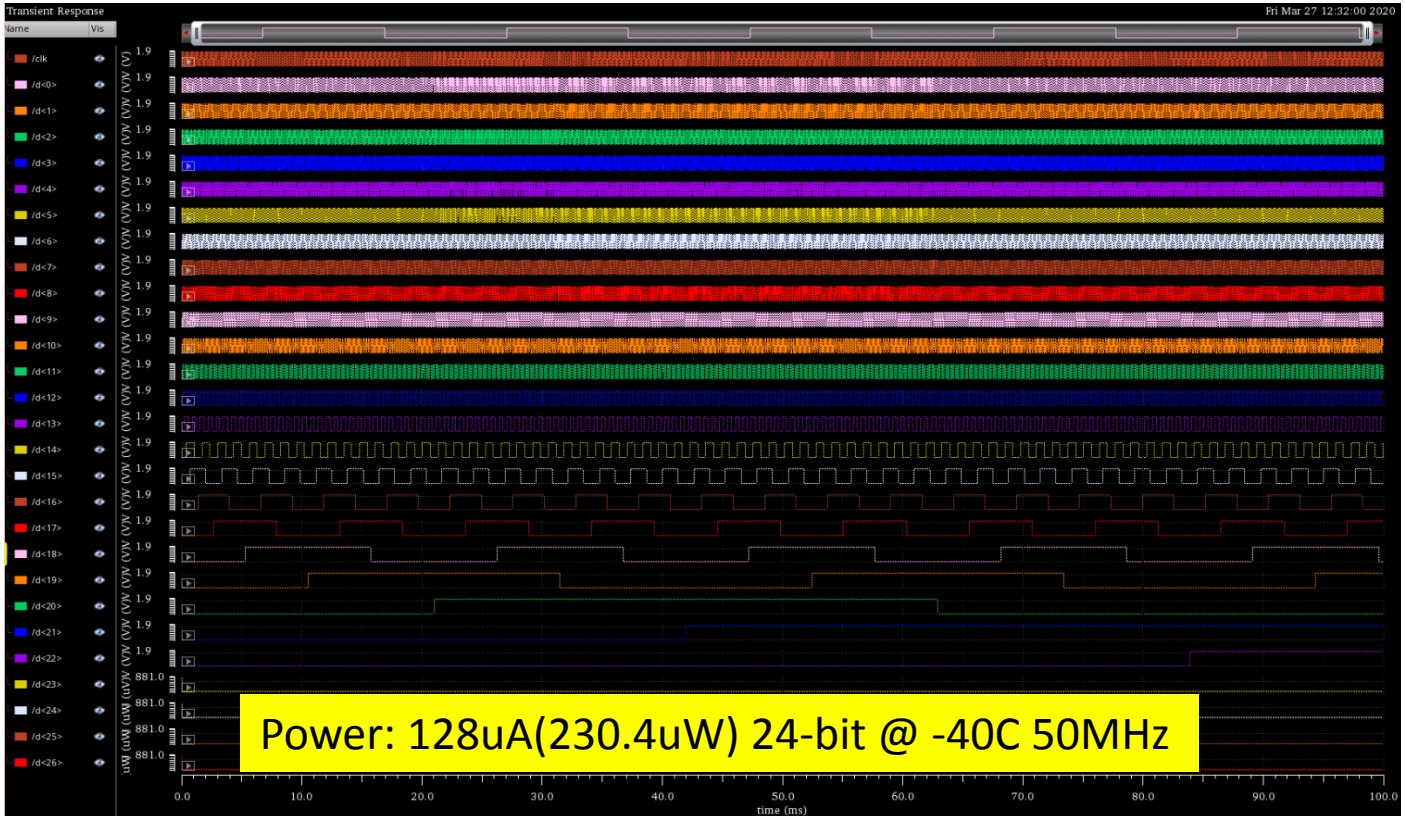
Size: 945.9um * 17.8um

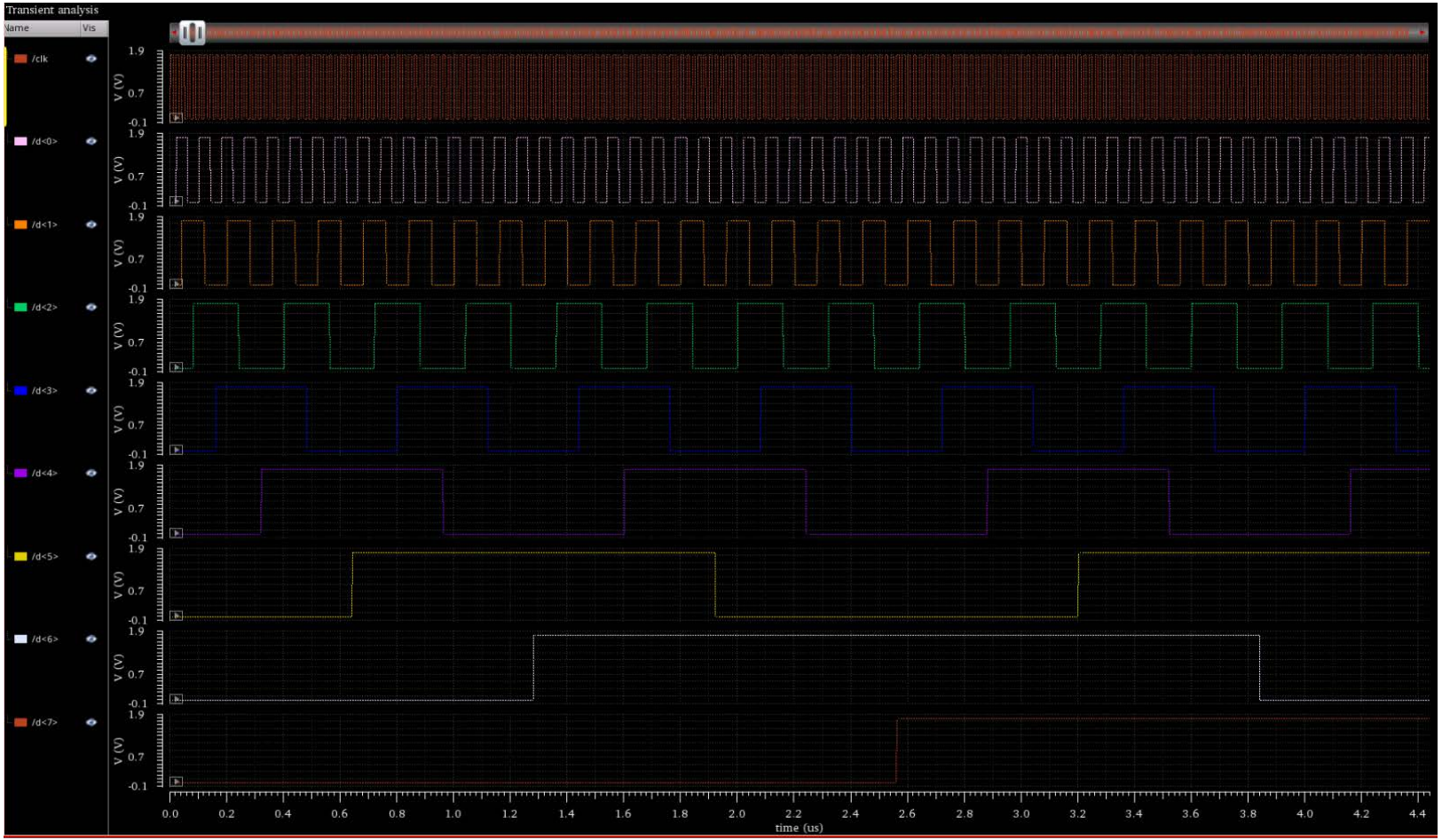
32-bit Gray Code Counter

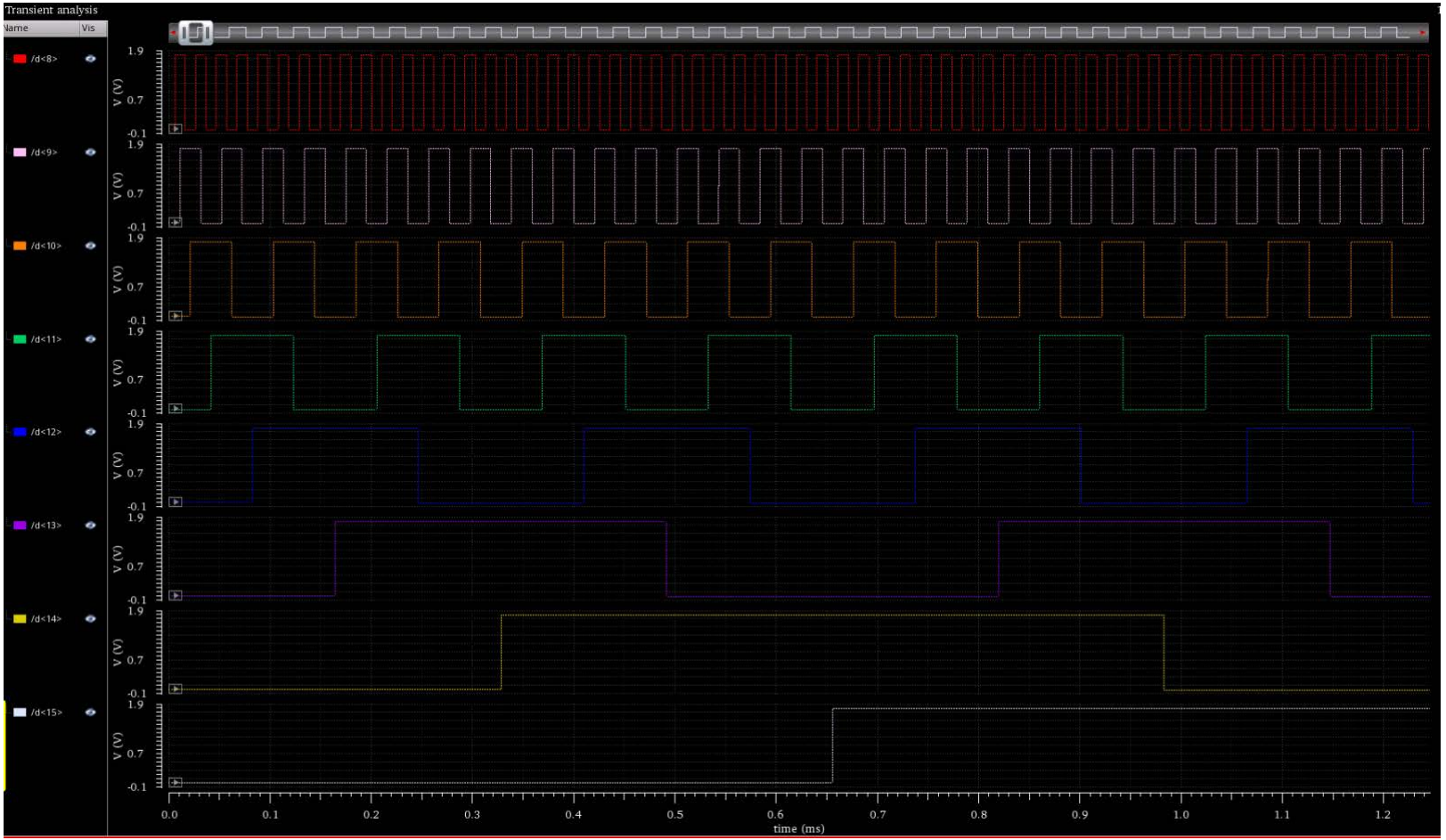




32-bit Gray Code Counter




Transient analysis
Name
Vis
/clk
/d<0>
/d<1>
/d<2>
/d<3>
/d<4>
/d<5>
/d<6>
/d<7>
V (V)
1.9
0.7
-0.1
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
2.8
3.0
3.2
3.4
3.6
3.8
4.0
4.2
4.4
time (us)


Transient analysis
Name
Vis
/d<8>
/d<9>
/d<10>
/d<11>
/d<12>
/d<13>
/d<14>
/d<15>
1.9
0.7
-0.1
V (V)
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
time (ms)

Thank you !