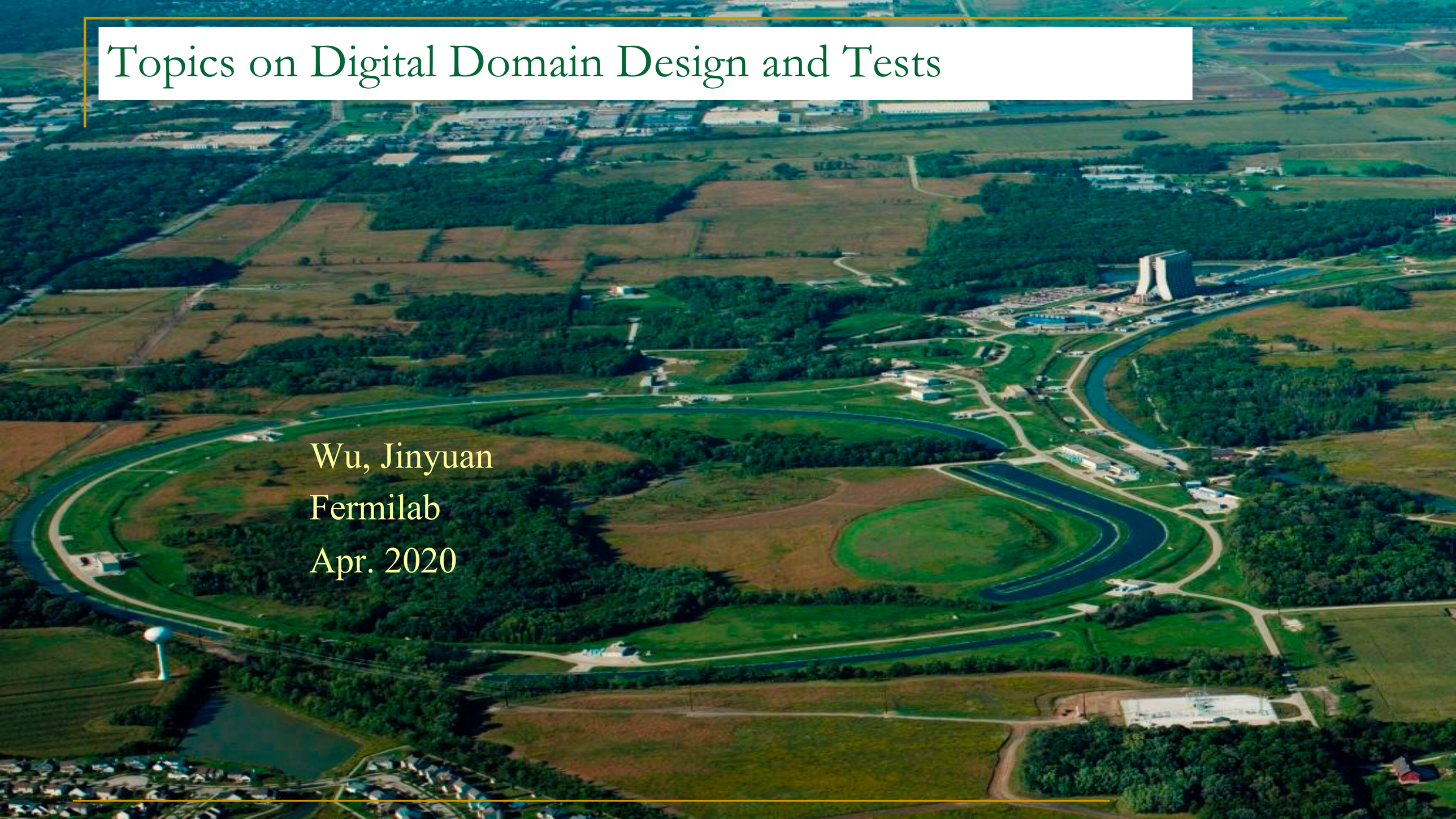
Topics on Digital Domain Design and Tests



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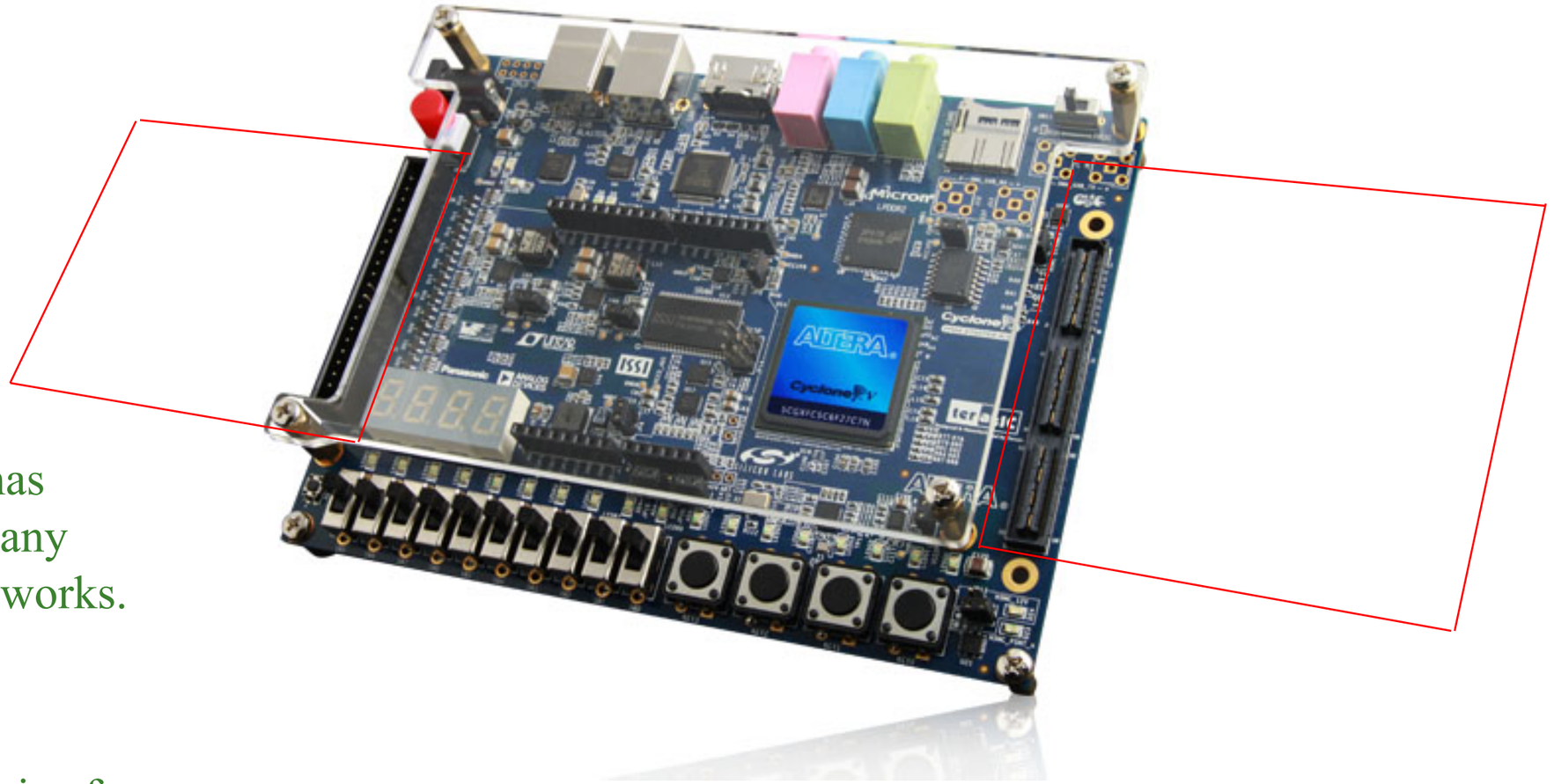
Fermilab
Apr. 2020

Introduction

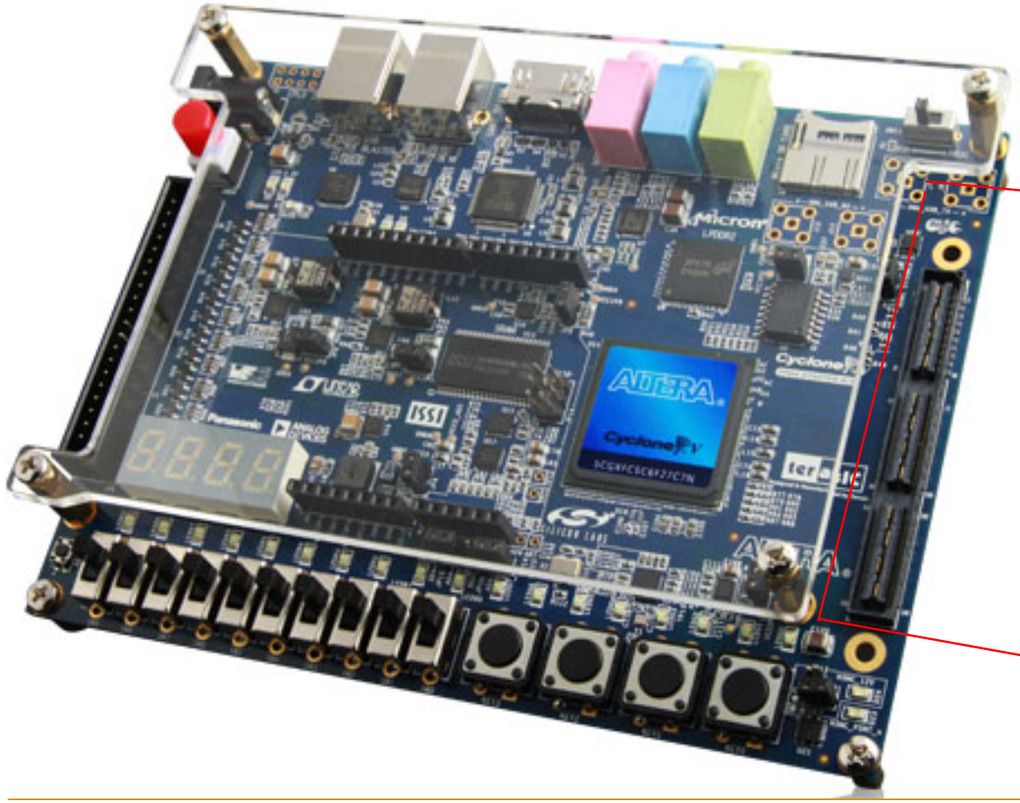
- The C5G Cyclone 5 FPGA Evaluation Module as AISC Tester.
- Inter-chip Communication Tester.
- DAQ for Testers.
- Design Practices for Reducing TDC Power Consumption.

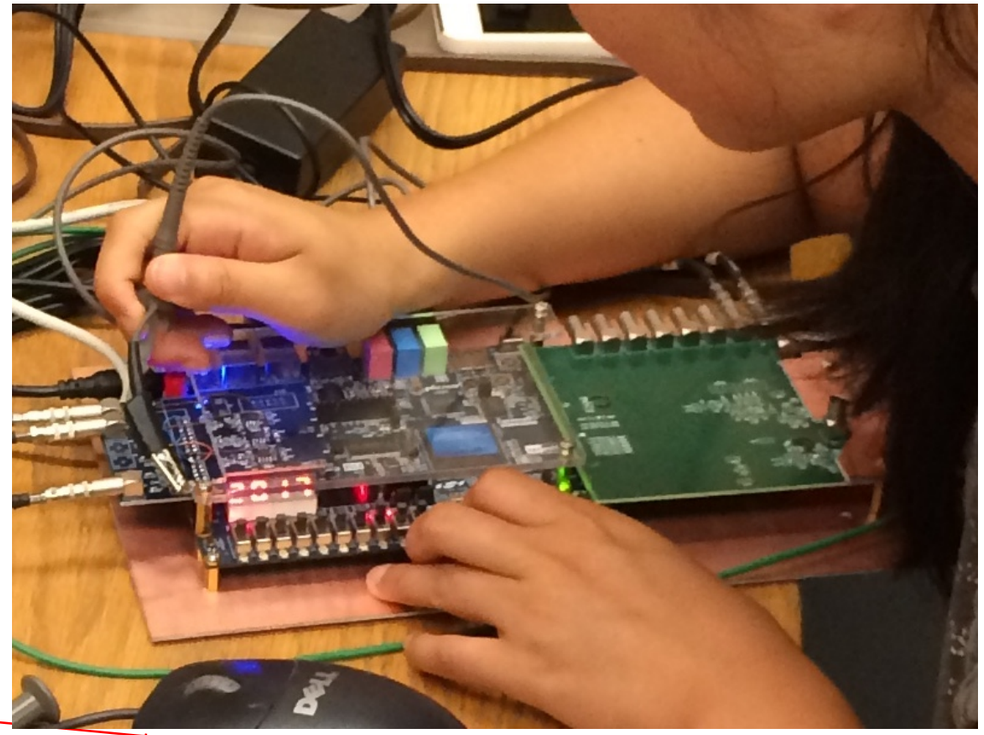
The C5G Cyclone 5 FPGA Evaluation Module



- The evaluation module has sufficient resource for many implementation and test works.
- $179 ea.
- I have two in hand.
- It could be a possible choice for ASIC tester and inter-chip communication tester

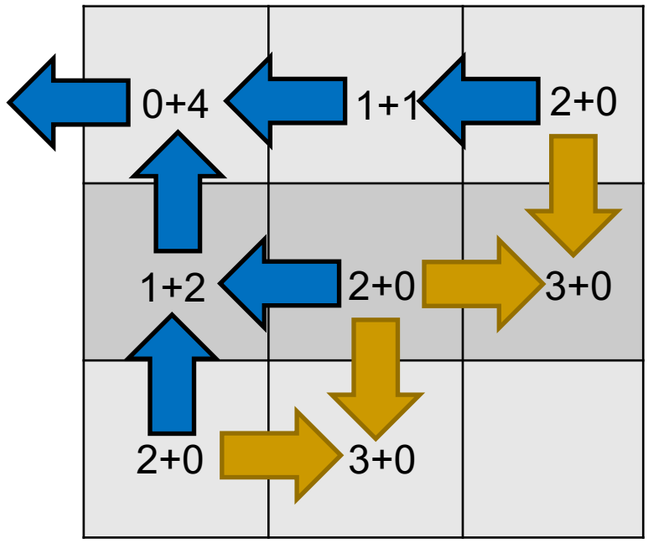
A Possible ASIC Tester



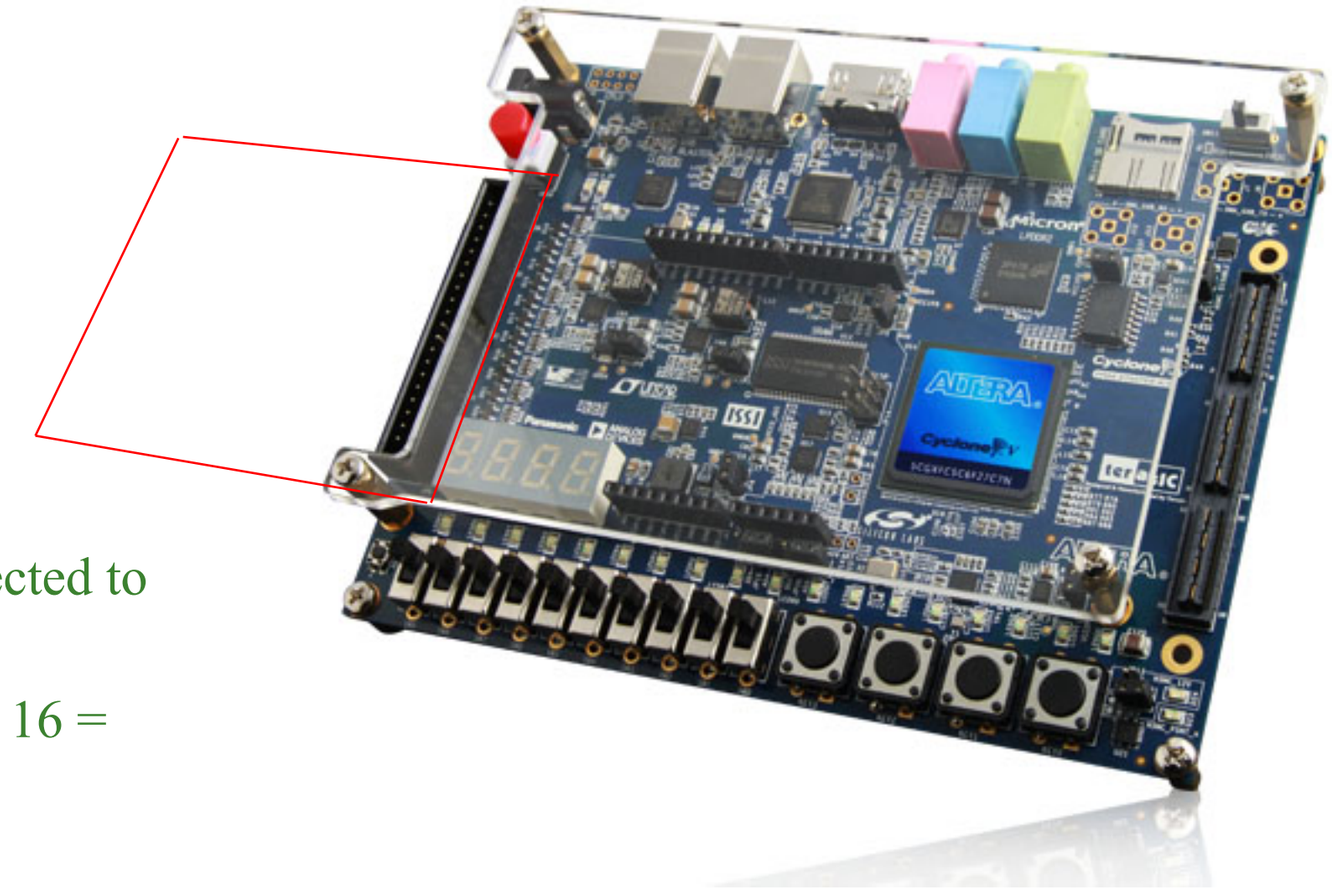


- A simple PCB (about 4 in. x 4 in.) with an HSMC connector is designed to carry the ASIC.
- All digital supporting functions including TDC are implemented inside the FPGA.

A Possible Inter-Chip Communication Tester



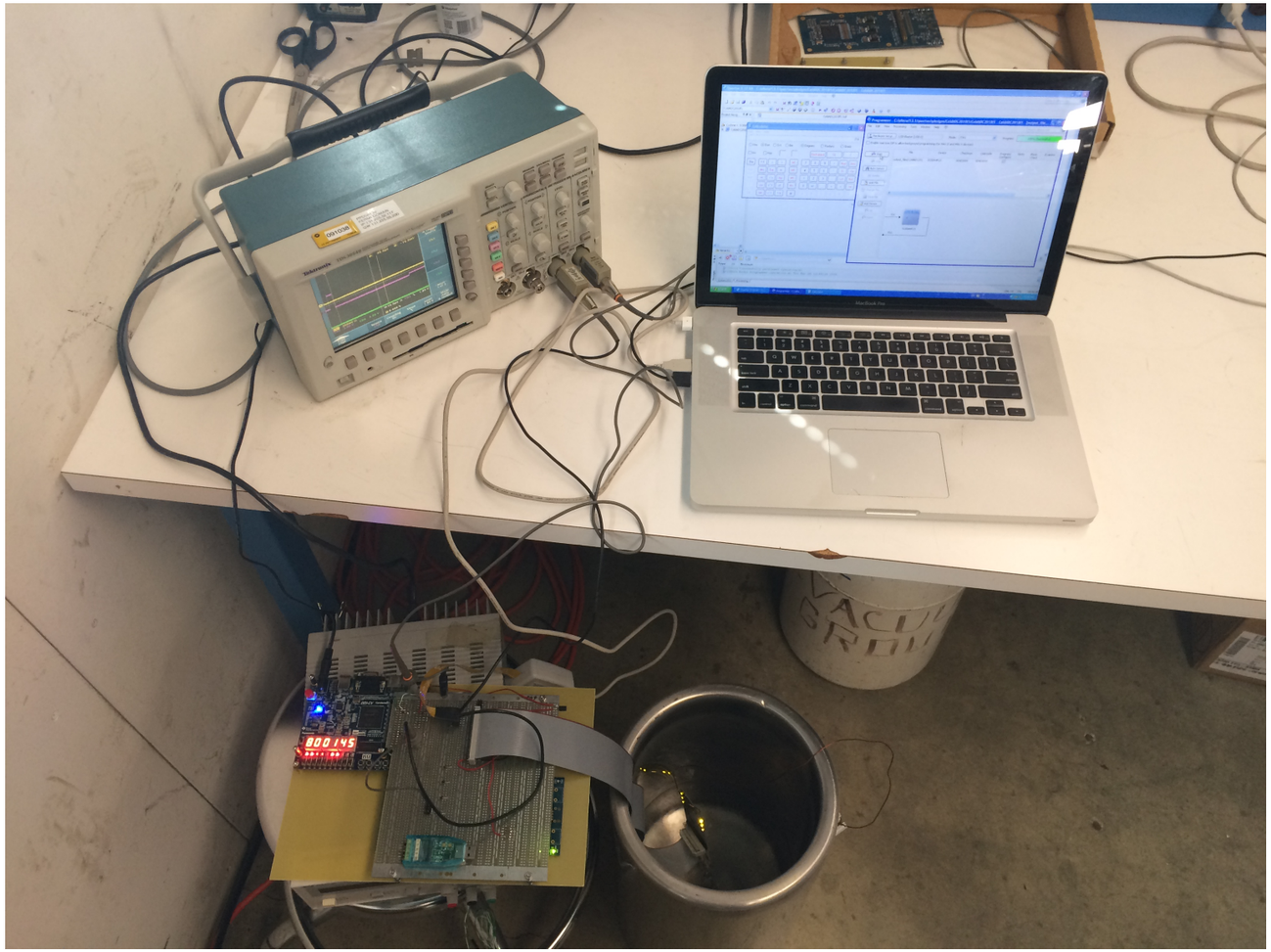
From U. Hawaii Group



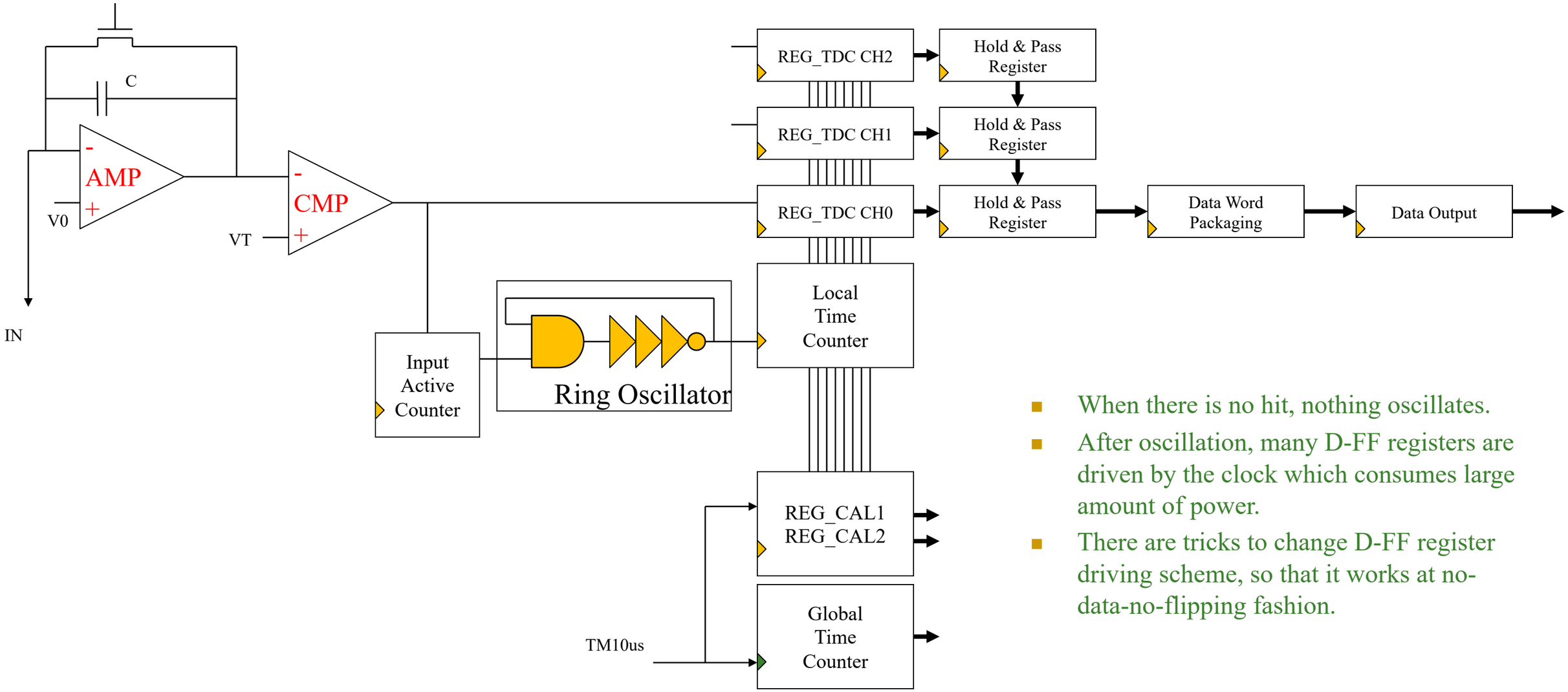
- The evaluation module can be interconnected to emulate AISC interconnections.
- For a 4 x 4 array, the total cost is: $179 x 16 = $2.8 K.

DAQ Supports Wanted

- Test stands can run with USB for quick evaluation.
- Wish list: It will be best if some simplified DAQ system becomes available at the test stand stage.



Lowering TDC Power

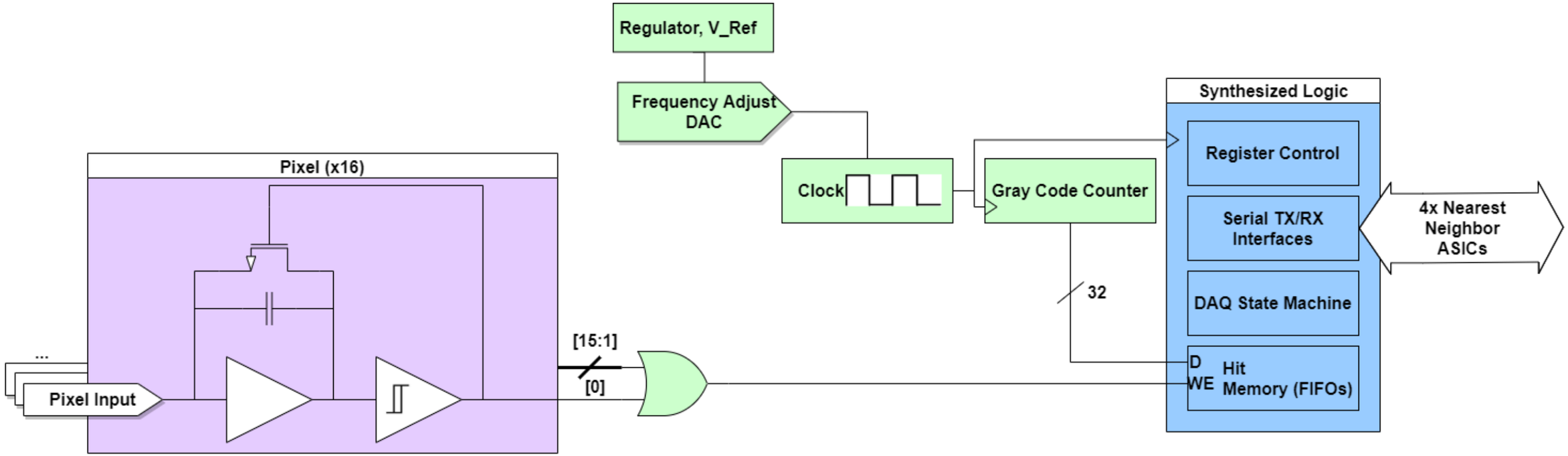


- When there is no hit, nothing oscillates.
- After oscillation, many D-FF registers are driven by the clock which consumes large amount of power.
- There are tricks to change D-FF register driving scheme, so that it works at no-data-no-flipping fashion.

Summary

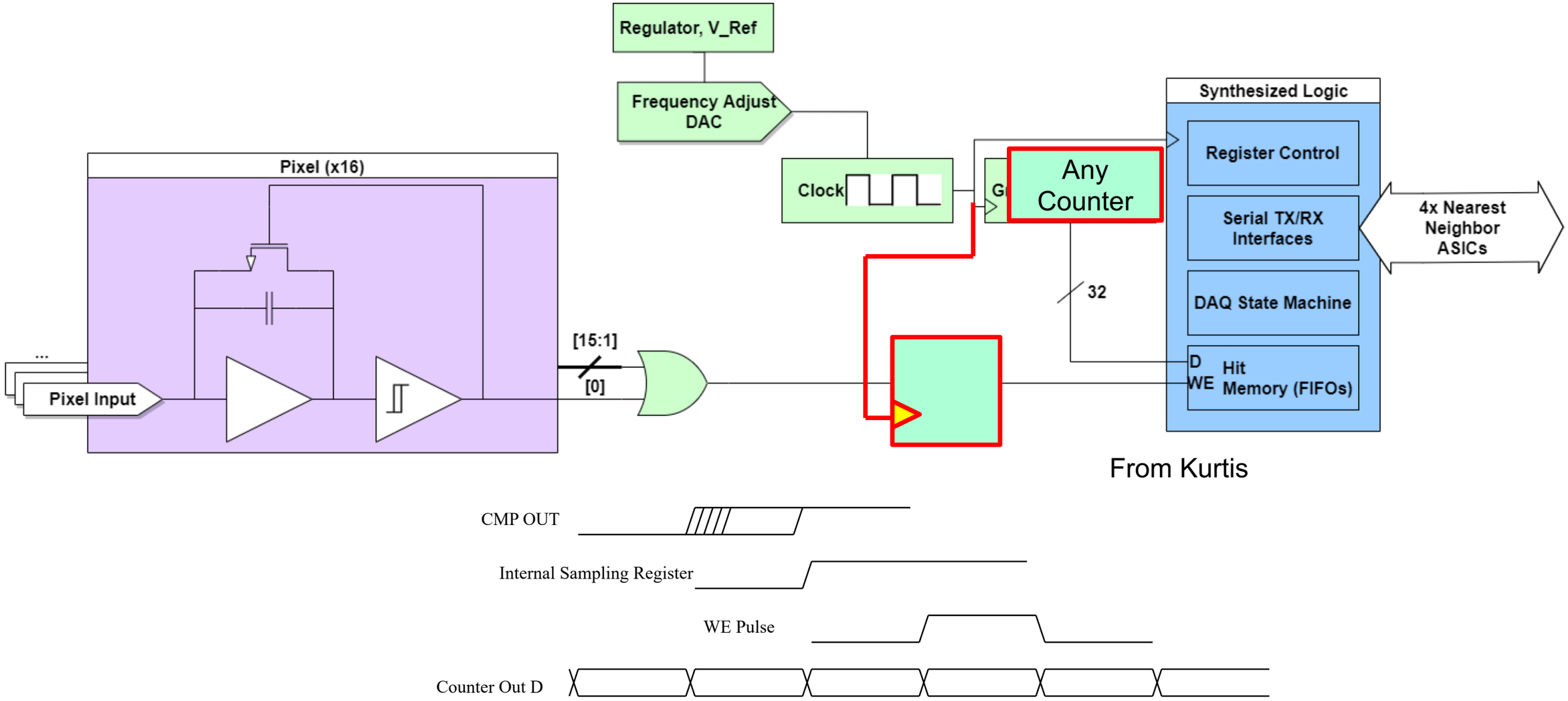
- The C5G Cyclone 5 FPGA Evaluation Module as AISC Tester.
- Inter-chip Communication Tester.
- DAQ for Testers. (A wish list item)
- Design Practices for Reducing TDC Power Consumption. (Wish: simulation of power consumption in 180 nm.)

Q-Pix BLOCK Design

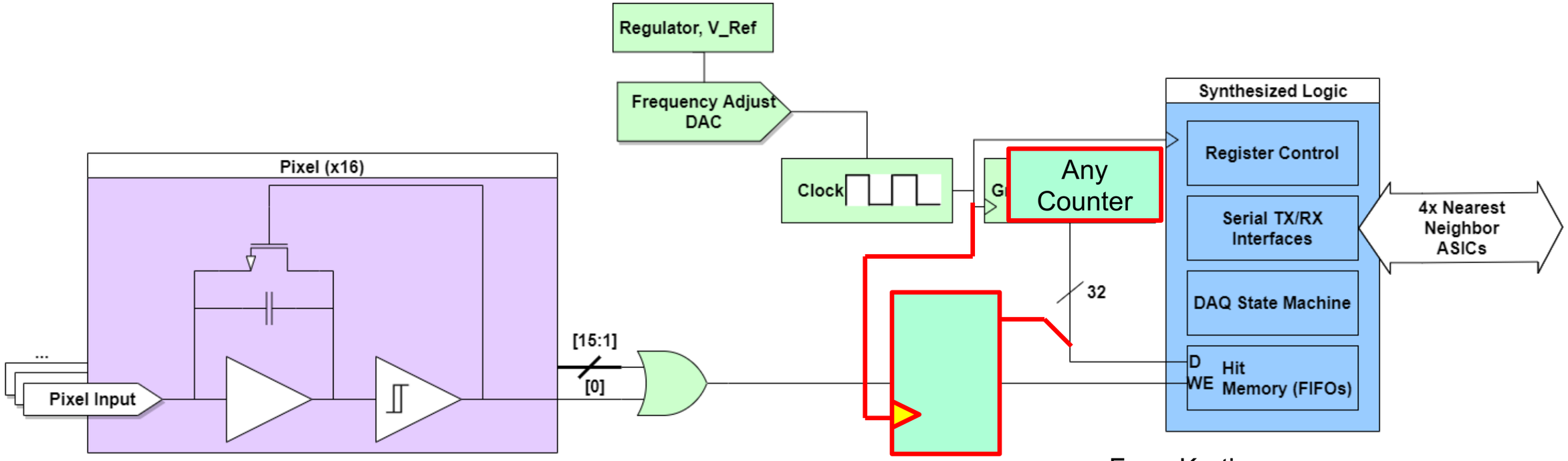


From Kurtis

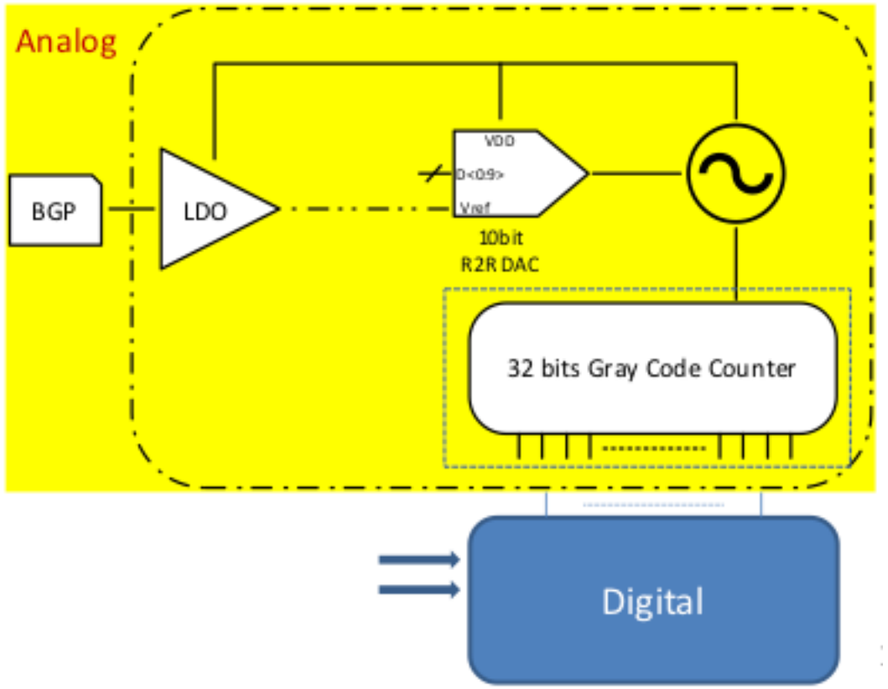
Re-Synchronize the Hit Input



Re-Synchronize the Hit Input



High Stability Clock?



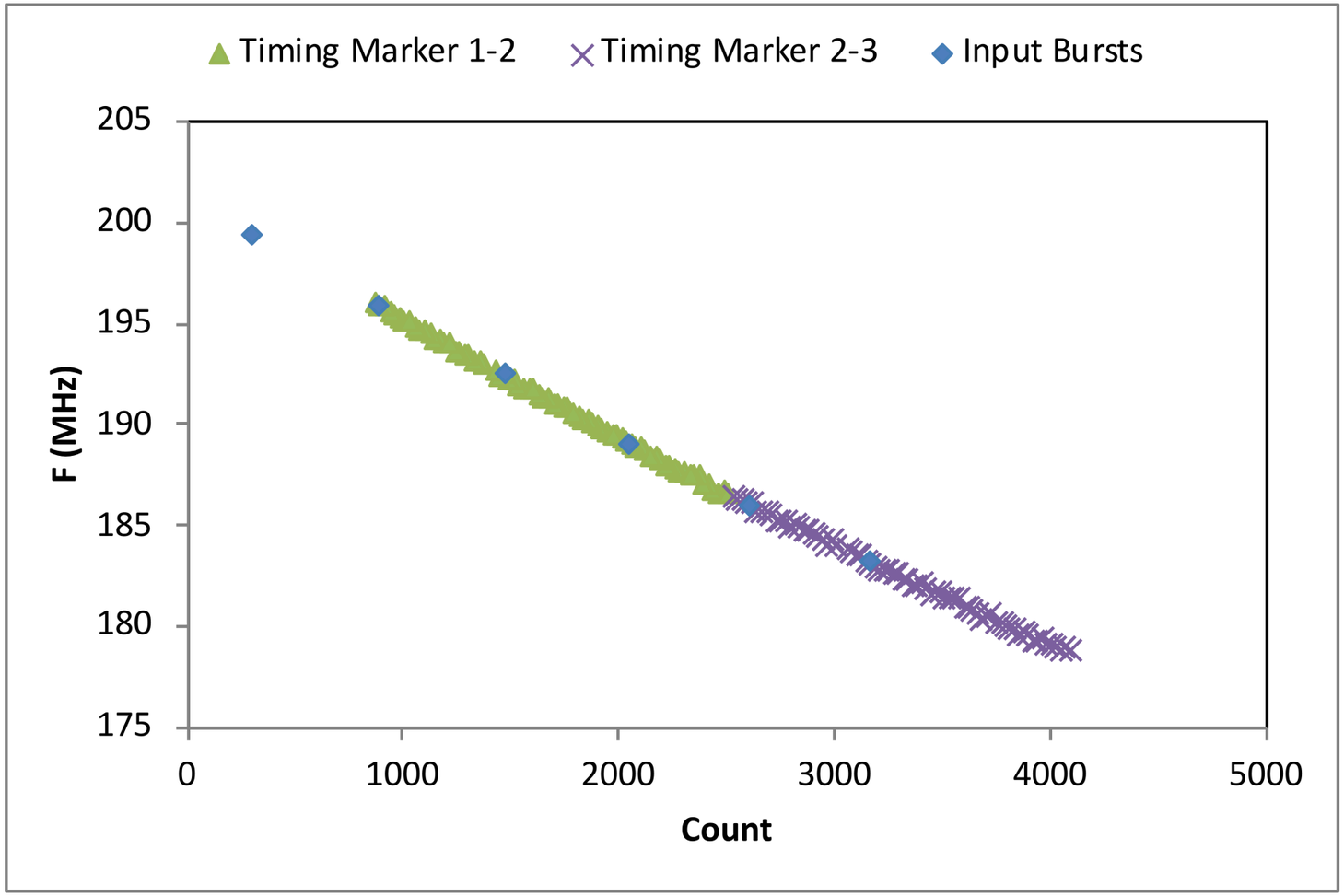
Component	Schematic	Layout	power
Ring oscillator	Done	Done	0.36mW
GCC	Done	Done	~0.23mW
DAC	Done	Done	0.22mW
Bandgap	Done	Done	0.34mW
Regulator	In process	In process	TBT
			Total: 0.36+0.23+ 0.22+0.34+Reg =1.15mW+Reg per ASIC

From Gang

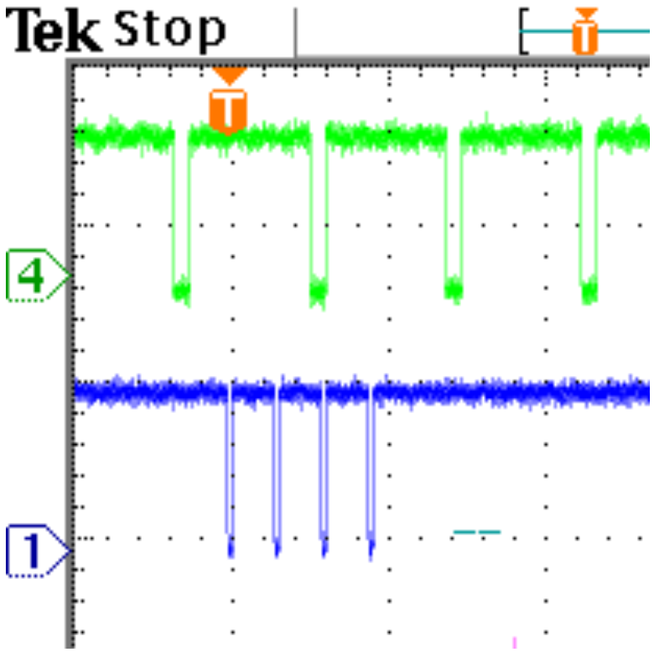
- Power Budget: 3.2 mW for 32 channel ASIC. (From LArPix number)
- Save power on digital backend so that more power can be used in front-end.

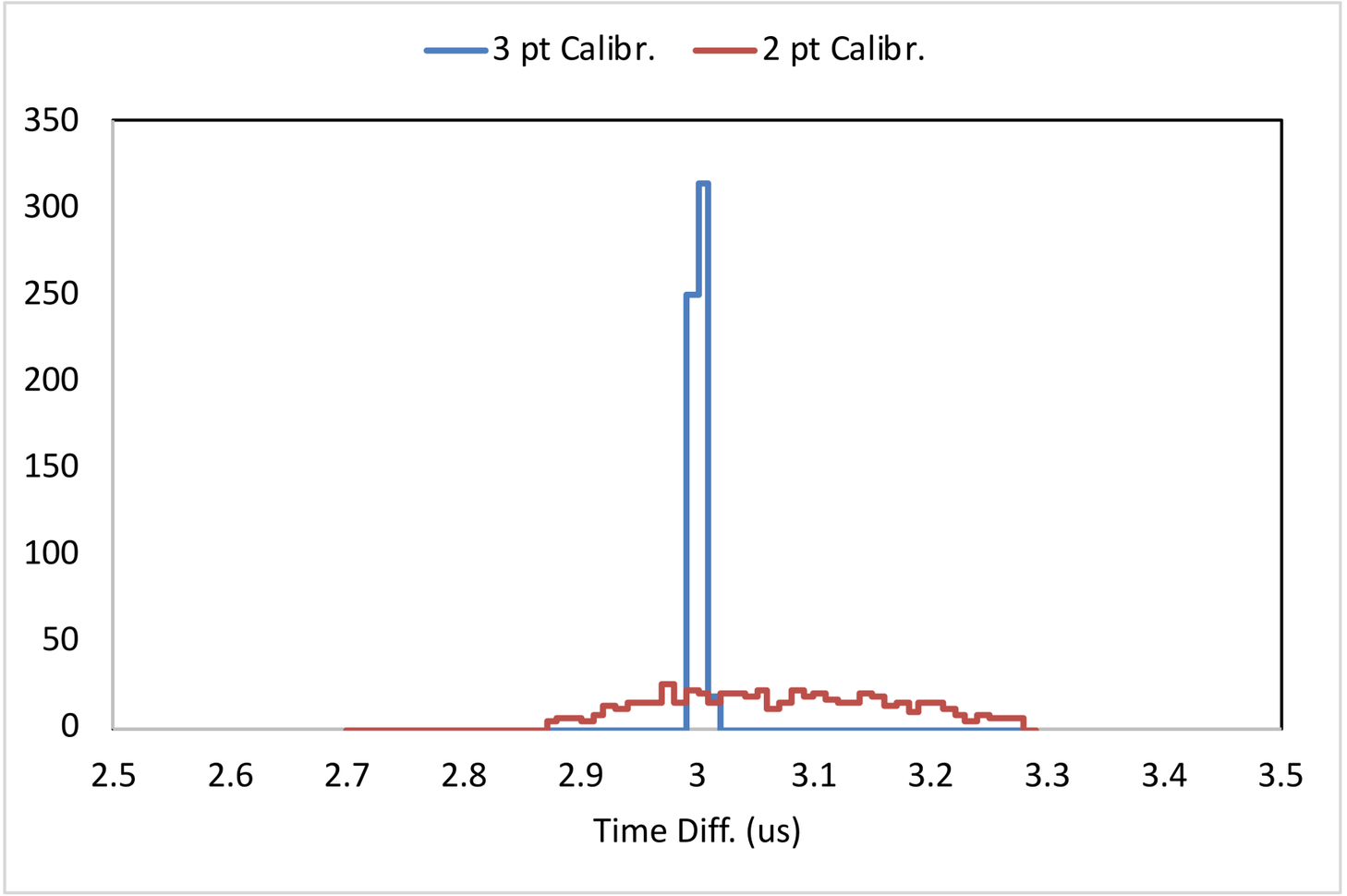
Ring Oscillator Slowing Down

- After startup, the ring oscillator slows down.
- The frequency drops at a rate of 5% per 10 us.
- The reason could be transistor heat up, or core voltage drop. (Discussed with Paul R., Gary D. and Gary V.)



Three-point Calibration vs Two-point Calibration





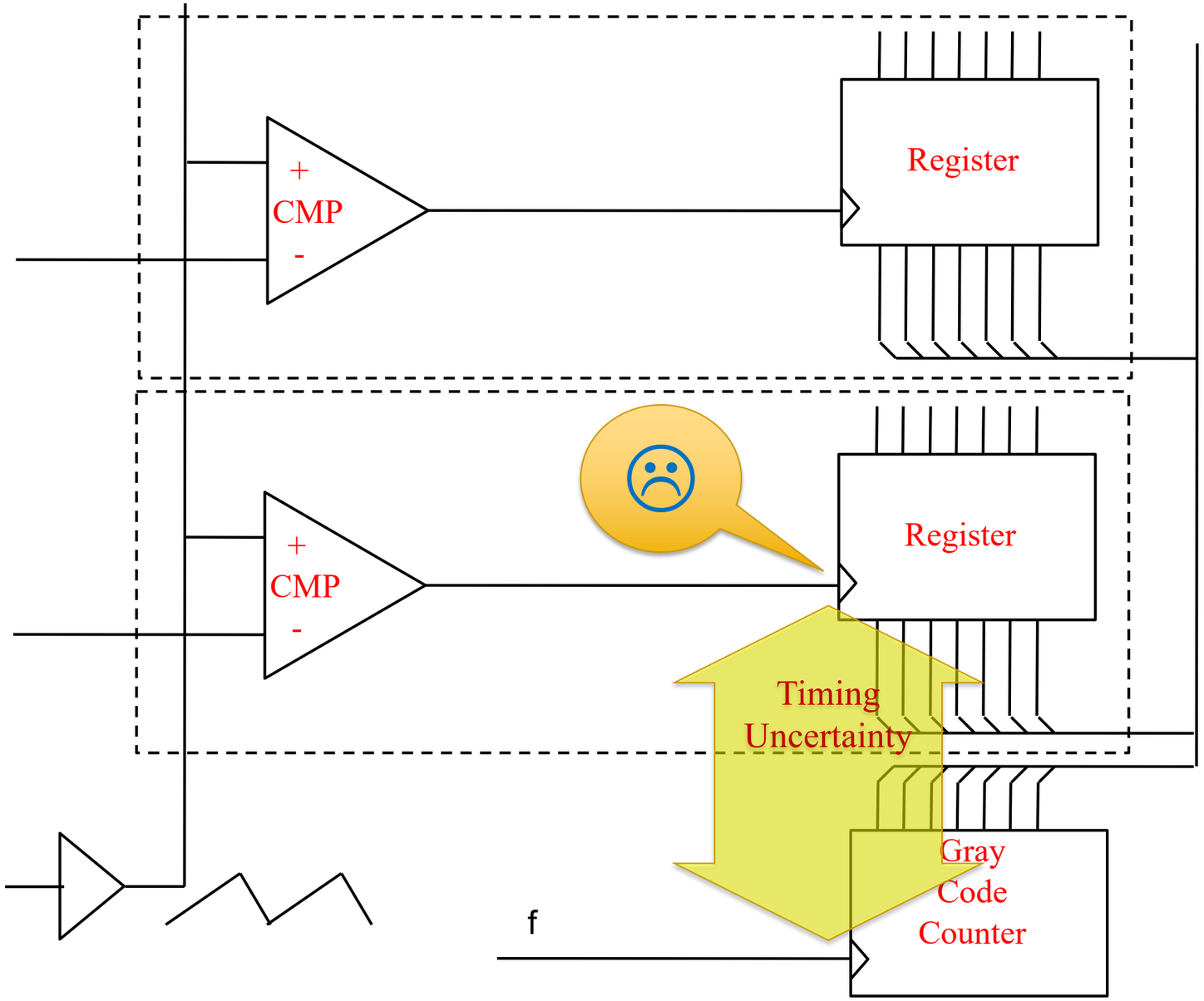
- Since the ring oscillator slows down, three timing marker are used for calibration.
- The time difference (3us) between the input burst are calculated.
- With three-point calibration, RMS is 4 ns.
- With two-point calibration, RMS is 98 ns.

Suggestions

- Rethink the architecture before working deep into the details.
- A few zoom meetings?


The End
Thanks

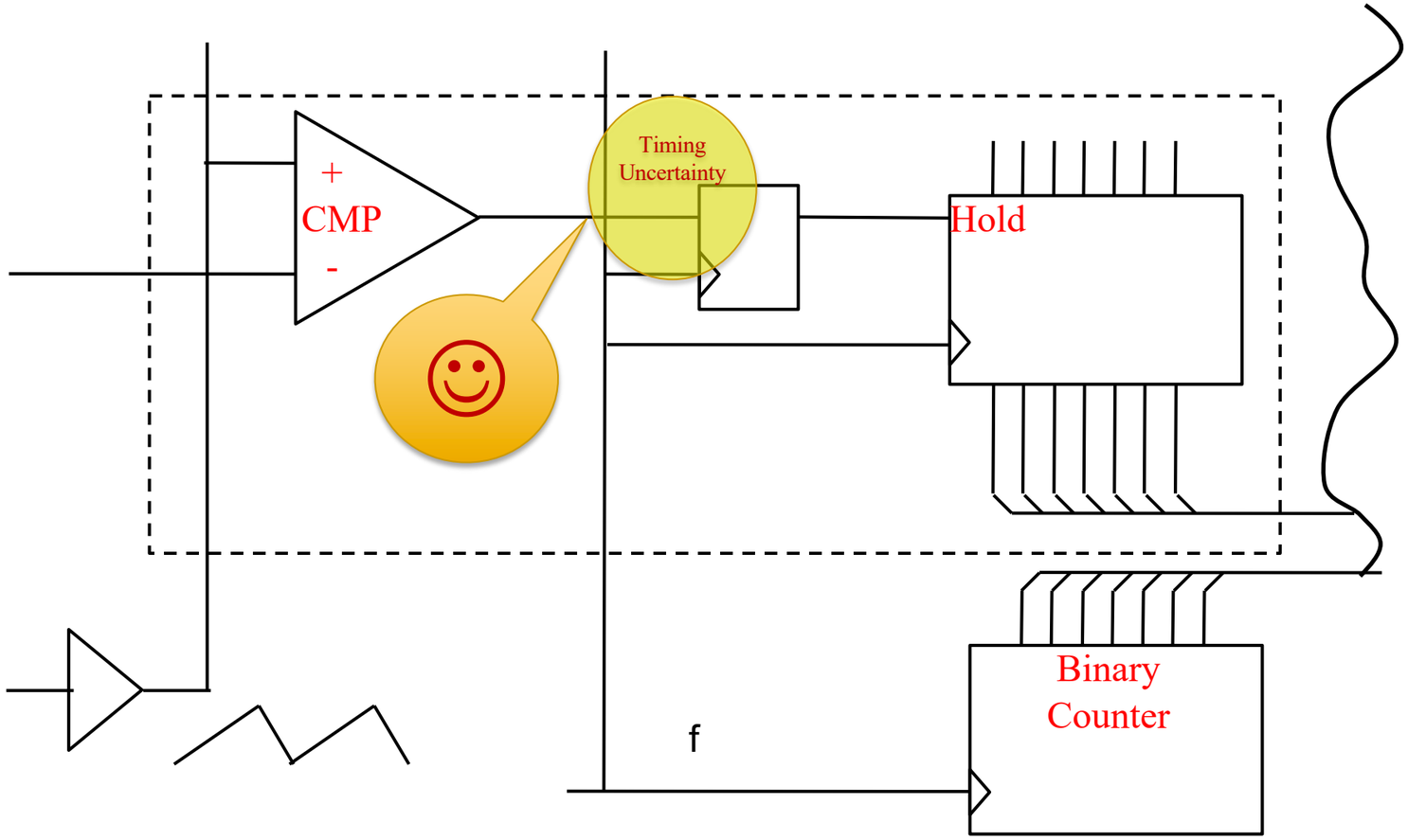
A Common Implementation



Feeding CMP output to CK port of the register causes unnecessary challenges due to unconfined timing uncertainty:

- Must use Gray Code Counter.
- Must match propagation delays of all bits.

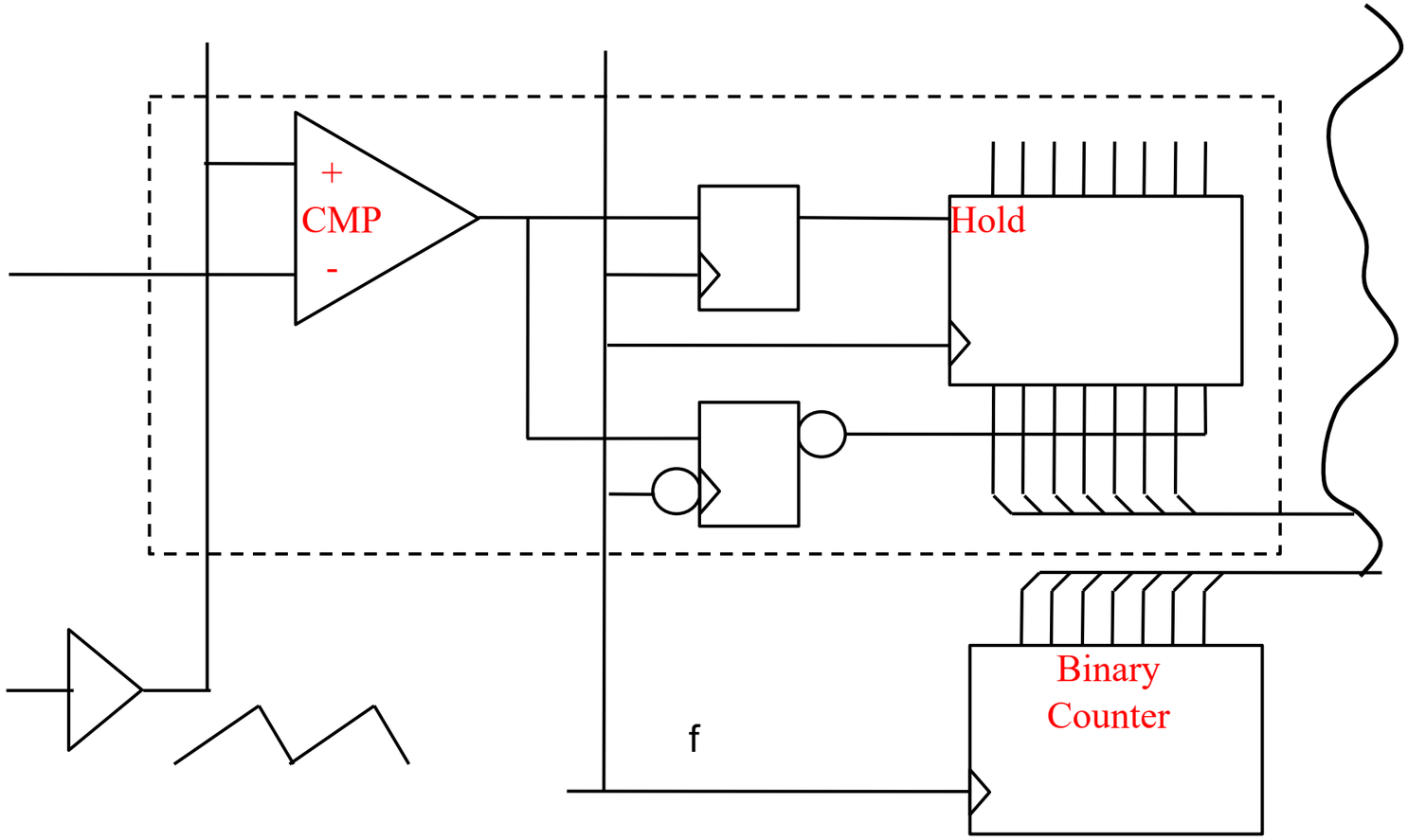
An Improvement



Feeding CMP output to D port of a FF reduces complexity:

- The counter is regular binary counter.
- No propagation delay matching is needed.

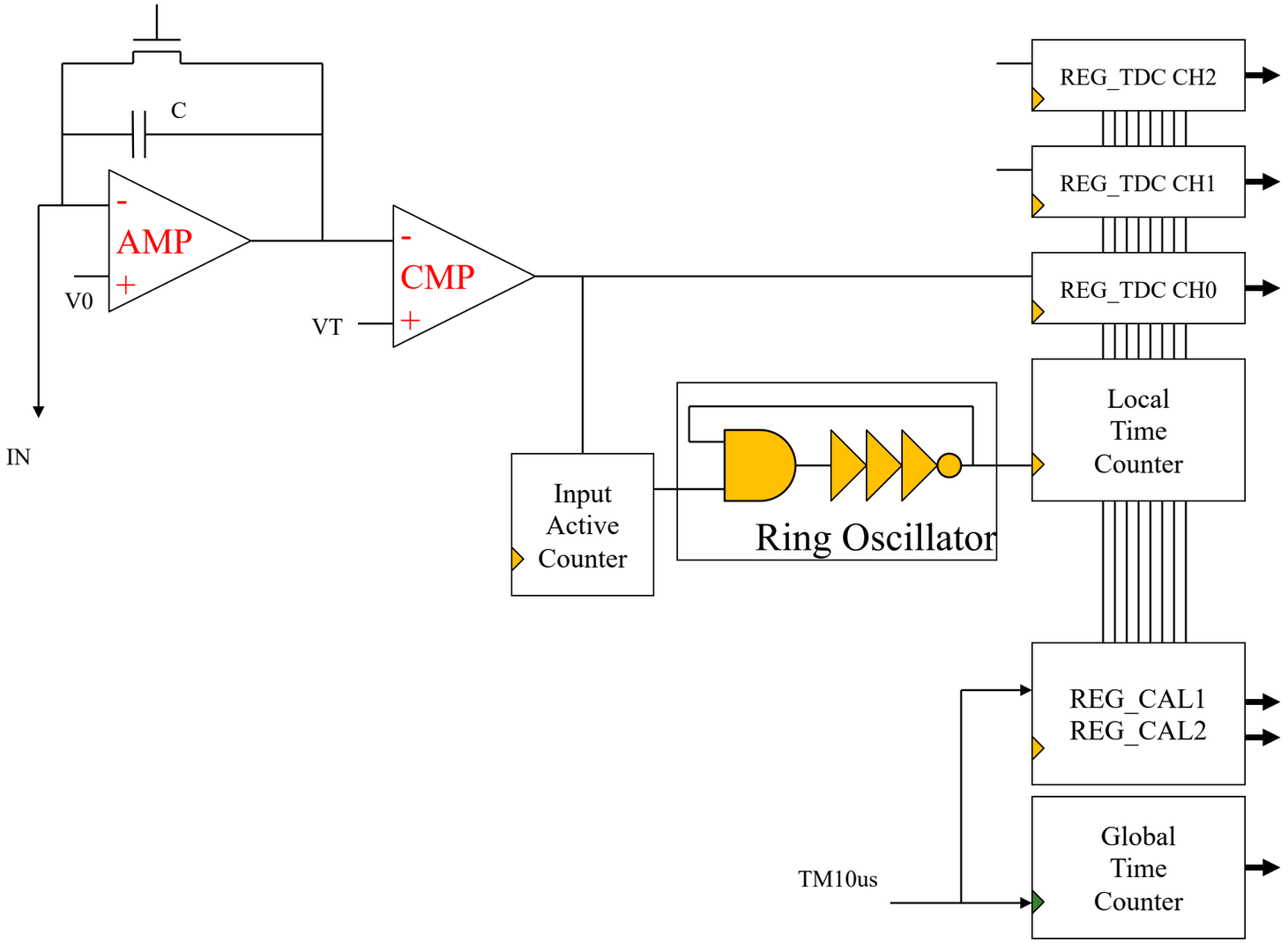
Doubling Digitizing Resolution



Confining timing uncertainty opens possibilities for further improvements:

- Resolution or sampling rate can be doubled easily.
- Improvements by a factor of 4, 8, 16, 32 etc. are possible.

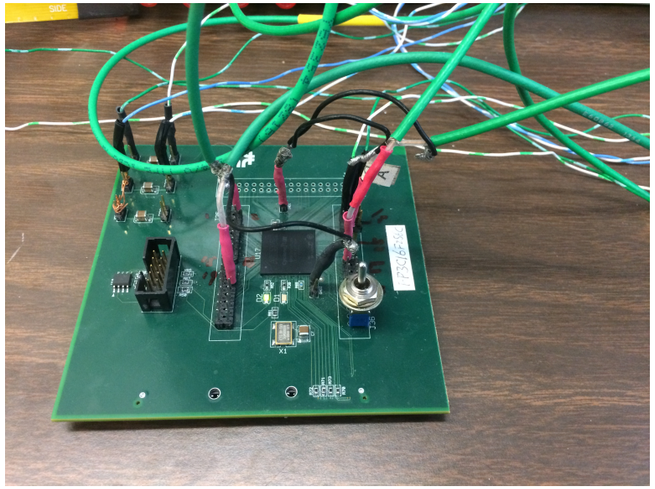
No-Hit-No-Op Ring Oscillator/TDC

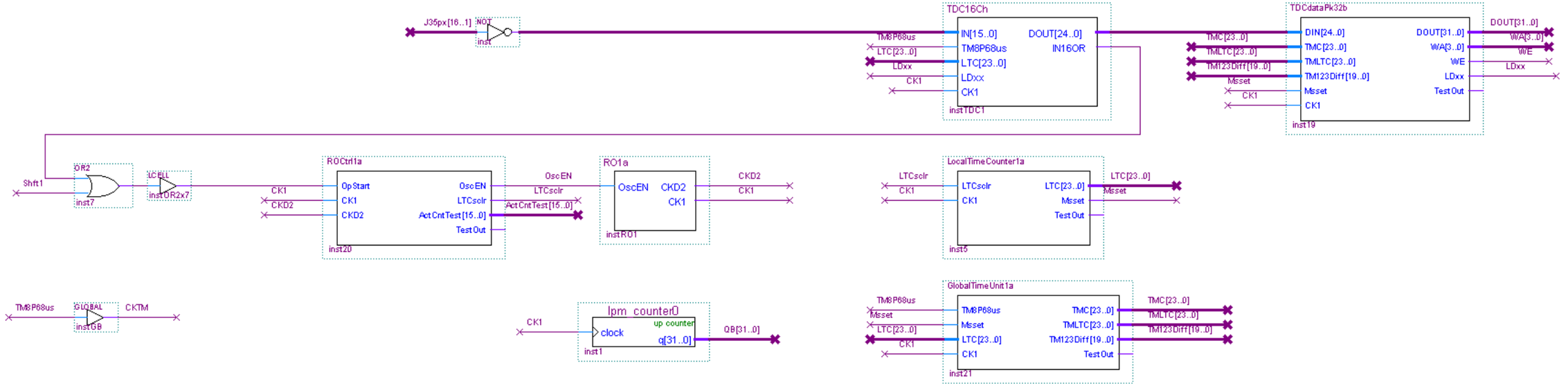


- When there is no hit, nothing oscillates.
- The time marker TM10us (which arrives every 10 us or even longer) updates the Global Time Counter.
- When the CMP output pulses high, the Input Active Counter is turned on.
- The Ring Oscillator is enabled to run.
- The Local Time Counter counts.
- The the arrival times subsequent hits are recorded at the REG_TDC with LSB depending on RO frequency (100 MHz => 5 ns = 10 ns/2)
- The local times of the next two TM10us are recorded in REG_CAL1 and REG_CAL2.
- If there is no hit for long enough time, the Input Active Counter expires. The RO is disabled, entire TDC part takes nap.

Hardware and Firmware

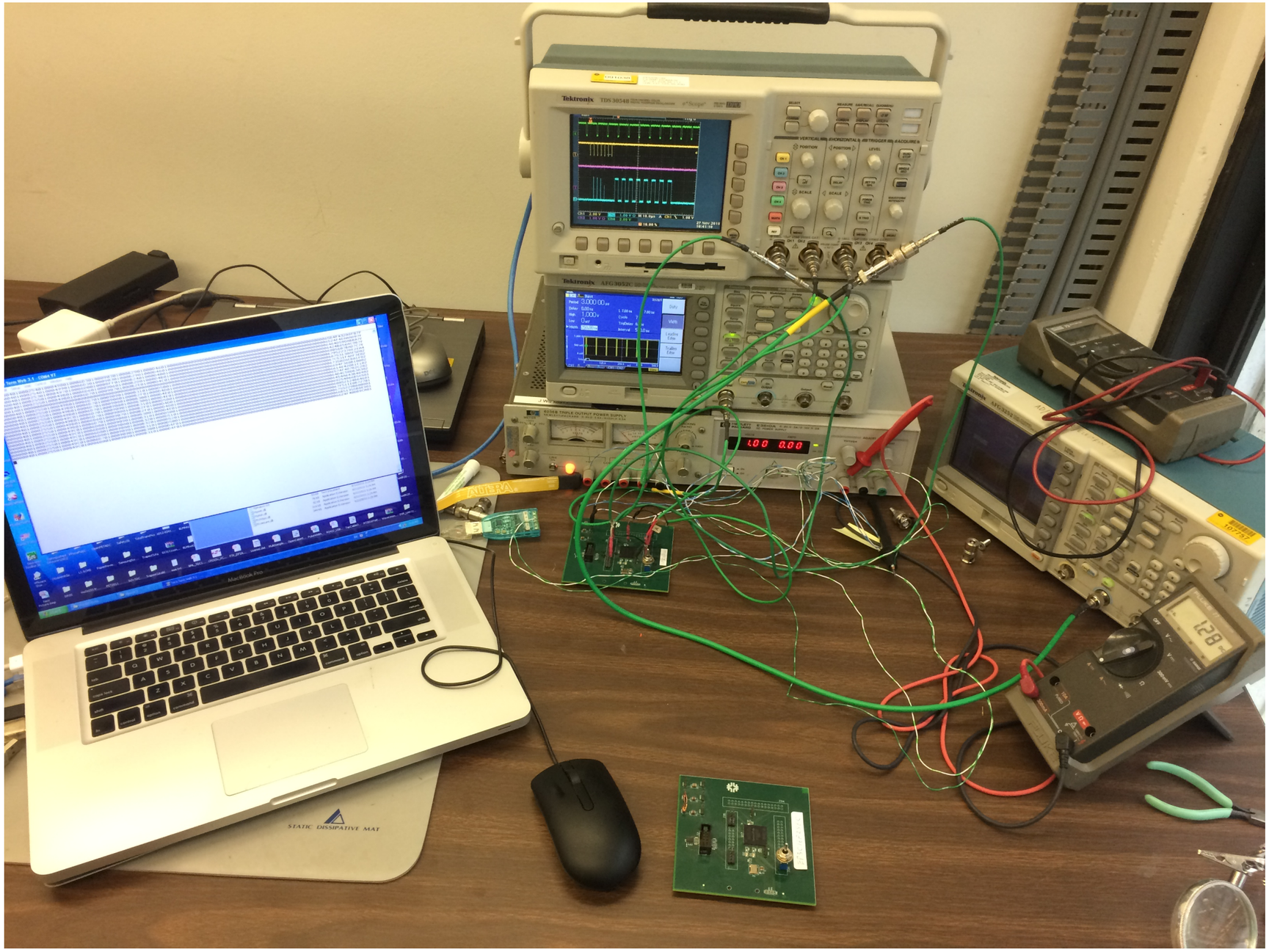
- An old test card with a Cyclone III (65 nm) FPGA (EP3C16F256C) is used.
- The FPGA emulates the digital portion of the ASIC.
- A ring oscillator runs at around 200 MHz
- A timing marker at 115200 Hz (8.68 us) is sent to FPGA.
- 16 channels of TDC (registers) are implemented.



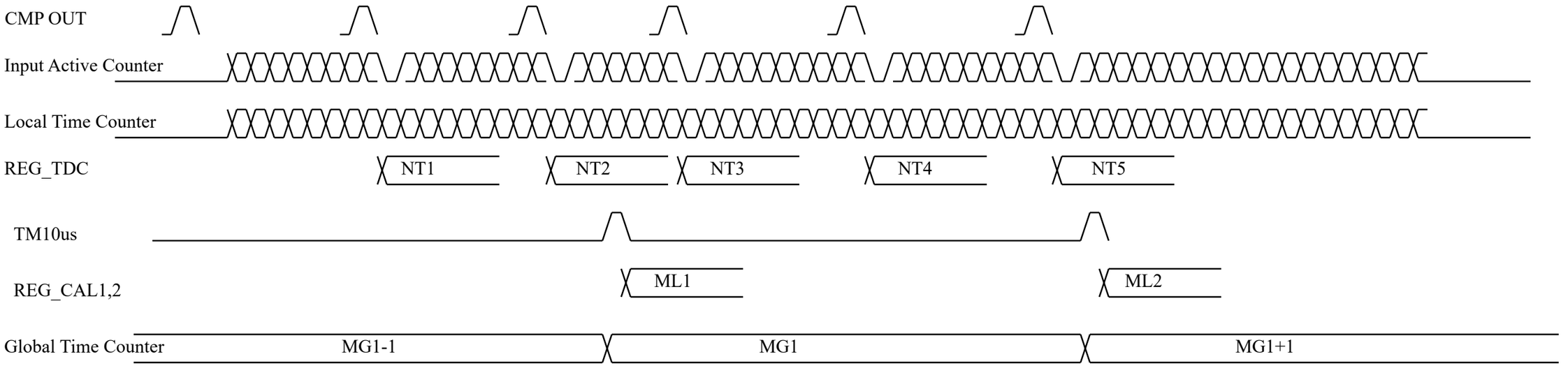


Test Setup

- A signal generator is used to generate a burst of input pulse.
- Another signal generator creates timing marker pulses at 115200 Hz (8.68 us).
- Once a burst is digitized, the TDC data are sent out via UART to computer.
- Digital multimeters are used to measure core power supply current.

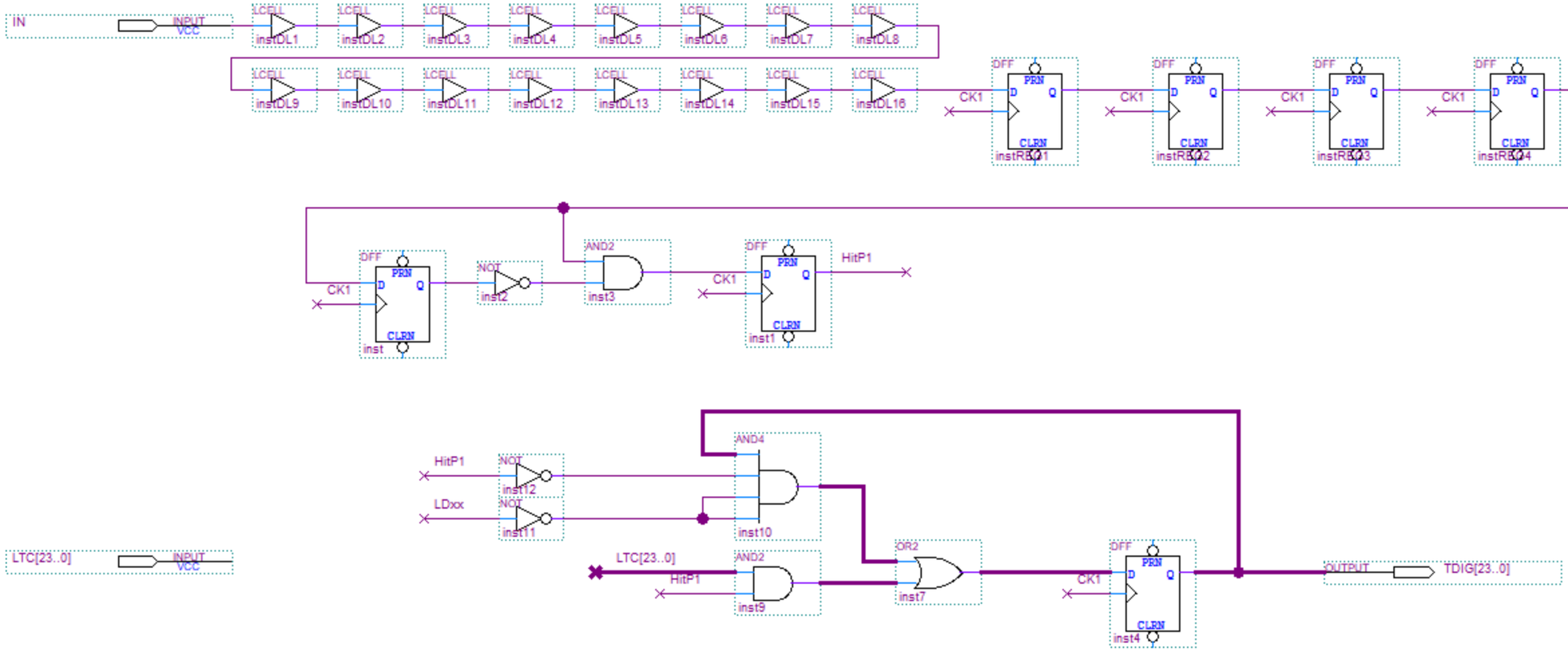


Timing Diagram



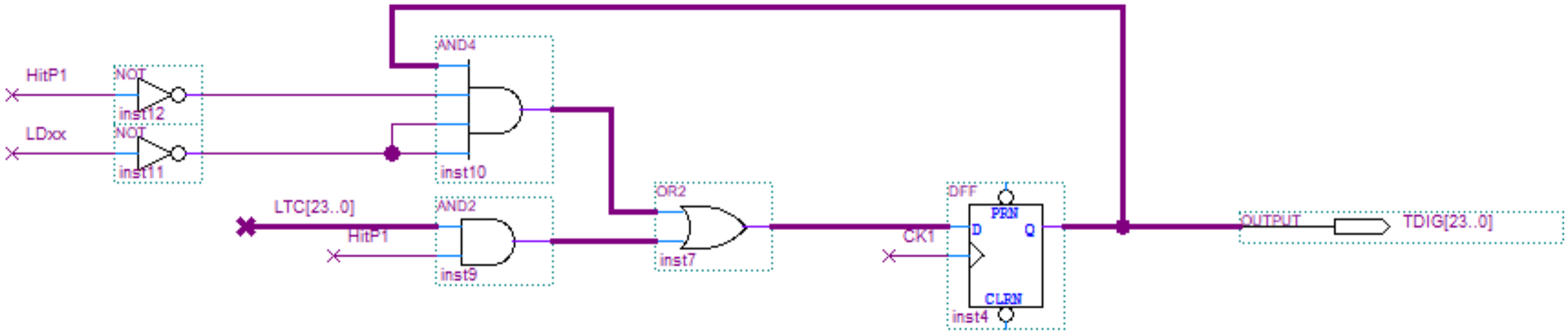
- RO Frequency:
  - F = (ML2-ML1)/10us
- Absolute (GMT) Time for any hit (e.g. hit 3):
  - T3 = (NT3 - ML1)*(10us/(ML2-ML1)) + MG1*10us + T0

TDC Block Diagram



- The TDC contains:
  - Constant delay.
  - Pules generation.
  - Count capture

TDC



- TDC is designed in pipeline structure.
- Therefore, the local time counter (LTC) can be a plain binary counter, not Gray code counter.
- Clocking scheme can be rearranged for lower power consumption.