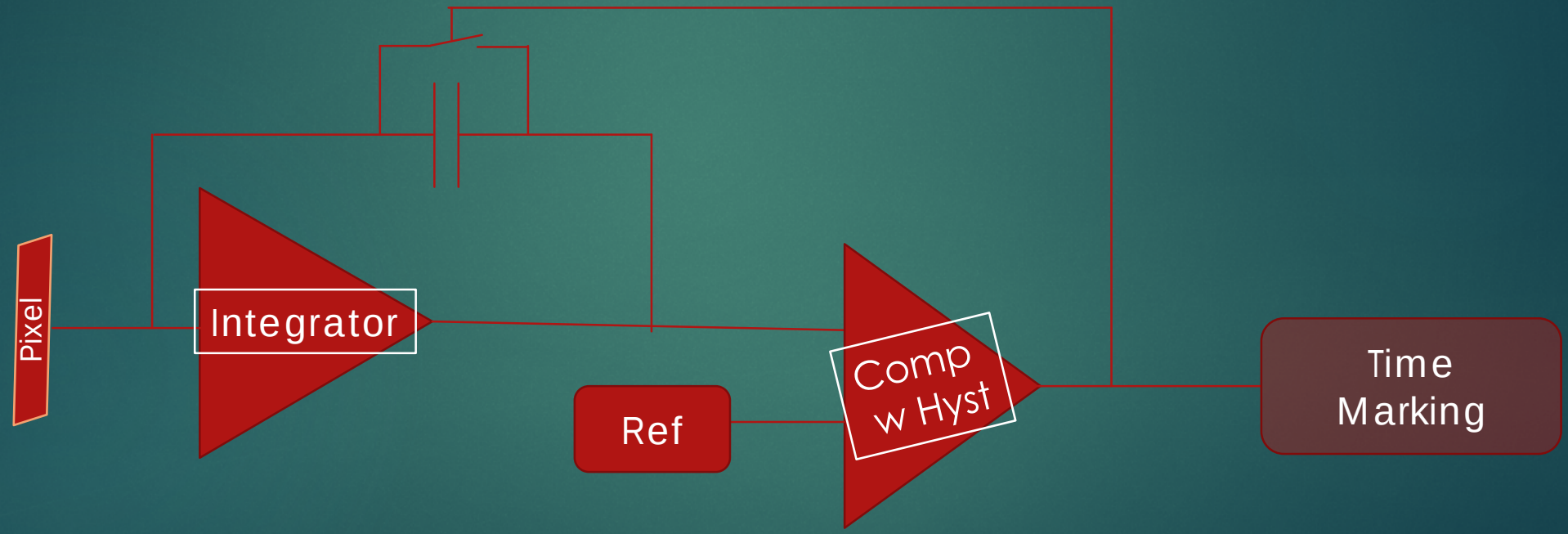
Qpix Frontend Prototype design & status

MITCH NEWCOMER PENN INSTRUMENTATION GROUP

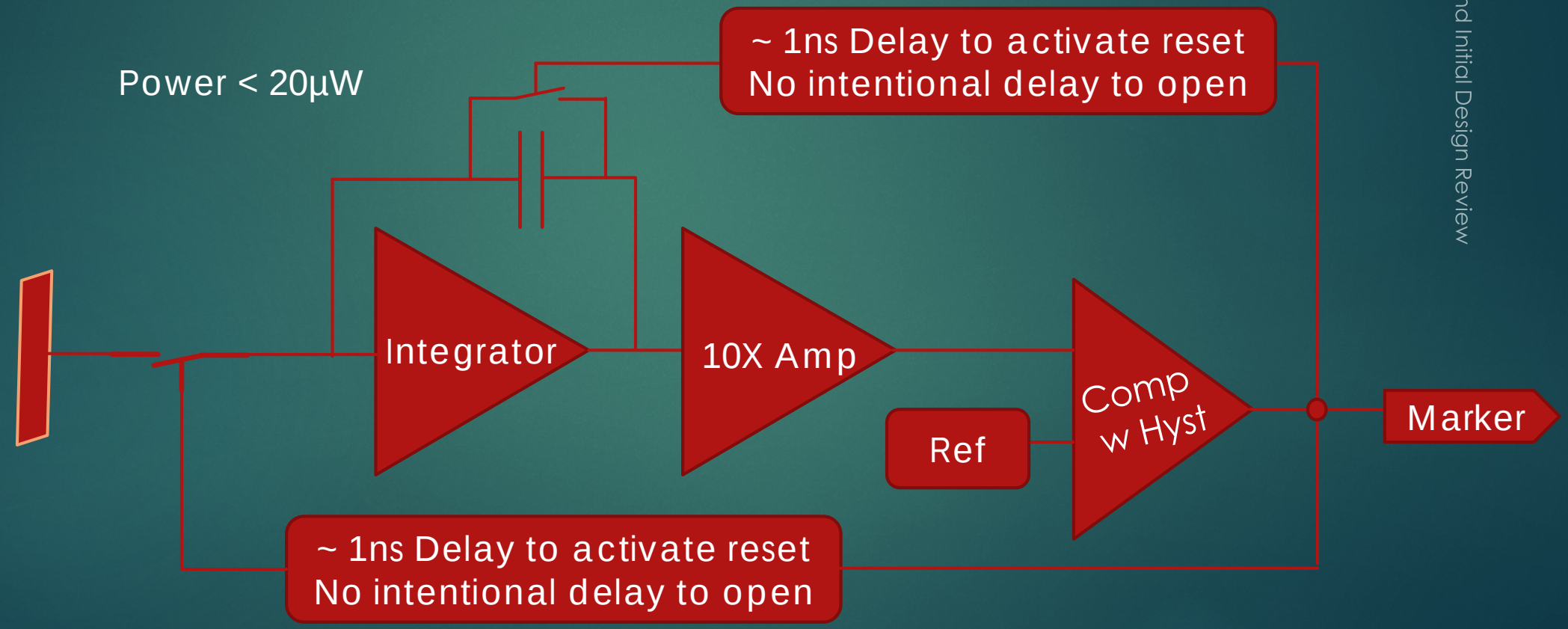
Front End Prototype Objective

- Simple, Reliable, Low Power, Low cost, Ionization Current Pixel readout.
- Provide sub-fempto Coulomb unit charge arrival time marker.
- Suitable for cryogenic ASIC implementation



Implementation

A Pixel disconnect *before* reset is essential to retaining charge during high rates of resets. Charge integrates on the pixel during the ~ 40ns reset.



Status

- Significant progress has been made since the November MOOD update.
  - 180nm Transistor studies led to a good understanding of the output impedance, source follower gain, variation with process etc.
  - A SPI interface has been developed, including 8bit serial → parallel unit with a simple SPI protocol
  - The One shot reset width control has been eliminated in favor of a "TOT+" comparator driven reset approach.
  - Physics driven inputs have been successfully read with a high degree of accuracy.
  - On March 11 The following note representing the thoughts of 3 of the 4 MSEE students working on the Qpix design was sent:

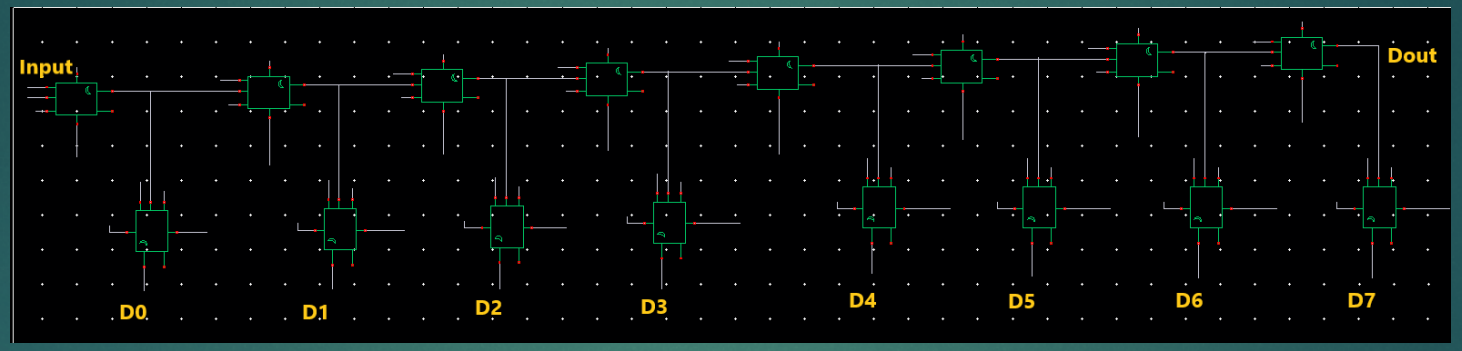
I am writing to say that I am sorry that I cannot go to the lab these days because of the coronavirus disease spreading in US. I am sorry that I am scared about this because I have seen how quickly that spread in China. And as Penn is planning to move our courses online and just extended our spring break for one week, I think it might be better to stay at home. ……

  - Archisman Datta - Developer of the SPI interface remains working with us but will not have access to the technology till the Lab re-opens. He is looking into various simple but useful digital blocks that we might find useful in the prototype.

Simple SPI Interface for slow control

- The SPI Module is designed to work as a serial to parallel data converted having the ability to process a 8 bit word at an instance. The Module consists of D Flip Flops connected as shown in figure 1.

signals
Serial Clock
Serial In
Serial Out
Load
D0… D7



Data are shifted into and out of the 8 bit/register words and may be looped back to the output

Progress since March 11

As the design had been left off there was no solution for working across the full temperature range 30 to -180C.

- A transistor study revealed the strengths of varied threshold voltage (vt) devices in the NMOS and PMOS 2V notably I am presently using a low vt transistor in the source follower output of our opamps.
- A biasing scheme is now in place that allows bias voltages used in our opamps to track with temperature
- → **The design is now operational over the full temperature range with no changes in biasing voltage.**
- Integrator performance has been studied important functional parameters:
- changes over temperature, input capacitance dependence, noise.

Noteable Work TBD ahead of LAYOUT

- Develop master Biasing scheme requiring fewer high value resistors. Current design explores reasonable techniques but can be simplified.

The following were studied/partially implemented in blocks studied by MSEE's but now need to be carried to the full design:

- Apply process resistors to current design
- Validate current design over process.
- Validate device mis-match performance.

- Develop suitable Threshold DAC
- Develop / Implement LVDS driver & receiver.

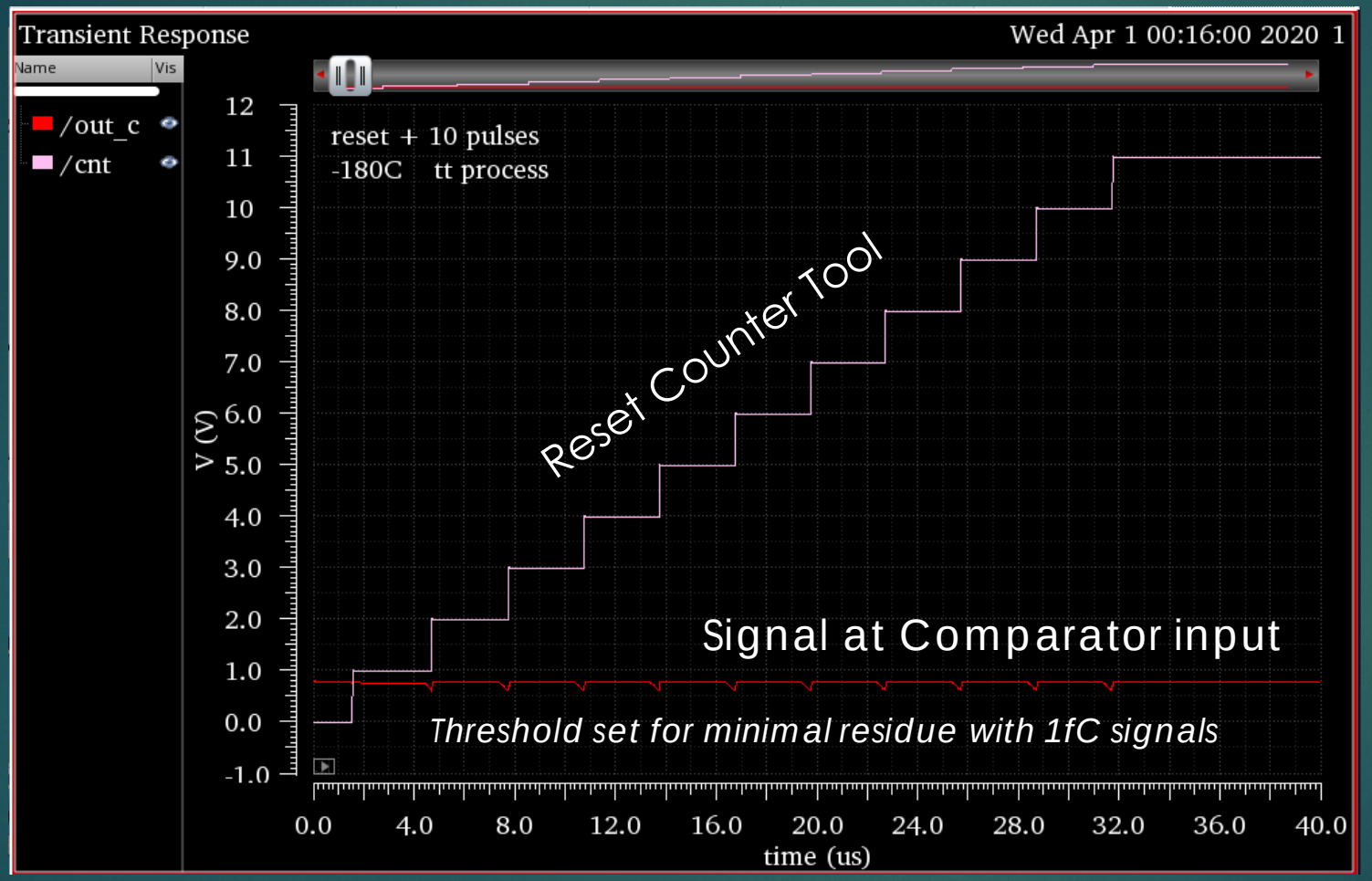
- SPI interface design

Issues

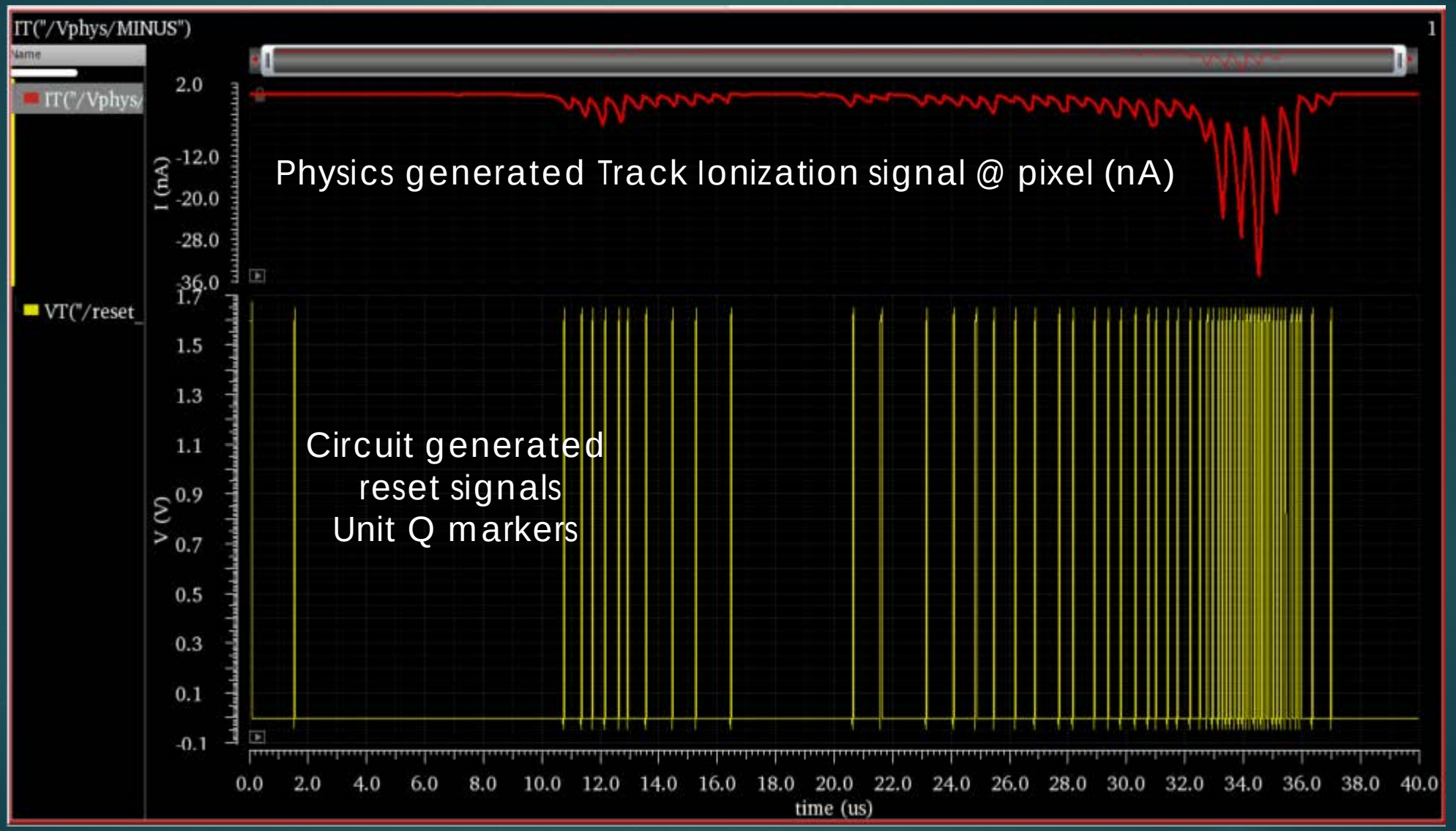
- BSIM 4.5 models
  - Not all studied transistor properties track sensibly to -180.
    - One of the low vt transistors has an unexpected significant increase in gm.
    - RMS noise decreases down to -120C but increases at -180C
- Not clear when MSEE help will restart to help with layout.
- Engineering staff has received no funding for the design effort.

Response to initialization reset & 10, 1fC pulses

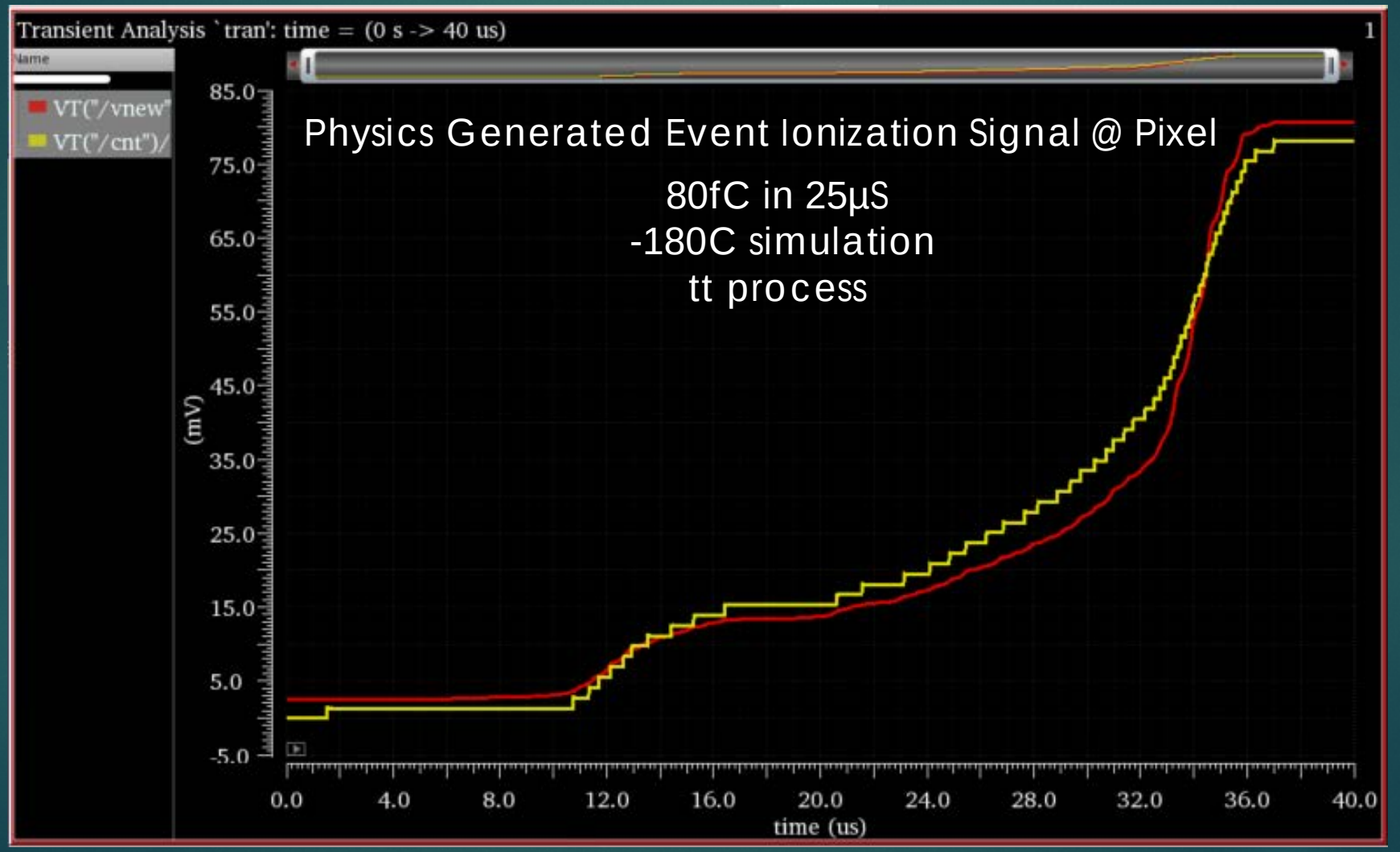
@ -180 C , tt models



Circuit response to Physics Generated signals.



Integrated Pixel event Signal on 1pF Cap
vs
Integrated Reset count at 1mV / Reset



Summary

- Significant progress has been made over the past 2 years. The design has been implemented in 3 ASIC processes and the circuit has matured along the way lowering power, defining and simplifying circuit elements. It appears to be reasonably responsive to physics generated signals. Higher fidelity is likely available at the cost of an increase in power.
- The most challenging blocks are understood and ready for or close to ready for layout in a prototype design.

- Progress will continue to be made on the design during our unplanned sequestration.
- Parts from other groups could be incorporated leading to a more complete prototype.
- MSEE help really can not be effective until the Lab is re-opened.
- Other implementations could be explored such as the Q replacement approached suggested by David Nygren.