"Analog" Components of Digital System: Status and Plans

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Overview structure

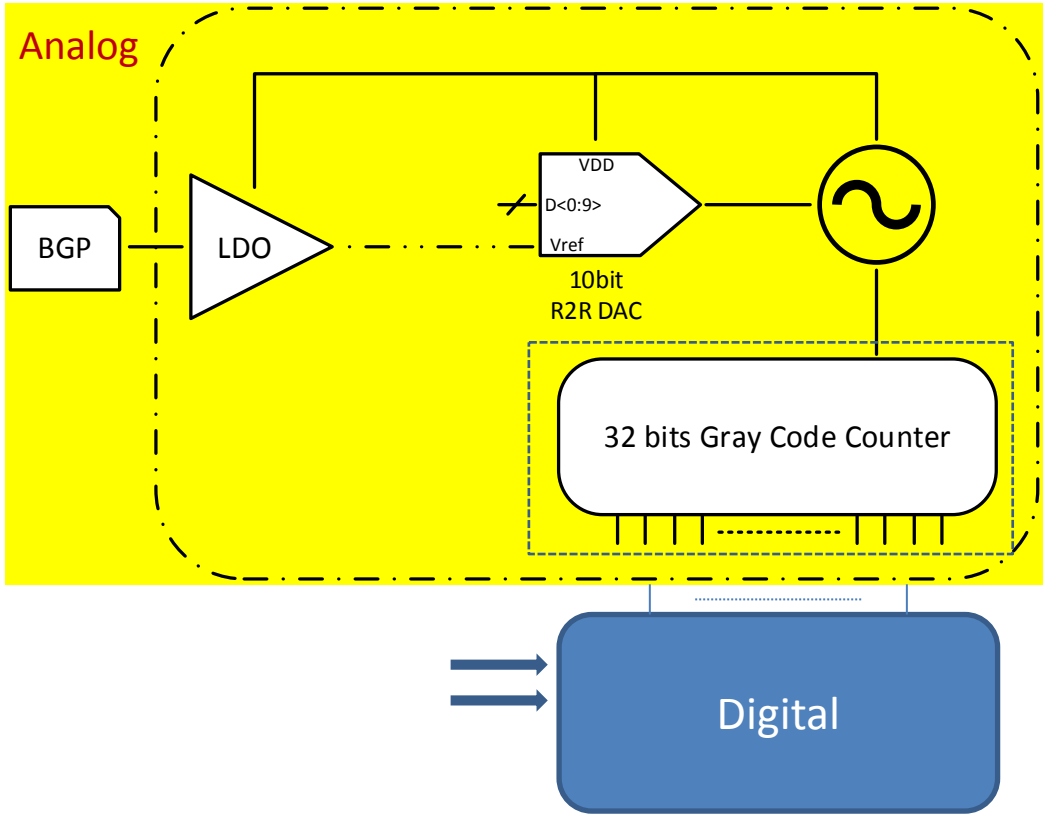
- **Ring oscillator:**

  Tune range, Resolution, Power
- **10-bit DAC:**

  Resolution, Power
- **Bandgap & Regulator**

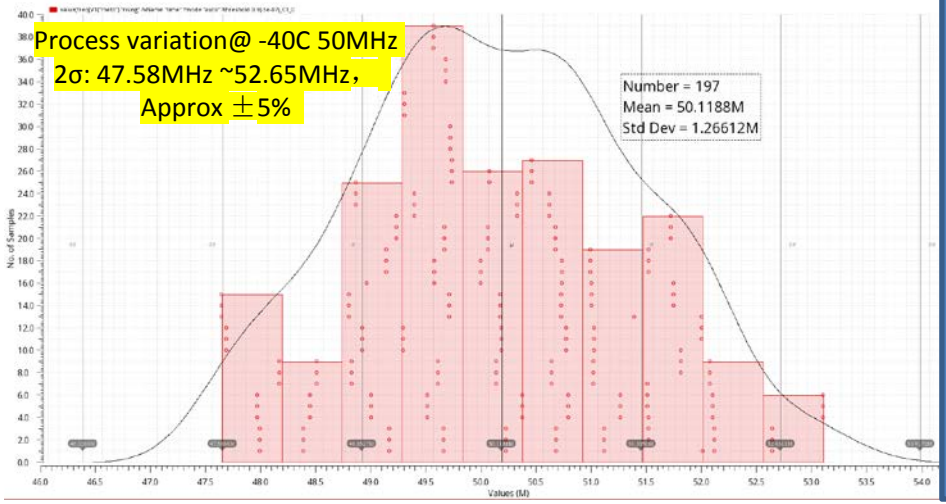
  Power
- **Buffer and etc.**

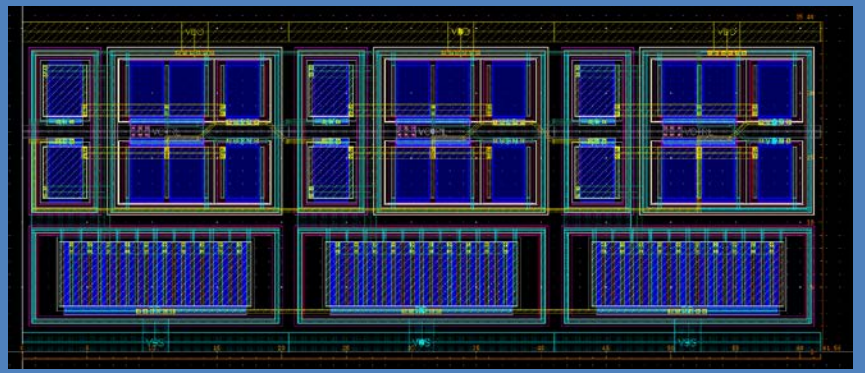
- **32-bit Gray code counter**

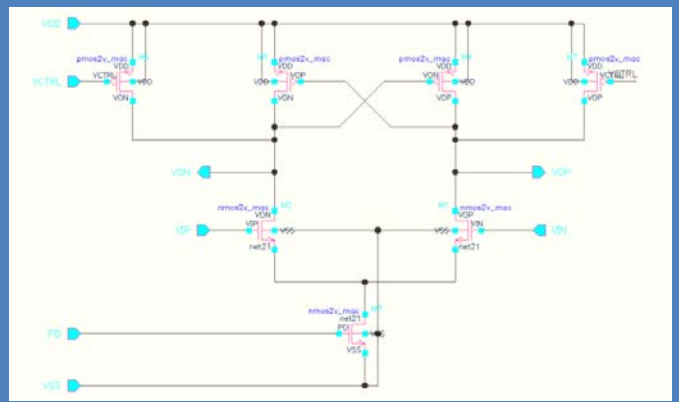


Ring Oscillator

- Tune range: 50MHz ~ 100MHz
- Based on differential delay cell
- Power-down mode
- Power: 0.36mW @ 50MHz -40C

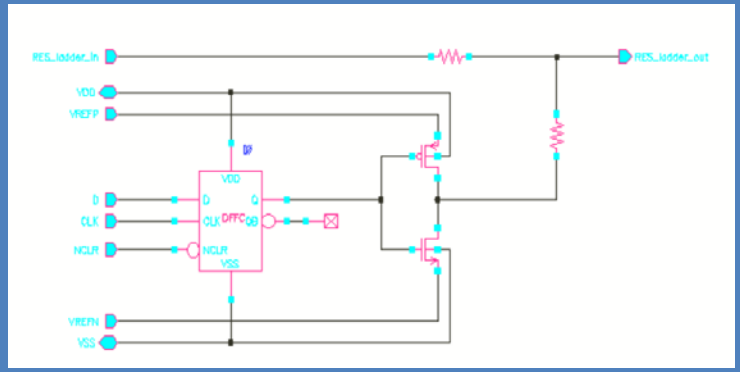


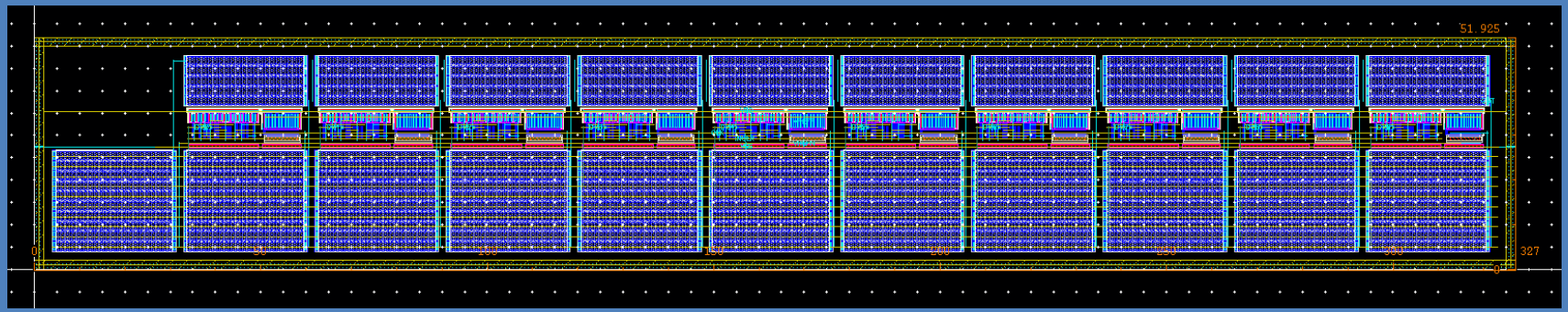




10-bit R2R DAC

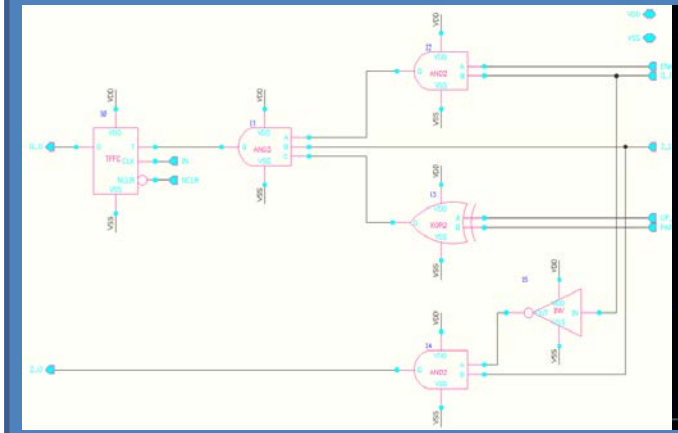
- R2R structure
- Based on 1-bit DAC, cascade to 10 bit
- DNL=0.95LSB, INL=0.78LSB
- ENB>8 bit, considering the process variation
- Quiescent power: 0.22mW @ -40C

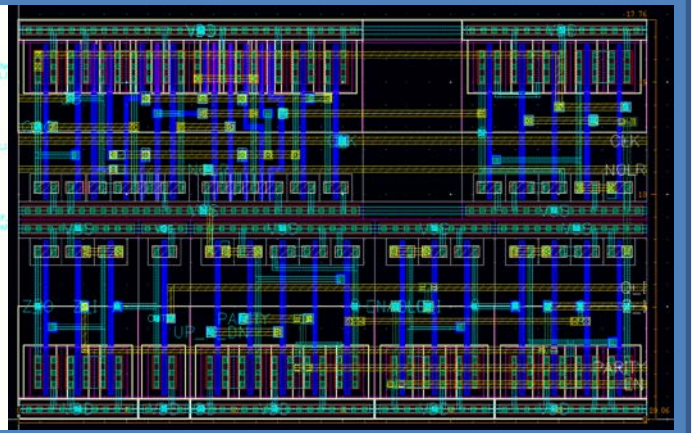


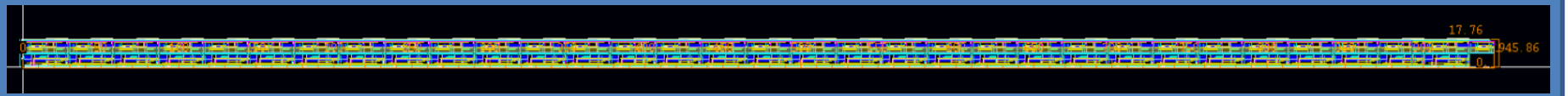


32-bit Gray Code Counter

- 1-bit GCC cell
- Cascaded to 32 bit
- Custom designed std cell
- Power: ~ 0.23mW



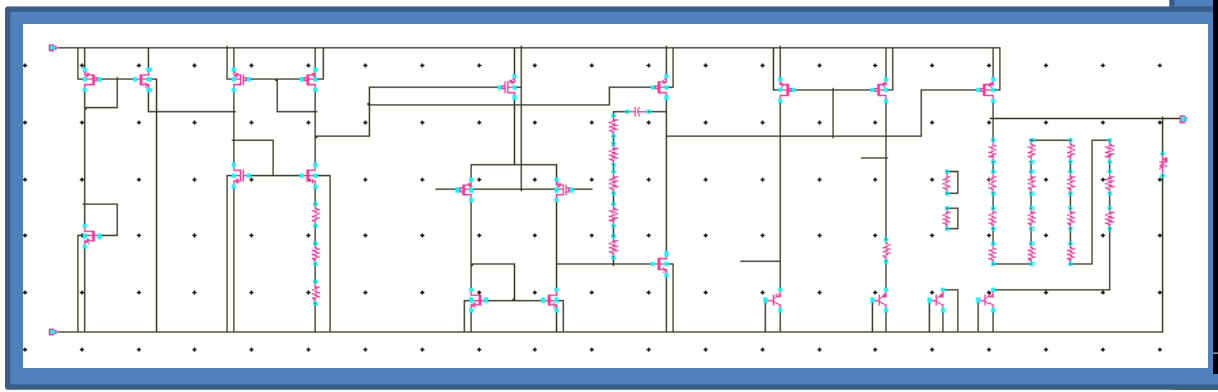


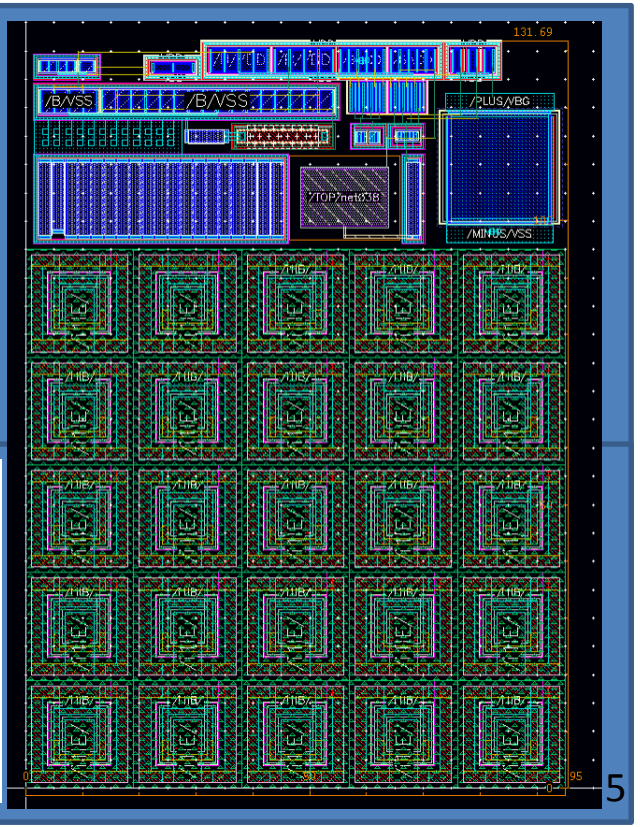


Bandgap

- First-order temperature compensation
- -40C to 55C temperature coefficient < 7ppm
- Power: 0.34mW @ -40C

- The regulator is in process.





Status

Component	Schematic	Layout	power
Ring oscillator	Done	Done	0.36mW
GCC	Done	Done	~0.23mW
DAC	Done	Done	0.22mW
Bandgap	Done	Done	0.34mW
Regulator	In process	In process	TBT
			Total: 0.36+0.23+ 0.22+0.34+Reg =1.15mW+Reg per ASIC

Future plan

- Finish the regulator design
- Cold model of the process ?
- Official Standard cell library ?
- Components to share, DAC, BGP ?

Thank you !