Plans on further HDL Development and Verification

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Q-Pix collaboration meeting
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Introducing myself

- UH postdoc from August 2018 working in Kurtis Nishimura team
- Background :
  - electromagnetic calorimeters (crystal and LXe) of Belle-II(KEK, Japan) and CMD-3(BINP, Russia) hardware/calibration/reconstruction/DAQ
  - Firmware development. Started from the FPGA firmware for luminosity monitoring electronics for Belle-II (BINP), at UH have been engaged in : Belle-II Time-Of-Propagation FEE(embedded software for a little bit), K_L/μ-detector(KLM) front-end electronics, KLM trigger electronics. Non-Belle-II UH projects LAPPD readout electronics
- Joining Q-Pix collaboration. Effectively will start intense work from the beginning of the next week with about 50% of FTE, increasing in coming months

Tasks

- HDL-level simulation of the ASICs communication with different protocols
- High-level simulation of the ASICs communication. Shahab Kohani (UH postdoc) will join this activity as well.
- ASICs TX/RX prototyping in FPGA

HDL-level simulation

- Penn Endevour protocol for the communication as a baseline
- Framework for simulation with easy replacement of TX/RX part
- Estimate the required tolerance on clock mismatch
- Open source instruments : ghdl + cocotb on python will allow to integrate low level and high level simulation
- Iterative development with HDL simulations to find optimal configurations

HDL-level simulation (continued)

HDL SIMULATION FRAMEWORK

- Building up a basic framework for digital logic and corresponding simulations.
- Allows for randomly seeded clock frequencies and phases:

```
constant N_ROWS_C : integer := 16;
constant N_COLS_C : integer := 16;
constant CLK_PERIOD_NOMINAL_C           : time := 20000.0 ps;
constant CLK_PERIOD_SPREAD_FRACTIONAL_C : real := 0.005;
```

```
# Clock Phases and Periods by ASIC Position #
# All time values given in ns #
# ASIC 15 15 :  20.00  20.05
# ASIC 15 14 :  12.95  19.98
# ASIC 15 13 :   0.74  19.97
# ASIC 15 12 :  13.29  19.96
# ASIC 15 11 :   4.08  19.97
# ASIC 15 10 :  13.10  19.96
# ASIC 15  9 :  18.20  19.96
```

- Basic UART implementation at 1/8 of core clock frequency.
- Creates NxM grid of ASICs, exercises a connection to external DAQ node(s) to inject/receive signal.

- Basic HDL simulation framework has been developed by Kurtis
- Taking it over

cocotb/ghdl instruments

cocotb

- `https://github.com/cocotb/cocotb`
- Coroutine based cosimulation library for writing HDL testbenchs in Python
- Advanced control over intrinsic signals
- Integration with high-level simulation

GHDL

- `https://github.com/ghdl/ghdl`
- The open-source analyzer, compiler and simulator for VHDL.
- Vendor independent, easy to use, and well documented

High level simulation

- Python implementation of the ASIC routing algorithm
- Study of the buffer depth needed depending on the pixels occupancy
- Study of the optimum array size and data rates

FPGA prototyping

- Demonstrate communication/routing algorithms of the ASICs in FPGA
- Implement ASIC array in FPGA and study it against input signal rate/internal osc frequency, robustness of the data transactions etc.
- Two basic options :

"Big" FPGA (Xilinx)

- Flexible control over internal processes and parameters
- Controllable clock skews and frequencies to model ASICs oscillator variations
- Minimum hardware work if use eval board

A set of cheap e.g. iCE40 (Lattice Semiconductor)

- A number of different small eval boards available
- More realistic data path
- Cheaper than Xilinx FPGAs

Plans and timescale

- About 1 month for handing over development (Kurtis) of the HDL framework and producing first results of the study of chips communication/routing
- Simultaneously with that do the study of different approaches for FPGA prototyping and present report in 1.5-2 months
- Longer term - work toward implementation of logic in a final ASIC (Need to learn digital ASIC design flow).