LArPix-v2 Update

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ArgonCube Meeting

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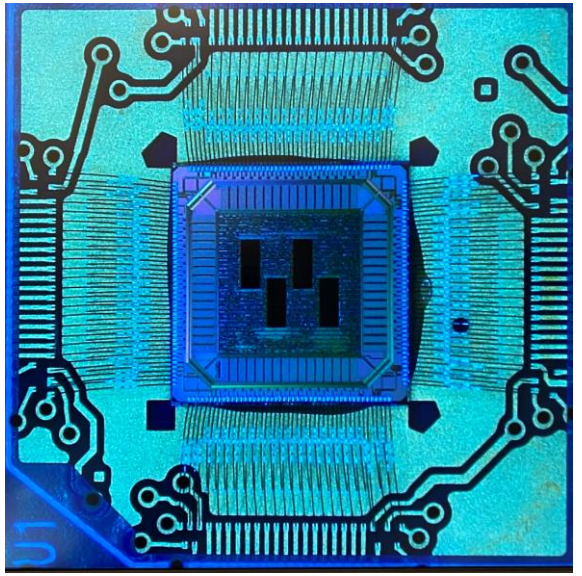
LArPix-v2 Bare Die Initial Power Up

- Initial testing focused on **verifying basic chip functionality**

- Power up current draw
  - Five bare dies tested
  - 231µW/channel average total power @ room temperature and full digital voltage
  - Power draw consistent between bare dies to 1%

15 LArPix-v2 bare dies received 2/7/20

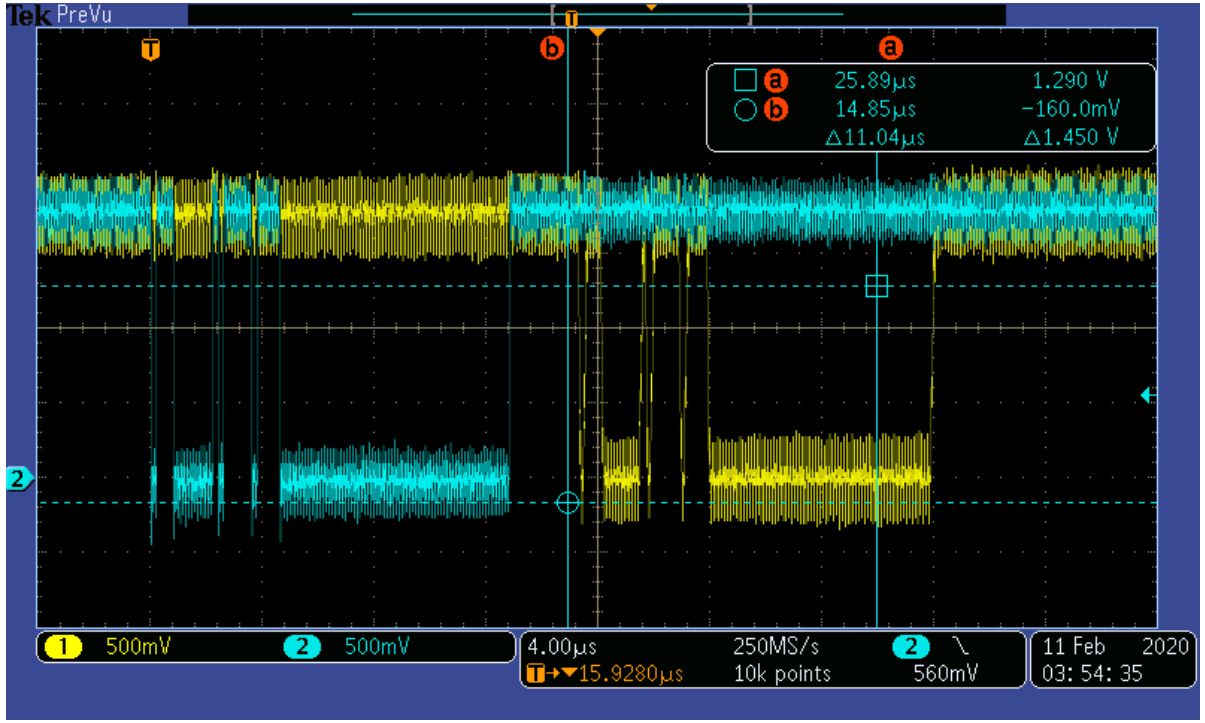


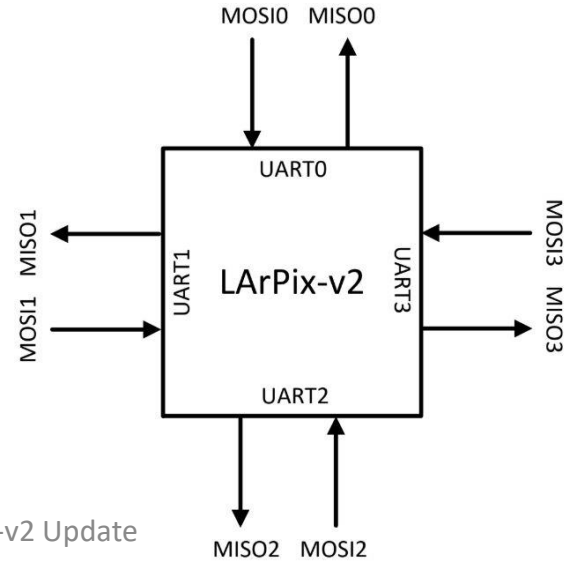
Chips wire bonded to chip-on-board (COB) PCB

Confirming Basic Communication

- ✓ Read registers
- ✓ Write registers
- ✓ Loop-back test
- ✓ Setting a chip ID
- ✓ Hydra I/O test
- ✓ Software reset
- ✓ Hard reset

Configuration read packet (in cyan) requesting the value of the downstream hydra I/O register on MOSI A. Chip response to request (in yellow) on MISO A.

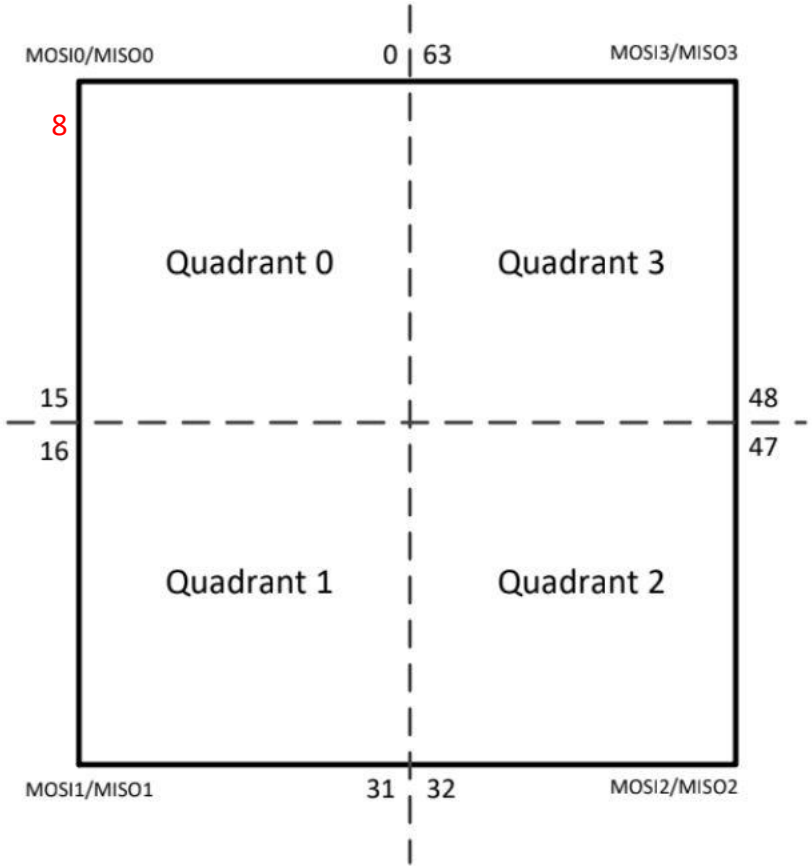




Default chip ID set to 1. Confirmed changing chip ID, enabling/disabling all miso downstream channels, enabling/disabling all miso upstream channels.

Confirm Chip Defaults

- ✓ Register values
  - 237 registers on LArPix-v2
  - All confirmed consistent with v2 datasheet with exception of two registers (both most likely typos in datasheet)
    - Register 65[0] (csa gain) expected 1 was 0
    - Register 80 (csa pulser bias current) expected 6 was 5
- ✓ Reference voltages
- ✓ Current, voltage consistency across quadrants 0-3
- ✓ Channel pedestal consistency (at room temperature with no shielding)
  - 63 channels ~380mV
  - Single channel (channel 8) ~280mV



Basic Operation

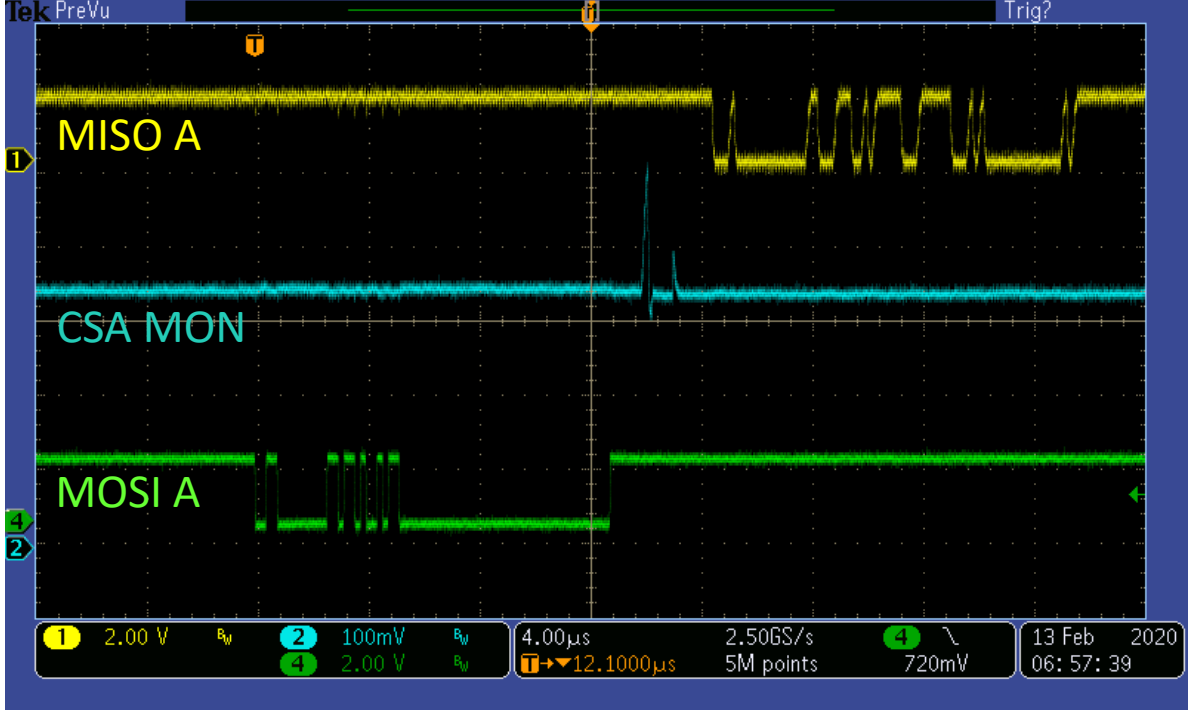
✓Channel masks

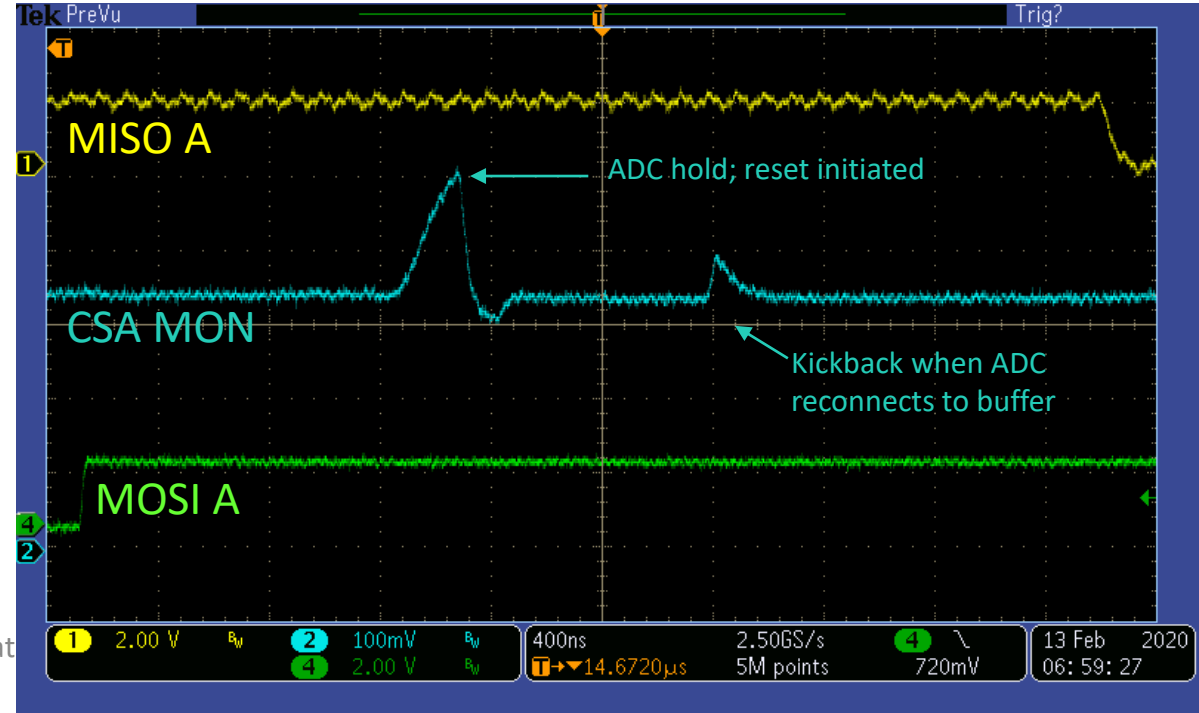
✓External triggering

✓Internal test pulse

✓Self triggering

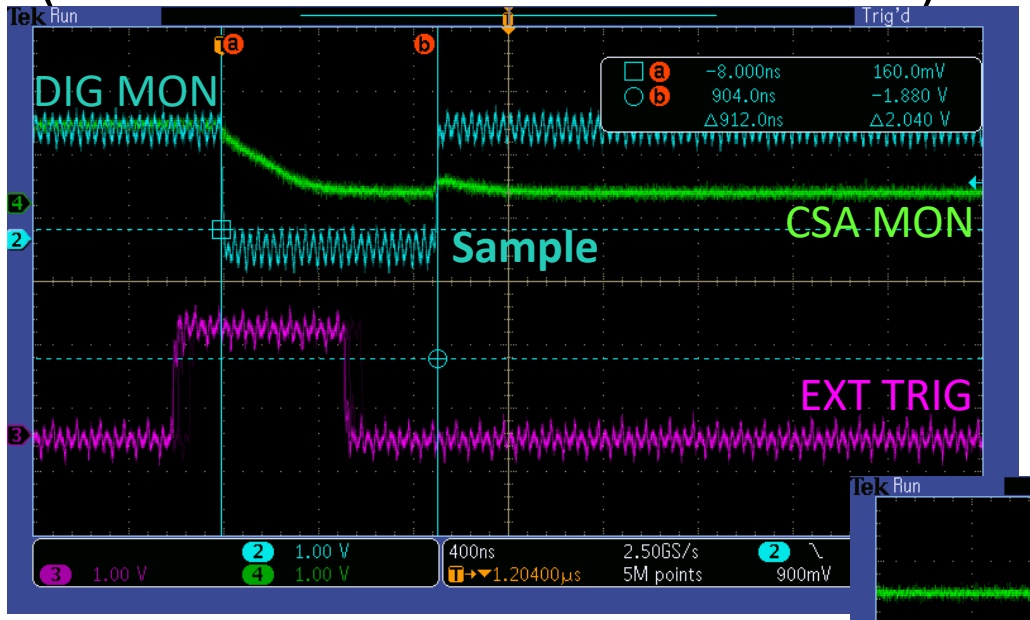
✓ADC range – confirmed full 8-bit range accessible

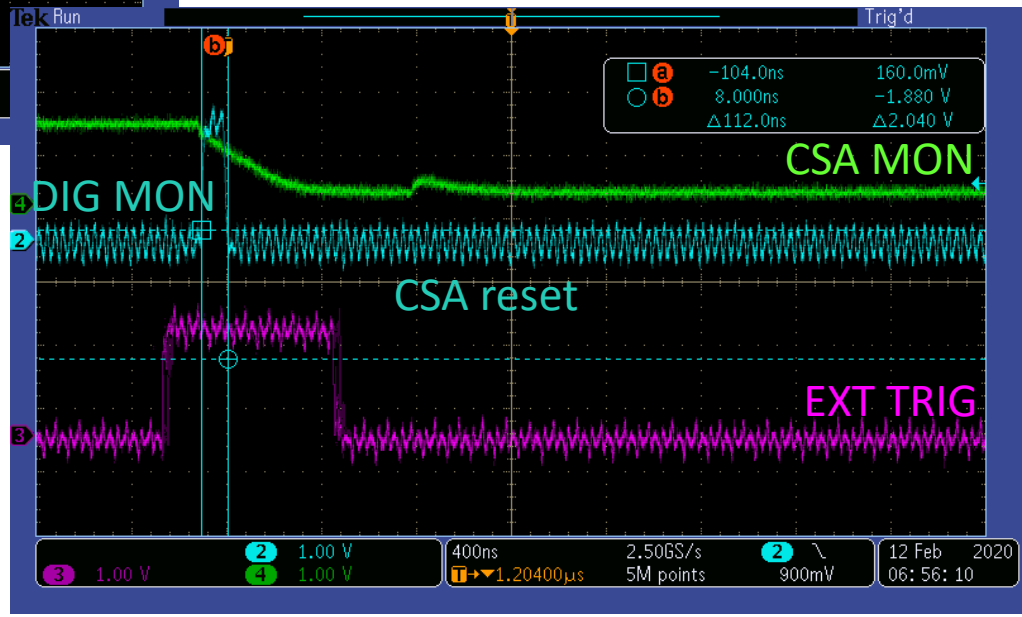




Digital Monitor (new feature on LArPix-v2)

- Hit
- Comparator
- Sample
- CSA reset
- Triggered natural
- Periodic trigger
- Periodic reset
- External trigger
- Cross trigger
- Reset/sync





Readout through a dedicated pin to observe internal digital signals. Handy for diagnostics/trouble shooting.

Front End, Digital Features

Issue #1: Data loss with near synchronous packet **@ nominal transmit clock rate**

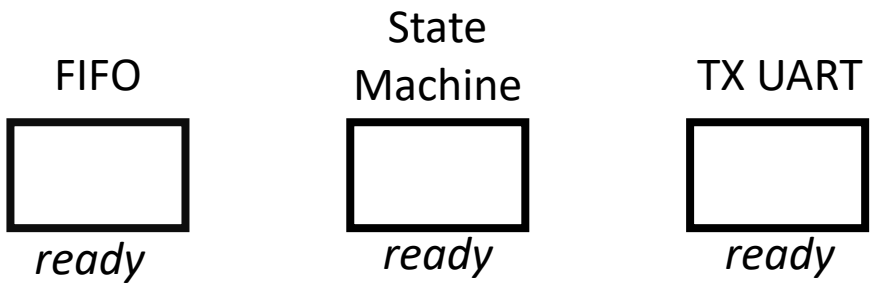
- 50% data loss if coincident signal registered across multiple channels
- Problem persists to a lesser degree until ΔT exceeds slightly larger than UART packet size
- Fix devised and exercised – with speedy isolation and debugging of the issue from C. Grace & D. Gnani

Issue #2: 512^{th} word swapped in memory

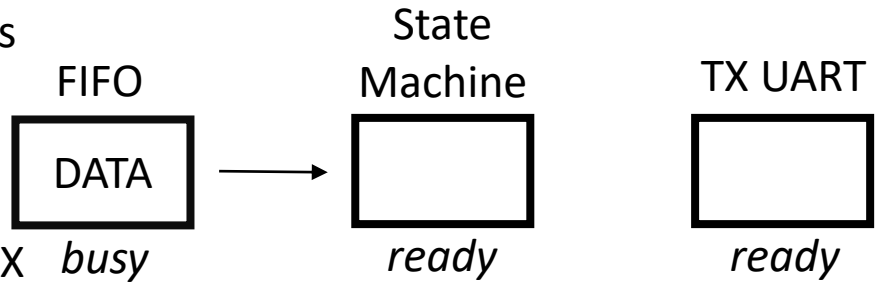
- Data recoverable

Issue #1: Data loss with near synchronous packet

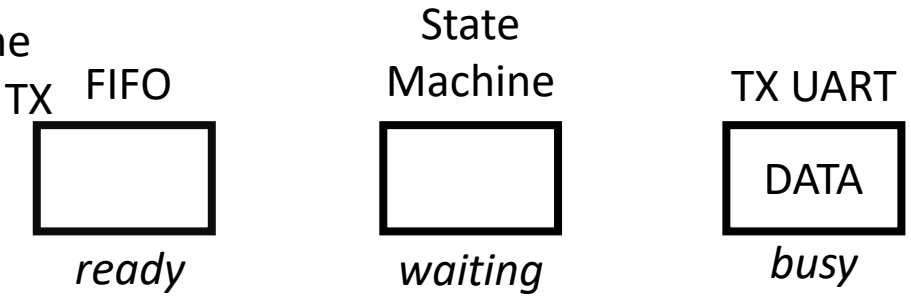
(0) State machine ready to receive data from FIFO when TX UART signals it is ready



(1) When FIFO has data, state machine reads data from FIFO and transfers to TX UART.



(2) State machine in wait state for TX UART busy to signal it is busy; sometimes TX UART busy signal is delayed.



Default setup:

10 MHz system clock, 5 MHz transmit clock

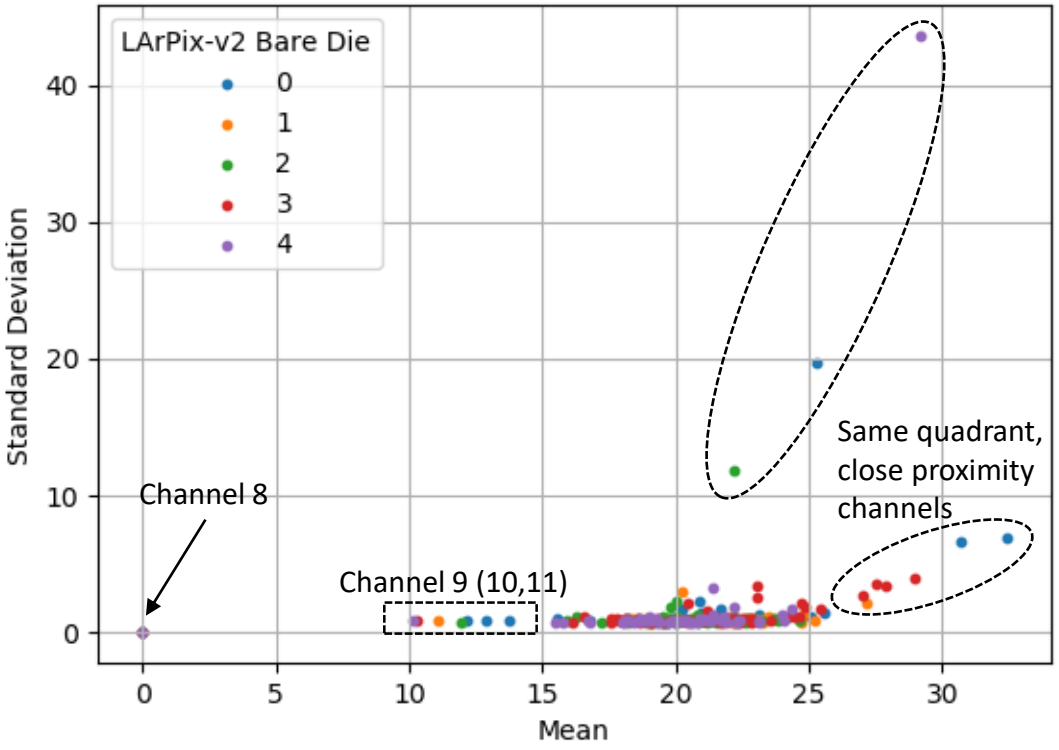
- Recover 50% packets cross triggering all channels (and natural triggers)

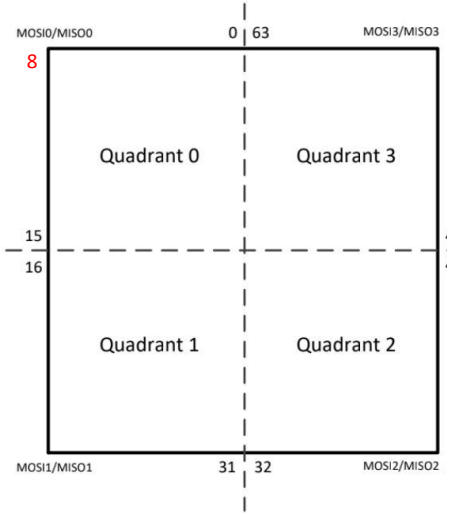
Modified setup:

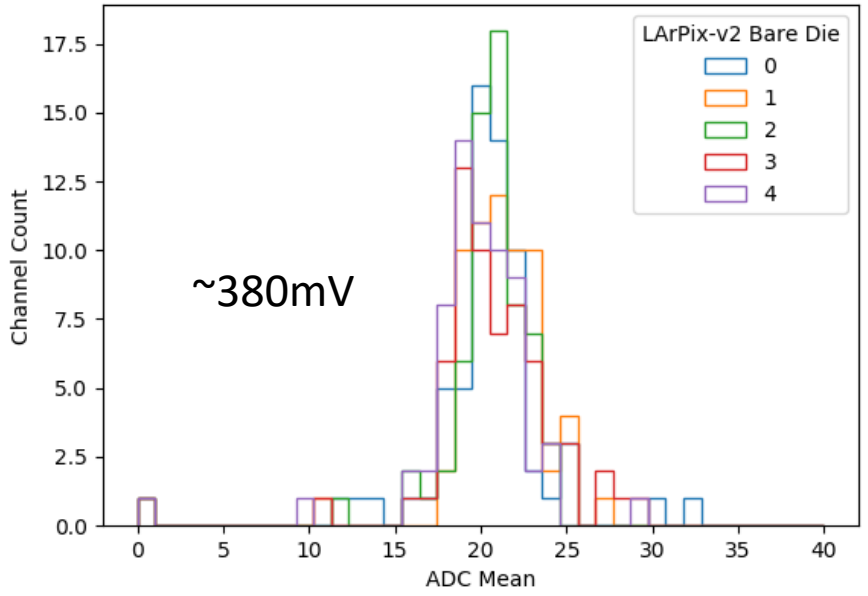
10 MHz system clock, *2.5 MHz transmit clock, UART word 2x as long*

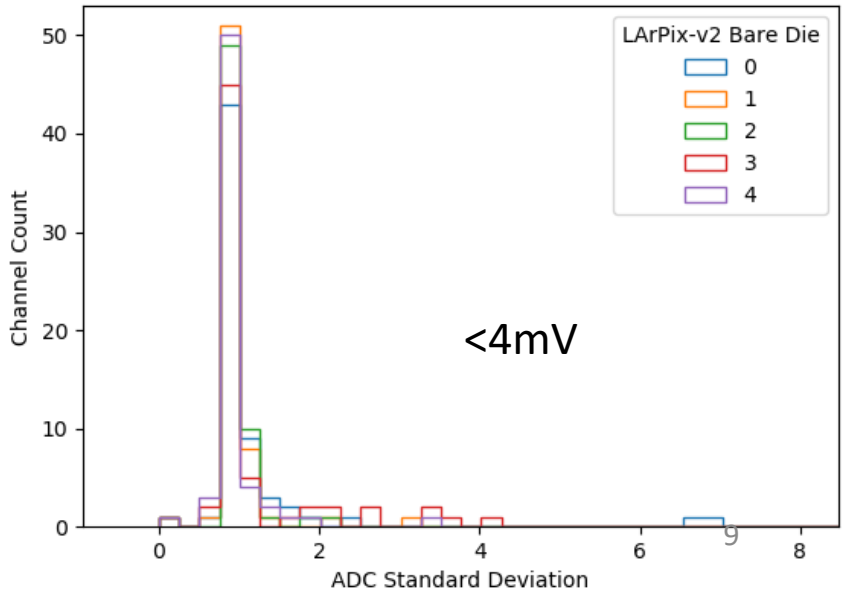
- Recover 100% packets cross triggering all channels (and natural triggers)
- Confirmed packet recovery with multiple chips linked through hydra I/O

Initial Noise Measurements









Noise measurements using a rolling periodic trigger at 100Hz, after rough tuning of bias currents, bias voltages (at full digital voltage)

Working Schedule

We are here (working in parallel) →

Critical decision →

Task	Duration	Start	End	Details
Produce: v2 ASIC	~10 weeks	Sep. 23	Jan. 6	11k ASICs produced by commercial vendor
Dice and Test: v2 ASIC Bare die	~4 weeks	Jan. 9	Feb. 3	Initial tests with bare silicon die to test viability, tune performance
Package: ~200 v2 ASICs	~5 weeks	Jan. 9	Feb. 10	Package a limited number of ASICs in two candidate packages to confirm/select optimum
Assemble: small-scale test pixel tiles	~2 weeks	Feb. 10	Feb. 24	Build initial test pixel tiles with a small number of packaged ASICs
Test: small-scale test pixel tiles	~3 weeks	Feb. 27	Mar. 14	Verify that packaging and pixel tile design provides sufficient performance
Select production package, procure 2500	~6 weeks	Mar. 17	Apr. 27	Start full-scale chip packaging, after selection of optimal package
Package ASIC QA, pre-assembly (2500)	~4 weeks	Apr. 30	May. 24	Room-temp socket test for ASIC alive/dead before pixel tile assembly
Milestone: FNAL Director's Review		Apr. 27		
Assemble: Batch #1 full-scale pixel tiles	~2 weeks	May. 27	Jun. 8	Assemble initial batch of full-scale pixel tiles
Test: Batch #1 full-scale pixel tiles	~3 weeks	Jun. 11	Jun. 29	Verify that full-scale pixel tiles meet requirements
Deliver: Batch #1 full-scale pixel tiles	~1 week	Jul. 1	Jul. 5	Ship first batch of pixel tiles to Univ. of Bern
Install and test in prototype ND module	~3 weeks	Jul. 8	Jul. 29	Integrated test of LBNL electronics in DUNE Near Detector prototype TPC module
Milestone: Preliminary Design Review		Jul. 1		Approximate date of PRD for DUNE Near Detector Electronics
Milestone: DOE Independent Project Review		Jul. 14		For entire LBNF/DUNE, including focused session on DUNE Near Detector
Package remaining ASICs and QA test (8000)	~10 weeks	Apr. 27	Jul. 8	Package and then room-temp socket test for ASIC alive/dead before pixel tile assembly
Assemble, test, deliver remaining v2 pixel tiles	~8 weeks	Jul. 8	Sep. 3	Assemble, test, and deliver pixel tiles for ND prototype system (four TPC module)
Install and operate in full ND prototype system	~8 weeks	Sep. 3	Oct. 28	Assemble and operate complete ND prototype system (four TPC modules)
Milestone: DOE CD-2 Review		Oct. 26		For entire LBNF/DUNE, including focused session on DUNE Near Detector

Bottom line: by mid-March determine if LArPix-v2 has requisite cryogenic functionality to instrument 2x2

Pac-Man Card Status

- Pac-Man v1 PCB in hand and board assembled
- Testing with Trenz on-going
  - Powered up and communicating

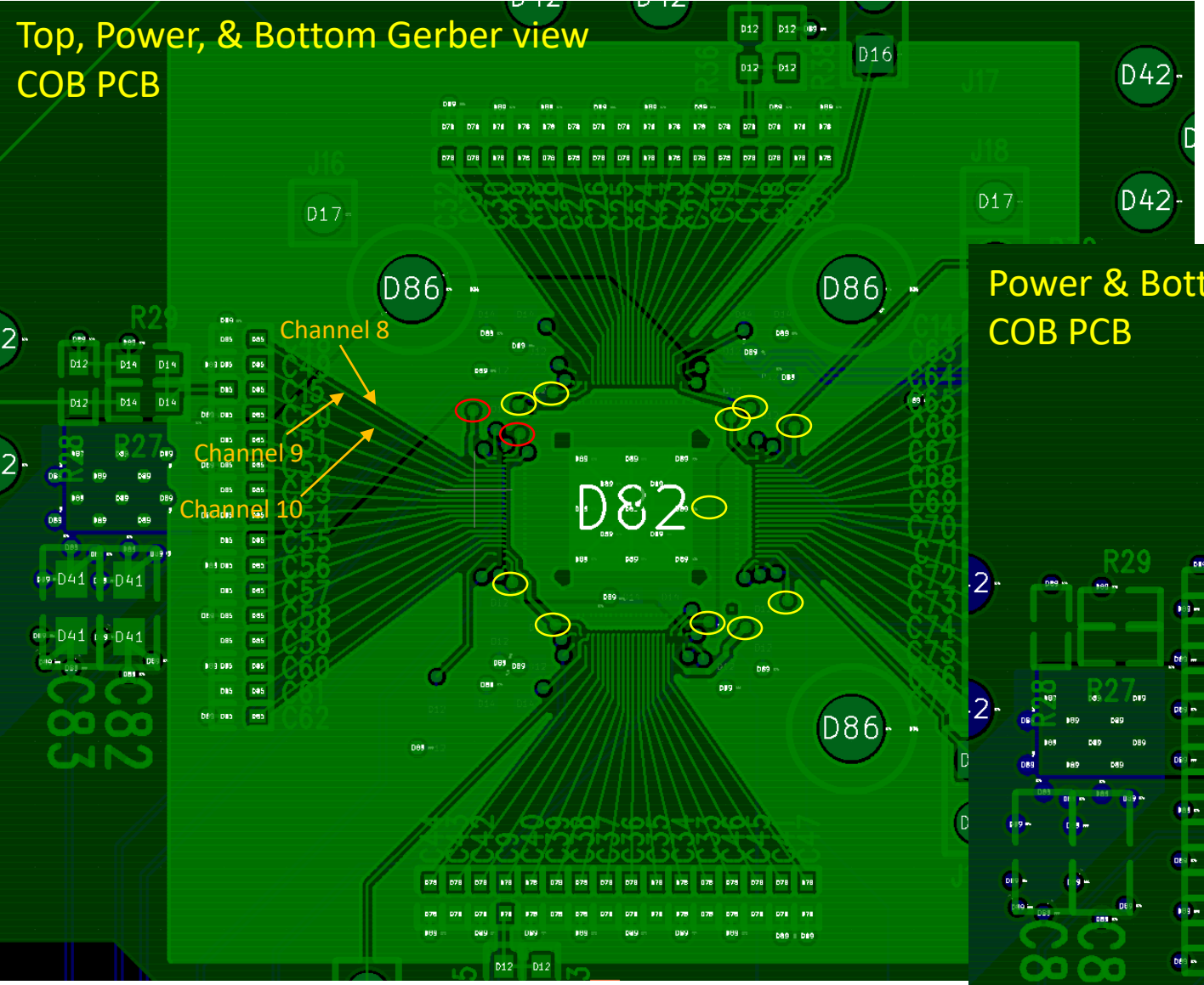
Hardware Feature Testing Plan

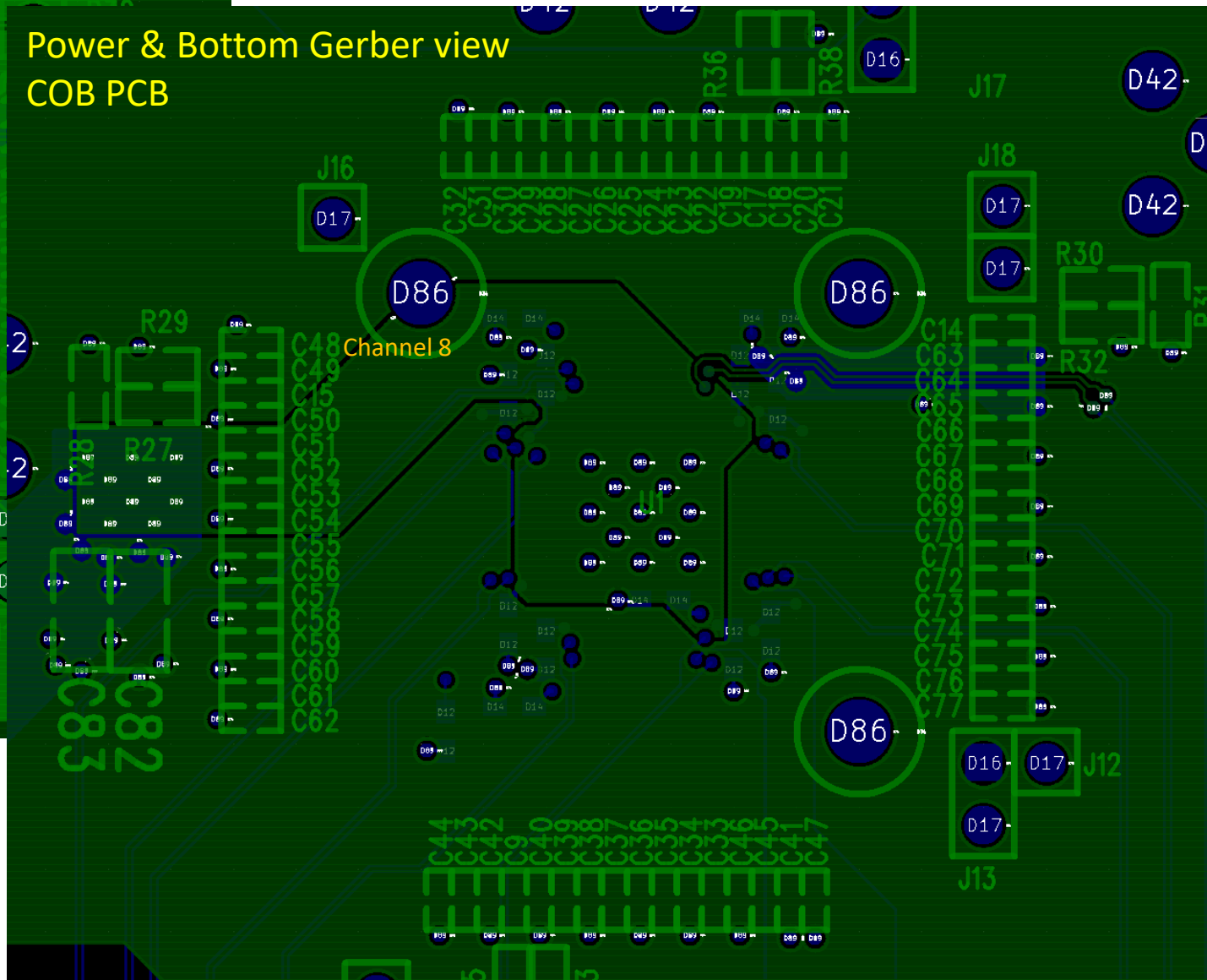
Test	Firmware Status
Trenz Hello World via JTAG and UART	Ready
Boot to Linux over SD Card, Ethernet	Ready
Blink LEDs	Ready
Pixel power (VDDA and VDDC) using PS I2C	To do
LVDS read/write and channel mapping	Nearly Ready
Pseudo-random loopback over LVDS	To do

from Mike Mulhearn 2/20/20

Summary

- Confirmed basic functionality of LArPix-v2
- Cold/warm analog assessment on-going
- ¼ tile test in next couple weeks


Top, Power, & Bottom Gerber view
COB PCB
Channel 8
Channel 9
Channel 10
D86
D82
D16
D42
D17


Power & Bottom Gerber view
COB PCB
Channel 8
D86
D16
D42
D17
J12
J13
J16
J17
J18
R29
R30
R32
R36
R38
C48
C49
C15
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