Updates on the TPC Electronics LBNC Meeting

David Christian, Marco Verzocchi

Fermilab

4-6 March 2020

Fermilab DUNE

Outline

- Status of ASICs and FEMBs developments and report from the DUNE internal preliminary design review (Feb 5-7 @ CERN)
- Progress with system test stands
- Preparation for the Warm Interface Board and system review (next week @ BNL), completing the preliminary design of all components (PTC, interface to interlocks)
- Progress with installation studies
- Schedule for run 2 of ProtoDUNE

ASICs and FEMBs review

- Held at CERN, 5-7 February
- Review committee: Philippe Farthouat (CERN, chair), Tim Andeen (Austin), Jaro Ban (Columbia), Michael Campbell (CERN), Gary Drake (Fermilab), Marek Idzik (Krakov), Jan Kaplon (CERN), Peter Lichard (CERN), Alessandro Marchioro (CERN), Paulo Moreira (CERN), Mitch Newcomer (Penn), Paul Rubinov (Fermilab)
- Slides and final report available at https://indico.fnal.gov/event/22423/other-view?view=standard

PDR – From the executive summary

- The committee would like to commend the team for putting together an as comprehensive as possible overview of the ASIC designs and FEMBs, and for responding to all the review committee questions promptly. The committee found the documentation and presentations useful in evaluating the maturity of the design, although the impossibility to have full access to some of the ASIC schematics has been limiting the work of the reviewers.
- The committee believes the current design does meet the standard for a 60% maturity. The committee has identified a number of recommendations which should be addressed. Many of these recommendations relate specifically to completing the specifications and to the design as well as design and verification methodologies of the ASICs.

PDR – Recommendations

- A complete and coherent list of specifications from both developments should be agreed and established.
- The design methodologies and verification methodologies need to be clarified and improved for all the ASICs.
- A programme and protocol for accelerated aging tests should be agreed and established for both solutions.
- Using a single clock source as master clock for all functions should be considered for the 3-chip solution (already done for the CRYO solution). In particular, as part of the design changes to be done for the COLDATA PLL, it should be considered to use the master 62.5MHz clock as input.
- For the 3-chip solution, the design of a single FEMB housing all the chips (i.e. no mezzanine) is to be pursued.
- The DUNE CRYO ASIC should be submitted only when all missing tests with nEXO version are finished. In particular, the test with the APA is to be done prior the submission. The schedule of this test is to be revisited if the DUNE CRYO is to be submitted in July.

PDR – Answers to review charge (2)

- Do the chips and boards satisfy the requirements ?
- Concerning the 3-chip solution, issues seem to be understood and simulation of the next version of designs are promising:
  - LARASIC has identified solutions. Consider improving the ESD protection on the input pads.
  - COLDADC issues also understood (with the exception of the large spread of power dissipation). The IR drop explanation for non-linearity requires a detailed analysis.
  - COLDATA has very small bugs. PLL issue seems understood
- CRYO is a less mature design (i.e. the design started only a year ago) and the first version of the CRYO ASIC has few issues (ADC speed, noise level to be understood, …) but fixes have been implemented in the second version (nEXO chip). Measurements of the nEXO chip should be used before going to next submission.

News since December meeting

- Completed bit error rate measurement on COLDATA (stopped at $< 2 * 10^{-15}$, test done without equalizers on the receiving end, 25 m cables, warm)
- Tests of packaged ColdADC indicate high yield (95 good chips out of 100 tested)
- Not much progress on CRYO:
  - nEXO version of the ASIC received last week, will be used to check that bugs found in first DUNE submission have been fixed, will also be used for system tests (ICEBERG), will allow for cross-talk studies
  - Still no progress on noise understanding (waiting for new test board)
  - Need to add pre-emphasis to line driver (unsuccessful data transmission tests with long cables) in next DUNE version

Design modifications for next version - LArASIC

- Addressed 3 issues in design
  - Ledge effect (decided to resize transistors that were causing the problems)
  - Baseline (improved uniformity)
  - Startup effect (increase yield in LN_2)
  - Simulations indicate that these 3 problems have all been solved
  - Remaining: complete layout and post-layout simulations (March)
- Remaining to do work
  - Add single ended to differential conversion, considering multiple options (port from ColdADC, test book design, add differential stage to single ended buffer)
  - Doing measurements (SDC test structure in COLDATA) and simulation to decide what is the best option to pursue
- Submission in June
- Committee recommends we revisit ESD protection
  - We may do so with separate submission after June

Design modifications for next version – ColdADC (i)

- Fixes for trivial mistakes
  - Input buffer level shifter
  - Wrong op-amp in BGR
- Non-linearity at room temperature most probably caused by IR drop
  - To be confirmed with IR tool, will reduce resistance of power network by using redistribution layer
- ADC Auto-Calibration
  - Failure (race condition) reproduced in simulation
  - Repartitioned digital logic to avoid problems
  - Most of the work already done

Design modifications for next version – ColdADC (ii)

- ADC Core Linearity
  - Increase closed-loop gain of op-amps in the ADC stages
- Linearity of multiplexer in ADC
  - Increase size of switches
  - Should also improve cross-talk performance
- ADC Data Overflow
  - Add protection logic
- Backend
  - Add power-on reset from COLDATA
  - Make it easier to synchronize the system
- Timeline
  - Driven by Core and Multiplexer Linearity issues
  - Goal: submission before end April

Design modifications for next version – COLDATA

- PLL locking at room temperature
  - Could either be an IR-drop issue or a reduction of the transconductance reduction in the voltage controlled oscillator
  - Investigating both
- Fix small I2C mistake
- Some changes in specification
  - Use 64 MHz/15 bits for the timestamp, instead of 2 MHz/8 bits
  - Improve E-Fuse interface
  - Remove one of the output data formats
  - Implement method for cable delay measurement
- From the review committee
  - Use 62.5 MHz clock to generate clock for data transmission PLL instead of external oscillator (discussing implementation)

Design modifications for next version – CRYO

- Add E-Fuses (hardware identifier for each chip, new requirement)
- Add tunable pre-emphasis to line driver (port from different SLAC design, required for DUNE, not needed for nEXO)
- Any additional change required to address noise, in case tests done with the modified test board indicate that the noise levels are still much larger than expected
- Any additional change required to address problems observed in system tests

Outline

- Status of ASICs and FEMBs developments and report from the DUNE internal preliminary design review (Feb 5-7 @ CERN)
- Progress with system test stands
- Preparation for the Warm Interface Board and system review (next week @ BNL), completing the preliminary design of all components (PTC, interface to interlocks)
- Progress with installation studies
- Schedule for run 2 of ProtoDUNE

Reminder – December status

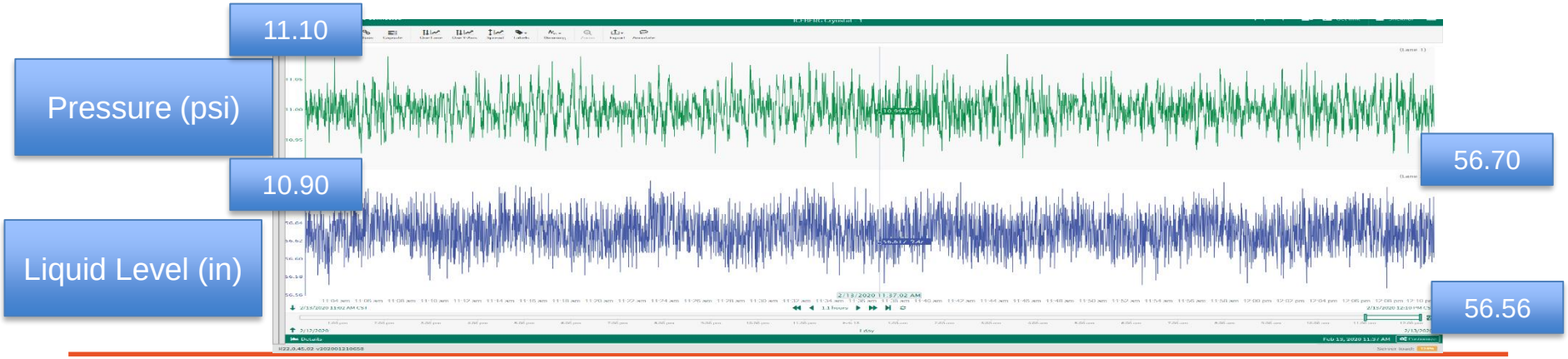
- Recommissioned cold box at CERN in front of ProtoDUNE-SP
  - Used 7th ProtoDUNE APA equipped with 20 ProtoDUNE FEMBs
  - Next run at CERN planned for late March / early April
- Working on improving the cryogenic system of ICEBERG to address issues observed in 2nd commissioning run
  - Pressure fluctuations
  - Issues with purifier
  - Understand damage to FE amplifiers

ICEBERG (i)

- Modifications of the cryogenic system
  - Improved control of pressure in the cryostat to prevent bubble formation (condenser)
  - Modifications to the filter
- Checked / redone all electrical connections between the TPC and the supplies / readout
  - Added interlock system to prevent unsafe situations for the detector
  - Identified damaged cable (providing high voltage to the cathode) that may have been the cause the cause of the discharges that damaged the FE electronics)

ICEBERG (ii)

- Modified condenser works fairly well, can maintain stable pressure level within ±0.1 psi
  - Need to raise pressure by 1 psi after ~1 hour interval (and then at a certain point lower the pressure, which involves turning off the cathode and bias voltages) to prevents bubbles from forming in the liquid
    - Procedure being made automatic, can run in stable conditions during day time, collect data
    - For the future will try to reroute some cables, add insulation outside the cryostat to reduce the need for this mode of operation

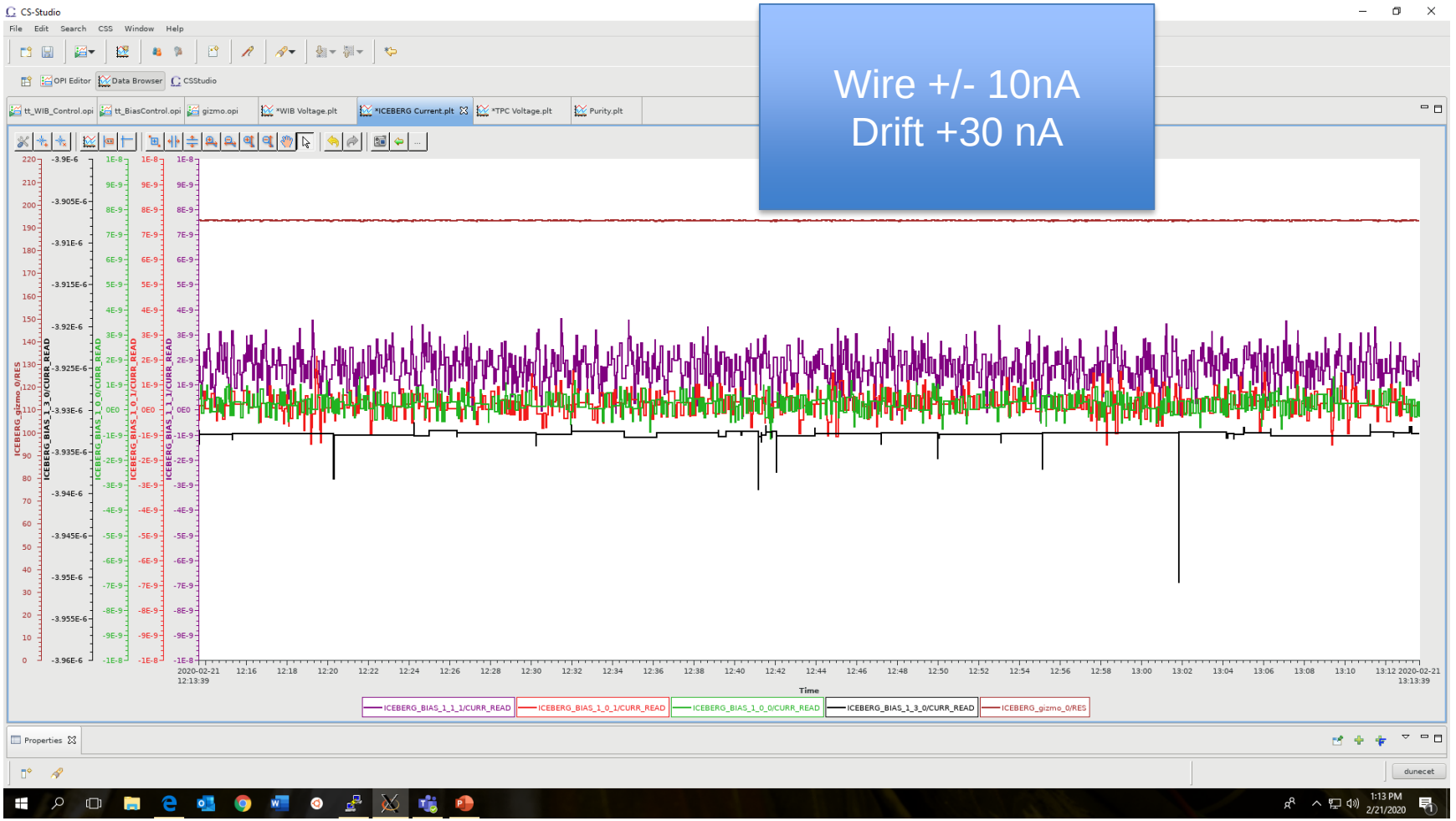


ICEBERG (iii)

- Modified condenser works fairly well, can maintain stable pressure level within ±0.1 psi
  - Need to raise pressure by 1 psi after ~1 hour interval (and then at a certain point lower the pressure, which involves turning off the cathode and bias voltages) to prevents bubbles from forming in the liquid
    - Procedure being made automatic, can run in stable conditions during day time, collect data
    - For the future will try to reroute some cables, add insulation outside the cryostat to reduce the need for this mode of operation

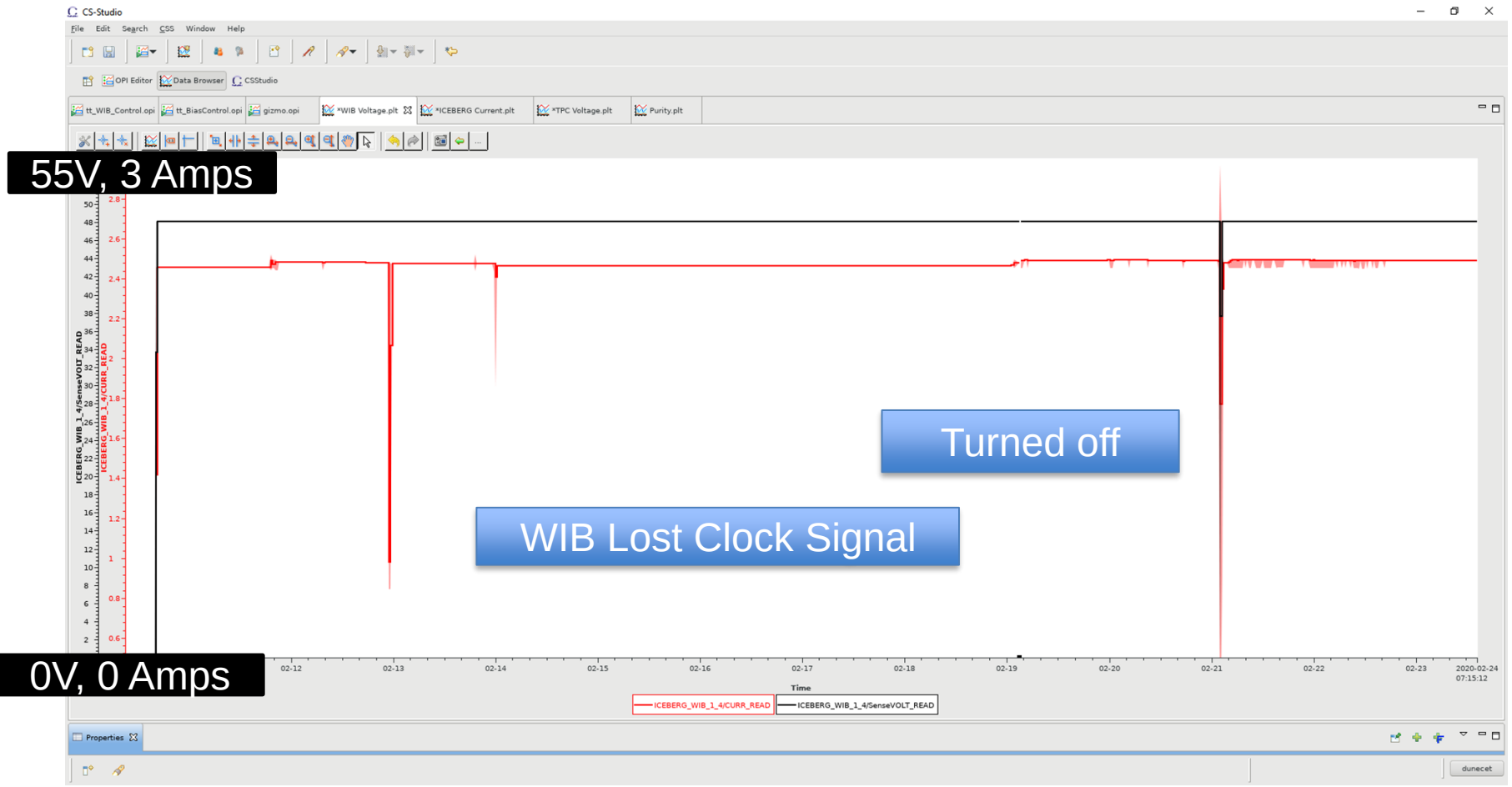
ICEBERG (iv)

- Very stable operating conditions: bias and cathode voltages (1h)



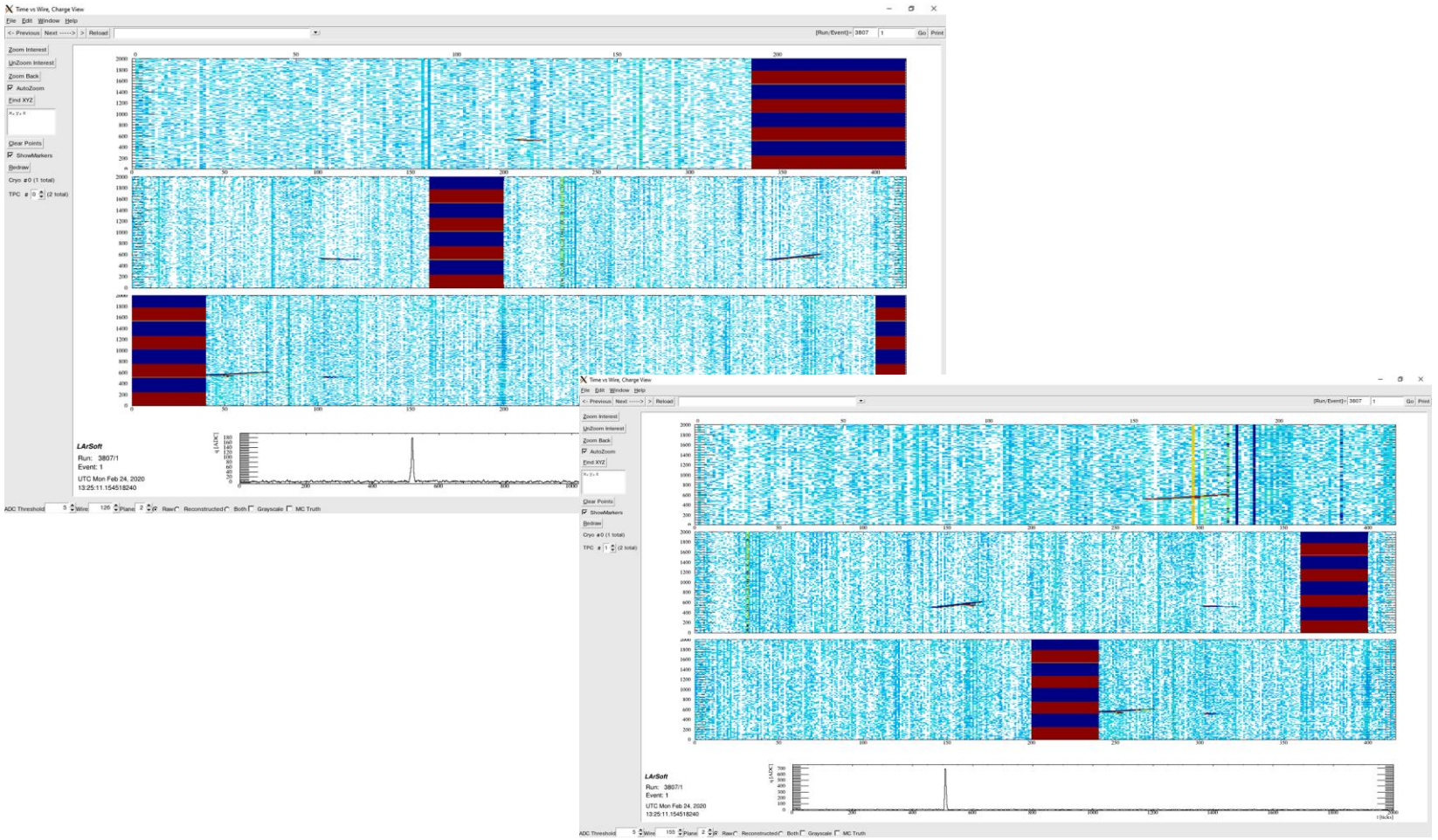
ICEBERG (v)

- Very stable operating conditions: power to FEMBs (12.5 days)



ICEBERG (vi)

- We see tracks (external cosmic ray trigger, few events / min)



ICEBERG (vii)

- Purifier still not working as planned
  - Limited lifetime (was 170 µs at the beginning of the fill, degraded to 100 µs over a period of 2 week, max drift distance is 190 µs)
  - Removed flow restriction last week, but speed of recirculation still too small (require 3 days to recirculate cryostat content)
  - Since then lifetime has increased to 110 µs
  - Planning for additional modifications to increase the heat exchange in the filter
  - Additional problem: pressure fluctuations up to 0.5 psi when the filter is emptied (for safety not operating the TPC when the filter is running)

ICEBERG (viii)

- Making progress with ICEBERG
- Will operate SBND style FEMBs in the next run of ICEBERG
- Can operate the cryostat reliably, but lifetime depends on purity of commercially provided argon
  - Not expecting significant improvements on the filter in the short time-scale
- Will operate photon detector system in June
  - Understand whether there is interference between TPC electronics and SiPMs readout/power
  - Will also make initial tests of additional RTDs on the APAs (planned for DUNE)

Outline

- Status of ASICs and FEMBs developments and report from the DUNE internal preliminary design review (Feb 5-7 @ CERN)
- Progress with system test stands
- Preparation for the Warm Interface Board and system review (next week @ BNL), completing the preliminary design of all components (PTC, interface to interlocks)
- Progress with installation studies
- Schedule for run 2 of ProtoDUNE

Review of WIB / System Aspects

- Third and final PDR for TPC electronics
- To be held at Brookhaven next week (10/11 March)
- Agenda page (includes charge, committee, documentation and slides will be posted later this week) available in Indico

08:30 - 08:50	Introduction *20'* Speaker: Marco Verzocchi (Fermilab)	
09:00 - 09:20	Grounding scheme *20'* Speaker: Linda Bagby (Fermilab)	
09:30 - 10:00	Warm Interface Electronics Crate Introduction *30'* Speaker: Bo Yu (Brookhaven National Lab)	
10:10 - 10:45	Experience with the WIEC, WIB, PTC in ProtoDUNE *35'* Speaker: Dr. Shanshan Gao (Brookhaven National Laboratory)	
10:55 - 11:10	Coffee break *15'*	
11:10 - 11:35	Intermediate WIB prototype hardware *25'* Speaker: Mr. Jack Fried (BNL)	
11:45 - 12:10	Hardware requirements for the DUNE WIB *25'* Speaker: Vladimir Tishchenko (BNL)	
12:20 - 13:10	Lunch *50'*	
13:10 - 14:25	WIB firmware and software requirements *1h15'* Speakers: Joshua Klein (University of Pennsylvania), Joshua Klein	
14:40 - 15:00	Changes to the PTC and PTB *20'* Speaker: Marco Verzocchi (Fermilab)	

Review of WIB / System Aspects

- Third and final PDR for TPC electronics
- To be held at Brookhaven next week (10/11 March)
- Agenda page (includes charge, committee, documentation and slides will be posted later this week) available in Indico

15:30 - 15:55	Interface with the FEMBs and the ASICs *25'* Speaker: David Christian (Fermilab)	
16:05 - 16:35	WIB firmware and software development plans *30'*	
16:45 - 17:30	Committee closed session *45'*	
18:00 - 20:00	Dinner *2h0'*	
Wednesday, 11 March 2020		
08:00 - 08:25	Interface to slow controls and interlocks *25'* Speaker: Marco Verzocchi (Fermilab)	
08:35 - 09:05	Design of the bias voltage and low voltage power supply plant and cable plant *30'* Speaker: Marco Verzocchi (Fermilab)	
09:15 - 09:40	Timeline, production and QC plans *25'* Speaker: Marco Verzocchi (Fermilab)	

Progress with WIB

- Intermediate WIB
  - Required for tests of FEMBs with COLDATA / CRYO
- Evolution of ProtoDUNE WIB
  - Uses Xilinx FPGA with Zynq CPU (more flexibility, cheaper FPGA)
  - Extended capabilities (and flexibility) for controlling / monitoring power lines to the FEMB
  - Evolutionary step toward DUNE WIB
- Two functioning prototypes
  - Need to develop new firmware

Further progress with WIB

- Collected requirements for hardware design of DUNE WIB
- In the progress of collecting firmware requirements for DUNE WIB
  - This also involves extensive discussions with DAQ consortium on how WIB, FELIX (DAQ backend), CCM (run control), and SC (slow control) interact
    - Significant updates to interface document, with additional material in the WIB firmware requirements document
- Planning for distributed team for WIB firmware design
  - Groups involved BNL, Penn, Pittsburgh, (Florida, Fermilab, UCDavis)
  - Need to have first version for tests of FEMBs with COLDATA / CRYO in ICEBERG / ProtoDUNE available in June (not all the capabilities will be implemented at the beginning, port firmware from ProtoDUNE)
  - Plan for integration tests with DAQ in view of ProtoDUNE Run 2 by the end of the year

System Design and Interlocks (i)

- No changes in grounding scheme (worked extremely well in ProtoDUNE)
- Value engineering for bias voltage distribution (contain costs, reduce number of crates / power supplies)
- Hardware interlocks (DUNE detector safety system – DDSS)
  - ICEBERG has demonstrated that these are absolutely necessary
  - Need to monitor status of FEMBs, WIBs, PTCs, low voltage supplies, bias voltage supplies, heaters and fans, receive inputs from other systems and facility (HV, cryogenic system, allow for eventual inputs from photon detector, calibration systems)

System Design and Interlocks (ii)

- DDSS not yet defined at this point
- We will modify the PTC to collect status information from the WIBs and pass it to the DDSS via dedicated optical links
  - Add small FPGA on PTC which will talk to WIBs via I2C bus on the crate backplane (will also add configurability via slow controls)
- Interlock on individual channels of bias voltage and low voltage power supplies
- Fans power supplies status will also be included in interlock decision, heaters supplies will be under complete control of DDSS
- Prefer to use industry standard solutions (i.e. PVSS-like system) but will still need some interface boards to translate levels, map connections between industrial modules and our supplies
  - Even if DDSS is not defined we have a conceptual design of the interface that is compatible with industrial solution

Documentation for reviews

- Significant effort in producing documentation for reviews
  - Datasheets for ASICs, documentation of planned design changes
  - Block diagrams, Gerber files, bill of materials for all custom printed circuit boards
  - Cabling diagrams (including naming conventions)
  - In the progress of updating all the interface documents with other consortia
- Quantity/quality of documentation is significant step forward relative to ProtoDUNE
- Reflected in the comments of the ASICs/FEMBs review and hopefully also of next week's review
- Still a lot to do to reach Final Design Review
  - Manufacturing plans
  - Quality control plans

Outline

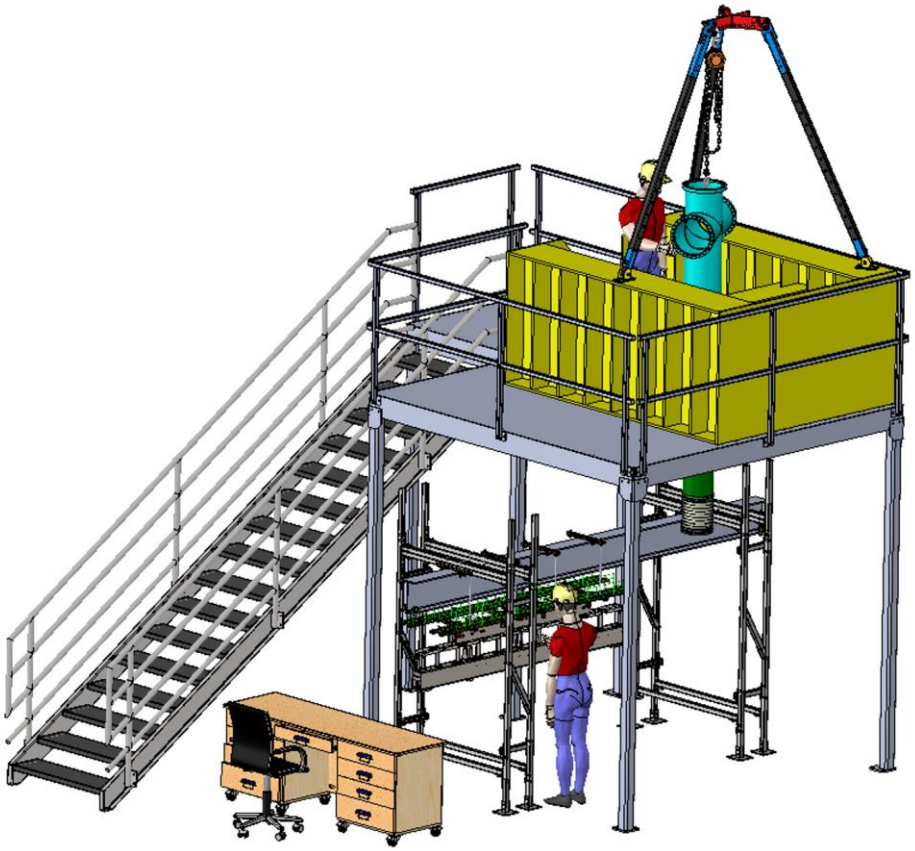
- Status of ASICs and FEMBs developments and report from the DUNE internal preliminary design review (Feb 5-7 @ CERN)
- Progress with system test stands
- Preparation for the Warm Interface Board and system review (next week @ BNL), completing the preliminary design of all components (PTC, interface to interlocks)
- Progress with installation studies
- Schedule for run 2 of ProtoDUNE

Brookhaven mockup (December)

Mockup of upper APA with cable trays, cryostat and DSS being built at BNL, ready for February 2020

- Practice installation of:
  - CE boxes
  - Cable trays, feedthrough
  - WIEC
- Practice cable routing
- Understand possible interface issues

Move to Ash River in 2020/2021
Make similar setup for lower APA



Brookhaven mockup (now)

Setup almost complete (need to add mockup of cryostat beams and cryostat penetration)

Brookhaven mockup (now)

Plans for studies in this mockup

- Understand support for cable grip holding cables going to lower APA
- Understand cable arrangements in cable trays (and whether we need bigger cable trays)
- Try procedures for routing cables through the cryostat penetration
- Test installation procedure of FEMBs and their support
- Understand process for removing trolley once the APA is its final position in the cryostat

First do it at a convenient height at BNL, then move everything to Ash River (with a complete APA) and repeat the process at 14m height

Study also cabling for lower APA (hang upside-down)

Outline

- Status of ASICs and FEMBs developments and report from the DUNE internal preliminary design review (Feb 5-7 @ CERN)
- Progress with system test stands
- Preparation for the Warm Interface Board and system review (next week @ BNL), completing the preliminary design of all components (PTC, interface to interlocks)
- Progress with installation studies
- Schedule for run 2 of ProtoDUNE

ProtoDUNE Run 2 Readiness (i)

The goal for ProtoDUNE Run 2 is to install 4 APAs with final FEMB prototypes in the Fall of 2021

Is this feasible for the TPC Electronics ?

- Assume submission of next round of ASIC prototypes by June 2020
- All ASICs received back from the foundry in September
- Start standalone testing and packaging
- Packaged ASICs available in October
- ASIC QC, installation on FEMBs, testing of FEMBs in November
- System tests in December and January (40% APA, ICEBERG, DUNE prototype APA at CERN)
- ASIC selection in February

ProtoDUNE Run 2 Readiness (ii)

The goal for ProtoDUNE Run 2 is to install 4 APAs with final FEMB prototypes in the Fall of 2021

Is this feasible for the TPC Electronics ?

- ASIC selection in February
- ASIC engineering run in March (MPW run needed to get sufficient number of ASICs)
- Packaged ASICs available in July
- ASIC QC, installation on FEMBs, FEMBs testing until October
  - 4 APAs: 640 LArASIC/ColdADC, 160 COLDATA/CRYO
- Installation on APAs, testing in cold box in October/November

ProtoDUNE Run 2 Readiness (iii)

Meeting the deadlines is not going to be easy

The first step is submitting ASICs by June

- ColdADC: planned submission date is April, starting integration work this week
- LArASIC: planned submission date is June, remaining big item is differential output buffer
- COLDATA: planned submission date is June, remaining big item is PLL
- CRYO: need results from system tests planned for July before submission (CRYO may not need engineering run prior to ProtoDUNE Run 2, can get enough ASICs in MPW run), main unknown is the noise level

ProtoDUNE Run 2 Readiness (iv)

We are fully aware of how tight the schedule for ProtoDUNE run 2 is

We have investigated ways of compressing the schedule and the only one available is very risky (i.e. make an engineering run for ColdADC and COLDATA in the Summer instead of doing first an MPW run followed by an engineering run)

Need to prevent any delays in the schedule

Conclusions

Preliminary design review of ASICs and FEMBs has validated our development strategy for the ASICs and indicates that we are on track for completing submissions of LArASIC/ColdADC/COLDATA in June

CRYO is recognized to be less mature than the other ASICs (but still a very impressive first prototype)

We are making significant progress with the design in all areas, hopefully this will be recognized also by the last PDR next week (WIB and system aspects)

Meeting the ProtoDUNE run 2 schedule is going to be challenging