PIP-II LCLK System

Technical Description

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Document Approval

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# Purpose

The LCLK-II System Technical Description provides a summary of the technical parameters, configuration and hardware needed to support the design and development of the Linac Clock System required by PIP-II.

# Scope

This document describes the technical requirements for the PIP-II Linac Clock System.

# Acronyms

|  |  |
| --- | --- |
| ACLK | Accelerator System Clock |
| BTL | Beam Transfer Line |
| CW | Continuous Wave |
| FAST | Fermilab Accelerator Science and Technology Facility |
| FPGA | Field Programmable Gate Array |
| FRS | Functional Requirements Specification |
| GRD | Global Requirements Document |
| HEP | High Energy Physics |
| L2 | WBS Level 2 System |
| L3 | WBS Level 3 System |
| LCLK-II | Linac Clock |
| LLRF | Low Level Radio Frequency |
| MEBT | Medium Energy Beam Transport |
| MIBS | Clock Event |
| MPS | Machine Protection System |
| PIP-II | Proton Improvement Plan II Project |
| PIP2IT | PIP-II Injector Test Facility |
| PMC | PCI Mezzanine Card |
| PMC-UCD | PCI Mezzanine Card Universal Clock Decoder |
| PRD | Physics Requirements Document |
| RF | Radio Frequency |
| TCLK | Tevatron Clock |
| TRS | Technical Requirements Specification |

# Introduction

The PIP-II Linac will be part of a larger accelerator complex involving 4 synchrotrons and associated beamlines supplying particle beams to high and low energy neutrino experimental areas (LBNF & SBN), muon experimental areas (g-2 & Mu2e) and the experimental test areas fed via Fermilab’s Switchyard (Mtest, Mcenter & Seaquest). It will be the task of the PIP-II Timing System to coordinate the operation of both the Linac and the rest of the accelerator complex by the distribution of the required clocks, machine resets, triggers and system state information.

* + The repetition rate of the Linac beam pulse (macro pulse) will be 20 Hz.
  + The macro pulse request (Booster Beam Resets) must be synchronized to the 60 Hz Booster mains frequency.
  + The timing system should distribute timing system information (via ACLK, TCLK or LCLK-II) to all relevant machine locations.

**PIP-II LINAC Timing System**

The Linac timing system is planned to be a two part system. The first part is a global timing system (here called ACLK) that provides high level, event based timing for the whole Fermilab accelerator complex while the second part is a RF synchronized clock system unique to the PIP-II linac itself (here called LCLK-II). This two level clock system concept has been used at Fermilab (TCLK & individual machine Beam Sync Clocks) to support complex operations for over 20 years through both the Tevatron and Neutrino operational eras. This concept provided significant operational flexibility that allowed for the successful completion of both the Tevatron Collider and Minos Experimental runs, with both programs operating in parallel.

The two systems are planned to have similar transmission and receiving hardware, with the LCLK hardware being a simplified version of the ACLK system. Both systems will be front ended for data communication, interface, event generation and overall clock system control. This is analogous to the TLG front end’s functionality with the existing TCLK system. There will also be console based applications developed to provide operator interface and system configuration. General purpose clock decoders are expected to be designed in a PMC format comparable to the PMC-UCDs presently used for TCLK decoding by front ends around the complex and as a FPGA design that can be included in other designs.

This document is intended to spell out the technical requirements for the LCLK-II system.

LCLK-II will use a Linac RF reference from the Linac LLRF system to allow beam synchronized event placement. Appropriate ACLK events (see appendix I) will be reflected onto LCLK-II to support AD/Control System based data acquisition. This is similar to the existing clock system setups at FAST and PIP2IT.

The LCLK-II system will have a single clock output with 16 bit event + 32 bit data field with frames broadcast at a harmonic of the 162.5 MHz of the PIP-II LLRF. Events are reflected from the accelerator clock system (ACLK/TCLK).

# LCLK-II LINAC RF Synchronous Clock System

LINAC Clock (LCLK-II) should be sourced via a single Clock Generator and transmitted on optical fiber along the length of the PIP-II Linac, to all transfer beamline devices, to the Booster Injection area and to the AD MAC Room.

The LCLK-II source should be supplied with and decode ACLK/TCLK. Pertinent ACLK/TCLK events and their associated data fields should be reflected onto LCLK. This would negate the need for LCLK listening front ends from having to decode ACLK as a second clock required for connection to AD/Control System.

LCLK-II will use an RF reference from the PIP-II LLRF system to allow for RF synchronized event placement. All LCLK-II events will be RF synchronized. Those events requiring beam synchronization (markers, etc.) will need to be sourced/triggered via the LLRF system. Appropriate ACLK events will be reflected onto LCLK-II to support existing accelerator control system-based data acquisition including all Booster Reset events. This is similar to the existing clock system setups at FAST and PIP2IT.

The LCLK-II system will have a single clock output with 16 bit event + 32 bit data field with frames broadcast at the RF harmonic frequency received from the PIP-II LLRF Master Oscillator. Events are reflected from the accelerator clock system (ACLK/TCLK). All events on LCLK-II will be synchronized with the RF. Beam synchronized events will be triggered via trigger inputs from the PIP-II LLRF system.

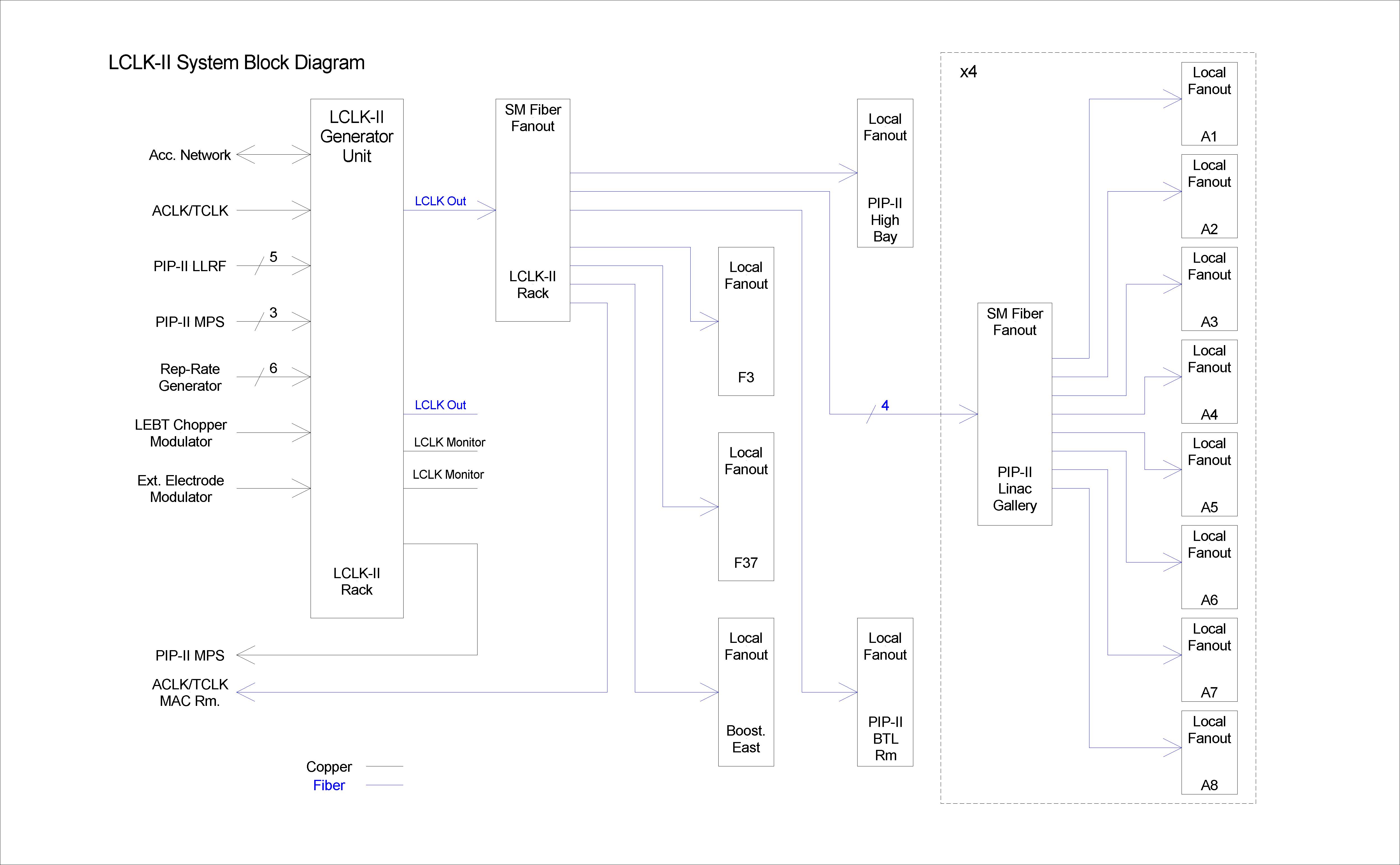
LCLK will broadcast PIP-II LLRF sourced beam synchronous events (Macro Pulse & Bunch markers).

LCLK-II will broadcast MPS sourced events (triggers, permit status, etc., for further information see MPS PRD).

LCLK-II will broadcast Rep-Rate Generator triggered event (10 Hz, 60Hz, variable rates).

LCLK-II will broadcast LEBT Chopper and Extraction Electrode Modulator triggered events.

LINAC Clock (LCLK-II) should be sourced via a single Clock Generator and transmitted on redundant optical fibers along the length of the PIP-II Linac, to all BTL device locations, to the Booster Injection area and to the Accelerator Division MAC Room for distribution to other AD/Controls systems and ACLK.



# LCLK-II General Requirements

The LCLK-II Timing System design shall satisfy the following requirements:

* Highly reliable, fail-safe operation;
* Compatible with the staged PIP-II commissioning;
* Capable of logging and time stamping all changes of its state;
* Generate a Master Beam Trigger Event for the LEBT.
* Capable of triggering loss of MPS/beam permit events to allow post mortem fault analysis;
* Restricted, documented privileges to access and modify configurations;
* Expandable in order to support modifications and future upgrades such as new operational scenarios without major modifications;
* Events capable of being individually enabled/disabled;
* 16 bit event + 32 bit data packet (total 48 bits of data in event frame)
* Event data phase locked to Linac RF harmonic (162.5 MHz)
* Standard encoding scheme (Modified Manchester, 8b/10b, Gigabit ethernet, etc.)
* LCLK status output to MPS (pull Linac beam permit if RF input fails, etc.)

# LCLK-II

1. High frequency phase locked to LINAC rf (162.5 MHz)

2. 16 bit LCLK event + 32 bit data field

a) Total transmission frame (48 bits + start & parity bits) < 80 nS

b) Data fields:

(1) LCLK Event (16 bits)

- $0000-$00FF defined to match existing TCLK events

- reflected ACLK/TCLK events

- $0100-$01FF defined as Machine State data

- MI, RR, BSSB, SWYD (data may be sourced from MDAT)

- Linac? Booster? GPS sync'd time stamp?

- $0200-$FFFE available for future definition

-$FFFF defined as null event (with $00000000 as event data)

(2) Event Data (32 bit)

- reflected ACLK event data for reflected ACLK events

- event count for TCLK events

- Machine State from TLG ($010n events)

c) Event Priorities (matches ACLK/TCLK priorities, see appendix 2)

(1) Primary Events $0000-$00FF, $0200-$0205

- highest level events, bump lower level events in queue

- $0200-$0205 events have highest priority

- $0000-$00FF events prioritized per TCLK priority chain (see appendix 2)

- Must have minimum of 1.2 uS spacing between TCLK related events

(2) Secondary events $0200-$FFFE

- placed between primary events in serial transmission

(3) Tertiary events $0100-$01FE

- placed between primary events in serial transmission

- may be bumped by Secondary events

(2) Null event $FFFF

- fills frame space not occupied by above events

3. redundant transmission

a) 2 fibers from repeater to repeater

b) constant monitor/comparison with auto switchover of local outputs at repeaters

- alarm in case of loss of redundant transmission (single fiber signal

failure )

- Beam inhibit if total clock loss at repeater

4. External inputs

a) 162.5 MHz from PIP-II LLRF

b) ACLK/TCLK

c) Fall of Linac Permit from MPS

d) Reset of Linac Permit from MPS

e) HEP Macropulse Start of Beam from LLRF

f) Linac Study Macropulse Start of Beam from LLRF

g) Linac CW Start of Beam from LLRF

h) Linac Bunch Trigger from LLRF

i) LEBT Chopper Modulator

j) Extraction Electrode Modulator

k) Rep-Rate Generator Triggers

5. Outputs

a) LCLK on Single Mode Fiber (Qty. 2)

b) LCLK monitor (LEMO, 50 ohm)

c) LCLK Status to MPS (LEMO, TTL, 50 ohm)

# LCLK-II Repeaters & Links

The Timing System will be carried on single mode optical fiber links throughout the various PIP-II areas, the Booster Injection area and back to the MAC Room. This will require the development of appropriate fiber repeaters with fanout capability. The fanout will need to be selected between either a copper (CAT-5?) or fiber connection to the clock decoders. This decision should be made as early as possible due to the impacts on both repeater and decoder designs.

# LCLK-II System Hardware

**LCLK Timing system hardware**

**LCLK Generator Unit** (LCLK-II) (2 units)

* ACLK/TCLK decoder
* Ethernet Interface
* LLRF Interface (triggers & RF)
* MPS Interface (triggers & LCLK Status out)
* Rep Rate Generator Interface (triggers)
* LEBT Chopper Interface
* Extraction Electrode Interface
* SM Fiber LCLK-II out (2 min)

**LCLK Global Distribution** (8 units)

* ACLK/LCLK Fiber distribution chassis (SM Fiber in – 12+ SM fiber out)

**LCLK Local Distribution** (40 units)

* ACLK/LCLK Local Fanout distribution chassis (SM fiber in – SM fiber & copper out)

**LCLK Decoding** (# units TBD)

* MFTU – ACLK/LCLK decoder configuration
* ACLK/LCLK – UCD module (PMC?)
* ACLK/LCLK – Decoder FPGA & Code

**LCLK-II Input sources**

ACLK/TCLK

* Input type
  + TCLK (LEMO, 50 ohm, TTL) (prototype system input)
  + ACLK (TBD, possibly sm fiber input)

PIP-II LLRF

* Linac RF harmonic (162.5 MHz, LEMO)
* HEP macro-pulse event trigger (50 ohm, TTL)
* Linac Pulsed Study macro-pulse event trigger (50 ohm, TTL)
* Linac Start of CW Study event trigger (50 ohm, TTL)
* Linac bunch trigger (50 ohm, TTL)

PIP-II MPS

* Linac Beam Permit Fall (50 ohm, TTL)
* Linac Beam Permit Reset (50 ohm, TTL)

PIP-II LEBT Chopper Modulator

* Chopper event trigger (50 ohm, TTL)

PIP-II Extraction Electrode Modulator

* Extraction Electrode event trigger (50 ohm, TTL)

PIP-II Rep-Rate Generator

* 10 Hz event trigger (50 ohm, TTL)
* 60 Hz event trigger (50 ohm, TTL)
* Rate “M” selectable event trigger (50 ohm, TTL)
* Rate “N” selectable event trigger (50 ohm, TTL)

# Hardware Requirements

**LCLK Generator Unit**

The LCLK Generator Unit (LGU) will serve as the source of the LCLK signal to be made available to all PIP-II controls equipment locations. It should have the following characteristics:

* 19” Equipment Rack mountable
* Ethernet Interface
* TCLK/ACLK Interface and decode capability
* PIP-II LLRF Interface
  + Event trigger inputs (4 minimum)
  + RF Input
* MPS Interface
  + Event trigger inputs (3 minimum)
  + LCLK Status
* Rep Rate Generator Interface
  + Event trigger inputs (6)
* LEBT Chopper Modulator Interface
  + Event trigger
* Extraction Electrode Modulator Interface
  + Event trigger
* Single-Mode Fiber Optic LCLK Output (2 minimum)
* LCLK Monitor Output (2 minimum)

**Single-Mode Fiber Fanout Unit**

* Based on existing Fiber Fanout unit design developed for SBND
* 19” Equipment Rack mountable
* Single-Mode Fiber LCLK Input
* Single-Mode Fiber LCLK Output (10 mininum)

**LCLK Local Fanout Unit**

* Based on existing Fiber to Copper Fanout unit design developed for SBND
* 19” Equipment Rack mountable
* Single-Mode Fiber LCLK Input
* Single-Mode Fiber LCLK Output
* Copper LCLK Output (8 mininum)

**Multi-Function Timing Unit**

* Based on existing MFTU with ACLK/LCLK FPGA decoding update
* 19” Equipment Rack mountable
* ACLK/LCLK Input
* LEMO Outputs

**ACLK/LCLK Universal Clock Decoder (UCD) Module**

* PMC based
* LCLK UCD FPGA & Code
* ACLK/LCLK Input

**ACLK/LCLK Universal Clock Decoder (UCD) FPGA & Code**

* ACLK/LCLK Input
* Event decode with settable delays
* FPGA based

# LCLK-II Event Descriptions

|  |  |
| --- | --- |
| **Event** | **Description** |
| $0000 | Super Cycle and Master Clock Reset";marks start of supercycle |
| $0002 | Time Plot Timestamp Reset:generated once every 50,000,000 TCLK cycles (every 5 seconds); not synchronized to any other event |
| $0007 | 720 Hz; synchronized to AC line |
| $000C | 20 Hz; synchronized to GMPS BMIN |
| $000F | 20 Hz; synchronized to A phase of AC line in MAC room |
| $008F | 1 Hz; Generated by GPS RCVR in computer room |
| $00FF | No-Op |
| $0100 |  |
| $0101 | Reserved BSSB State |
| $0102 | Reserved LINAC State |
| $0103 | Reserved Booster State |
| $0104 | Reserved Recycler State |
| $0105 | Reserved Main Injector State |
| …. |  |
| $0200 |  |
| $0201 | LINAC Start of HEP Beam Event; triggered by Linac LLRF |
| $0202 | LINAC Start of Pulsed Studies Beam Event; triggered by Linac LLRF |
| $0203 | LINAC Start of CW Studies Beam Event; triggered by Linac LLRF? |
| $0204 | Linac Variable Bunch Trigger Event |
| $0205 |  |
| $0206 |  |
| $0207 |  |
| $0208 | "Beam Event"; Beam cycle event triggered by LEBT Chopper Modulator |
| $0209 | "Beam Event"; Beam cycle event triggered by Extraction Electrode Modulator |
| $020A | "1 Hz"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator |
| $020B | Rate N"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator  Selectable rate: 0.2, 0.5, 1, 2, 2.5, 5, or 10Hz |
| $020C | Rate M"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator  PIP2IT Commissioning; Selectable rate: 0.2, 0.5, 1, 2, 5, 10 or 20Hz |
| $020D | "10 Hz"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator |
| $020E | "60 Hz"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator |
| $020F | "20 Hz"; synchronized to AC line and RF Master Oscillator, triggered by Rep-Rate Generator |
| $0210 |  |
| $0211 | LINAC Beam Permit has Dropped; triggered by MPS |
| $0212 | LINAC Beam Permit Reset; triggered by MPS |
| $0213 |  |
| $0214 |  |
| $0215 |  |
| $0216 |  |
| …. |  |

# TCLK Event Priority

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Priority | Event |  | Priority | Event |  | Priority | Event |  | Priority | Event |
| 1 | $0000 |  | 58 | $001D |  | 134 | $003C |  | 195 | $0070 |
| 4 | $0090 |  | 60 | $000C |  | 135 | $00A3 |  | 197 | $0028 |
| 5 | $0091 |  | 61 | $00F1 |  | 136 | $00A4 |  | 198 | $00E4 |
| 6 | $0085 |  | 62 | $00AC |  | 137 | $0083 |  | 199 | $009E |
| 7 | $000E |  | 63 | $001B |  | 139 | $00E8 |  | 200 | $0096 |
| 8 | $0093 |  | 68 | $0007 |  | 140 | $00ED |  | 201 | $0097 |
| 9 | $0094 |  | 69 | $000F |  | 143 | $002C |  | 202 | $0098 |
| 12 | $001A |  | 71 | $0087 |  | 144 | $0058 |  | 203 | $0052 |
| 15 | $0080 |  | 74 | $0027 |  | 147 | $007A |  | 204 | $0053 |
| 17 | $00A5 |  | 75 | $002F |  | 148 | $00B3 |  | 205 | $0038 |
| 19 | $0030 |  | 76 | $00EF |  | 149 | $001E |  | 206 | $0039 |
| 21 | $00AE |  | 77 | $00E7 |  | 150 | $001F |  | 213 | $00F6 |
| 22 | $008E |  | 78 | $00BA |  | 151 | $0034 |  | 214 | $0024 |
| 24 | $0032 |  | 80 | $007C |  | 155 | $0050 |  | 215 | $003A |
| 25 | $0004 |  | 81 | $00DD |  | 156 | $0051 |  | 217 | $0072 |
| 26 | $00EA |  | 82 | $008C |  | 157 | $008D |  | 218 | $007E |
| 27 | $00BE |  | 83 | $00DA |  | 158 | $0082 |  | 221 | $003B |
| 28 | $00BF |  | 84 | $00A0 |  | 159 | $000B |  | 223 | $00A9 |
| 32 | $0020 |  | 85 | $00A1 |  | 160 | $0088 |  | 225 | $00A7 |
| 33 | $0021 |  | 87 | $0079 |  | 161 | $000A |  | 227 | $00B0 |
| 34 | $0023 |  | 88 | $0031 |  | 169 | $0095 |  | 228 | $00B1 |
| 36 | $00E0 |  | 90 | $0018 |  | 170 | $0084 |  | 233 | $00F3 |
| 37 | $00E1 |  | 91 | $00A2 |  | 172 | $0037 |  | 238 | $00A8 |
| 38 | $00E2 |  | 93 | $00B2 |  | 173 | $0005 |  | 239 | $008F |
| 39 | $00E3 |  | 94 | $00B5 |  | 174 | $0035 |  | 244 | $00BB |
| 40 | $00E9 |  | 97 | $0002 |  | 175 | $0036 |  | 245 | $00BC |
| 41 | $0029 |  | 99 | $00A6 |  | 176 | $0057 |  | 247 | $00B9 |
| 42 | $002A |  | 100 | $0003 |  | 177 | $0033 |  | 248 | $0009 |
| 43 | $002B |  | 104 | $0086 |  | 178 | $003F |  | 249 | $00F7 |
| 45 | $002D |  | 105 | $0089 |  | 179 | $00AF |  | 251 | $00B8 |
| 46 | $002E |  | 109 | $00AD |  | 184 | $0099 |  | 252 | $000D |
| 47 | $00DE |  | 114 | $00B4 |  | 185 | $009A |  | 253 | $00BD |
| 49 | $0011 |  | 115 | $003E |  | 186 | $009B |  | 254 | $00FA |
| 50 | $0012 |  | 116 | $003D |  | 187 | $009C |  |  |  |
| 51 | $0013 |  | 117 | $007B |  | 188 | $009D |  |  |  |
| 52 | $0014 |  | 119 | $00E6 |  | 189 | $007D |  |  |  |
| 53 | $0015 |  | 123 | $0022 |  | 190 | $00B6 |  |  |  |
| 54 | $0016 |  | 124 | $0010 |  | 191 | $009F |  |  |  |
| 55 | $0017 |  | 126 | $0025 |  | 192 | $004C |  |  |  |
| 56 | $0019 |  | 127 | $0026 |  | 193 | $007F |  |  |  |
| 57 | $001C |  | 133 | $0081 |  | 194 | $0092 |  |  |  |

# Summary

The Timing System is vital to ensuring safe and long-term reliable operation of PIP-II and the entire Fermilab accelerator complex. Its role is to provide timing and coordination to the accelerator complex.

# Reference Documents

|  |  |  |
| --- | --- | --- |
| **#** | **Reference** | **Document #** |
| 1 | PIP-II Global Requirements Document (GRD) | ED0001222 |
| 2 | PIP-II Timing System PRD | ED0010229 |