Clocking System
by Mark Austin

Cost: $5000
Size: 4U chassis

The Clocking System consists of a 4U chassis with a 12V 650W internal power supply. This supply feeds the Power Supply Board (PwrBoard). The PwrBoard contains a connector with up to 4 different screw terminal connections for each of the following supplies: 12V, 5V, 3.3V, 1.8V, 2 manually adjustable positive supplies settable from 0.6V to 5V, as well as 2 manually adjustable negative supplies settable from -3.3V to -30V. The positive supplies are capable of up to 200W each and the negative supplies are capable of up to 75W each given that the total of all supplies cannot exceed the total 650W main supply.

Each supply can be monitored for appropriate voltage and each supply can be independently enabled or disabled (except the 12V supply; if it is off, the FPGA is powered down). The positive power supplies also have remote sensing pins that can be wired to other locations. This allows the power supply to automatically adjust the voltage if there is a small voltage drop at the remote location.

The 12V supply feeds the BaseBoard located within the chassis. The BaseBoard has the connectors to receive an Arria 10 SOC SOM (system-on-chip and system-on-module) manufactured by Reflex CES. This SOM contains an ARM dual-core Cortex-A9 MPCore and up to 660KLEs. The I/O connectors external to the chassis available from the system include a USB 3.0 connector, a USB connector for connection to the hard processor system and the MAX10 on the SOM, a USB-OTG, a JTAG connector, 2 ethernet-RJ45 connectors, and 4 SFP+ connectors for fiber transceivers. The I/O connectors internal to the chassis include an I2C/SPI, PMBUS, FX3, as well as 2 Off-Board connectors that each contain 10 transceivers and 40 LVDS pairs (all of which are tuned to match trace length from the FPGA to the connector). These two Off-Board connectors are meant to be used for connecting yet to be designed riser cards, front panel cards, or back panel cards, etc. that will reside within the chassis and be powered by the other connections available on the PwrBoard.

This Clocking System can be tailored to handle all sorts of I/O interfaces and designs by utilizing the 2 Off-Board connectors. These inputs and outputs will be fed into the FPGA where various code can be implemented. The system will contain some base code that will be standard to all systems. This includes but is not limited to the encoding/decoding of the new clock that will supersede TCLK as well as a connection to the controls network. The replacement clock will be a 650MHz serial signal which uses an encoding scheme called bi-phase or modified Manchester coding. This is the method used with TCLK. The new ACLK will contain 65-bits so as to align with the old TCLK transitions. There is a start bit, a 16-bit EVENT, 32-bits of data, a parity bit and 15 padded bits (the padded bits could be utilized for possible error checking). While the LCLK will contain 52 bits so as to align with the 162.5MHz of the RF clock. There is a start bit, a 16-bit EVENT, 32-bits of data, a parity bit and 2 padded bits.