

# Overview of DUNE SP-PD Readout System

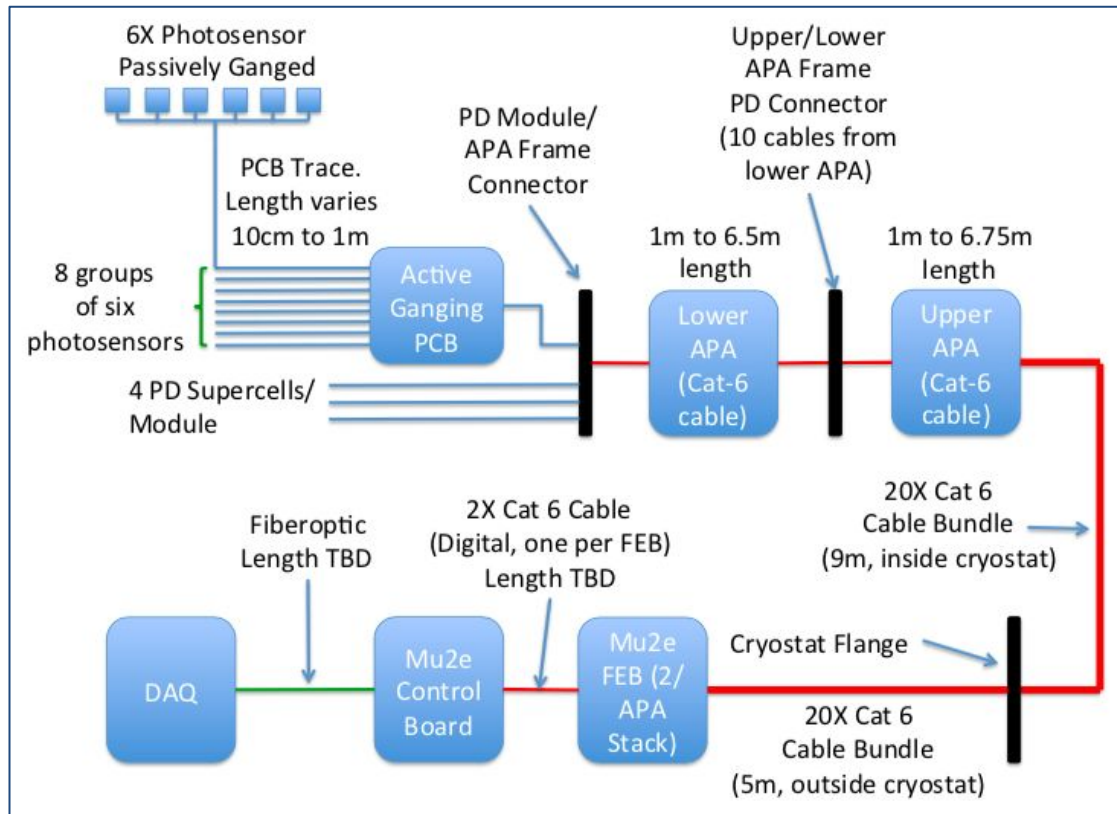
Matt Toups, FNAL

6/19/2020

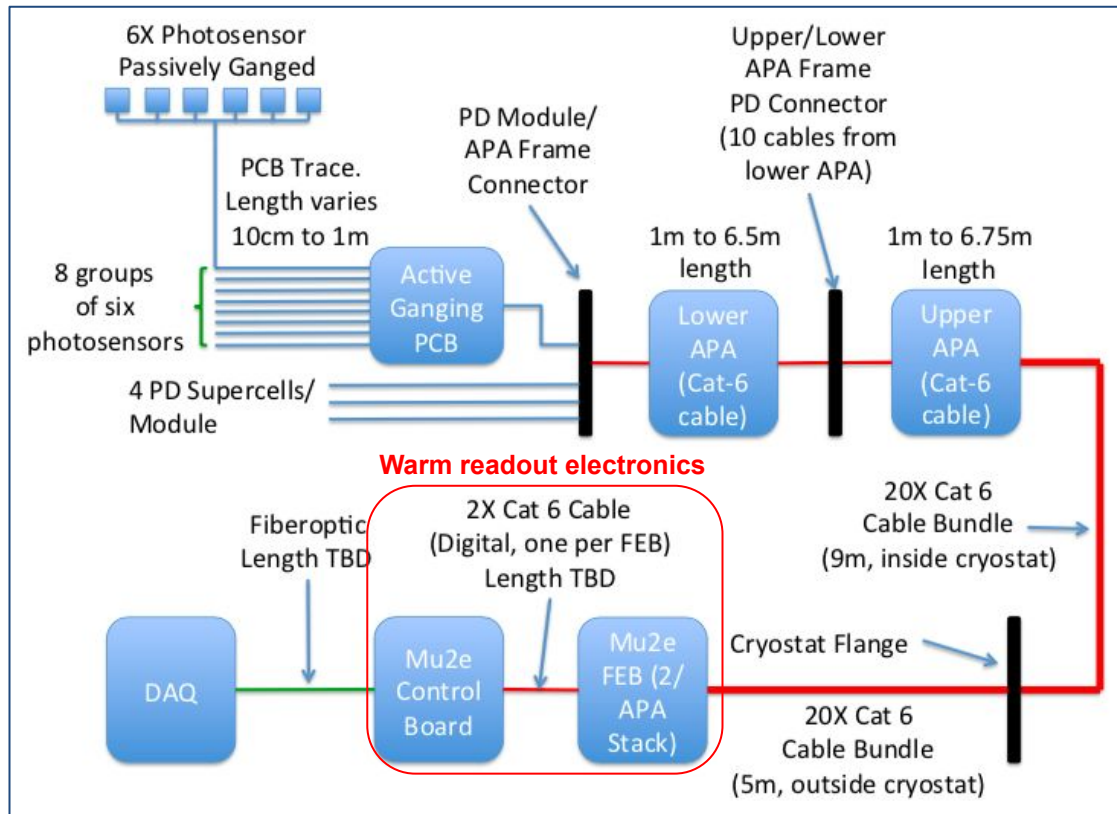
# Outline

- Overview of Readout Chain
- DAPHNE
- DAPHNE Power Delivery
- DAPHNE Internal Review
- Summary

# Overview of Readout Chain (TDR)

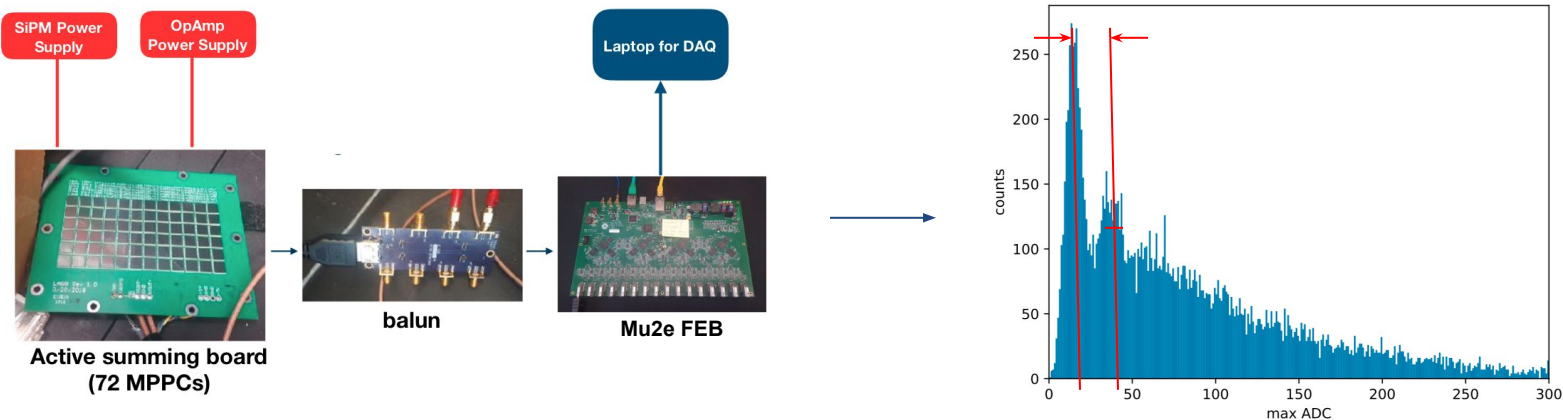


# Overview of Readout Chain (TDR)



# Mu2e FEB Testing

- Bench test in liquid nitrogen of 72 actively summed Hamamatsu MPPCs read out by Mu2e FEB demonstrated a signal-to-noise of 4



# Requirements Affecting Warm Readout

## Executive Board Held Requirements

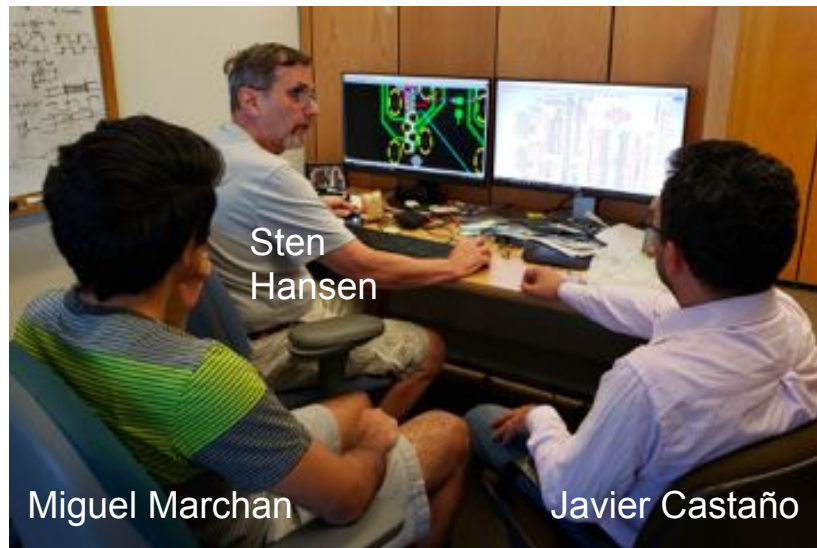
- **SP-FD-4:** Time resolution  $< 1 \mu\text{s}$  (goal  $< 100 \text{ ns}$ )

## Technical Board Held Requirements

- **SP-PDS-13:** Data transfer  $< 8 \text{ Gbps}$  to DAQ
- **SP-PDS-14:** Signal-to-noise  $> 4$
- **SP-PDS-15:** Dark noise rate  $< 1 \text{ kHz}$
- **SP-PDS-16:** Dynamic range  $< 20\%$

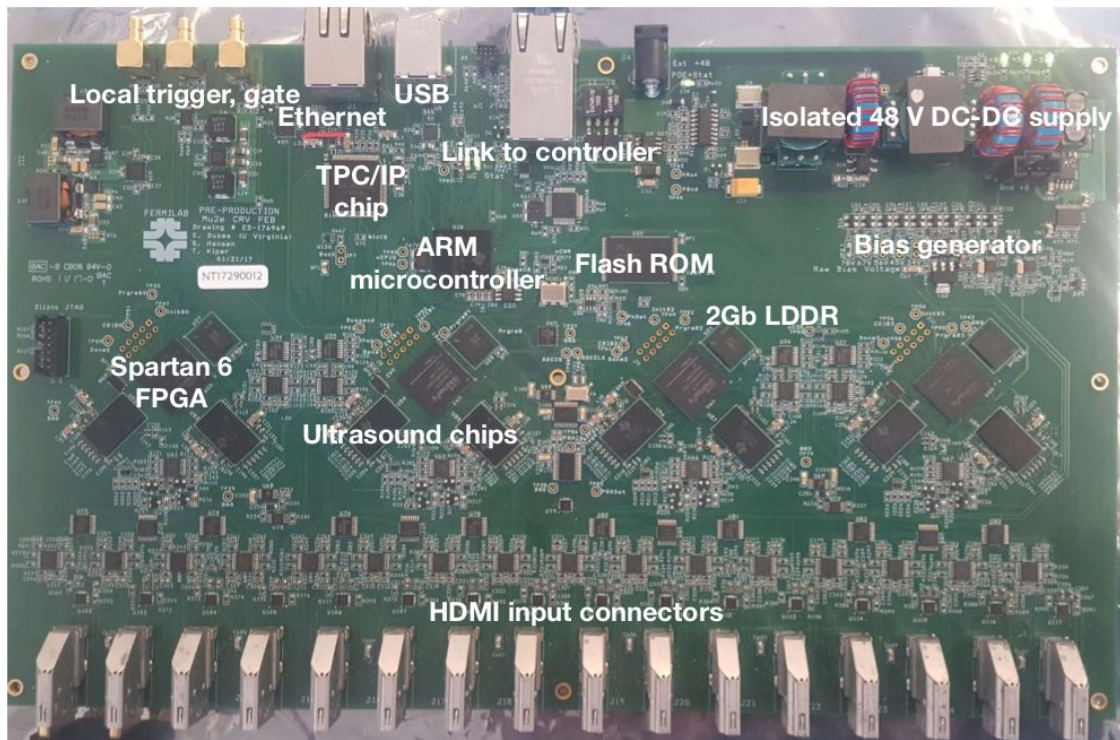
# DAPHNE

- Detector electronics for Acquiring PHotons from NEutrinos
  - Warm readout electronics for the DUNE SP-PD
- Developed as a partnership between FNAL and Latin America based off of the FNAL design of the Mu2e cosmic ray veto FEB
  - Visits to FNAL by Javier Castaño and Juan Vega Martinez in 2019



# DAPHNE

- Developed based on lower-sampling-rate commercial ultrasound ASIC chips
- Meets the performance requirements while optimizing cost
- Inspiration for the system comes from the Mu2e experiment cosmic ray veto (CRV) front-end board (FEB)

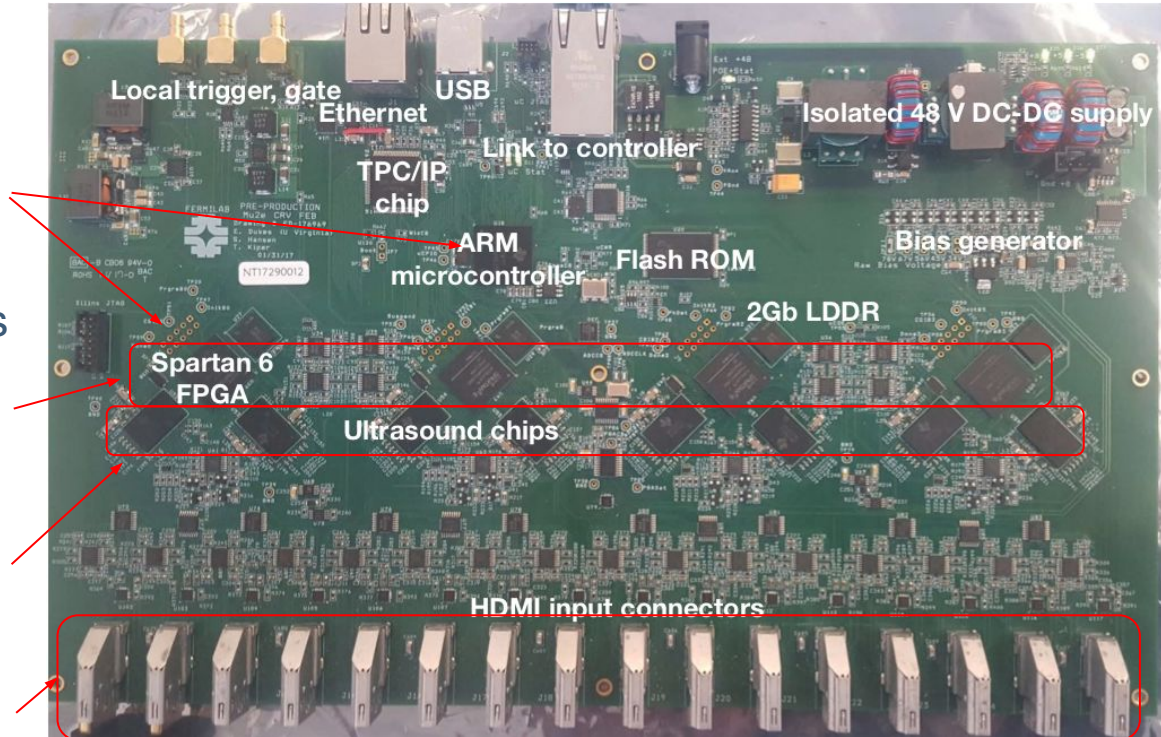


Pre-production Mu2e CRV FEB



# TDR: “Electronics Next Steps”

1. Replace outdated/obsolete components
  - 1.1. Spartan-6 → Artix-7
2. Increase FPGA logic resources
  - 2.1. Consolidate everything into single large FPGA
3. Increase dynamic range
  - 3.1. 12-bit → 14-bit ADCs
4. Customize design for readout of DUNE APA (40 channels)



Pre-production Mu2e CRV FEB

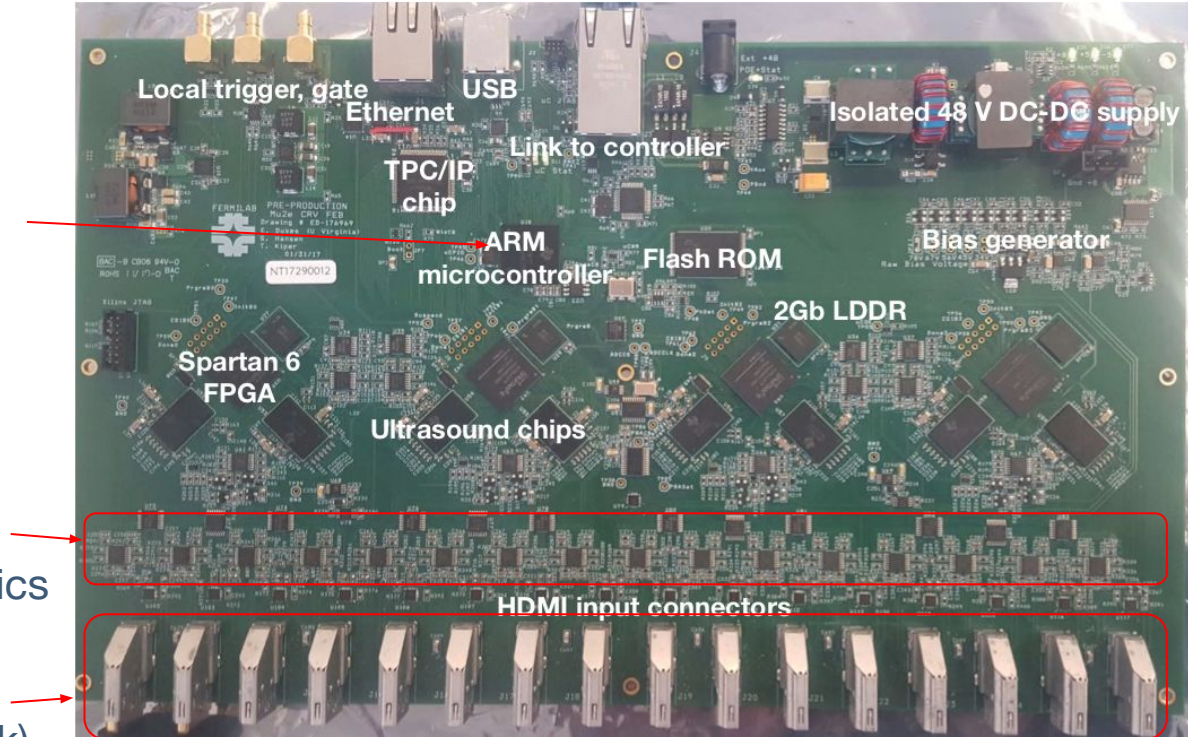
# Additional Design Changes

Since the TDR: >10 increase in expected data rate

- Remove  $\mu$ C from data path
- Remove controller module
  - Add external 48V supply (see next slides)

30% Design Review Feedback

- Remove superfluous Mu2e functionalities
- Provide power to cold electronics (Javier's talk)
- System-level grounding & connections plan (Claudio's talk)



Pre-production Mu2e CRV FEB

# Summary of Readout Specifications

DAPHNE electronics readout noise	<1 ADC	The AFE5808A datasheet lists 77-dBFS SNR at 65 MSPS
DAPHNE charge Measurement Dynamic Range	13 bits	The AFE5808As are 14-bit ADCs
DAPHNE analog voltage input range	250 mV - 1 V (peak-to-peak)	The AFE5808As low-noise amplifier supports a range of input signals
DAPHNE timing resolution	<16 ns	The sampling frequency of the AFE5808As will be set to the 62.5 MHz experiment clock
DAPHNE internal trigger threshold	1.5 PE	Reduce the trigger rates from radiological backgrounds
DAPHNE detection of Triplet (late) photons	5 micro-seconds	Improves light yield by also collecting late scintillation light
DAPHNE maximum average data rate	3 Gbps	DAPHNE's Artix-7 GTP transceivers capable of up to 6.6 Gbps
DAPHNE SiPM common bias control	34 V, 45 V, 55 V, 66 V, or 77 V	Coarse voltage settings include ranges suitable for testing Hamamatsu SiPMs both warm and cold
DAPHNE SiPM trim bias control	0...4.096 V	DAC used to select trim voltage across 4V range
DAPHNE SiPM bias and trim voltage monitoring	Yes	Voltage read back and current monitoring capabilities included
DAPHNE cold electronics bias voltage monitoring	Yes	Voltage read back and current monitoring capabilities included

# DAPHNE Power Delivery

- The power delivery system used in ProtoDUNE was highly informative in the development of the current system
- There are a few significant differences

	ProtoDUNE	Current system
<i>Supply</i>	Each SSP : 20 VDC @ 1.5A	Each DAPHNE : <u>48</u> VDC @ <u>0.55</u> A
<i>Power Device</i>	Wiener crate w/ MPV8030, MPV8060	Wiener crate w/ MPV80 <u>60</u> i
<i>Bias Voltage</i>	Provided externally	Generated on DAPHNE

- The 25 meter cable run between power supply and load will result in voltage drop in the long cables
- The ability to sense the supply voltage at DAPHNE is very important
- The power delivery system provides for this

Jon Ameel

# DAPHNE Power Delivery - Power Supply

- The power source is a 19" rack mounted WIENER system

Quantity	MFG	Model	Description	Height	Channels	Output	Price	Cost	Vendor
2	WIENER	MPOD EC-LV	Full size 19" MPOD crate with 10 slots	8U	10 slots		\$5,700.00	\$11,400.00	W-IE-NE-R
2	WIENER	option	Reversed card cage, slots in rear		n/a		\$143.00	\$286.00	W-IE-NE-R
20	WIENER	MPV8060i	0.60V DC @ 1A per channel		8	48V @ 0.55A	\$2,862.00	\$57,240.00	W-IE-NE-R
1	HP Enterprise	DL360e	1U Rack Server - 1 x Intel Xeon E5-2420 V2 2.2GHz	1U	4 x 1Gb ports		\$568.05	\$568.05	<a href="http://Newegg.com">Newegg.com</a>

- Two Mpod EC-LV crates, populated with 10 MPV8060i in each crate can provide for 160 individually configurable 48V channels at up to 1 Amp each.
- The MPOD EC-LV control board permits SNMP, SSH or HTTP (webpage) interface over ethernet. The power delivery system includes a 19" rack server to connect local control with experiment-wide control systems.

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# DAPHNE Power Delivery - Power Cabling

MPV8060i provides each output channel with 8 contacts,

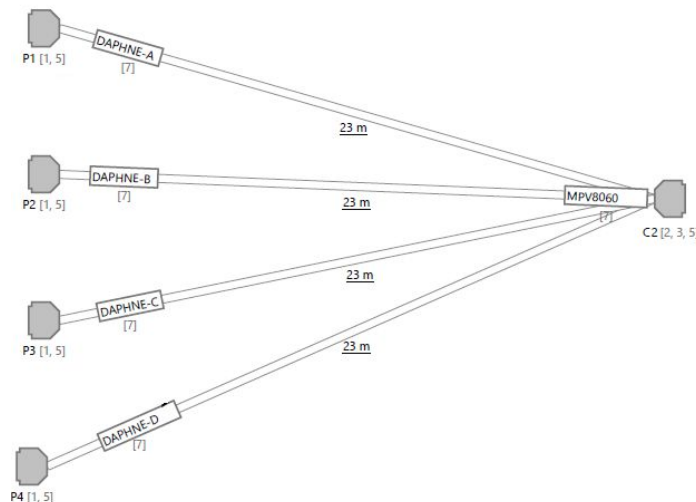
- [3x] VOUT, Return
- Sense+, Sense-

DAPHNE will connect to 6 contacts

- 48V, Return
- +48V, Return (redundant)
- Sense+, Sense-

Alpha Wire EcoCable Mini. [78126]

- 6 pairs, 24 AWG, foil shielded, 4.2mm diameter
- Low specific gravity, low outgassing, and halogen free
- 32% smaller and 44% lighter than standard 300V cable
- Completely recyclable high-performance cable



Jon Ameel

# Summary of Power Supply Specifications

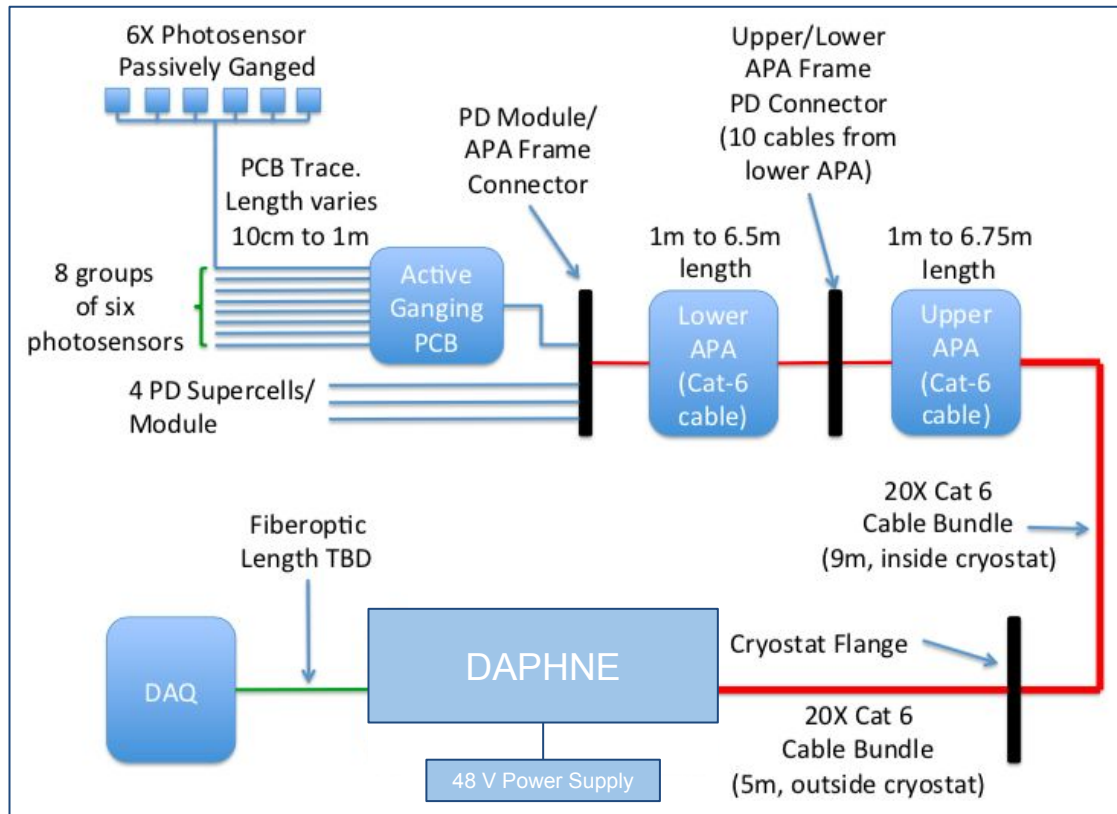
Power Supply Voltage Range(source)	0.0 Vdc..60.0 Vdc
Power Supply Voltage Range(load, 25m length)	0.0 Vdc..58.25 Vdc
Power Supply Voltage Drop(max)	1.75 Vdc (2.92%)
Power Supply Voltage Resolution	+/- 4 mV
Power Supply Voltage Ripple	<2.0 mVpp
Power Supply Voltage Rampup	1 V/s..500 V/s
Power Supply Current Resolution	+/- 0.06 mA
Power Supply Voltage Stability	0.2% / 10k
Power Supply Voltage Monitoring Resolution	15 bit
Power Supply Voltage Monitoring Accuracy	+/- 0.1% of full scale
Power Supply Current Limit	0.0..1.0 A
Power Supply Current Monitoring Resolution	15 bit
Power Supply Current Monitoring Accuracy	+/- 0.5% of full scale
Power Supply Voltage Dynamic Regulation	<100 mV
Power Supply Voltage Recovery Time	<5 mS
Power Supply Interlock Loop Available	Yes
Power Supply Isolation	125 Vdc, 500 Vdc tested

# Summary of Design Changes/Actions

- TDR Electronics Next Steps → Actions
  - Replace outdated components → old  $\mu$ C & Spartan-6 replaced with new  $\mu$ C & Artix-7
  - 40-channel prototype board → new design has 5 octal ADCs
  - FPGA logic resource needs → combine smaller FPGAs into single large Artix-7 FPGA
  - Increase dynamic range → Replace 12-bit AFE5807 ADC with 14-bit AFE5808A ADC
- Additional 30% Design Review Comments/Recommendations → Actions
  - Power to active cold electronics through a pair of conductors added to the custom PD cable terminated with ProtoDUNE-SP-style Hirose (rather than HDMI) connectors with system-level grounding plans documented
  - Functionalities specific to Mu2e were removed from DAPHNE design
- New requirements since 30% Design Review → Actions
  - Expected 1-3 Gbps data rate → Remove controller module and connect directly to (FELIX) DAQ optically
    - Requires also adding external 48 V supply
- Tests planned for ICEBERG not completed due to integration (grounding) issues with cold electronics
  - Combined with slowdowns related to COVID-19, has resulted in ICEBERG tests being pushed to later in 2020
    - No results comparing DAPHNE and SSP and delay in final integration tests with DAQ
- Internal review of DAPHNE schematic to validate design changes since the TDR (see next slides)
  - Parts-availability check also performed to identify long lead-time parts and swap them for alternate ones



# Overview of Readout Chain



# DAPHNE Internal Review

- Purpose is to review DAPHNE design before fabricating prototype boards
- Scope of internal review: DAPHNE + its interfaces
  - Documents prepared for the internal review provided a strong foundation for documents supplied for this 60% review
- Internal reviewers: Terri Shaw (chair), Paul Rubinov, and Jamieson Olsen of FNAL EED
- Report made available on June 12 (see next slide)
  - <https://edms.cern.ch/document/2385075/1>
  - Reviewers have volunteered to work with DAPHNE team to address the recommendations

## DAPHNE Review Kick-off Meeting

Friday May 15, 2020, 11:00 AM → 12:35 PM US/Central

Deywis Moreno Lopez (UAN) , Matthew Toups (FNAL)

- 11:00 AM** → 11:15 AM **System Overview**  
Speaker: Matthew Toups (FNAL)
- 11:15 AM** → 11:35 AM **DAPHNE Hardware description**  
Speaker: Javier Castaño (UAN)
- 11:35 AM** → 11:55 AM **DAPHNE Firmware description**  
Speaker: Manuel Arroyave (EIA)
- 11:55 AM** → 12:15 PM **Grounding Overview**  
Speaker: Claudio Gotti (INFN Milano Bicocca)
- 12:15 PM** → 12:30 PM **Summary of Documentation**  
Speaker: Deywis Moreno Lopez (UAN)

# Internal Review Recommendations

- Complete “clean” schematic.
  - Validate there are no issues at the design level using commercial tools
- Power distribution scheme should be reconsidered.
  - Implementation used difficult-to-fabricate custom parts carried over from Mu2e design, which had different requirements (PoE, magnetic field, etc.)
  - DAPHNE should be able to make sure of commercial solutions
- Review the need for the external DDR2 DRAM chip
  - With switch to larger Artix-7 FPGA can perhaps instead make use of internal BlockRAM resources
- Layout of the PCB should be carefully reviewed
  - Reviewers volunteer to work with DAPHNE team on this
- Compile and simulate a prototype version of the firmware
- Review choice of FPGA to ensure the design will comfortably fit

# Schedule & Impacts

- Expect resolution of items raised during internal review to take up to 8 weeks, followed by 2 weeks for fabrication, and 2 weeks for assembly

Activity	2019					2020												2021				
	AUG	SEPT	OCT	NOV	DEC	JAN	FEB	MAR	APRIL	MAY	JUN	JUL	AUG	SEPT	OCT	NOV	DEC	JAN	FEB	MAR		
DAPHNE PCB development	█																					
DAPHNE Firmware/software development	█																					
DAPHNE Preprod. Prototype fabrication and testing														█								
DAPHNE Design verifications and improvements								█	█	█	█	█	█	█	█	█	█					
DAPHNE Board's fabrication and testing																				█		

# Proposal for tests/goals for first DAPHNE prototypes

- A. Demonstrate that the ultrasound ADC chip works in the mode where the baseline restoration is turned off and allows us to get about 13 bits of range out of the ADC
  - B. Demonstrate successful interface with cold electronics
  - C. Show single-pe readout of 48-ganged SiPMs
  - D. Demonstrate slow control functions (bias adjustment, ADC gain)
  - E. Demonstrate successful interface and data transfer to DAQ at 4.8 gbs
  - F. Demonstrate readout through near-final cable harness (in cold box outside ProtoDUNE, fall/winter 2020)
  - G. Investigate DAQ integration and x-talk with TPC in ICEBERG2
  - H. Assuming that the 4.8 gbs readout works, act as a test bed to allow development of firmware for the next generation of DAPHNE (readout, timing, slow control)
- Producing 7 DAPHNE prototypes distributed to 6 different institutions

# Summary

- DUNE's SP-PD Readout System, DAPHNE, has been designed to meet warm readout system requirements at reduced cost
- Design of DAPHNE has evolved in accordance with the plan outlined in the TDR and in response to recommendations from the 30% design review + new requirements that have arisen
- Internal review of DAPHNE performed to validate design changes
- After addressing internal review recommendations, prototype DAPHNE board fabrication will begin at the end of the summer

# Backups

# DAPHNE testing plan (I)

- Post-assembly testing
  - Visual inspection
  - Connector checks (unpowered/powered)
  - Basic communication tests
  - Reading of devices
  - Saving of internal configuration
  - Verification of bias voltage and monitoring



# DAPHNE testing plan (II)

- Characterization and calibration testing (after post-assembly testing)
  - Repeat visual inspection after arrival at Laboratory, connect external power supply and optical fibers to SFP transceivers, check ground and input impedances, verify basic communication, and test advanced functionality:
    - Blink LEDs
    - Exercise monitoring SiPMs voltage and current delivery
    - Check analog DC input and noise levels with no inputs
    - Verify operation of timing interface
    - AFE5808A functionalities like linearity, dynamic range, gain of every channel using external charge generator
    - Data-throughput loopback test
    - FPGA temperature monitoring

# Proposal for DAPHNE prototypes & location of tests

- A. FNAL (board #1), UAN (board #2), EIA (board #3)
- B. Univ. of Milano-Bicocca (board #4)
- C. Univ. of Milano-Bicocca (board #4)
- D. FNAL (board #1), UAN (board #2), EIA (board #3)
- E. CERN (board #5), FNAL (board #1), UAN (board #2), EIA (board #3)
- F. CERN (board #5)
- G. FNAL (board #6)
- H. FNAL (board #1), UAN (board #2), EIA (board #3), Campinas (board #7)

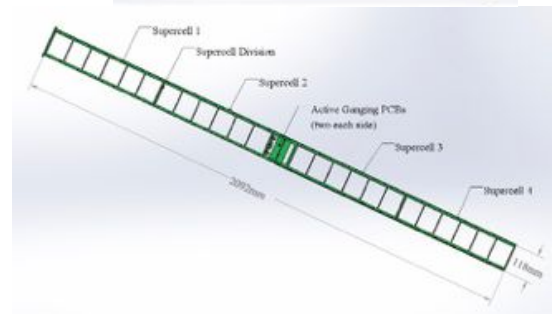
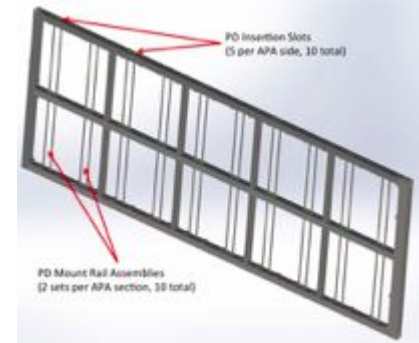
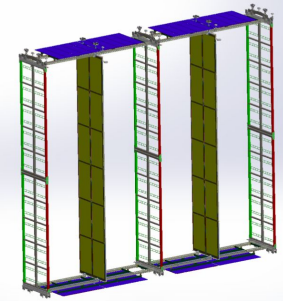
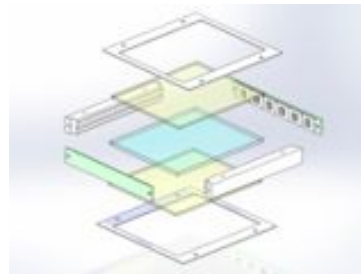
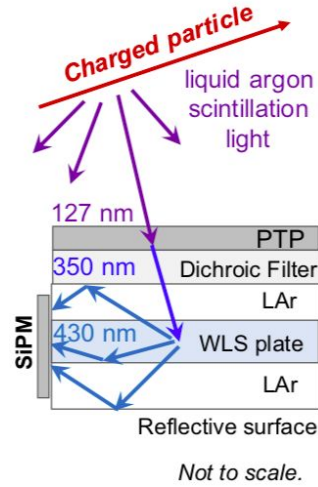
➤ Producing 7 DAPHNE prototypes

# DUNE SP-PD Overview (I)

LAr scintillation light collector based on the X-ARAPUCA concept

PD modules, ten per APA, each 209 cm long by 12cm wide, consist of 4 “supercells”, each of which consists of 6 X-ARAPUCAs

Photon detectors are mounted inside the APA frame structure on stainless steel rails.



# DUNE SP-PD Electronics (I)

Signals read out with 6 x 6 mm<sup>2</sup> SiPM photosensors Hamamatsu (Japan), FBK (Italy)

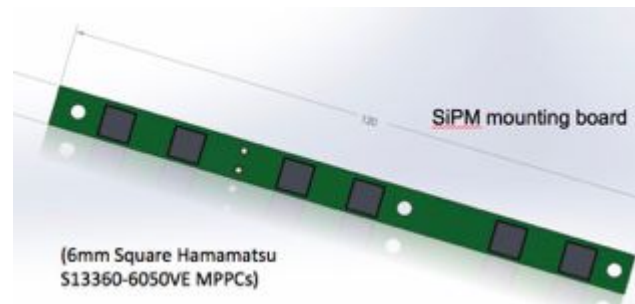
- 6 photosensors ganged passively

Cold active ganging electronics

- Sums 8 groups of 6 photosensors

Individually shielded twisted pair cables carry signals from 4 X-ARAPUCA supercells through APA frame to feedthrough

Warm Readout Electronics (DAPHNE) responsible for digitizing signals and shipping to DAQ



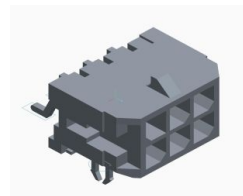
# DAPHNE Power Delivery - Power Connections

Each DAPHNE board will include a

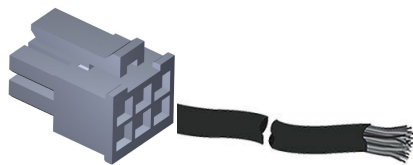
MOLEX 43045-0608 Micro-Fit 3.0 Right-Angle Header

- 3.00mm Pitch, Dual Row, 6 circuits
- Positive locking, PCB strain relief available
- 600V, 8.5A max current per contact

43045-0608



43025-0600

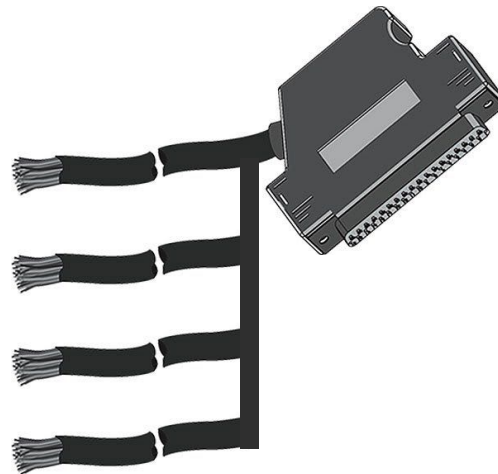


From	To	Conductor	Color	Gauge	From Contact PN
P1.1	C2.1	CBL1.Black	Black	24 AWG	
P1.2	C2.20	CBL1.Brown	Brown	24 AWG	
P1.3	C2.2	CBL1.Red	Red	24 AWG	
P1.4	C2.21	CBL1.Orange	Orange	24 AWG	
P1.5	C2.4	CBL1.Yellow	Yellow	24 AWG	
P1.6	C2.23	CBL1.Green	Green	24 AWG	
P1.N/C	C2.19	CBL1.Drainwire	White	24 AWG	

Each MPV8060i module includes a standard 37p D-SUB connector

A Multicomp SPC15230 connector will terminate the power cable.

- Accepts 28-20 AWG wires
- Screw fasteners locking
- 500V, 5A max current per contact
- 45° nickel plated backshell [SPC14997]



From	To	Conductor	Color	Gauge	From Contact PN
C2.1	P1.1	CBL1.Black	Black	24 AWG	
C2.2	P1.3	CBL1.Red	Red	24 AWG	
C2.4	P1.5	CBL1.Yellow	Yellow	24 AWG	
C2.5	P2.1	CBL2.Black	Black	24 AWG	
C2.6	P2.3	CBL2.Red	Red	24 AWG	
C2.8	P2.5	CBL2.Yellow	Yellow	24 AWG	
C2.9	P3.1	CBL3.Black	Black	24 AWG	
C2.10	P3.3	CBL3.Red	Red	24 AWG	
C2.12	P3.5	CBL3.Yellow	Yellow	24 AWG	
C2.13	P4.1	CBL4.Black	Black	24 AWG	
C2.14	P4.3	CBL4.Red	Red	24 AWG	
C2.16	P4.5	CBL4.Yellow	Yellow	24 AWG	
C2.19	P1.N/C	CBL1.Drainwire	White	24 AWG	
C2.19	P2.N/C	CBL2.Drainwire	White	24 AWG	
C2.19	P3.N/C	CBL3.Drainwire	White	24 AWG	
C2.19	P4.N/C	CBL4.Drainwire	White	24 AWG	
C2.20	P1.2	CBL1.Brown	Brown	24 AWG	
C2.21	P1.4	CBL1.Orange	Orange	24 AWG	
C2.23	P1.6	CBL1.Green	Green	24 AWG	
C2.24	P2.2	CBL2.Brown	Brown	24 AWG	
C2.25	P2.4	CBL2.Orange	Orange	24 AWG	
C2.27	P2.6	CBL2.Green	Green	24 AWG	
C2.28	P3.2	CBL3.Brown	Brown	24 AWG	
C2.29	P3.4	CBL3.Orange	Orange	24 AWG	
C2.31	P3.6	CBL3.Green	Green	24 AWG	
C2.32	P4.2	CBL4.Brown	Brown	24 AWG	
C2.33	P4.4	CBL4.Orange	Orange	24 AWG	
C2.35	P4.6	CBL4.Green	Green	24 AWG	

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