Cold electronics, cable harness, and grounding

DUNE 60% design review

19 june 2020

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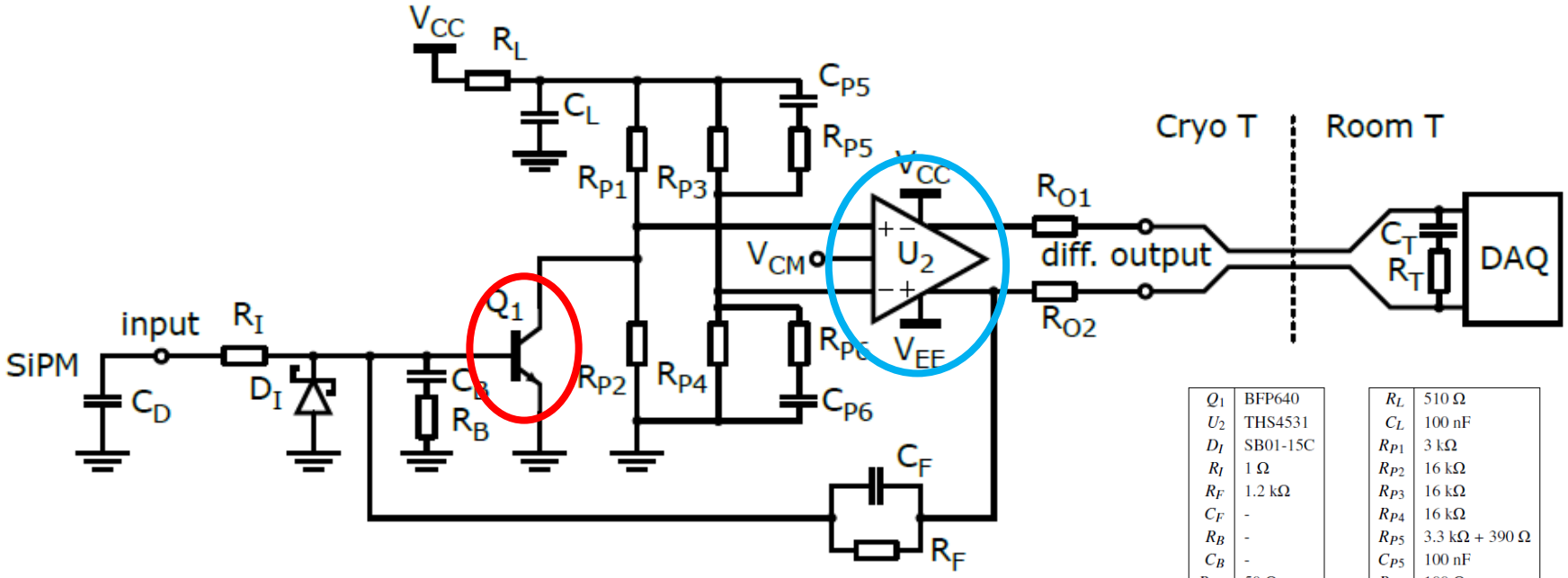
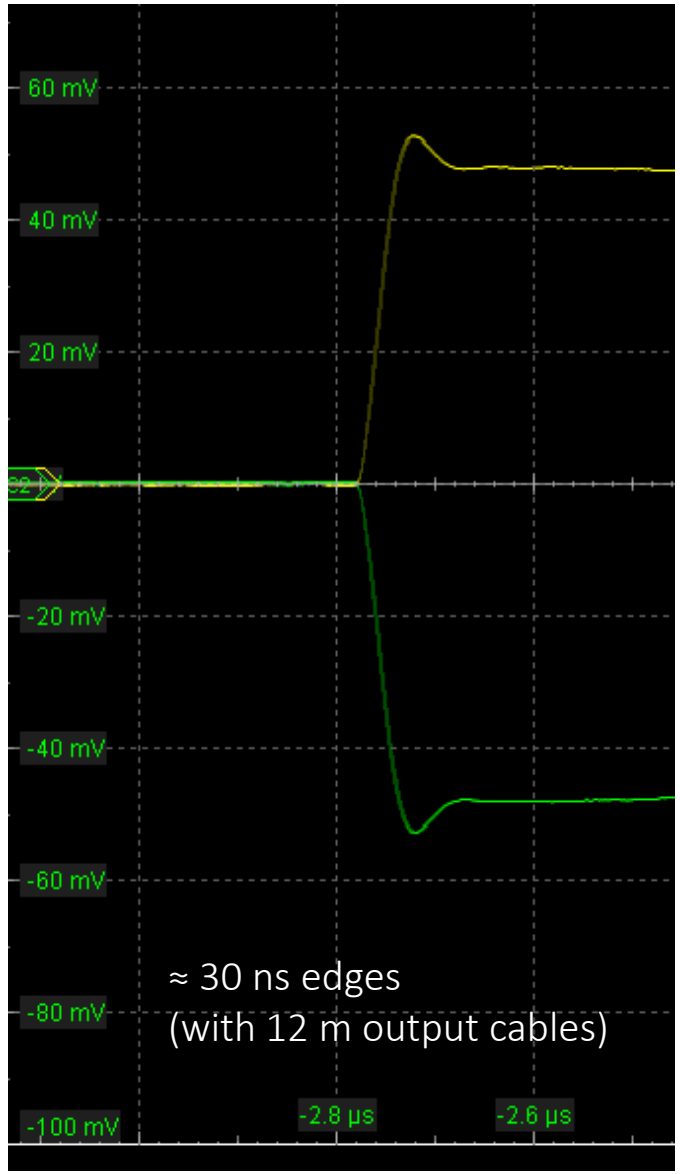
On behalf of the DUNE photon detector & electronics working groups

Cold amplifier design



Q_1	BFP640
U_2	THS4531
D_I	SB01-15C
R_I	1 Ω
R_F	1.2 kΩ
C_F	-
R_B	-
C_B	-
R_{O1}	50 Ω
R_{O2}	50 Ω

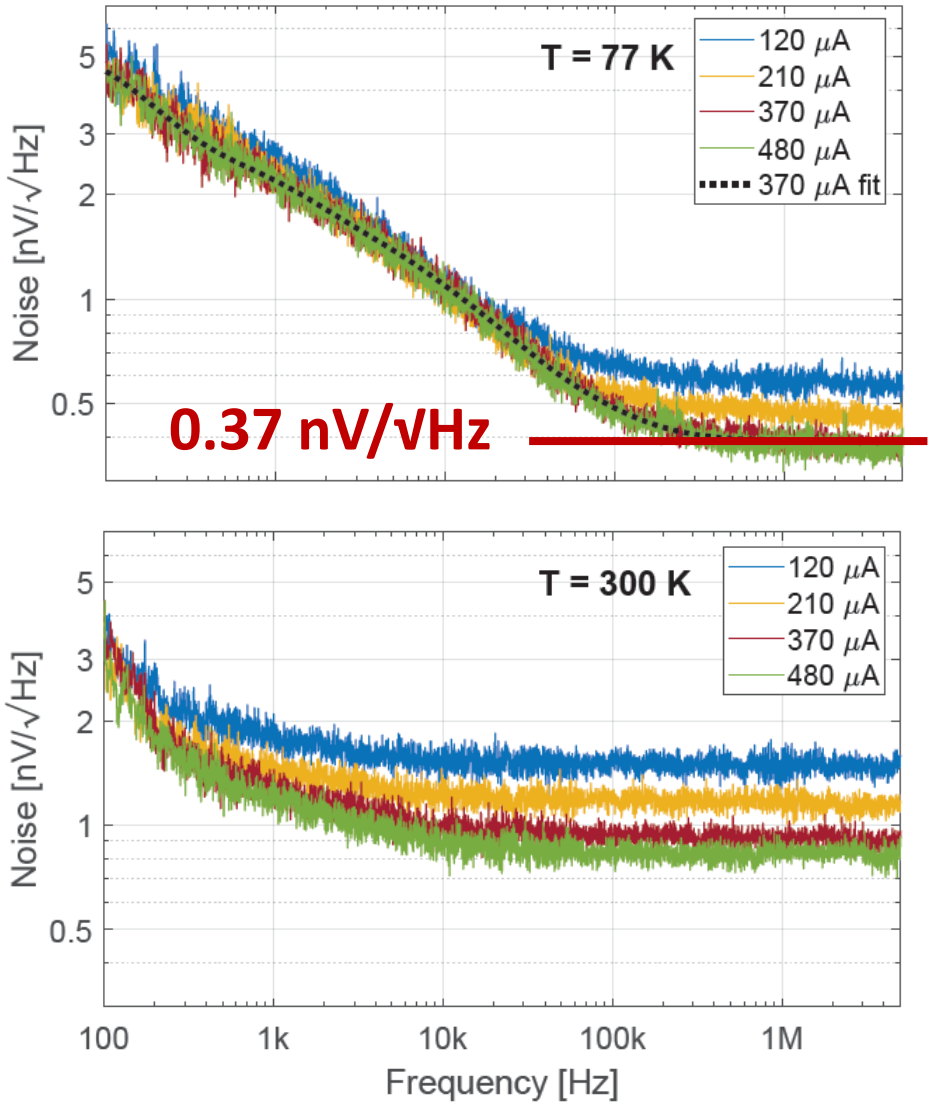
R_L	510 Ω
C_L	100 nF
R_{P1}	3 kΩ
R_{P2}	16 kΩ
R_{P3}	16 kΩ
R_{P4}	16 kΩ
R_{P5}	3.3 kΩ + 390 Ω
C_{P5}	100 nF
R_{P6}	100 Ω
C_{P6}	2.2 nF

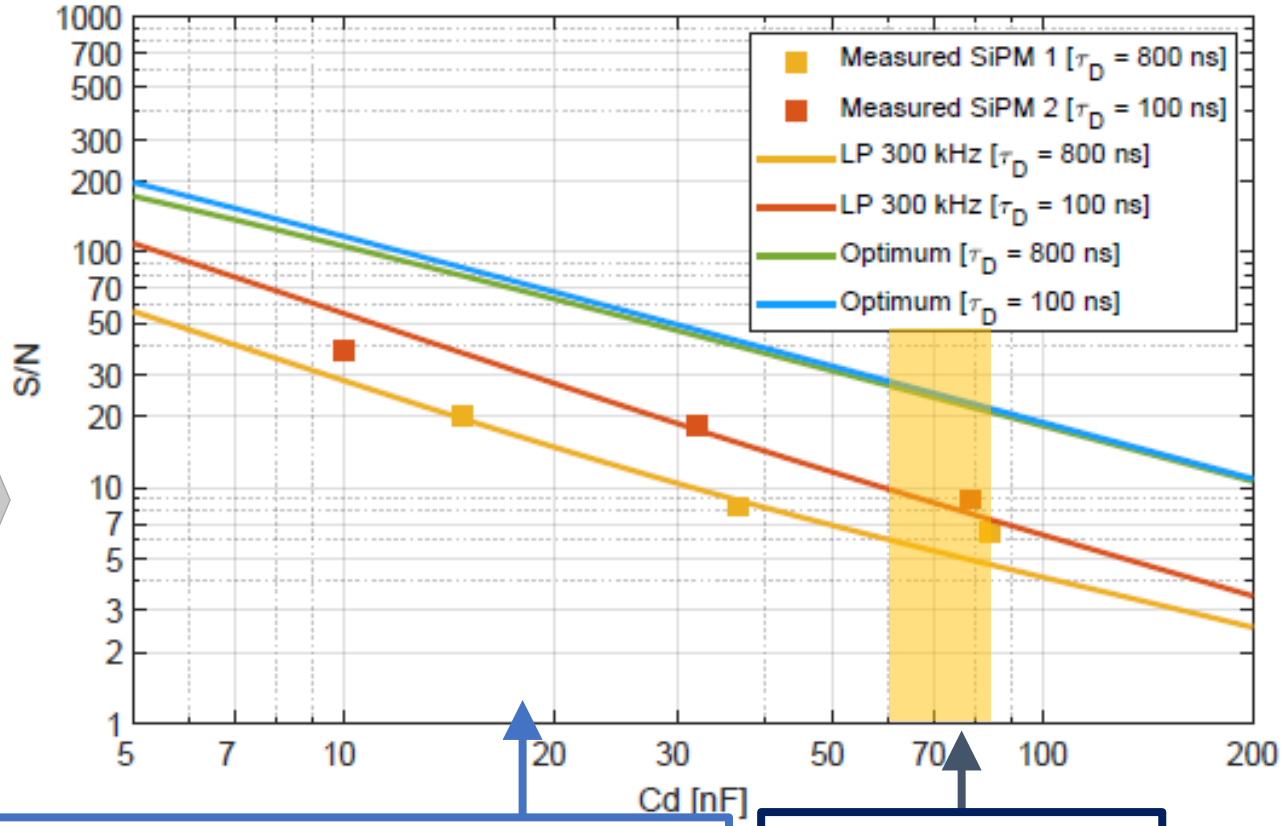


- Evolution of the design described in the TDR
- **Two-stage design** gives lower noise, lower power, higher flexibility, wider output dynamic range (Q1: SiGe bipolar transistor BFP640 - U2: Fully differential opamp THS4531)
- Max closed loop bandwidth **≈10 MHz**; gain-bandwidth product in the GHz range
- Noise: see next slide
- (Almost) rail-to-rail outputs on (AC-coupled) 100-ohm differential line
- Low power consumption (**≈2.5 mW/channel**)
- Details: 2020 JINST 15 P01008 also available as arXiv:1911.06562

Noise and S/N ratio

- Noise spectra at different operating currents of the input transistor (chosen: 370uA)





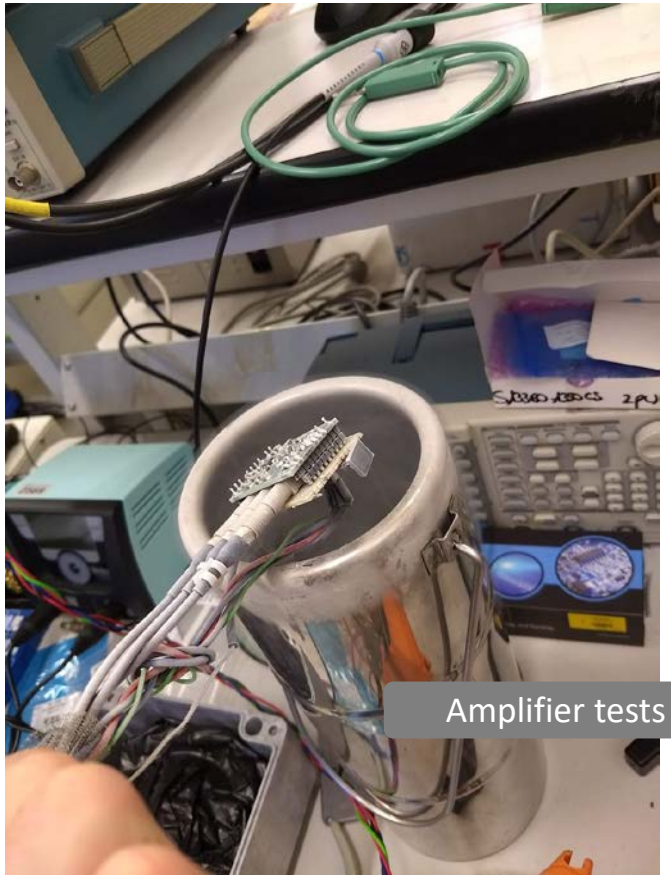
Ganging tests up to ≈20 nF (24x 4x4 mm² SiPMs) are also discussed here: arxiv:2001.09051

Expected capacitance for 48x 6x6 mm²

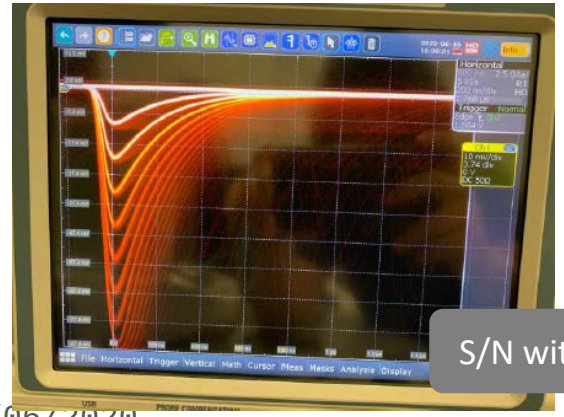
- S/N calculated & measured at **3V OV** (gain 2.4x10⁶) with a 4x4 or 6x6 mm² SiPM + capacitors added in parallel to simulate ganging
- Yellow/red : calculated (lines) & measured (dots) for SiPMs with tau ≈ 800 ns/100 ns, 300 kHz low pass filter
- Green/blue: calculated with optimum (matched) filter → $\left(\frac{S}{N}\right)^2_{OF} = \frac{1}{2\pi}\int_{-\infty}^{\infty}\frac{|\tilde{V}_O(\omega)|^2}{N(\omega)}d\omega$ (best S/N achievable)

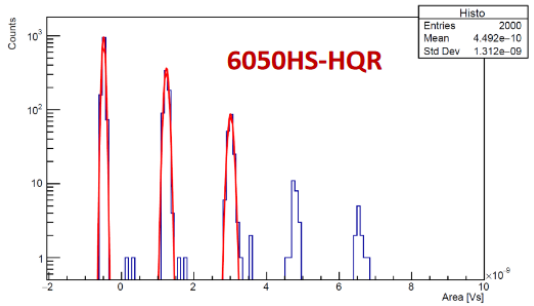
Tests and reliability at cold

- During amplifier lab tests and component tuning, the first prototypes were thermal cycled hundreds of times between 300 K and 77 K (most of the times not gently)
- Just one issue was observed so far at 77 K
  On some samples (3 out of the 10 tested so far), the opamp shuts down at 77 K if its «nPD» pin goes below ≈2.8 V, which is too close to the nominal 3 V supply
  → Solution: add margin and increase the supply voltage from +3 V to +3.3 V or maybe higher
  (This is the reason why the power supply is now specified in the range 3-5 V. It will be fixed later on)
- Amplifier prototypes are also being used for SiPM tests in different labs
  (see presentation on SiPMs)
- Systematic tests and qualification at cold are planned at INFN Laboratori Nazionali del Sud (LNS):
  1) Thermal cycling and tests of passive components
  2) Thermal cycling and tests active components (BFP640 and THS4531) biased at their maximum operating voltage
  3) Thermal cycling and tests of full amplifiers

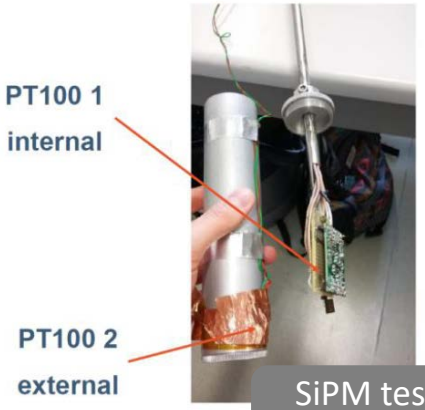


Amplifier tests





S/N with a single 6x6 SiPM

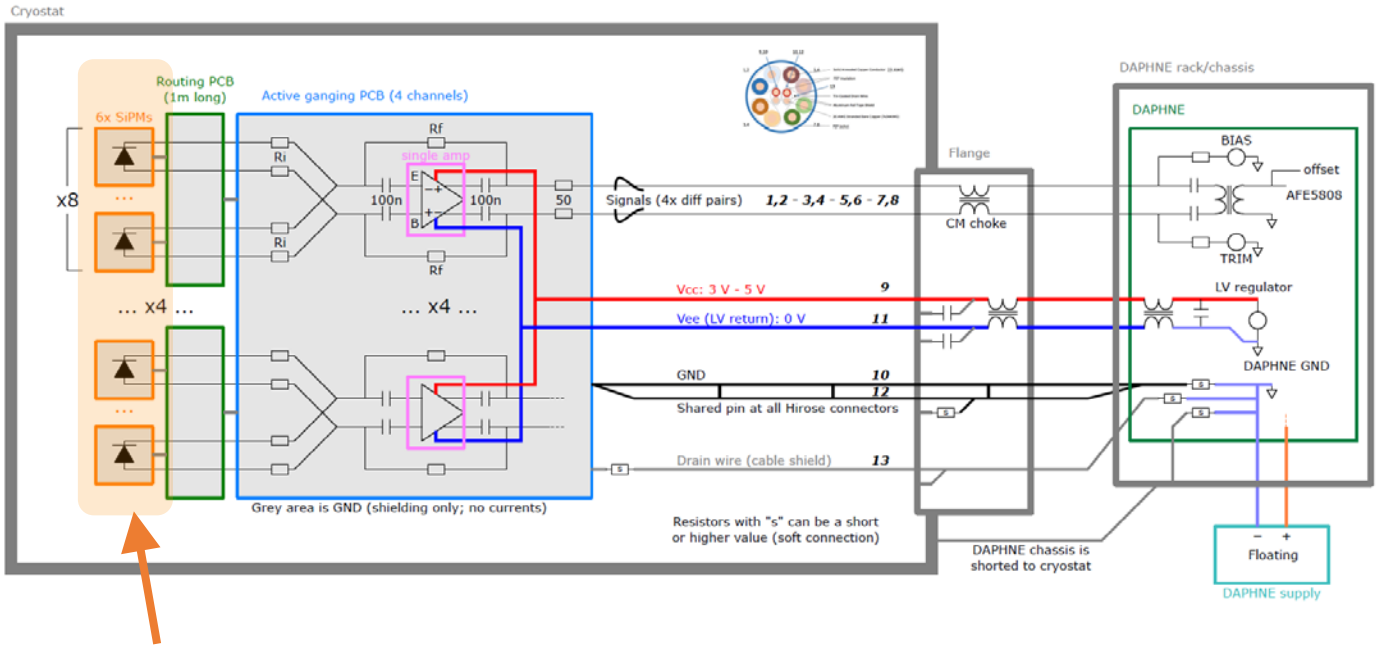


SiPM tests in Milano-Bicocca

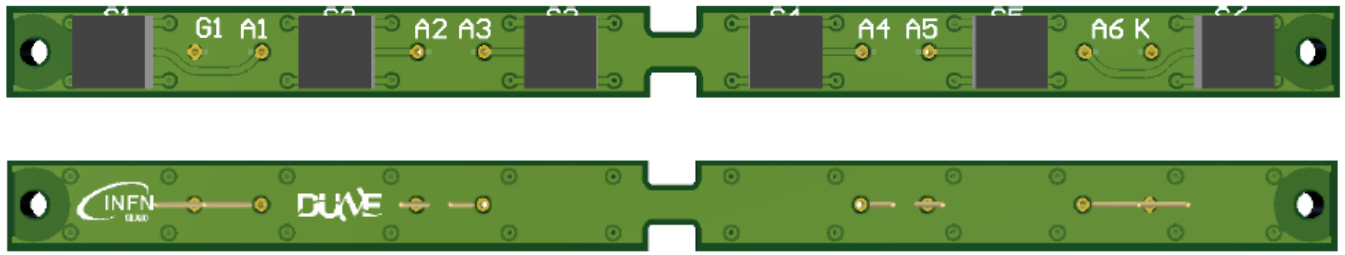
SiPM test setup at CIEMAT Madrid

SiPM mounting

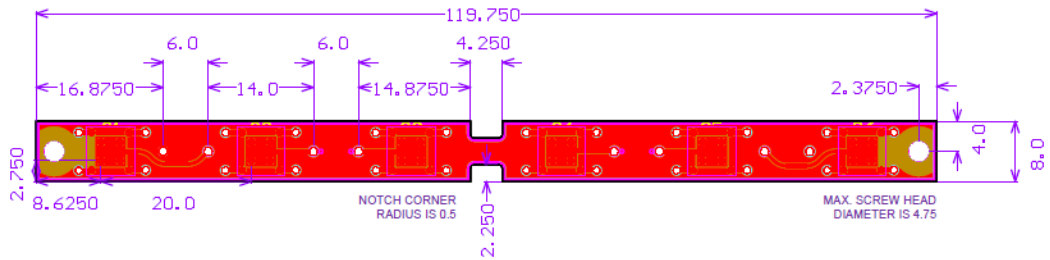
PCB design by N. Gallice and M. Lazzaroni (Milano)
Schematic and layout ready



- Each mounts 6x SiPMs (surface mount devices)
- Anode and cathode pins for each SiPM, to allow testing before module assembly
- 4 layers, ground plane for shielding

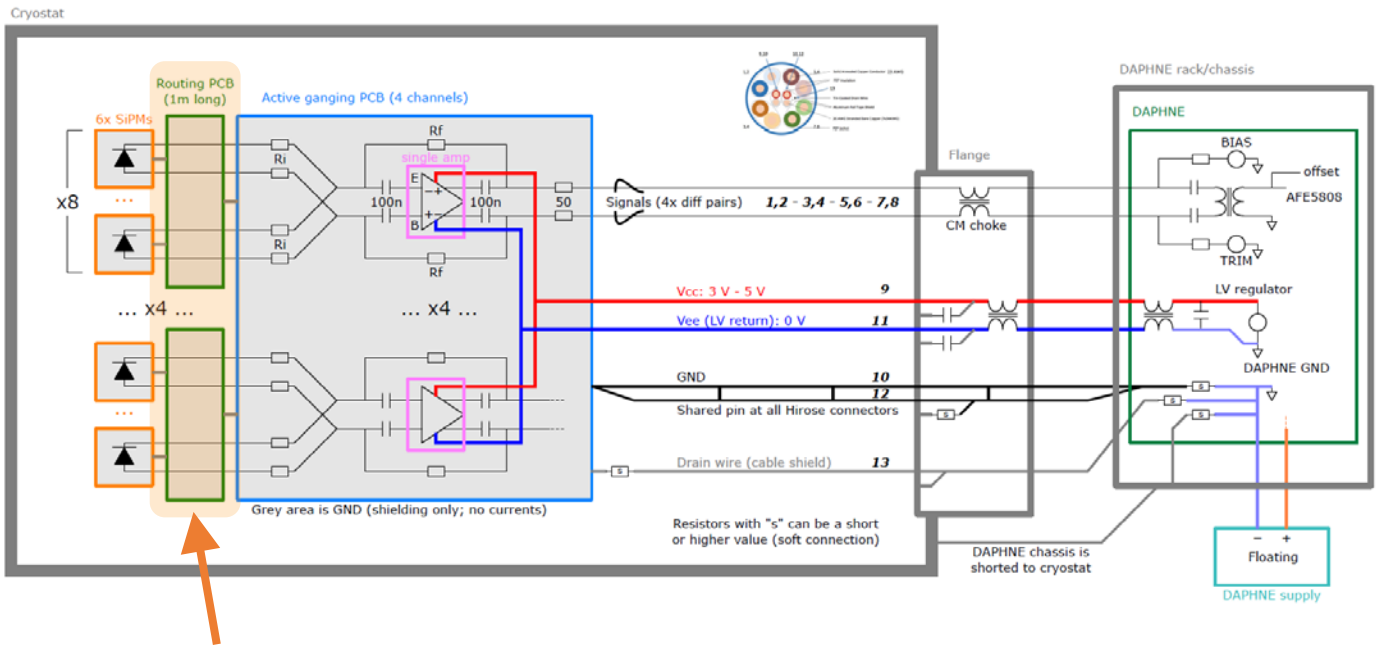


Pins: MillMax 5435-2-05-15-00-00-03-0
(male, single pins, through hole press-fit + solder)



SiPM signal routing

PCB design by N. Gallice and M. Lazzaroni (Milano)
Schematic and layout ready

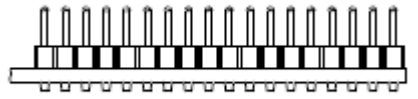


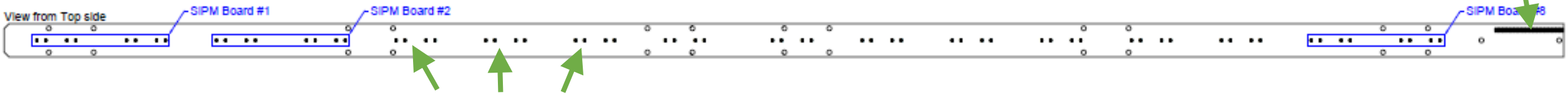
- Passive ganging of 6x SiPMs and routing of 8x signal pairs to the cold amplifier
- 1m long PCB; non standard size, but vendors already identified
- 4 layers, ground plane for shielding

Pins to connect to active ganging PCB
MillMax 800-90-018-61-001000
(male, 100-mil pitch, through hole press-fit + solder)

Output Connections

# Pin	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Type	GND	K	A	K	A	K	A	K	A	K	A	K	A	K	A	K	A	GND
# SiPM Board	-----	1	1	2	2	3	3	4	4	8	8	7	7	6	6	5	5	-----

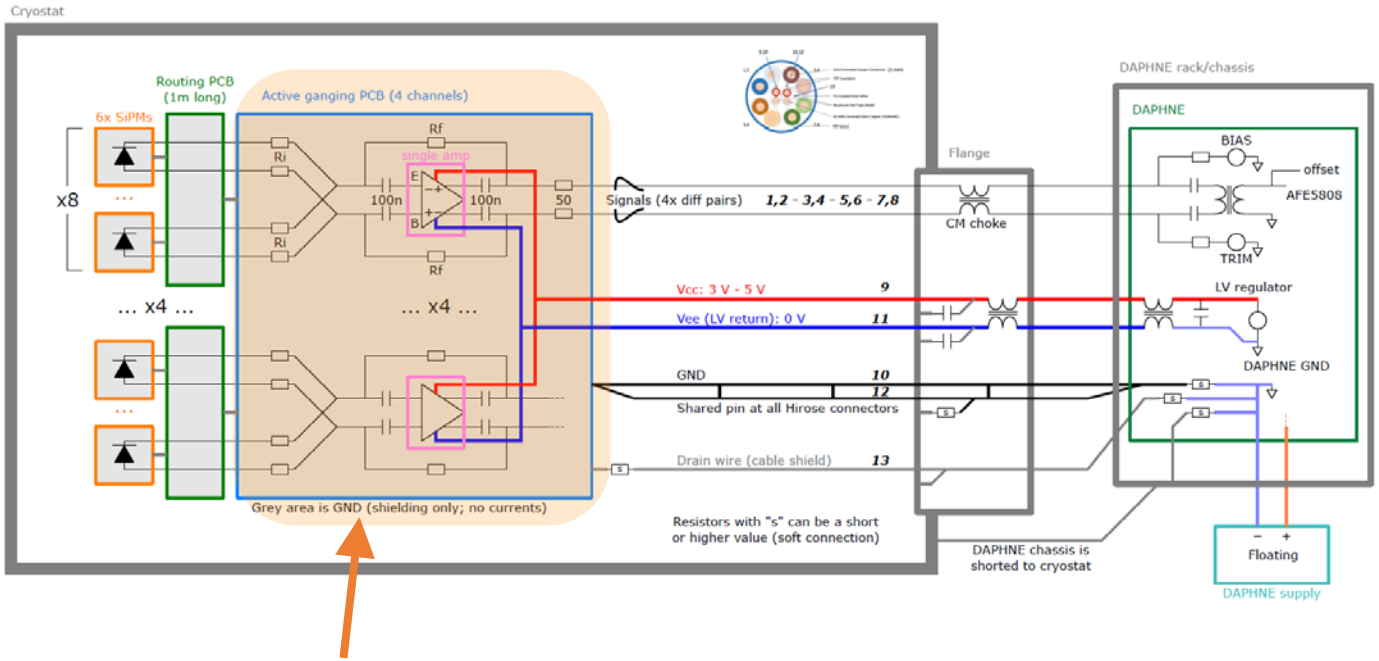


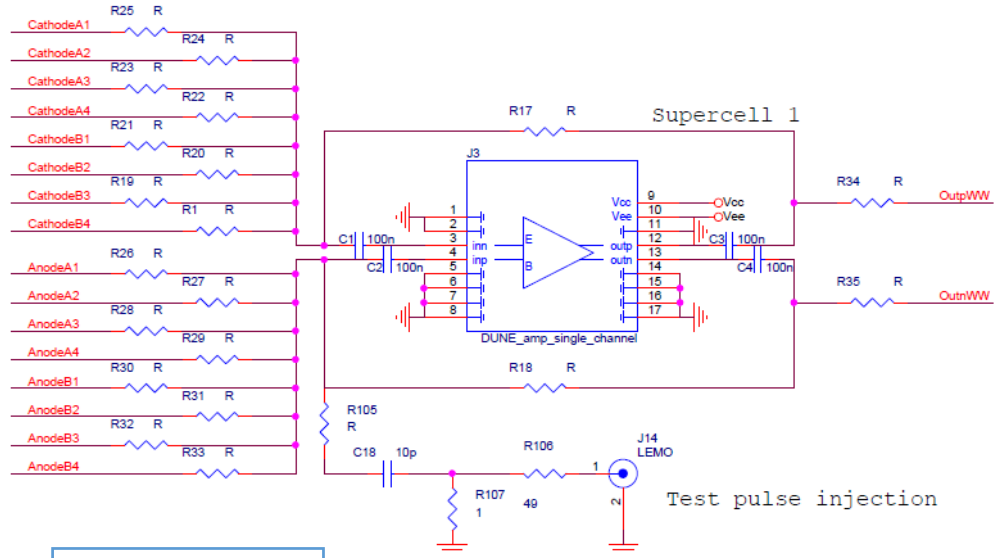


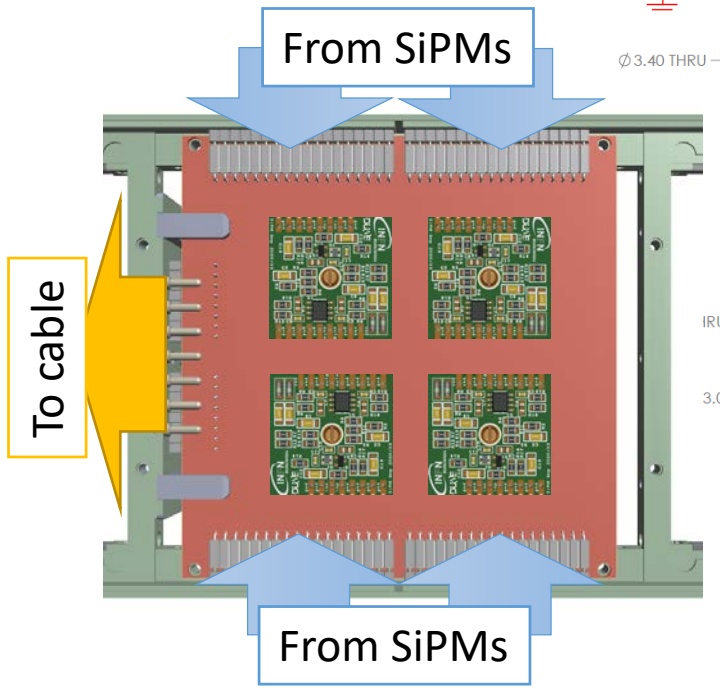
Pins from SiPM boards
MillMax 0627-0-15-15-11-27-10-0
(female, single pins, through hole press-fit + solder)

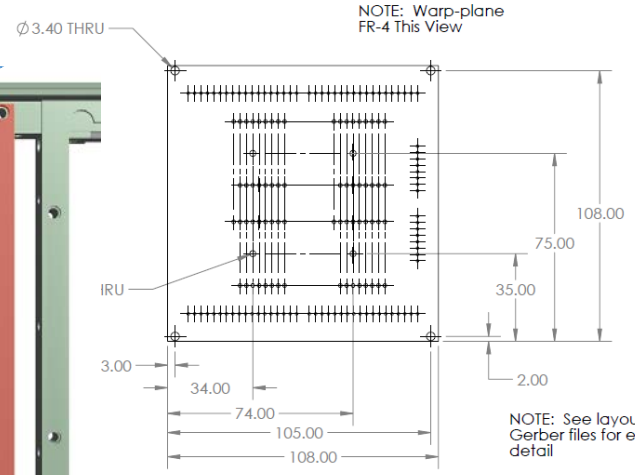
Cold amplifier (mothercard)

PCB design by P. Carniti, C. Gotti, G. Pessina (Milano-Bicocca)
Schematic ready, PCB layout in progress





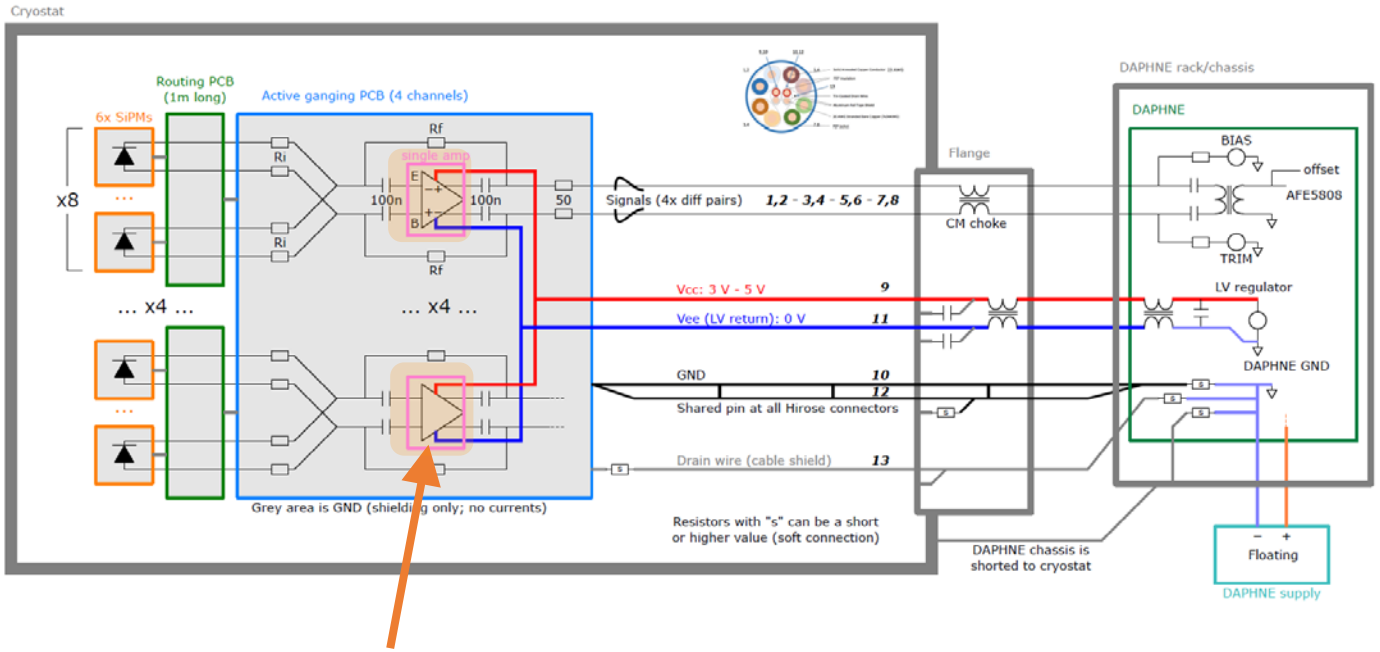


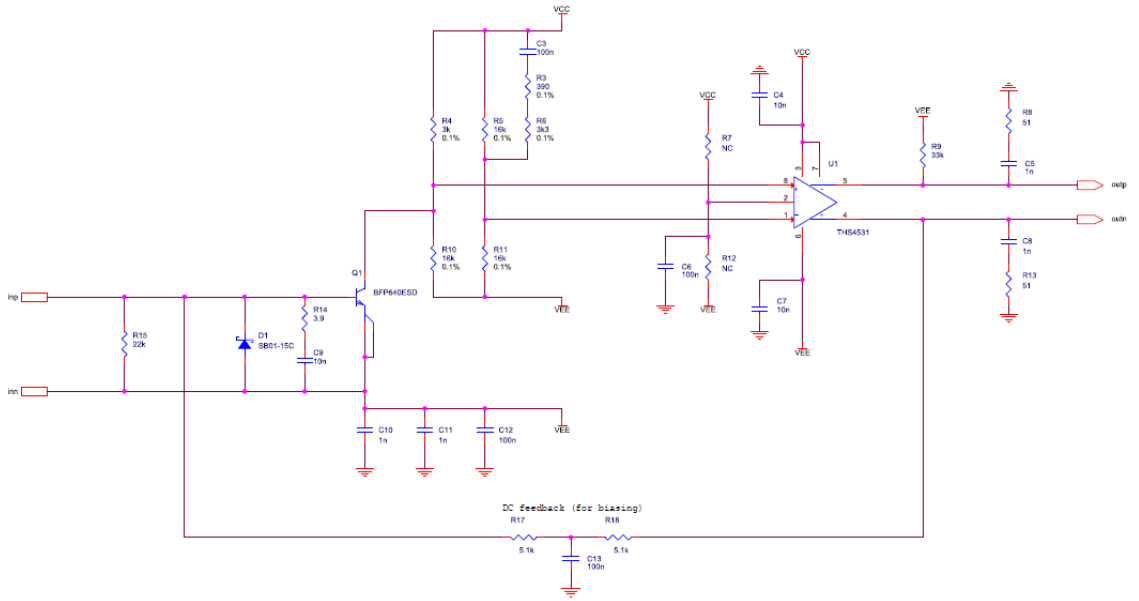


- 4-channel mothercard where 4x single channel daughter cards are plugged in
- Mother + daughter approach gives flexibility during testing. Can be merged back to a single 4 channel board in the future
- Only passive components on the mothercard (pins, resistors, capacitors)
- Present design includes additional connectors to inject test signals to the amplifiers (useful for first tests)

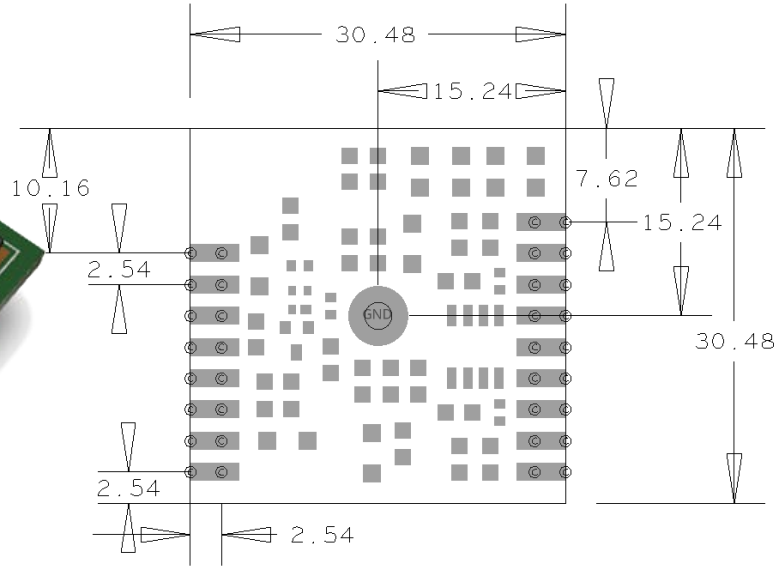
Cold amplifier (single channel)

PCB design by P. Carniti, C. Gotti, G. Pessina (Milano-Bicocca)
Schematic and layout ready, final checks pending



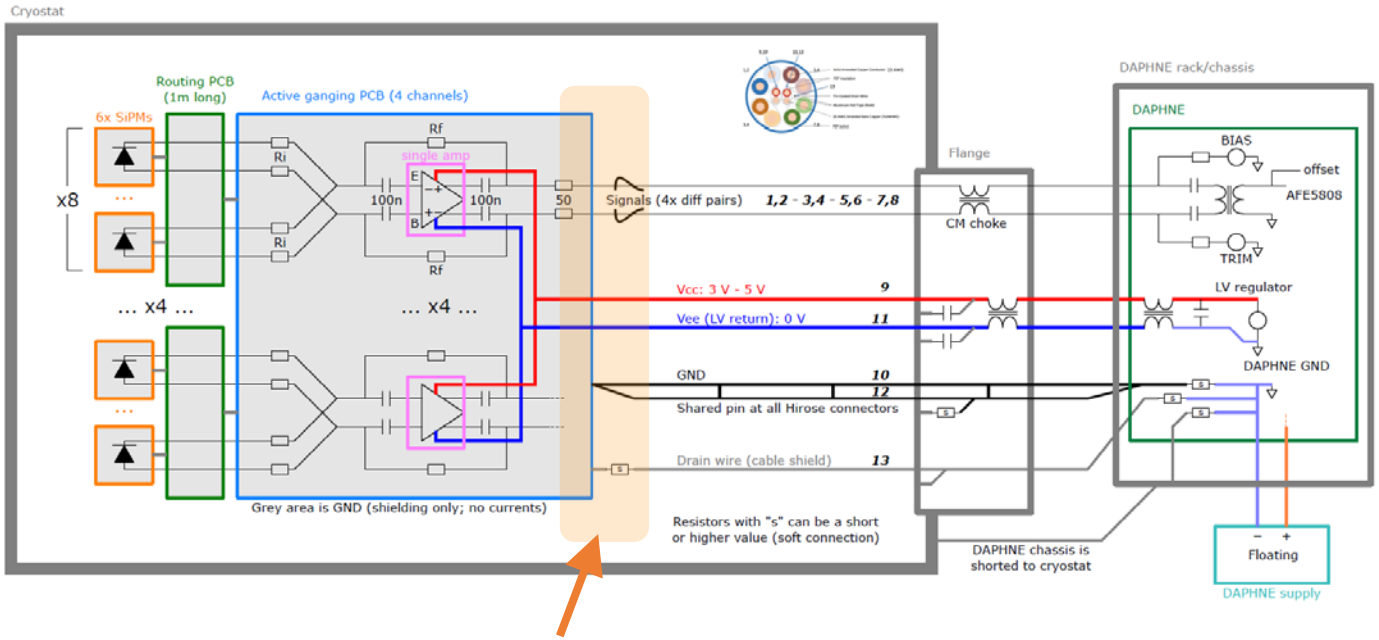


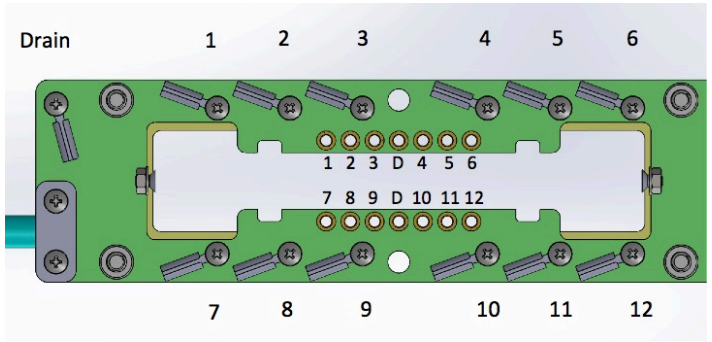
- Single channel differential gain block
- Main change since previous version (slide 2):
  DC current of Q1 now goes to Vee
  → compliant with grounding scheme
- Thin metal film resistors (±10ppm/°C)
- C0G (NP0) ceramic capacitors (±30ppm/°C)



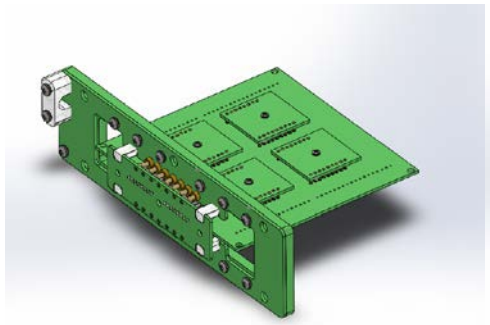
From cold amplifier to cable

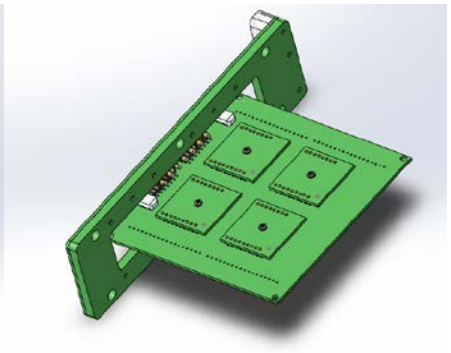
PCB design by J. Ameel (UMich)
Schematic and layout ready

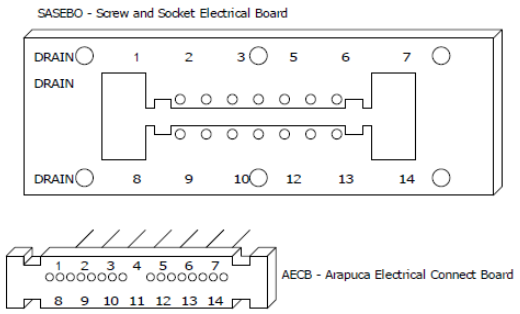




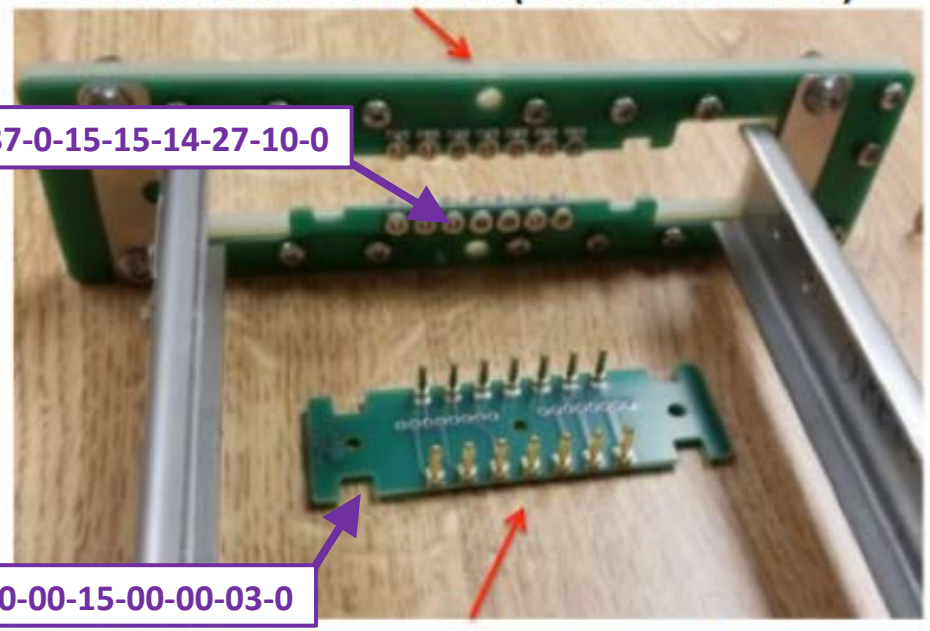
- Interface between cold amplifier (mounted to module) and cable (mounted to APA)
- Cable ends with lugs, screwed to the board
- Pins (Ø 2 mm) make contact as the module is inserted







PD Connector Block PCB (Mounted to APA)

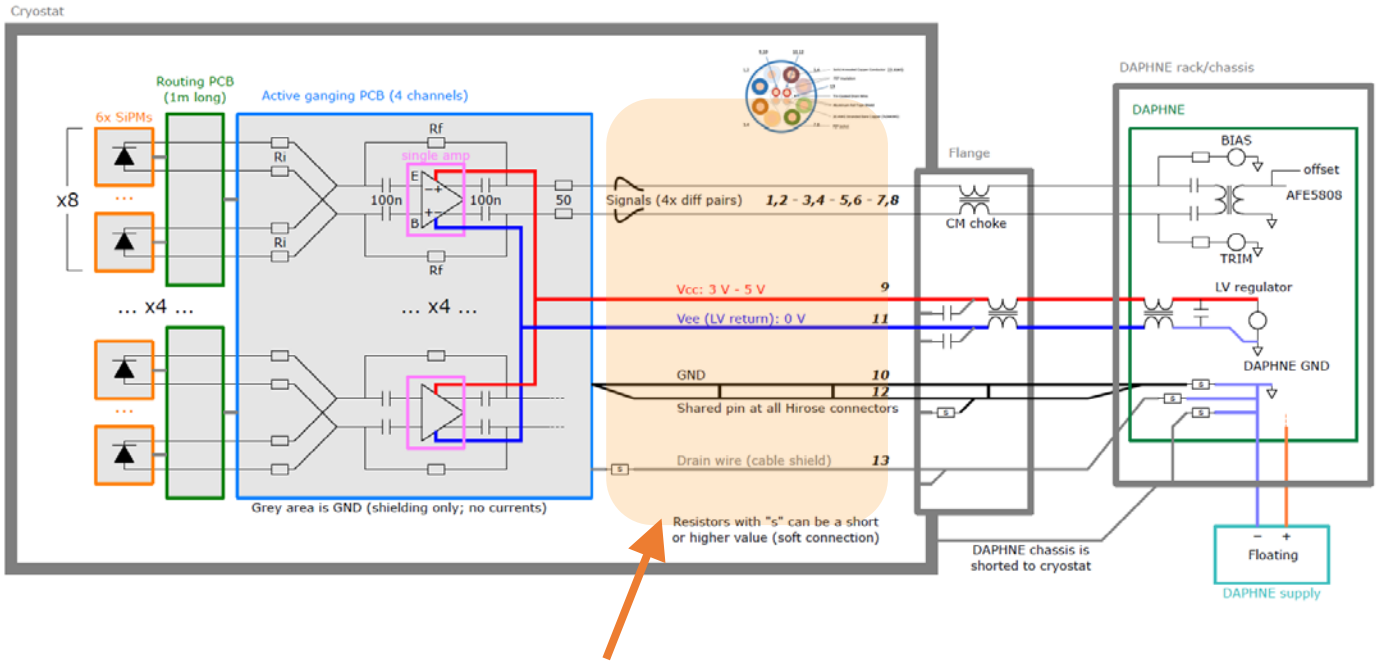


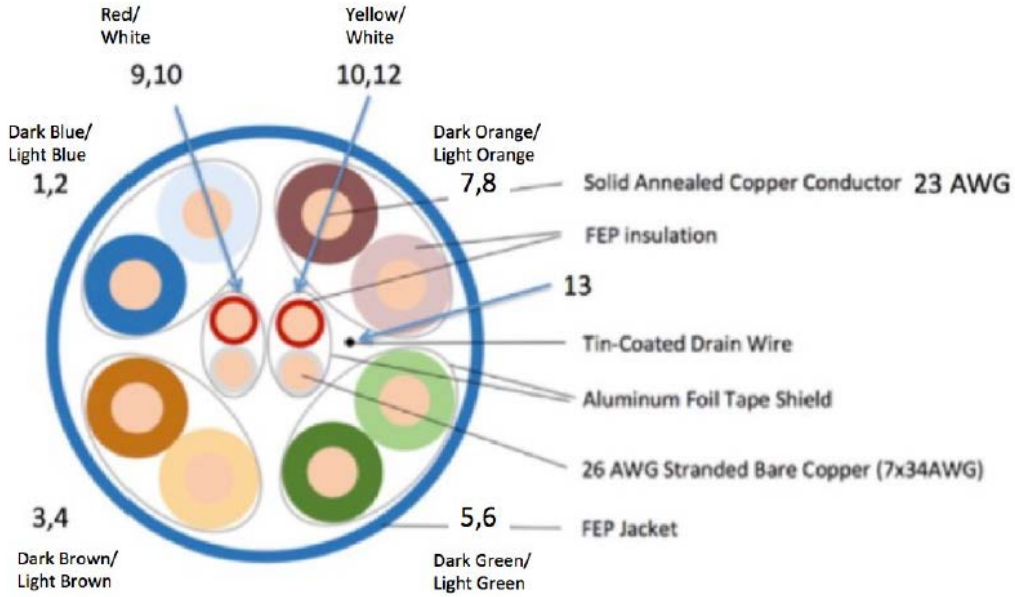
Pins: MillMax 9837-0-15-15-14-27-10-0

Pins: MillMax 5920-0-00-15-00-00-03-0

Connector (mounted to module)

Cable

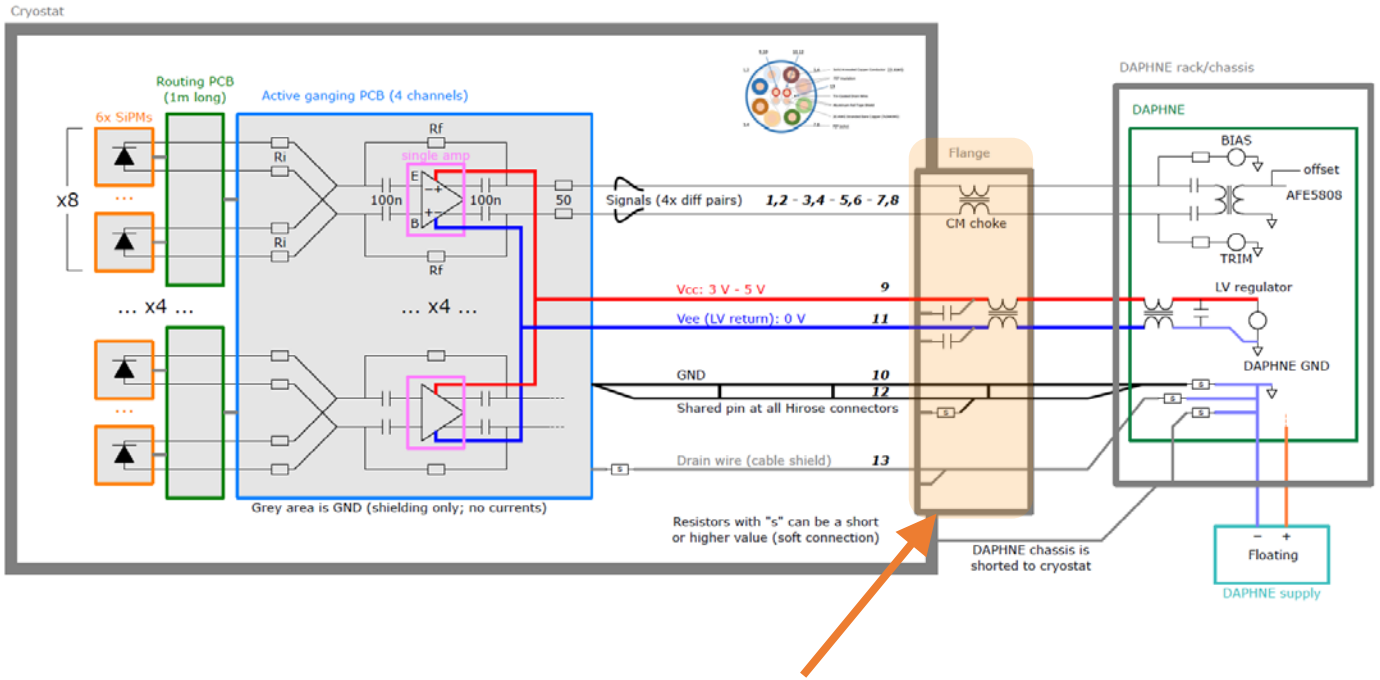


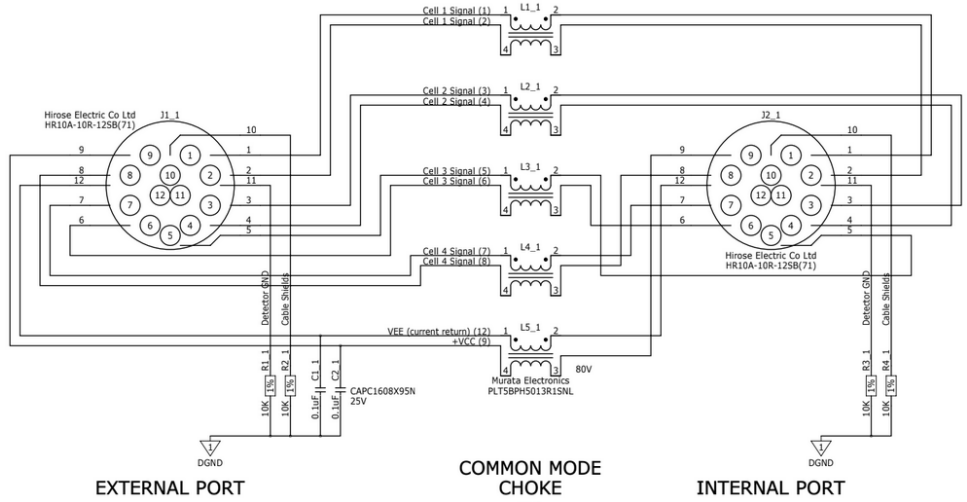


- One cable per module
- 4x 23AWG 100-ohm differential lines (CAT6A) for SiPM signals and bias, each pair individually shielded
- 2x 26AWG pairs for Vcc/GND and Vee/GND (R ≈ 4Ω for 30m length, current ≈ 5 mA)
- GND wires shorted together at connectors along the path (shared pin)
- Drain wire (cable shield) with (soft) connection to GND

Flange

PCB design by J. Ameel (UMich)
Schematic and layout ready

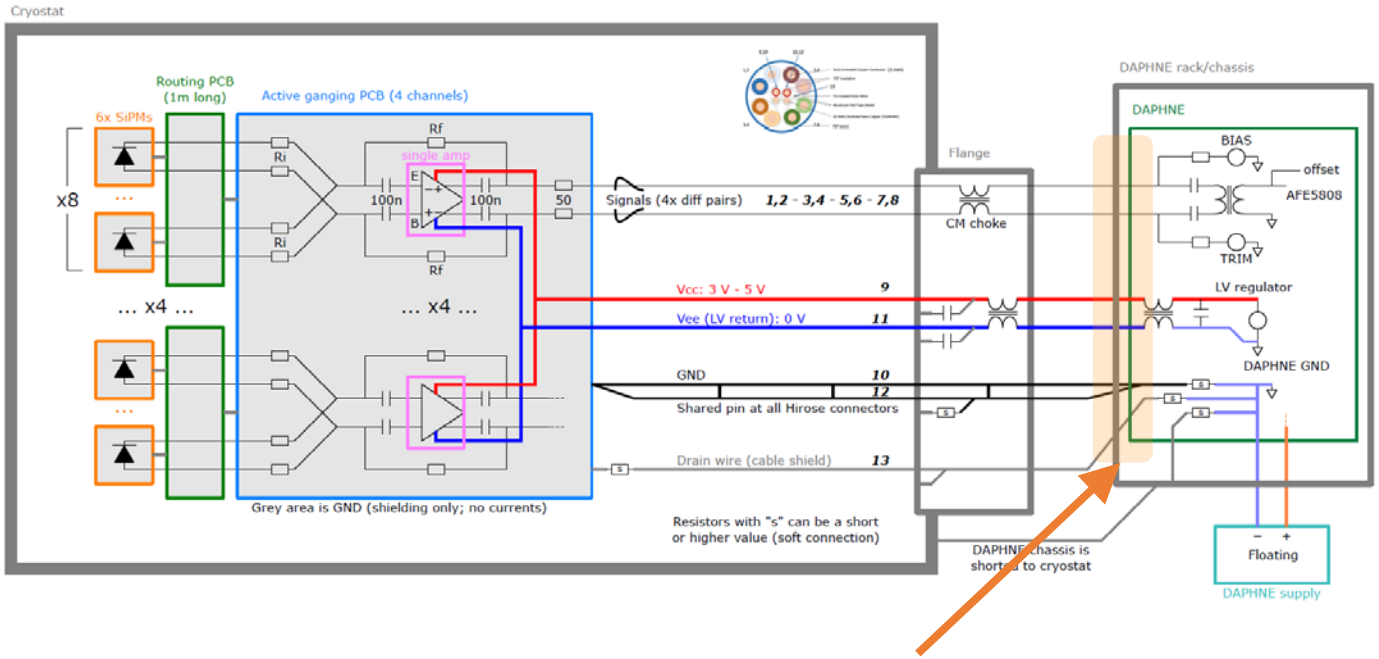


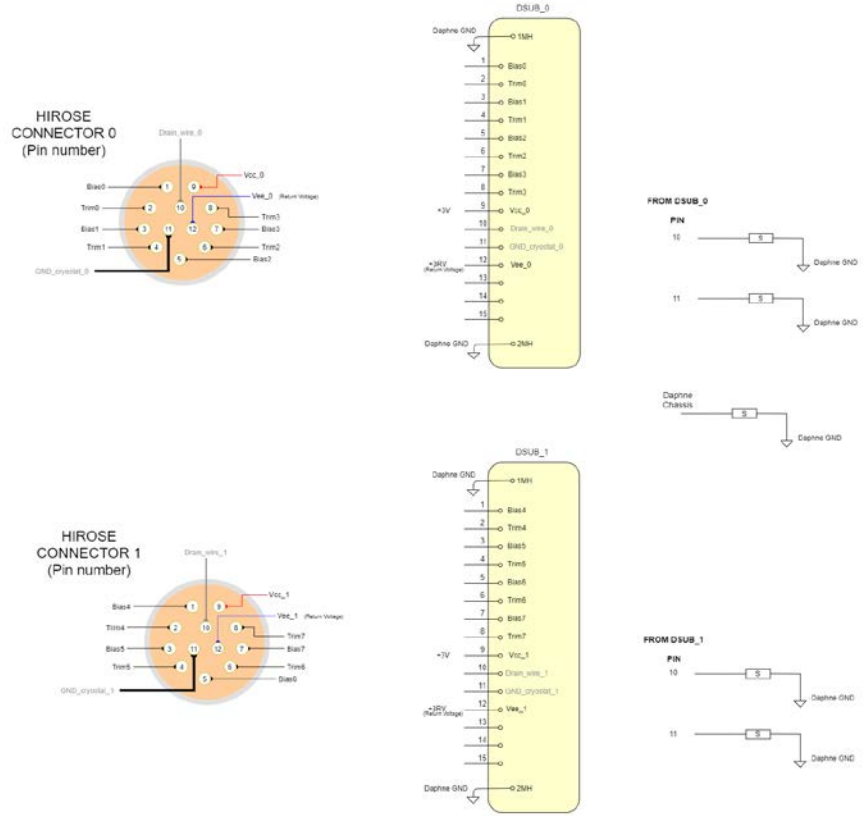


- Cryostat flange (cable feedthrough)
- Origin of GND connection
- Common mode chokes on signal lines
  (Murata Electronics PLT5BPH5013R1SNL, rated for 80Vdc,
  CM impedance 500 ohm at 10 MHz)
- Same common mode chokes and 100 nF capacitors to ground on Vcc, Vee
- Soft ground connections on ground lines and cable shield (drain wire)

DAPHNE input

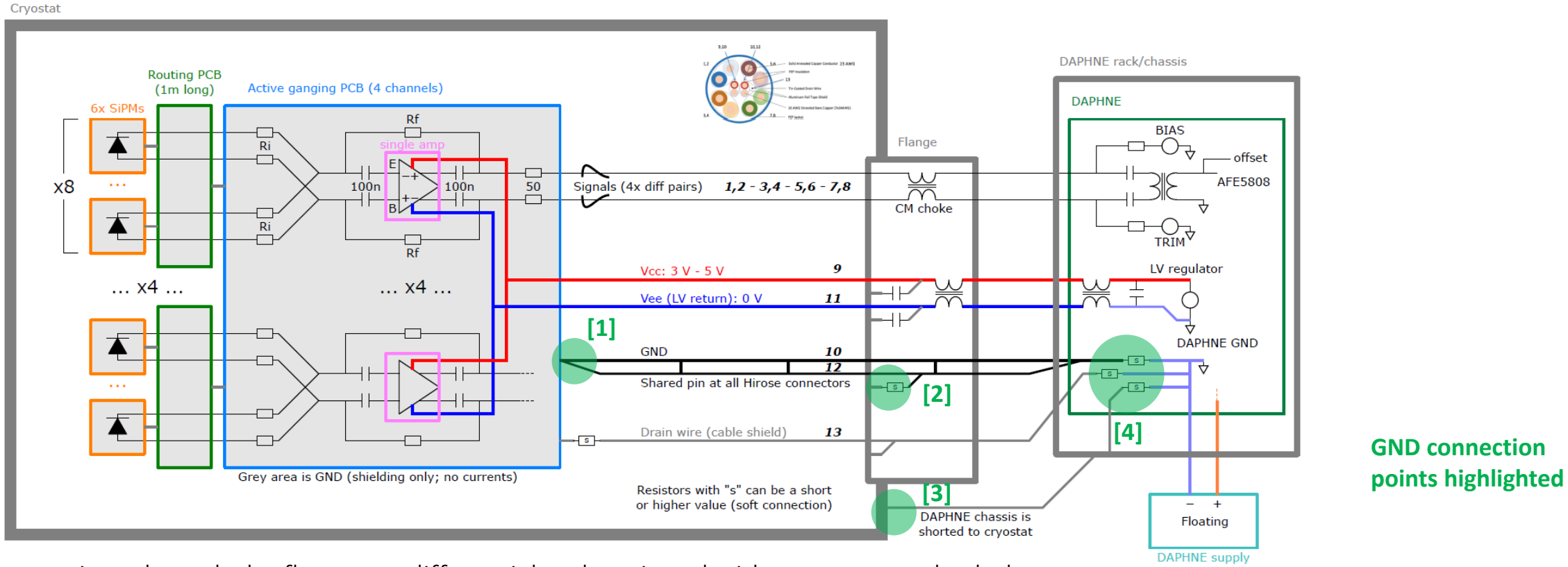
(See full presentation on DAPHNE)





- Options for DSUB or HIROSE (circular) connectors:
  1) short wires connecting chassis HIROSE connectors to DAPHNE (baseline, but not preferred for the final design)
  2) flex circuit to connect chassis HIROSE connectors to DAPHNE
  3) fabricating cables with HIROSE plugs on one end (to connect to the feedthrough) and D-sub plugs on the other end for direct connection to D-sub connectors mounted on DAPHNE.
- Signal pairs:
  - Transformer for differential to single-ended conversion
  - Active 100-ohm termination inside the front-end chip (AFE5808A)
  - Max dynamic range: 1 V
- Power supply:
  - 3-5 V with linear regulator, current ≈ 5 mA

Grounding summary



GND connection points highlighted

- All penetrations through the flange are differential and equipped with common mode chokes
- Ground on PD module is just for shielding and reference (no DC currents), and is tied to detector ground at the flange (star origin) **[1,2]**
- DAPHNE rack and chassis are tied to detector ground (safety) **[3]**
- Soft ground connection between DAPHNE board ground and chassis **[4]**
- Each DAPHNE board is powered by a floating voltage supply
- Soft (kΩ) connections preferred everywhere in the design, to keep flexibility to choose between short, soft, open

Cold electronics: summary and plans

Present status:

- Performance of the cold amplifier demonstrated with SiPM + capacitance to simulate ganging
- Design of PCBs for integration into module well advanced (or complete)

Plans:

- 2020 Q3:
  - PCB prototype fabrication
- 2020 Q4:
  - System tests with SiPMs + routing board + cold amplifier + oscilloscope
  -Demonstrate S/N in realistic ganging configuration (see also: tests of SiPM high level specs)
- 2021:
  - Full system tests with DAPHNE
  - Cryogenic reliability studies
  - …

Summary of specifications/requirements

- Cold electronics:

Power supply voltage	+ 3-5V / -0V	Value of the positive supply will be fixed within the indicated range. The negative supply (current return) is at ground
Power supply current	<20 mA/module or <5 mA/channel	Limit IR drop on cable. Current estimate is 4 ohm resistance for 30m of AWG26. Also, limit power consumption of the cold amplifier.
Power supply precision/stability	+/- 2%	
Power supply noise/ripple	<1 mVpp	Includes filtering
Amplifier gain	100 V/A	1V max dynamic range at DAPHNE input for a typical 2000pe signal. Depends on SiPM gain, overvoltage and recovery time. Value will be tuned depending on those.
Amplifier gain accuracy / uniformity	1%	
Signal to noise ratio	>4	Depends on SiPM operating voltage and signal processing (i.e. filtering)
Differential output impedance	100 ohm	Needs to match cable impedance
Crosstalk	<0.05%	A 2000 p.e. signal on a channel will give less than 1 p.e. crosstalk on the others

- Cabling:

Differential impedance of signal pairs	100 ± 15 ohm	
Shielding of signal pairs	Each pair individually shielded	
Crosstalk	<0.05%	A 2000 p.e. signal on a channel will give less than 1 p.e. crosstalk on the others
Resistance of power supply lines	0.2 ohm/m	Resistance below 6 ohm for a 30m length

Spare

Cold amplifier design in the TDR