DAPHNE DESIGN

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DUNE SP-PDS
60% DESIGN REVIEW

On behalf of the DUNE SP-PD Consortium
June 19th, 2020

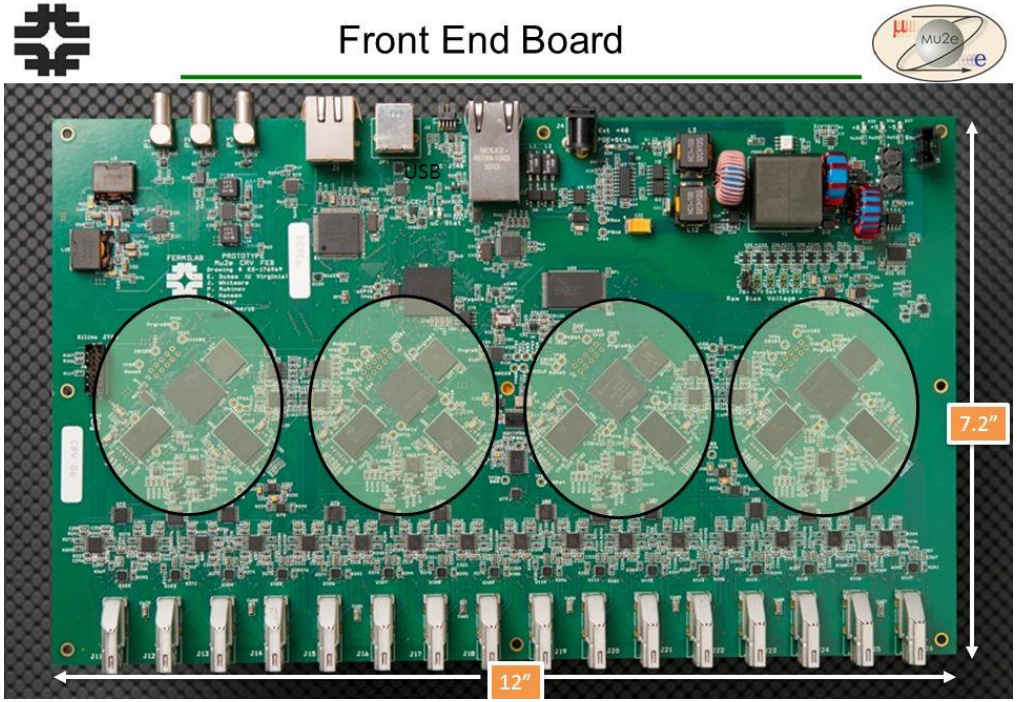
Outline

- DAPHNE design
- DAPHNE features and plan
- DAPHNE Summary

DAPHNE (Detector electronics for Acquiring PHotons from NEutrinos)

REQUIREMENTS:

- Signal-to-noise > 4 (SP-PDS-14
- Time resolution < 1us (SP-FD-4
- Dark noise rate < 1kHz (SP-PDS-15)
- Dynamic range < 20% (SP-PDS-16)



- DAPHNE hardware: Fermilab-LA Collaboration
- DAPHNE firmware and software: LA responsability

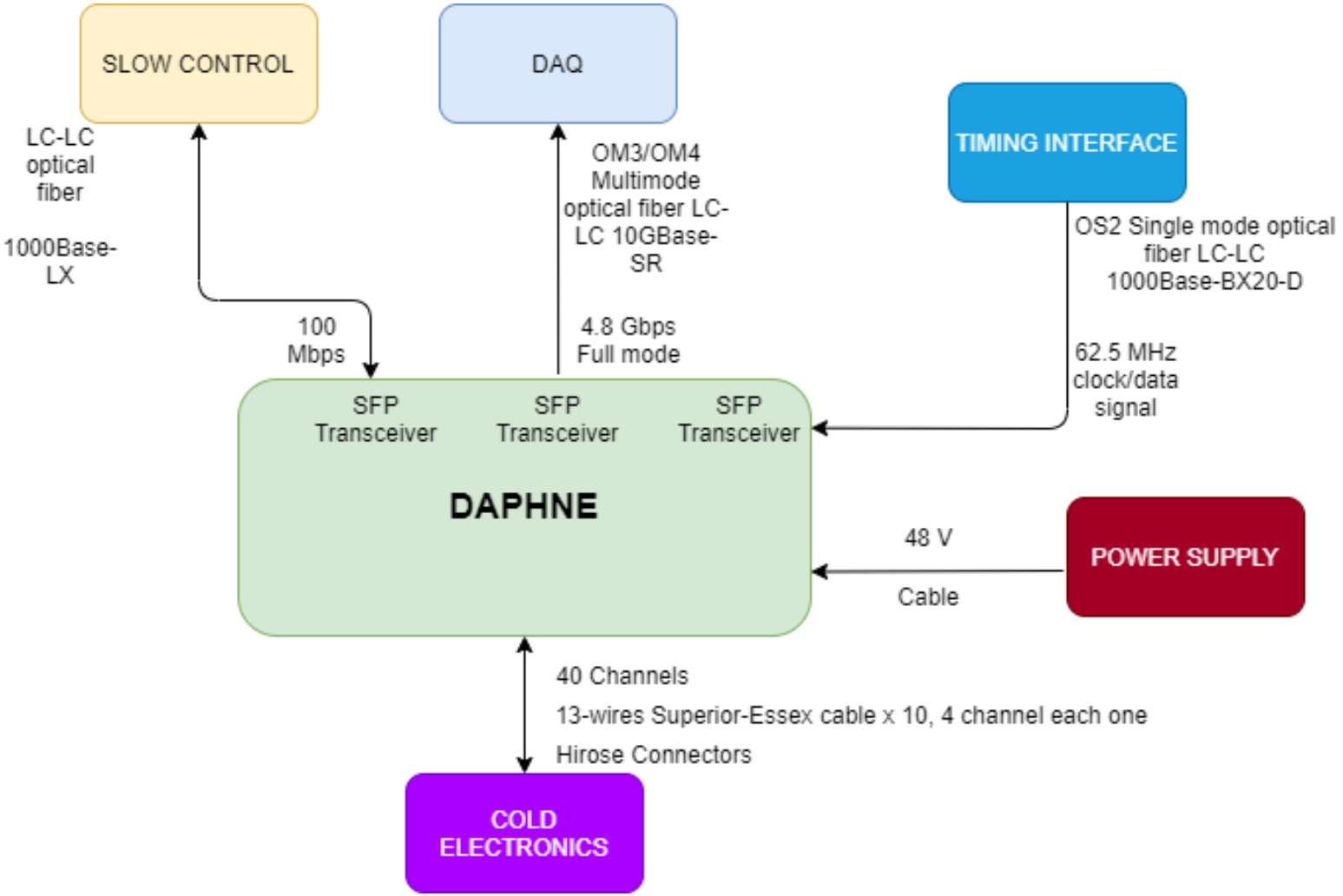
Initially conceived as a Mu2e board upgrade
Same AFE device (ADC+signal conditioning)
Same basic power supply scheme

DAPHNE DESIGN

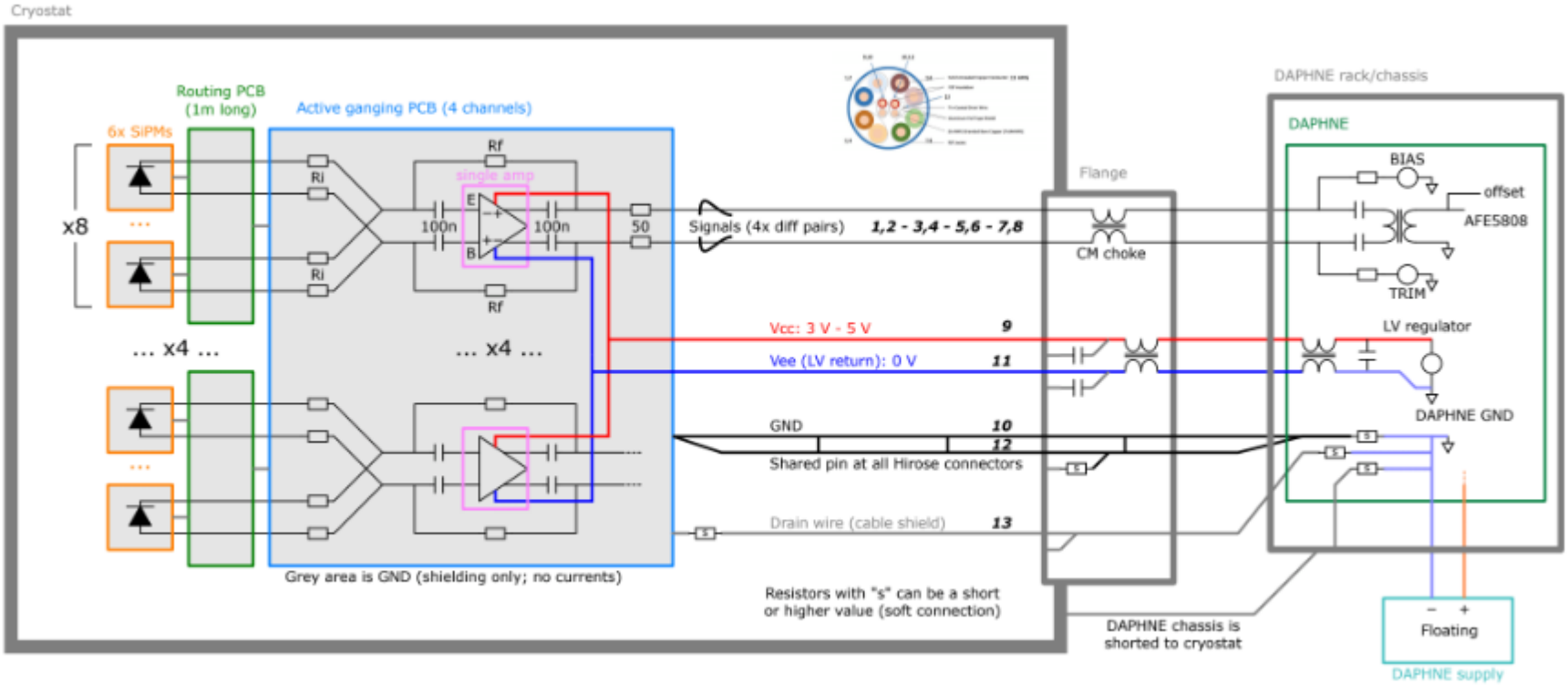
- Schematic and layout implemented on Altium Nexus, using Fermilab Vault. Developed by Sten Hansen, Miguel Marchan, Nina Mobienko (Fermilab), Javier Castaño (UAN, Colombia), Juan Vega (CONIDA, Peru)

- Gateware/firmware/software development:
  - Software: microcontroller STM32 (Led by Juan Vega-CONIDA, Peru – Javier Castaño-UAN, Colombia), Zephyr RTOS
  - Gateware/Firmware: Artix-7 FPGA, Vivado, Migen-Litex core (Led by Manuel Arroyave-EIA, Colombia))
  - Full-mode 4.8 Gb/s link (Led by Diego Arana, Carlos Montiel, Paraguay)

DAPHNE


SLOW CONTROL
DAQ
TIMING INTERFACE
LC-LC optical fiber
1000Base-LX
100 Mbps
OM3/OM4 Multimode optical fiber LC-LC 10GBase-SR
4.8 Gbps Full mode
OS2 Single mode optical fiber LC-LC 1000Base-BX20-D
62.5 MHz clock/data signal
SFP Transceiver
SFP Transceiver
SFP Transceiver
DAPHNE
48 V
Cable
POWER SUPPLY
40 Channels
13-wires Superior-Essex cable x 10, 4 channel each one
Hirose Connectors
COLD ELECTRONICS

INTERFACE TO COLD ELECTRONICS



- 40 Channels (differential pair), 5 D-SUB connectors, 50 USD/channel
- 5 options for Bias Voltage, 5 groups with enable signal (each AFE/ADC)
- Variable trimming voltage/channel, from 0 V to 4.096 V (fine adjustment for SiPM Array Voltage), current monitoring per channel
- +3 V/channel, power supply for Cold Electronics amplifiers, current monitoring
- D-SUB Connectors on DAPHNE, Hirose connectors on chassis

DAPHNE-DAQ (FELIX) LINK

General Milestones for Gateware development

As discused in the DAQ interface document, the milestones for the Firmware development are as follows:

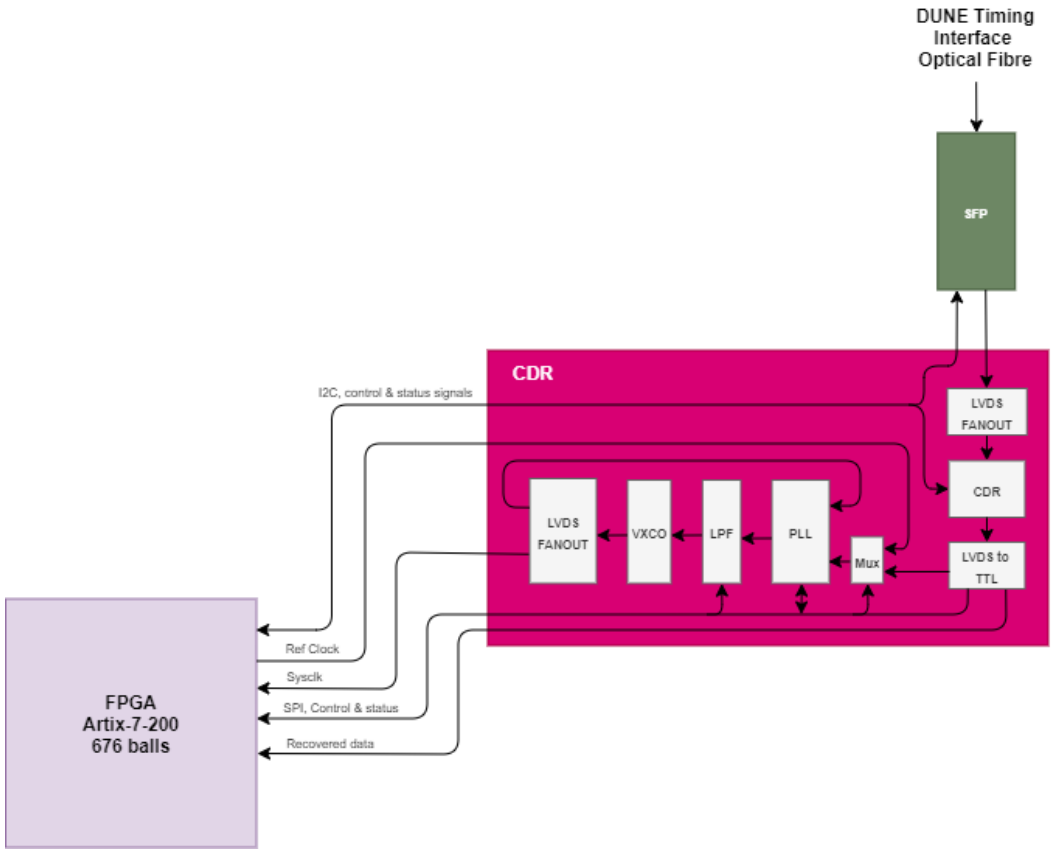
- Q3 2020: Demonstration of the 4.8 Gb/s FULLMODE link with FELIX+Artix7 evaluation board. First checkpoint for allocating resources towards a major re-design of DAPHNE.
- Q4 2020: DAPHNE-timing and readout integration milestone. Final checkpoint for allocating resources towards a major re-design of DAPHNE.
- Q1 2021: LCM-timing integration milestone.
- Q2 2021: DAPHNE and LCM system integration in VST milestone.

Full-mode link according to CERN specification (ATLAS note AT1-DQ-ES-0001 June 3, 2019), basic 8b/10b encoding

2 SFP connectors, 2 optical transceivers at 4.8 Gbps (Artix-7)

Originally, full-mode is defined for 9.6 Gbps. DAPHNE team is working with DAQ consortium to try to implement full-mode at 4.8 Gbps to accommodate Artix-7 limitations. Contingencies (using a Kintex-7 FPGA or aggregator boards) have also been defined in case this change cannot be accommodated.

TIMING INTERFACE



Based on the original PDTS (UoB)

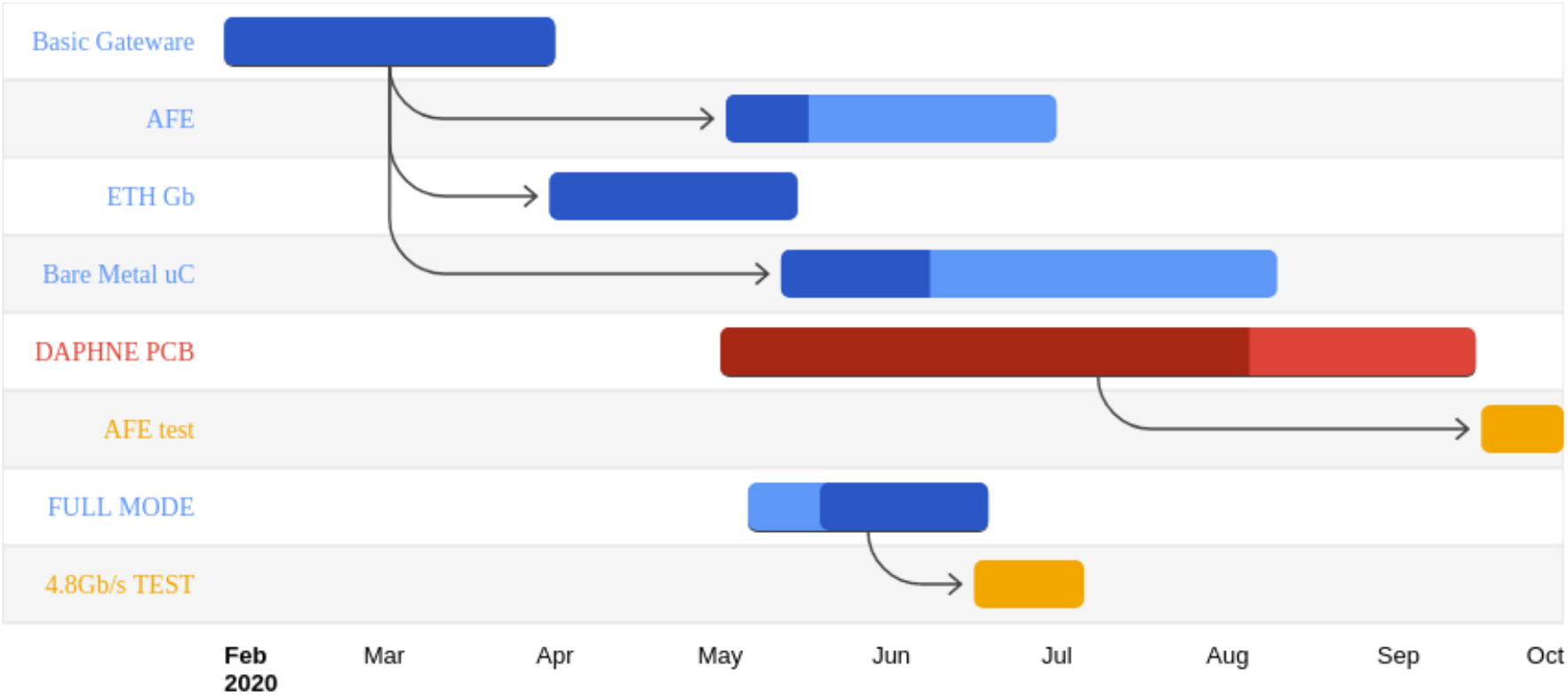
62.5 MHz VCXO/PLL system, supporting fiber disconnection or fail

Alarms supporting via Slow Control Interface

Clock and data recovery

Implementing PDTS system module on the FPGA

FIRMWARE/GATEWARE DEVELOPMENT PLAN



POWER SUPPLY

Designed by Miguel Marchan, based on Mu2e board designed by Sten Hansen

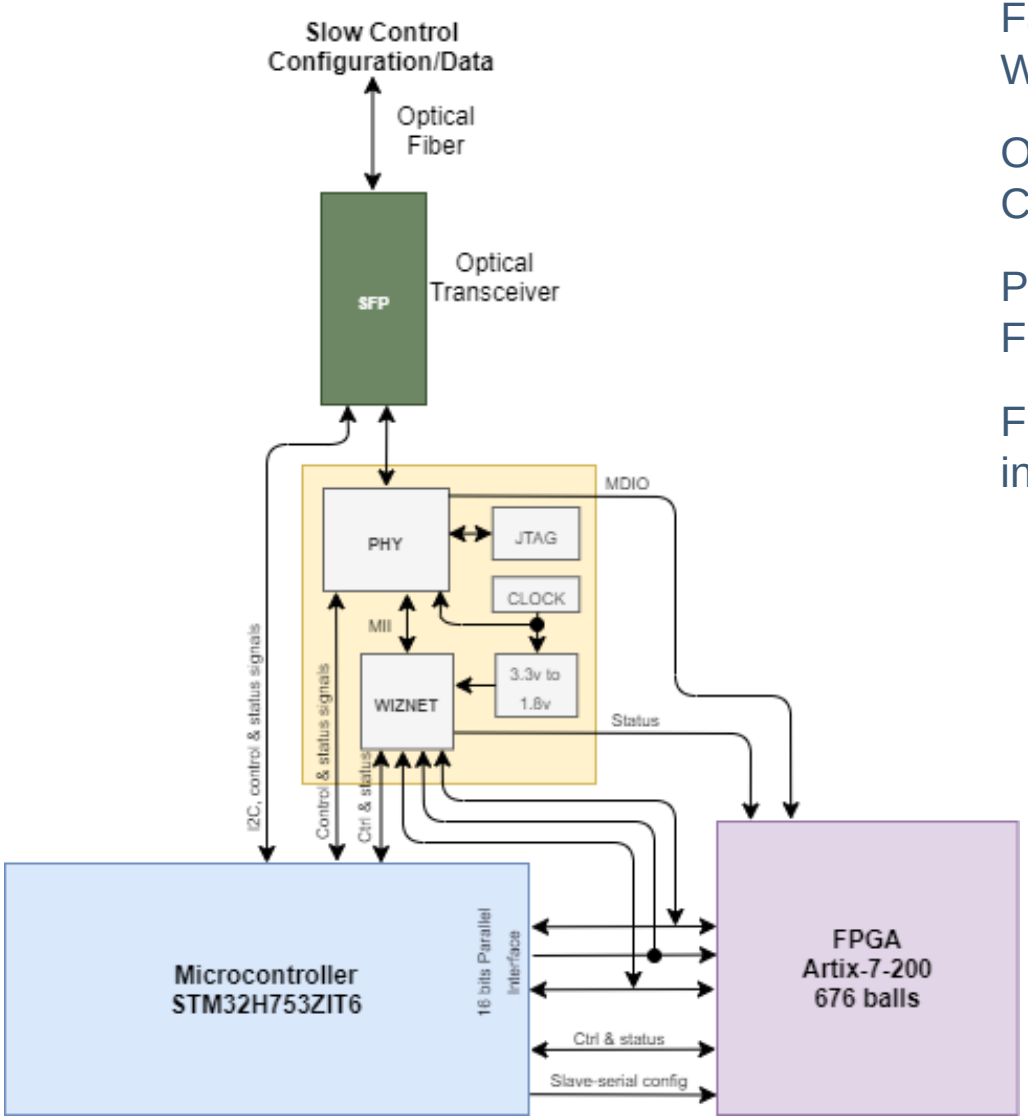
New power supply scheme:

- start up power sequence for Artix-7 (required for stability and operation)
- Generation of different voltages: 1, 1.2, 1.8, 2.5, 3.3 V. + 5, -5
- Circuit for the Cold Electronics supply with 2 stages regulator,

+ 3 V output voltage

- Bias and trimm voltage for the Cold Electronics
- About 26 W with 48 V input

SLOW CONTROL



Fast Ethernet, optical interface via Wiznet chip

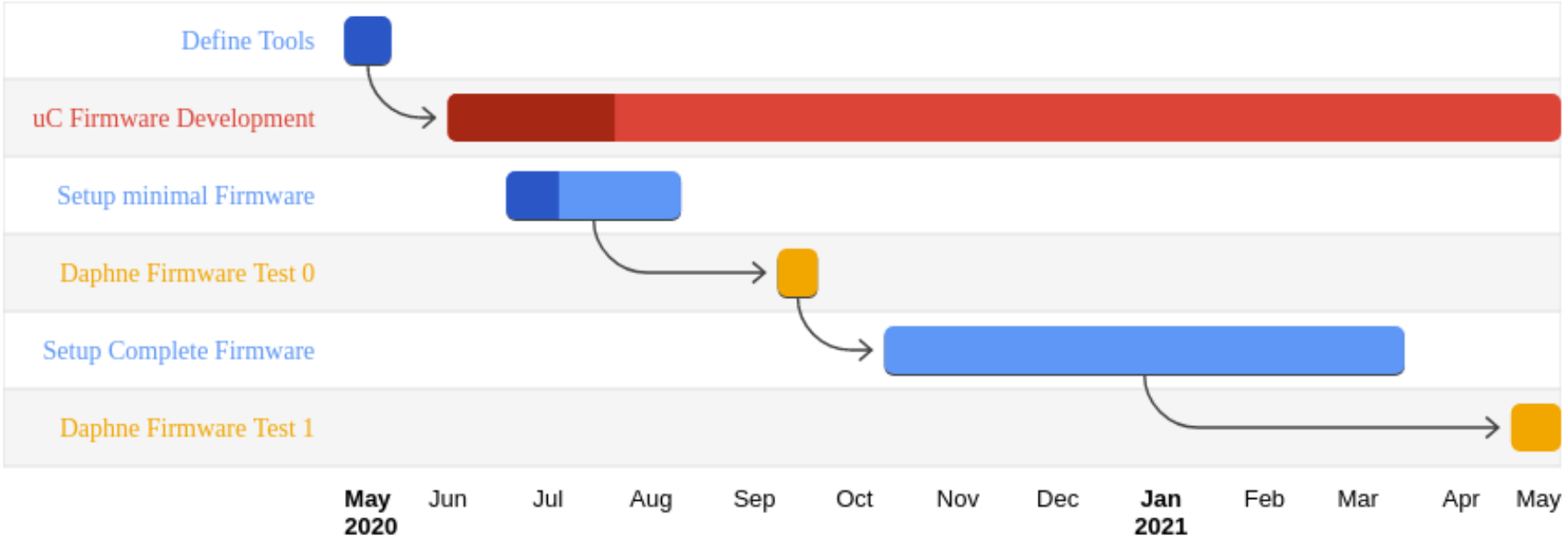
OPC-UA Server as specified by DAQ Consortium

Parallel interface FPGA-Microcontroller, FMC-based

FPGA Configuration via Slave-serial interface

- AFE/ADC configuration
- Wiznet and PHY configuration
- Current/voltage monitor
- FPGA temperature
- Trimm and offset voltages monitor
- SFP transceivers
- Timing Interface

MICROCONTROLLER DEVELOPMENT PLAN



SUMMARY OF SPECIFICATIONS/REQUIREMENTS

SPECIFICATION/REQUIREMENT	DESCRIPTION
Estimated cost per channel	50 USD
Channels	40
Resolution (bits)	14
Sample rate	62,5 Msps
Voltage Supply to Cold Electronics	Bias: 5 options (34, 45, 55, 65,75) Trimm: per channel 0-4,096 Power Supply: +3V (Electronics)
Monitoring	Bias, Trimm Power Supply (all DC voltages) FPGA Temperature
Data link	Optical 4,8 Gbps, Full-mode protocol, SFP transceiver
Timing Interface	Optical, 62,5 MHz, aux LEMO input and output
Slow Control	Optical Fast Ethernet, SFP transceiver, OPC-UA Server on Microcontroller
Power Supply	48 V input, estimated power 26 W
Firmware/Gateware/Software	Artix-7 FPGA, Migen/Litex Core/STM32H753 Microcontroller, Zephyr RTOS

Full upgrade of the Mu2e board with many improvements and new features

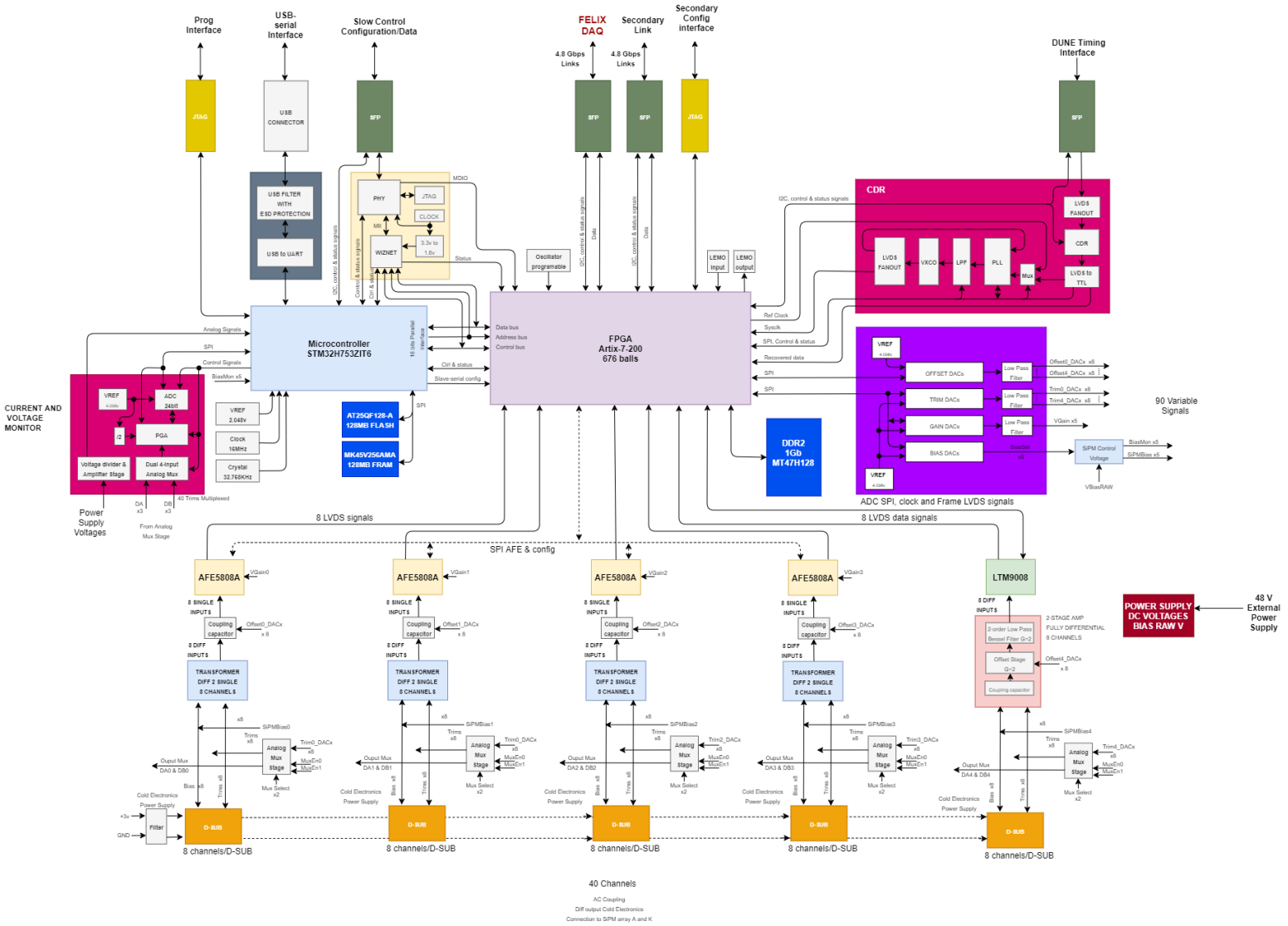
THANKS!

BACKUP

STATUS FROM 30% REVIEW

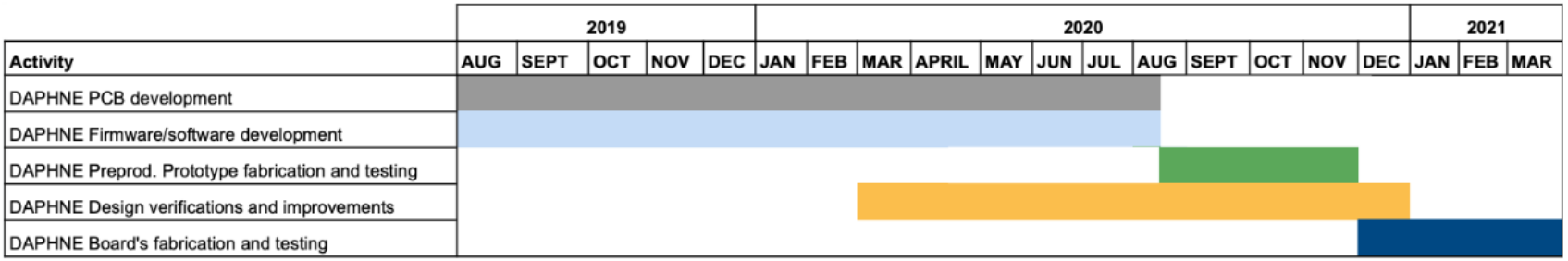
- TDR Electronics Next Steps —> Actions
  - Replace outdated components —> old µC & Spartan-6 replaced with new µC & Artix-7
  - 40-channel prototype board —> new design has 5 octal ADCs
  - FPGA logic resource needs —> combine smaller FPGAs into single large Artix-7 FGPA
  - Increase dynamic range —> Replace 12-bit AFE5807 ADC with 14-bit AFE5808A ADC
- Additional 30% Design Review Comments/Recommendations —> Actions
  - Power to active cold electronics through a pair of conductors added to the custom PD cable terminated with ProtoDUNE-SP-style Hirose (rather than HDMI) connectors with system-level grounding plans documented
  - Functionalities specific to Mu2e were removed from DAPHNE design
- New requirements since 30% Design Review —> Actions
  - Expected 1-3 Gbps data rate —> Remove controller module and connect directly to (FELIX) DAQ optically
    - Requires also adding external 48 V supply
- Internal review of DAPHNE schematic to validate design changes since the TDR
  - Parts-availability check also performed to identify long lead-time parts and swap them for alternate ones

DAPHNE (Detector electronics for Acquiring PHotons from NEutrinos)

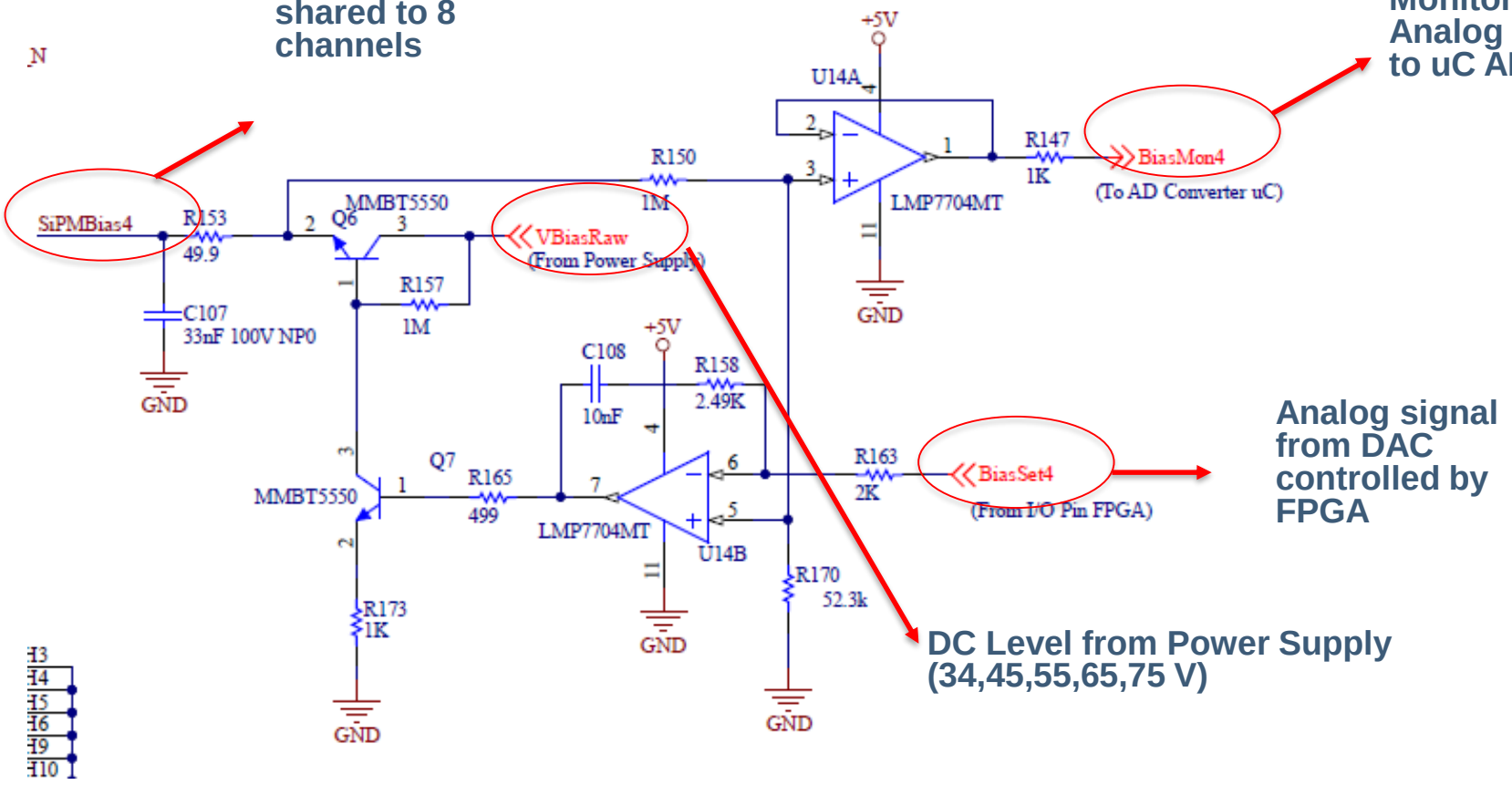


Schedule & Impacts

- Expect resolution of items raised during internal review to take up to 8 weeks, followed by 2 weeks for fabrication, and 2 weeks for assembly

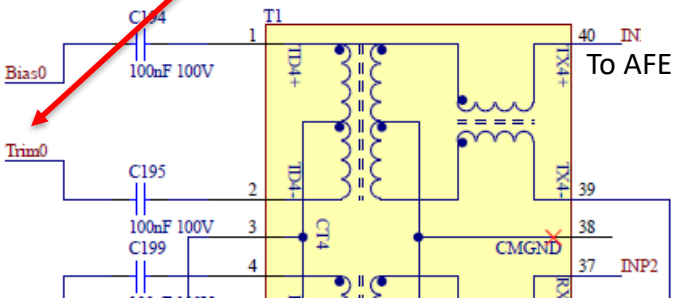


SiPM Biasing-Bias Voltage

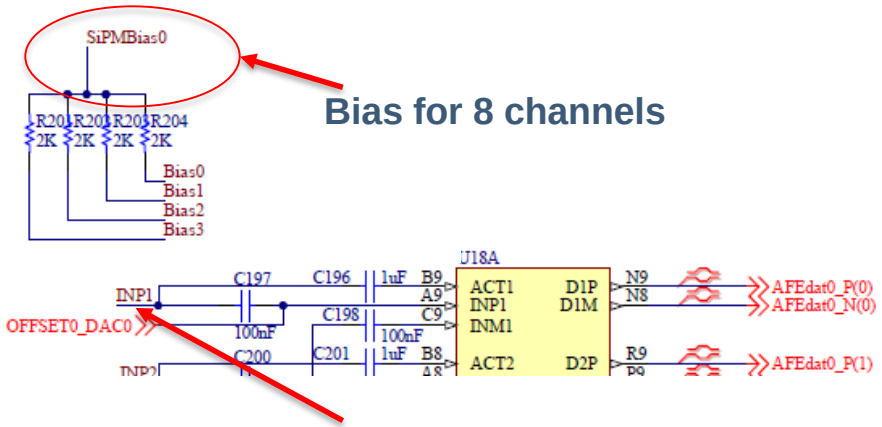


SiPM Biasing-Trimm Voltage

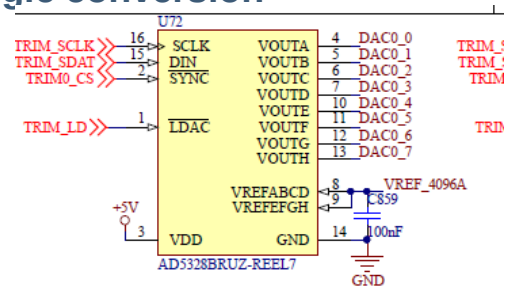
To Cold Electronics (per channel)

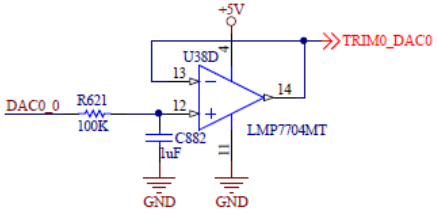


To AFE single input



8 channels transformer, diff-single conversion



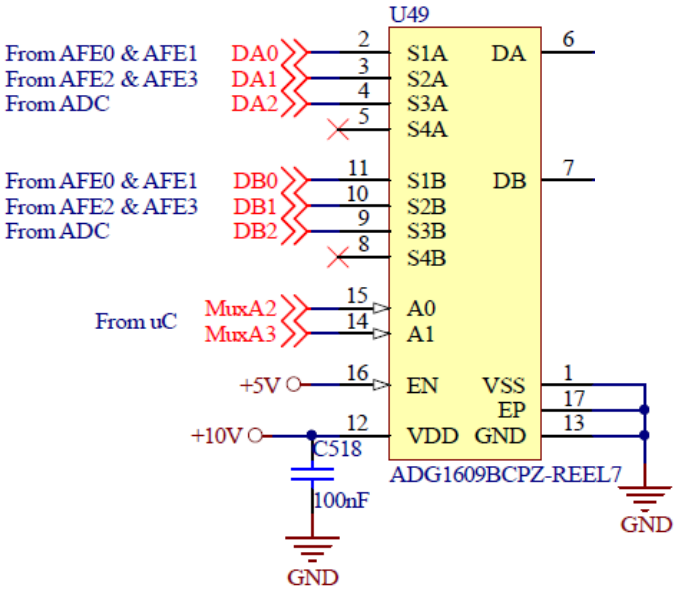


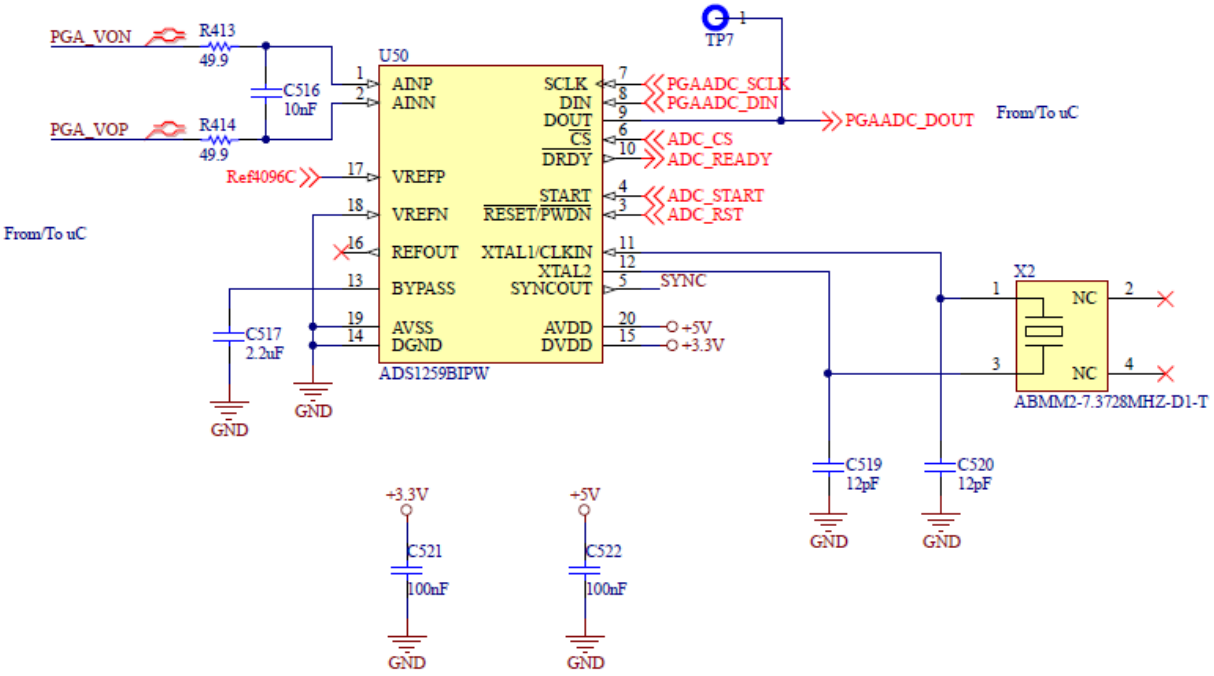
40 Trimm Voltages generated by 5 DACs

Controlled by the FPGA

0 V to 4,096 V

SiPM Biasing-Trimm Monitoring





Multiplexed scheme for 40 channels

PGA+24-bit ADC controlled by the FPGA/STM32 Microcontroller