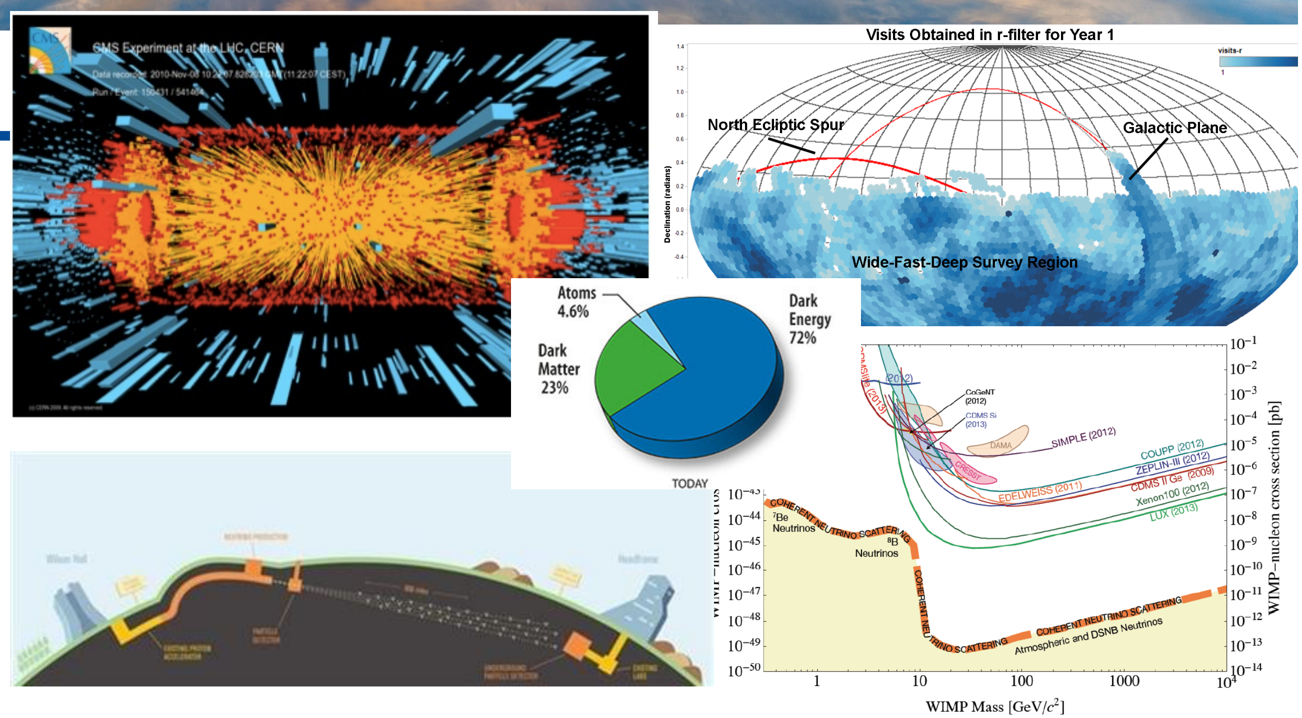
Highlights on FNAL R&D activities: Trigger and DAQ



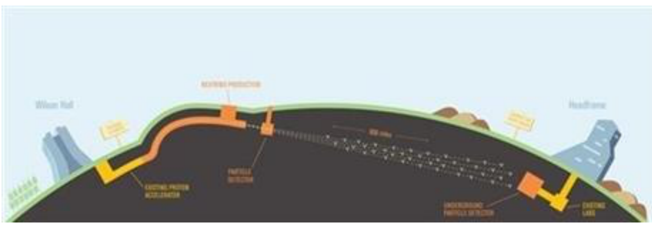
Ted Liu

CPAD meeting at Caltech

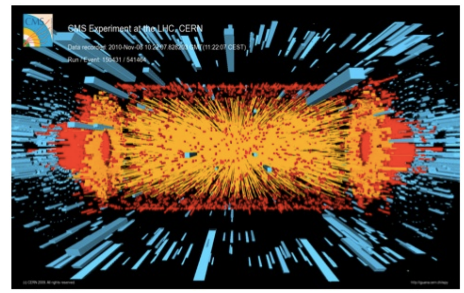
Oct 9th, 2016

Future Trigger & DAQ challenges

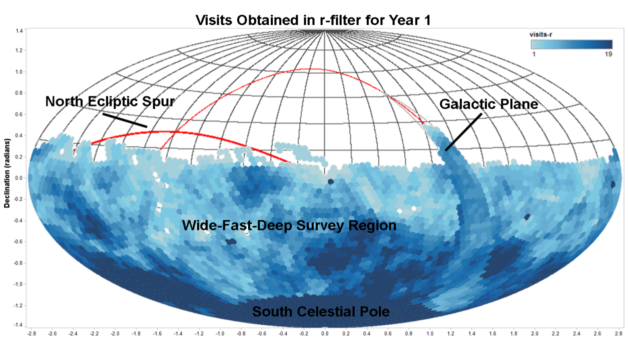
Reliable Cryogenic readout electronics



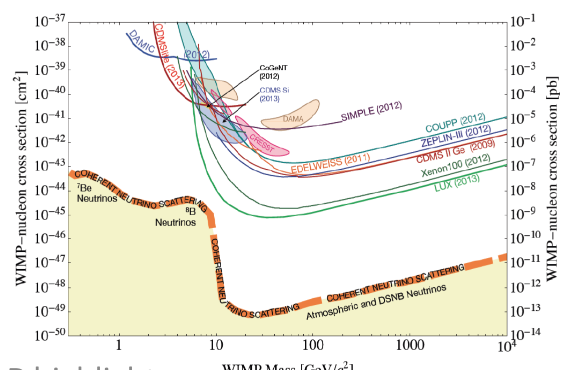
High luminosity/radiation/occupancy…
(e.g. HL-LHC and beyond)



Huge data volume per channel
(e.g. MKID for Dark Energy)

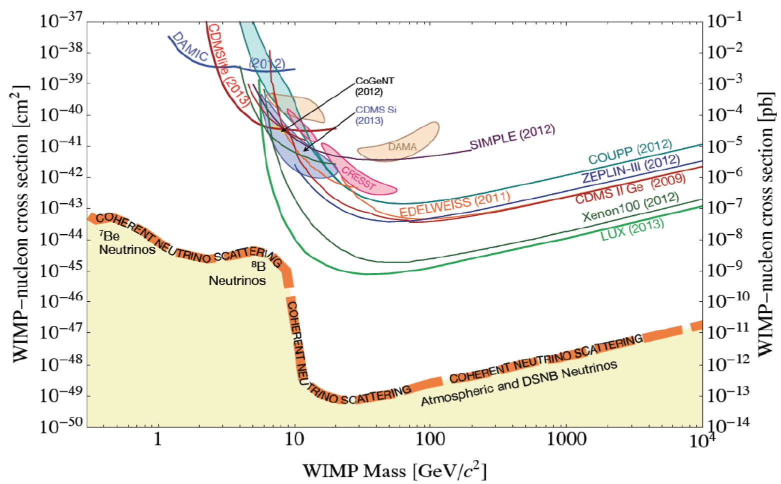


Extremely Low noise
(e.g. CCD readout for Dark Matter
and coherent n scattering)



Low noise CCD readout R&D goals and accomplishments

- Future experiments using CCDs for Neutrino coherent scattering or Dark matter search: need to increase the detector mass and lower the noise.
- FNAL CCD R&D has demonstrated the proof of concept of a time multiplexed readout approach.
  - Full low noise images were generated for proof of concept
  - Fermilab has developed a system capable of a large number of CCDs.
  - The noise is low enough to benefit from a new generation of low noise CCDs (with higher gain and skipper CCDs).
  - The DAQ could use Fermilab SCD ARTDAQ/off-the-shelf software
- The R&D has been successful, and there is opportunity to launch new experiment



Proof of concept work done: a multiplexed readout for CCDs

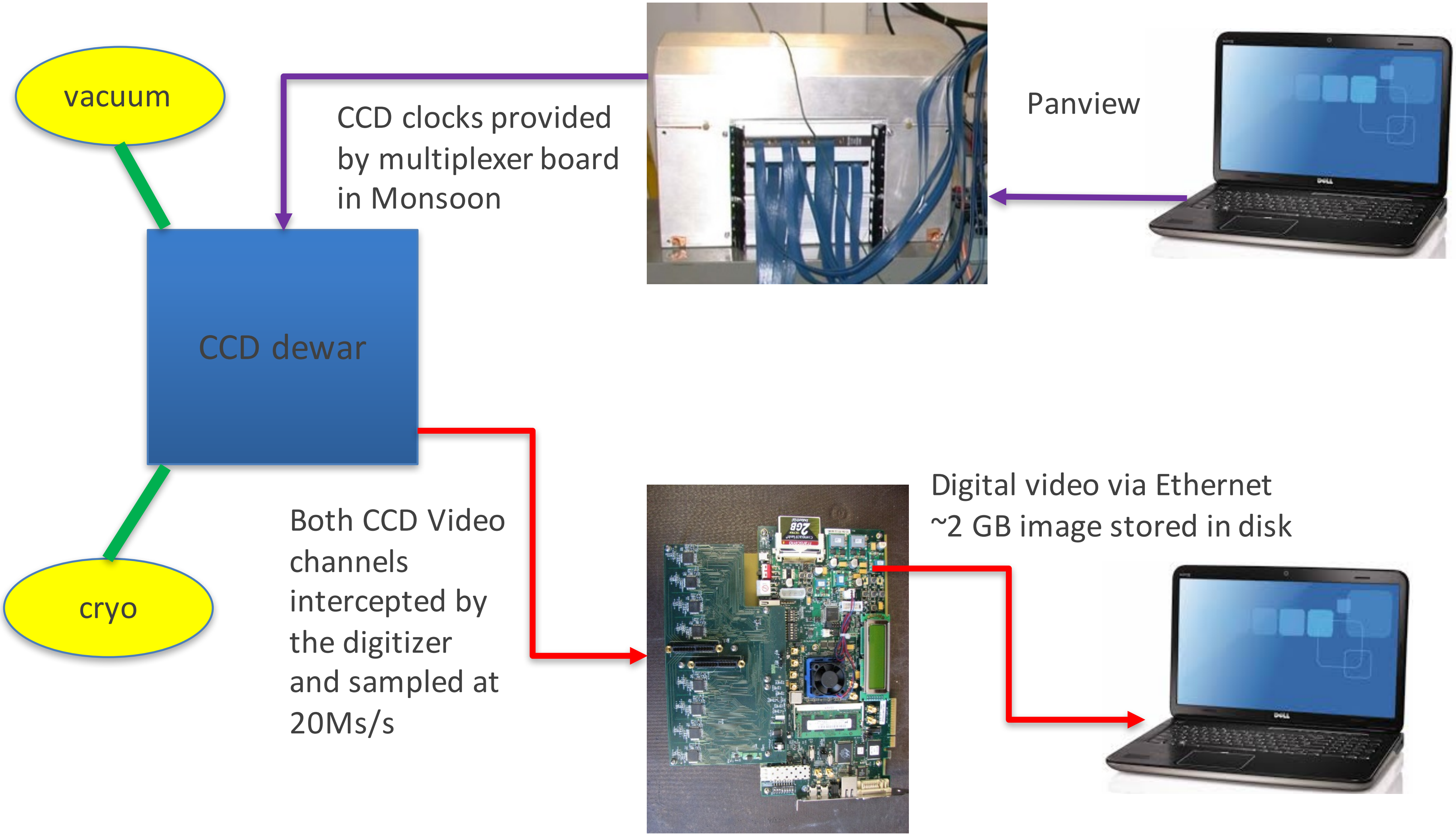
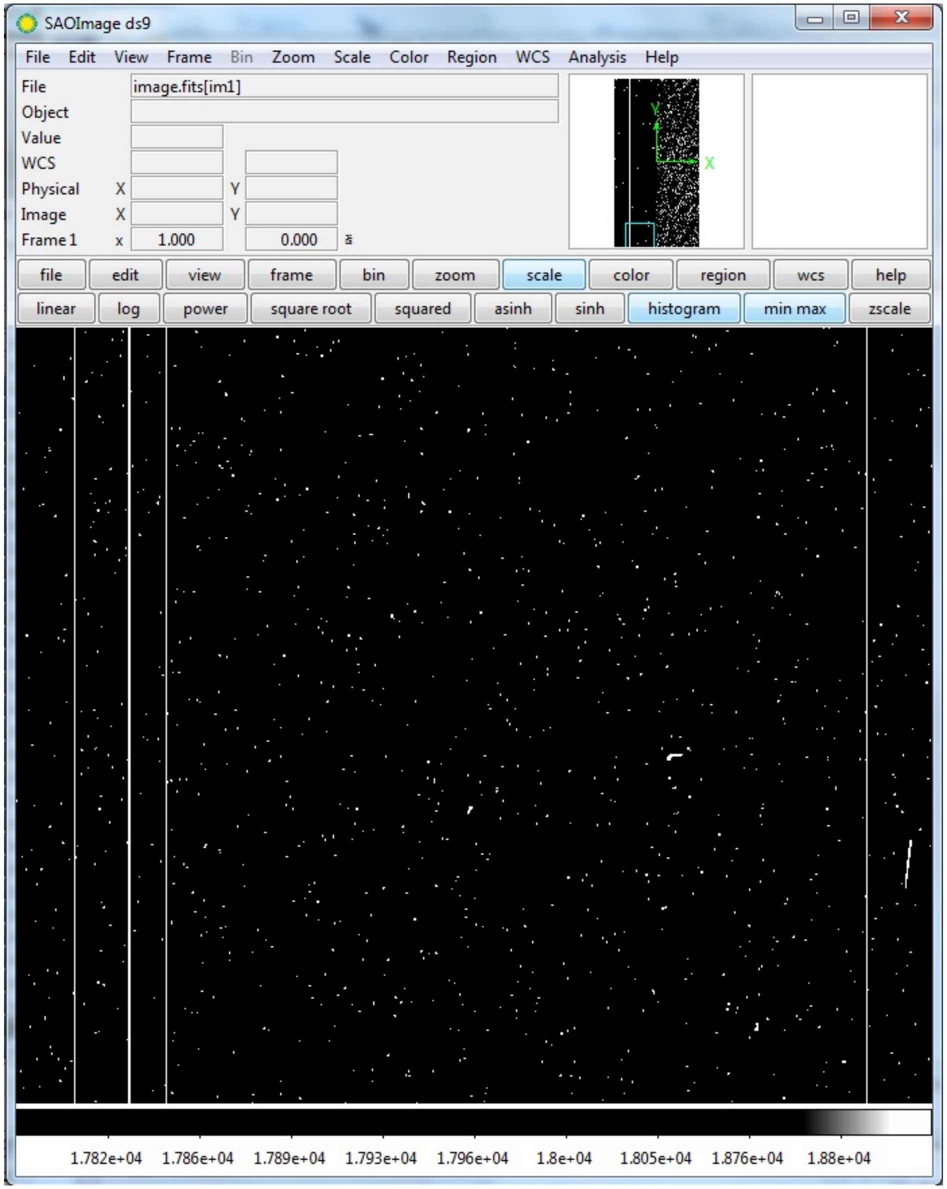
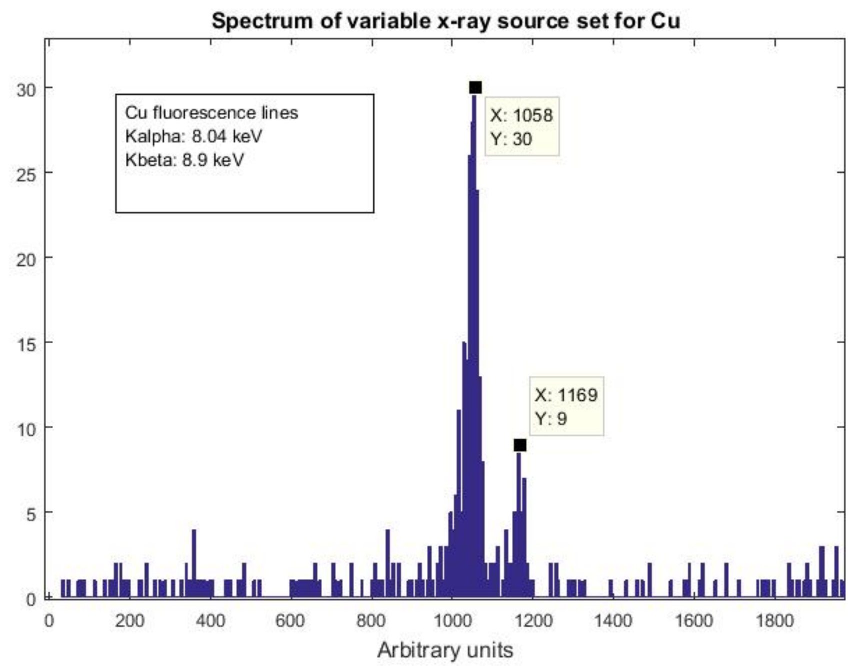


Image size depends on pixel time: 4 samples/usec

Accomplishment: Reconstructed digital images with calibration x-rays

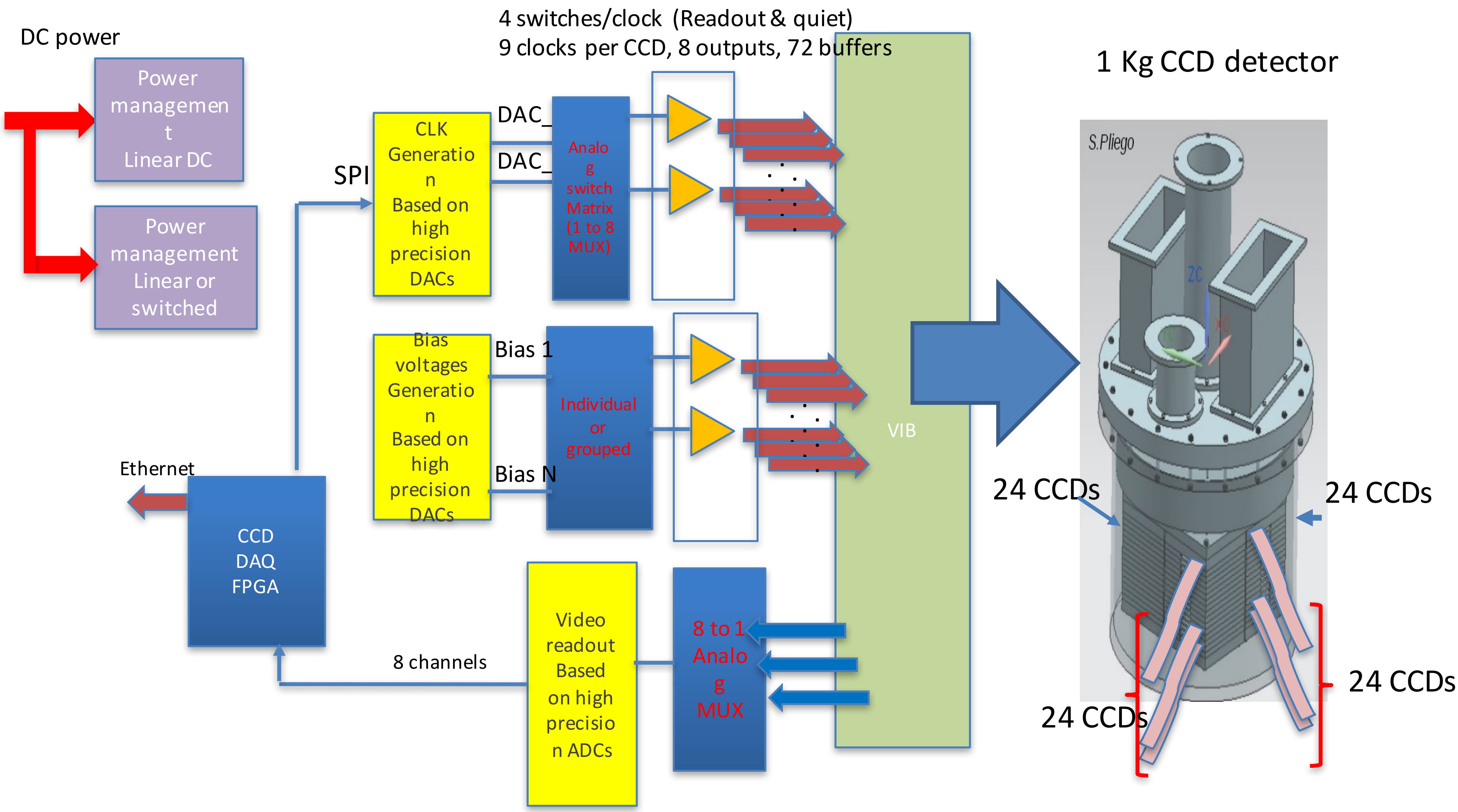


- Low noise,
- Cu fluorescence
  - Kalpha: 8.04 keV
  - Kbeta: 8.9 keV



Develop a system demonstrator for 64 channels that meets low noise requirements using the full multiplexer concept.

Low noise DAQ for n x 24 CCDs developed at Fermilab



Future Trigger & DAQ challenges

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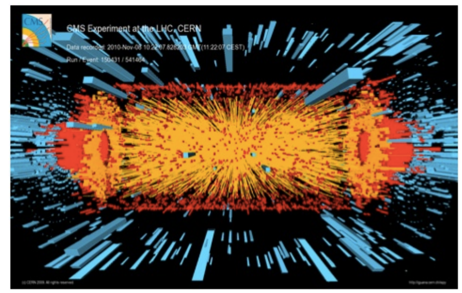
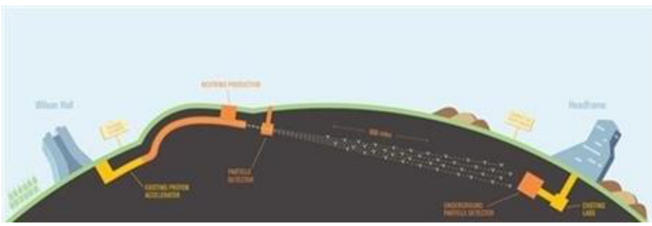
(e.g. HL-LHC and beyond)



Reliable Cryogenic readout electronics



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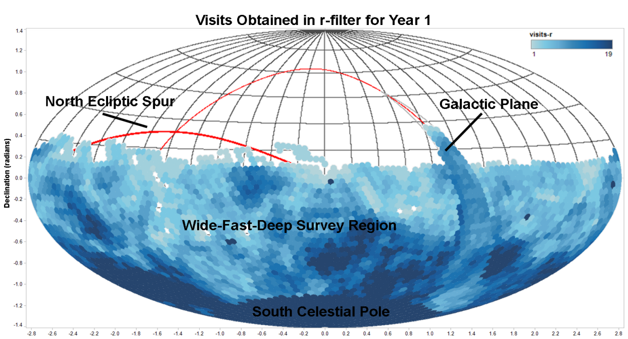

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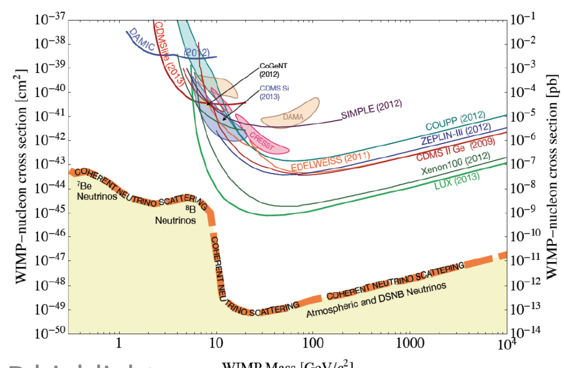
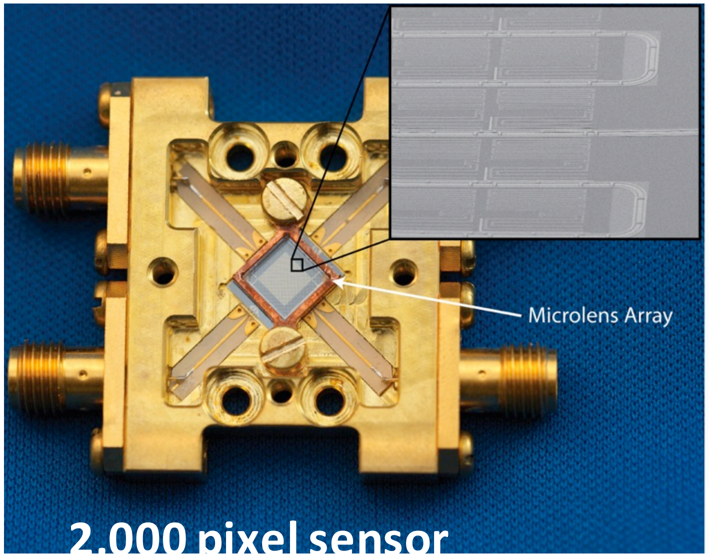
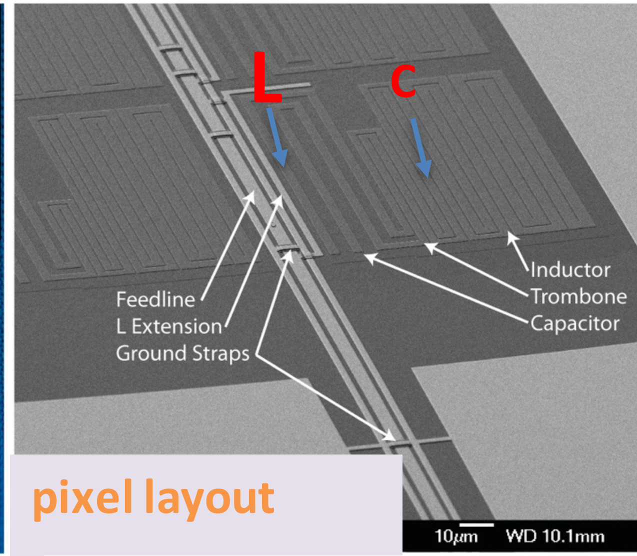
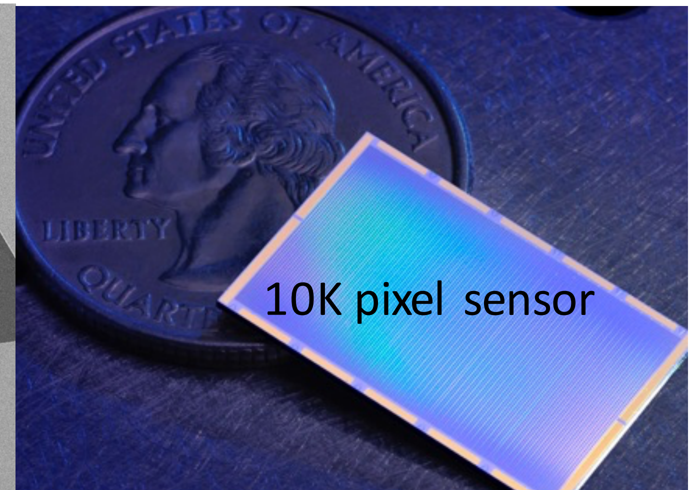


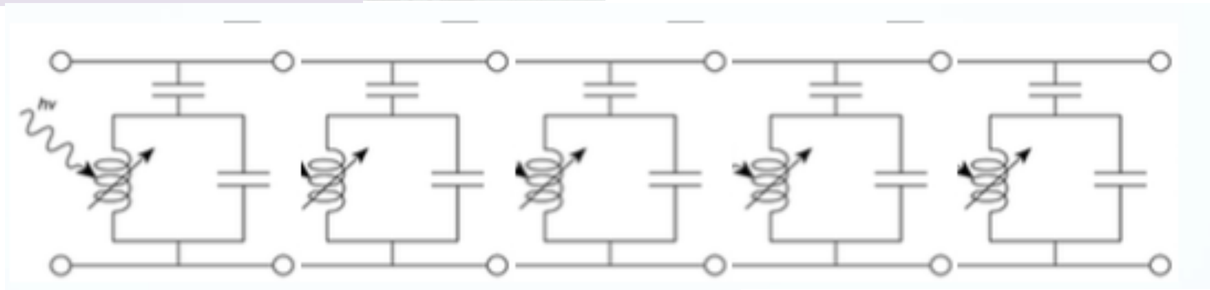
MKID: superconductor detectors for optical-NIR cosmology

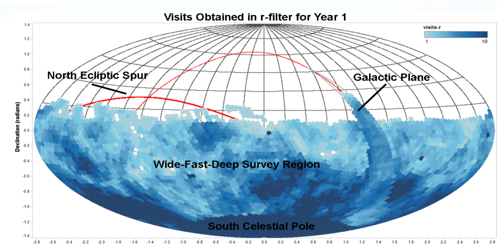






First science array





- Pixelated RF resonator array.
  - **pixels multiplexed in frequency coupled to RF feed/readout-line.**
- More than just a single photon detector:
  - **Can provide energy resolution (E/ΔE) of 80, in the visible and near infrared spectrum, and photon tagging with 1usec resolution.**
  - **Spectroscopy opportunity for >1 billion galaxies, QSO and other objects guided from DES & LSST data.**

Fermilab R&D for 10K MKID pixel DAQ

- MKID DAQ challenges:
  - Huge data throughput for a $1cm^2$ detector.
    - The MKIDs 10Kpixel detector has 5 inputs and 5 outputs and requires 80GB/s of excitation signal from the DAQ and 60GB/s is readout by the DAQ. → *~ 1 Tbps data volume for $1cm^2$*
    - 60 GB/s data is crunched down to ~100MB/s for storage.
      » *A factor of 600 info reduction within one FPGA*
    - No trigger. All data is readout & processed with photon catalog generated on the fly.
    - *Extremely faint signals, ~ 7×10^{-23} watts/Hz.*
    - Linearity and equal amplification for 10K channels in 4-8 GHz.

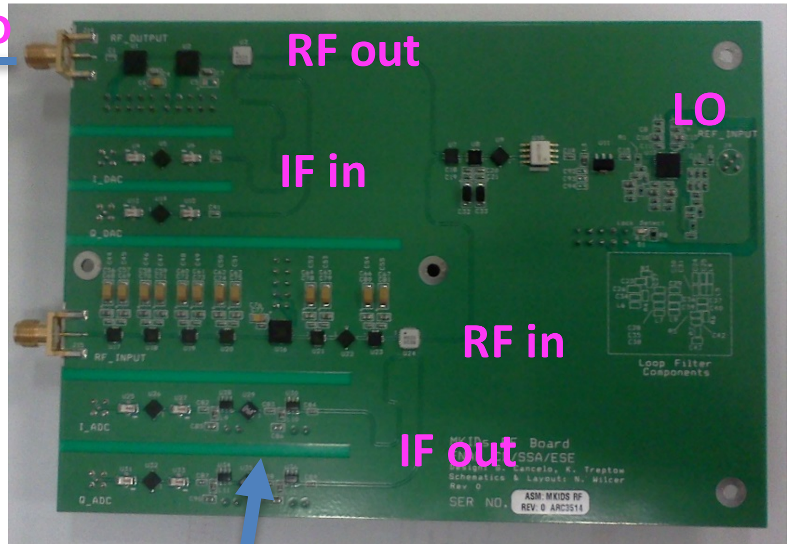
A 10K pixel DAQ from Fermilab

To MKID

Up conversion, amplification, attenuation and filtering

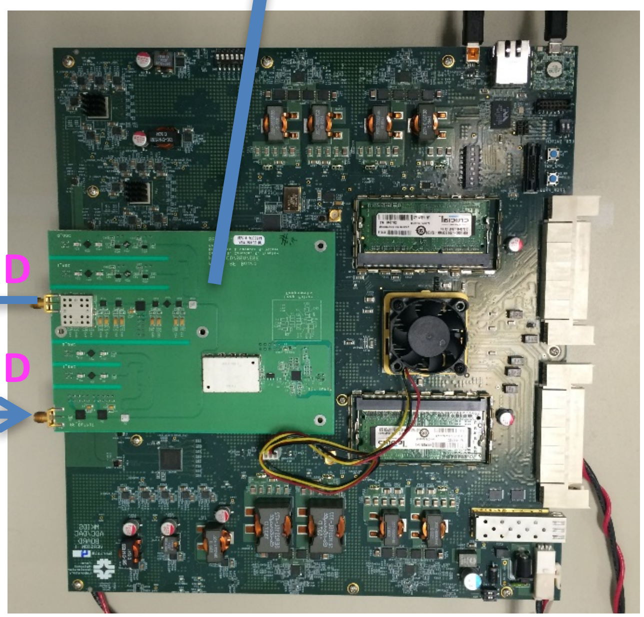
from MKID

Down conversion, amplification, attenuation and filtering

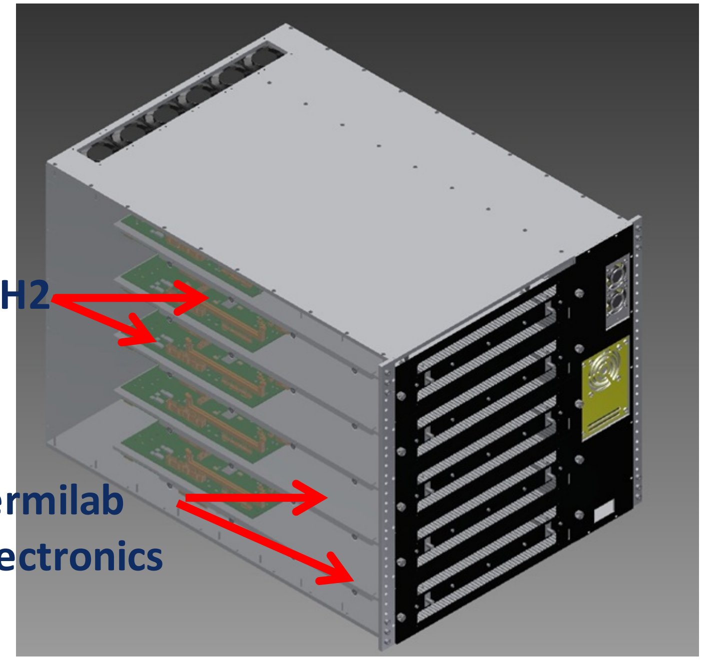


To MKID

from MKID



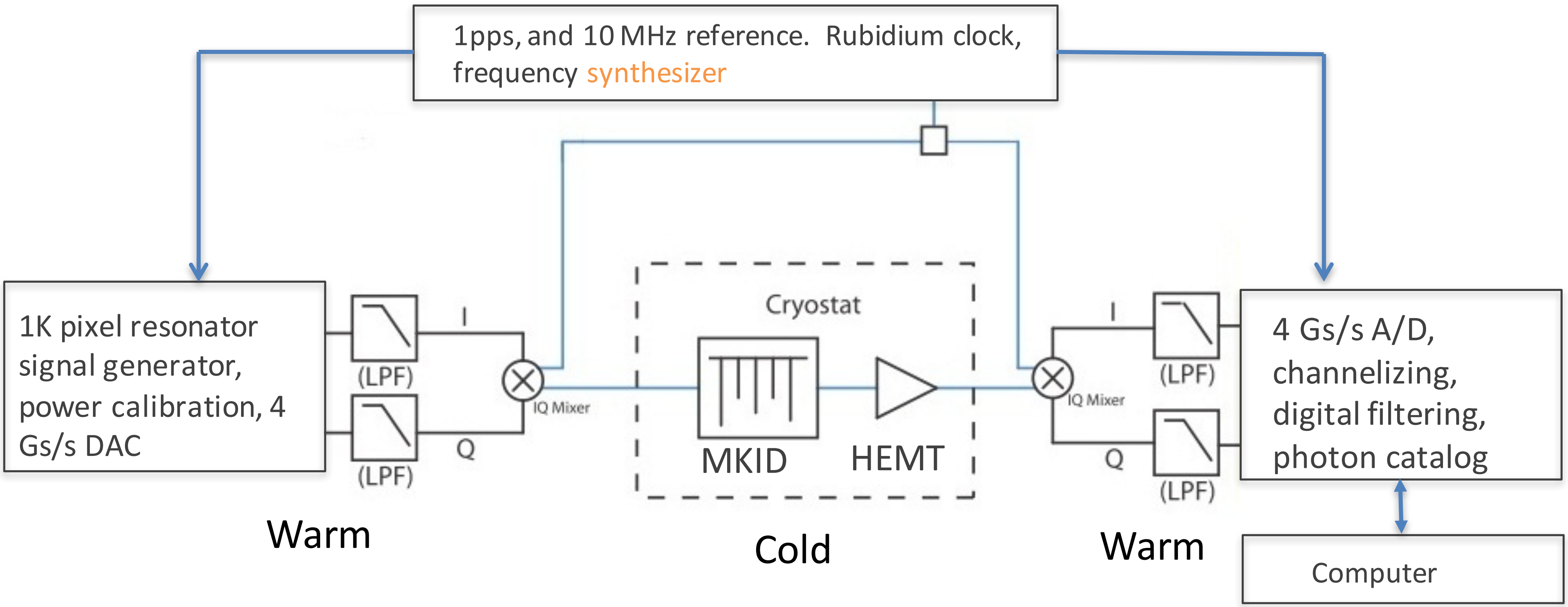
10 K pixels crate



Fermilab/UCSB collaboration.
A 10K pixel system was commissioned and saw first light at Palomar in July 2016:
Work ahead:

- Integration/calibration/commissioning of the system.
- Proof-of-principle operation of the instrument at SOAR.

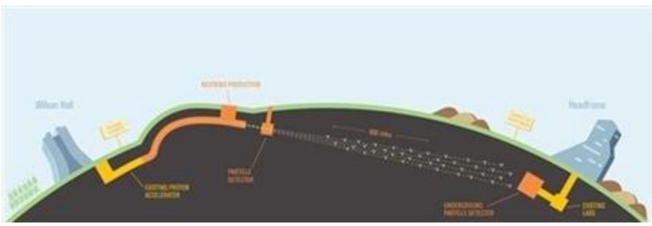
DAQ block diagram



- Each DAQ board generates signals for 1K pixels.
- Each DAQ board live streams data from 1K pixels at 1 MHz sampling per channel.
- After generation signals are up converted to RF and down converted again before sampling.
- The 1st amplifier is a HEMT at 3K with a noise temperature of 5K.

Future Trigger & DAQ challenges

Reliable Cryogenic readout electronics
(see talks on DUNE/SBN)



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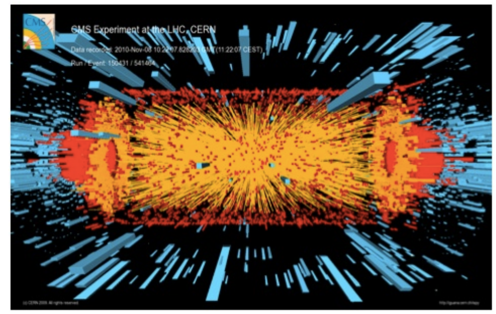

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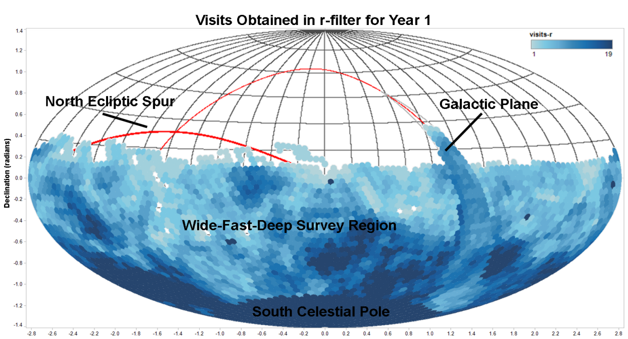

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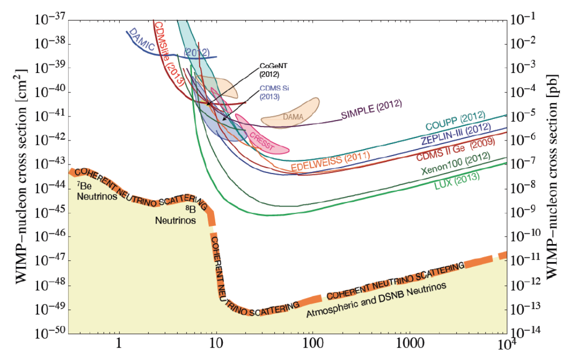
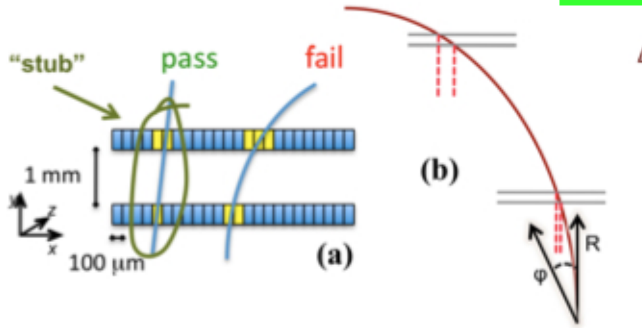


L1 Tracking Trigger challenges at HL-LHC

Detector design for triggering



Data transfer

Data formatting

Partition detector into trigger towers/sectors

Pick your favorite method:

Associative Memory Approach

Hough Transformation

tracklet

your choice here

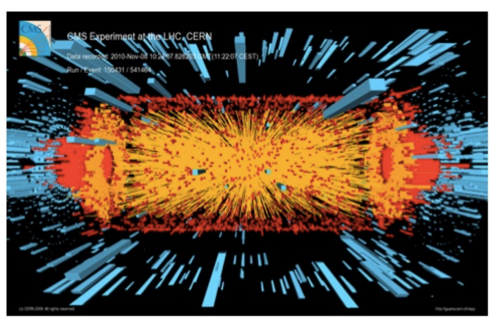
Pattern Recognition

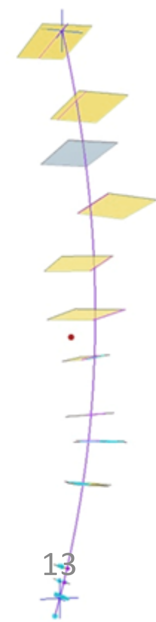
Finer pattern recognition

Track Fitting

The Full chain:

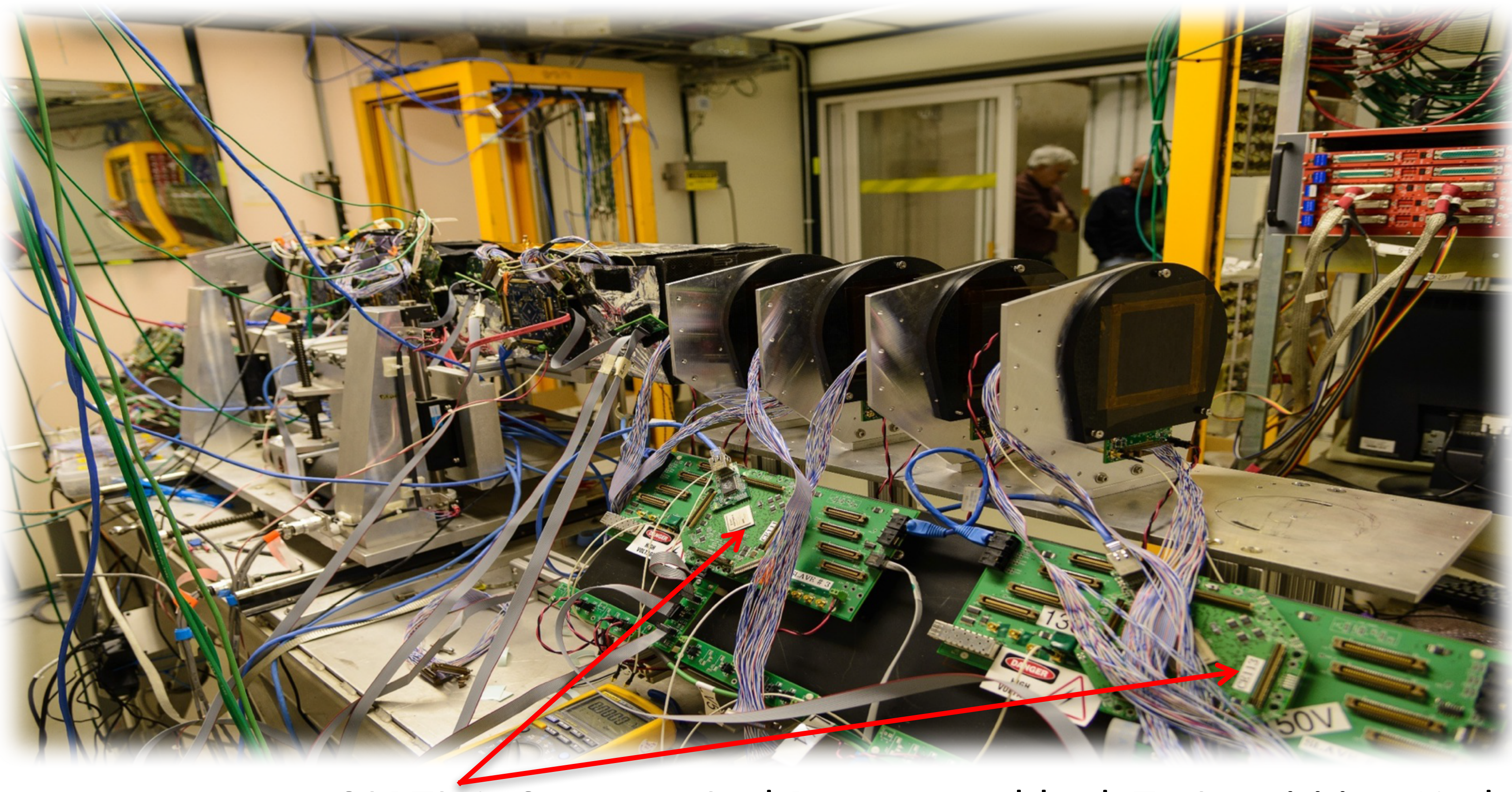
(1) Sensor/module design
(2) Data Transfer (rad hard, high bandwidth, low power link)
(3) Data Formatting
(4) Pattern Recognition
(5) Track Fitting …





Fermilab Test Beam Facility is central:

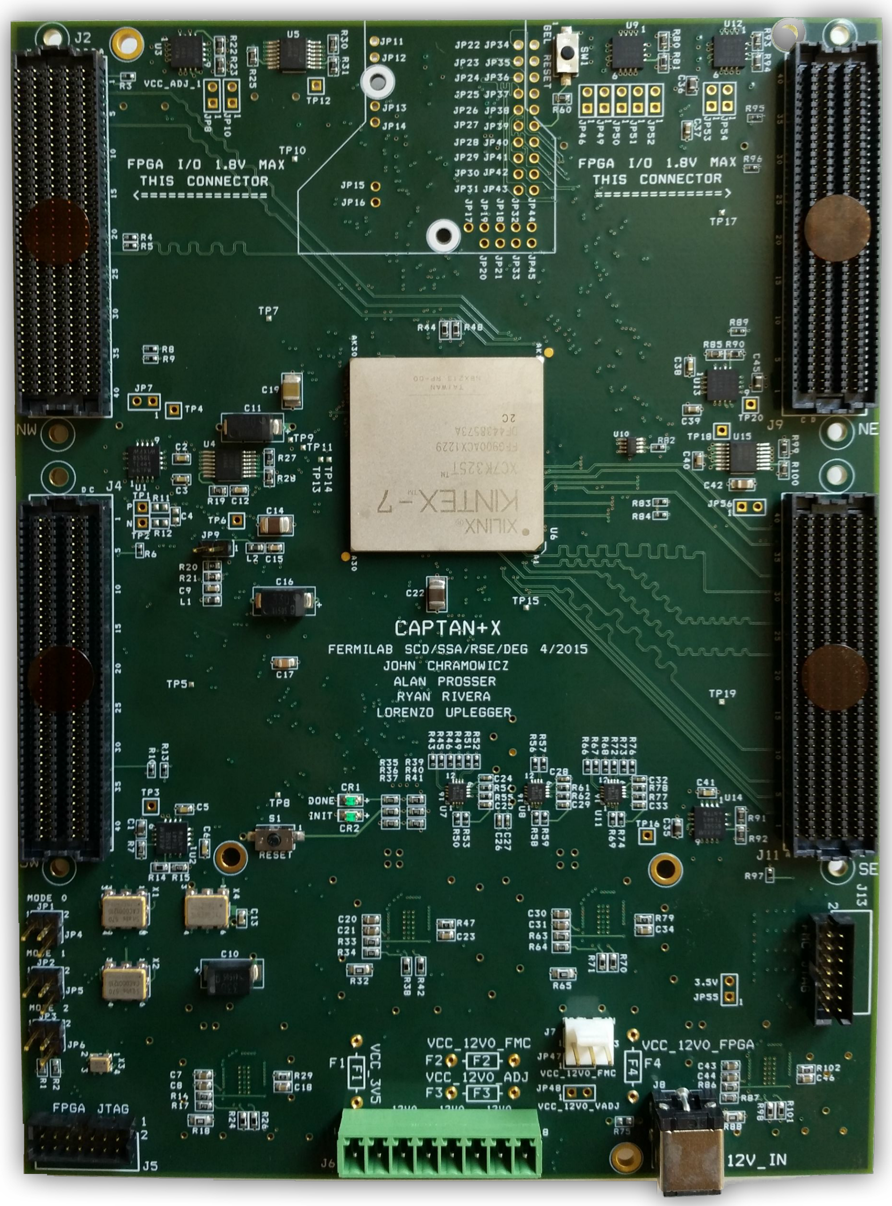
- Old pixel telescope DAQ is based on CAPTAN
    - Triggered, 2.5cm^2 coverage, and 8μm track resolution
- New strip telescope is based on CAPTAN too.
    - Dead-timeless, 16cm^2 coverage, and 5μm track resolution
- For the last 6 years CAPTAN supported all versions of the CMS pixel chip
- Recently tested the VIPIC Read Out Chip from FNAL



CAPTAN: Compact And Programmable daTa Acquisition Node

New CAPTAN+X

- CAPTAN+ ("CAPTAN plus") is the next generation CAPTAN card.
  - Based on Xilinx 7 series.
- **Features:**
  - Gigabit Ethernet
  - 4 FMC connectors, 16 Links
  - 400 GPIO



Next Steps in DAQ Support

- For DAQ systems:
  - Proceed with "Off-the-Shelf" DAQ concept
  - Demonstrate the feasibility of low-cost, high-bandwidth, commercial approach to data acquisition based on standard networking technology.
  - Support a library of software, firmware open source code for a small representative menu of hardware.
  - Effort will leverage CAPTAN, *artdaq* software, and test beam experience.

Detector design for triggering

L1 Tracking Trigger challenges at HL-LHC

Partition detector into trigger towers/sectors

Data transfer

Pick your favorite method:

Associative Memory Approach

Hough Transformation

tracklet-based

your choice here…

Data formatting

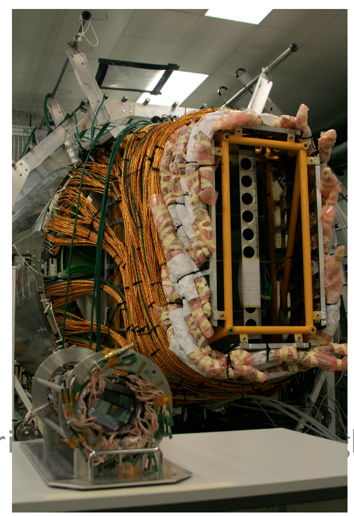
The Full Chain:

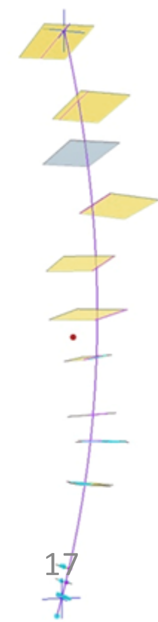
Pattern Recognition

Finer pattern recognition

(1) Data Reduction at detector/sensor stage
(2) Data Transfer (rad hard, high bandwidth, low power link)
(3) Data Formatting
(4) Pattern Recognition
(5) Track Fitting …

Track Fitting

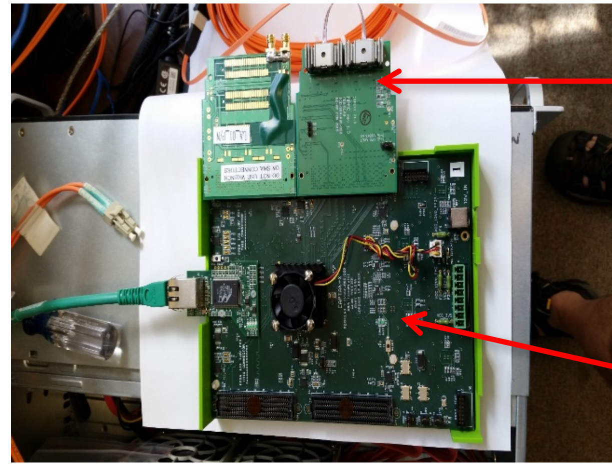




Versatile Link Plus Common Project (HL-LHC)

Collaborating Institutions

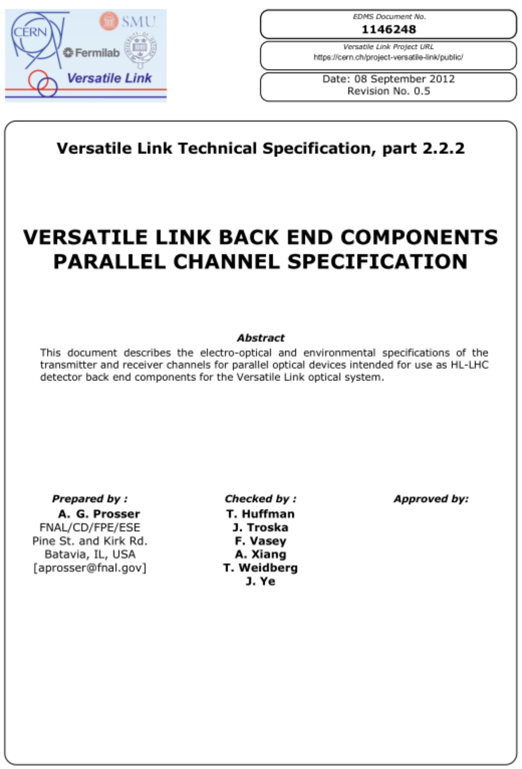
Southern Methodist University
  10 Gbps VCSEL Array Driver ASICs
CERN
  Opto Die, Modules, Passives
Fermilab
  Back End Components, System Spec and Test
Oxford University
  Opto Module Reliability



MicroPod FMC Card (100 Gbps bidirectional)

CAPTAN+x

Project Specifications Documentation



EDMS Document No.
1146248
Versatile Link Project URL
https://cern.ch/project-versatile-link/public/
Date: 08 September 2012
Revision No. 0.5

Versatile Link Technical Specification, part 2.2.2

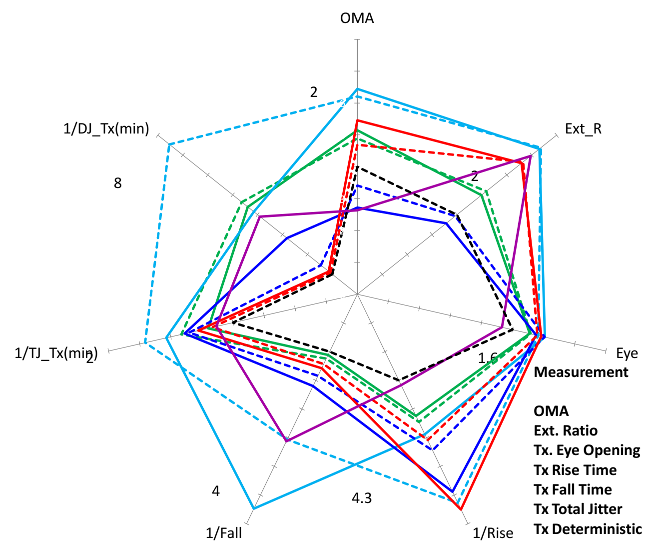
VERSATILE LINK BACK END COMPONENTS PARALLEL CHANNEL SPECIFICATION

Abstract

This document describes the electro-optical and environmental specifications of the transmitter and receiver channels for parallel optical devices intended for use as HL-LHC detector back end components for the Versatile Link optical system.

Prepared by :	*Checked by :*	*Approved by:*
A. G. Prosser FNAL/CD/FPE/ESE Pine St. and Kirk Rd. Batavia, IL, USA [aprosser@fnal.gov]	T. Huffman J. Troska F. Vasey A. Xiang T. Weidberg J. Ye	

Parallel Optics Transmitter Radar Plot

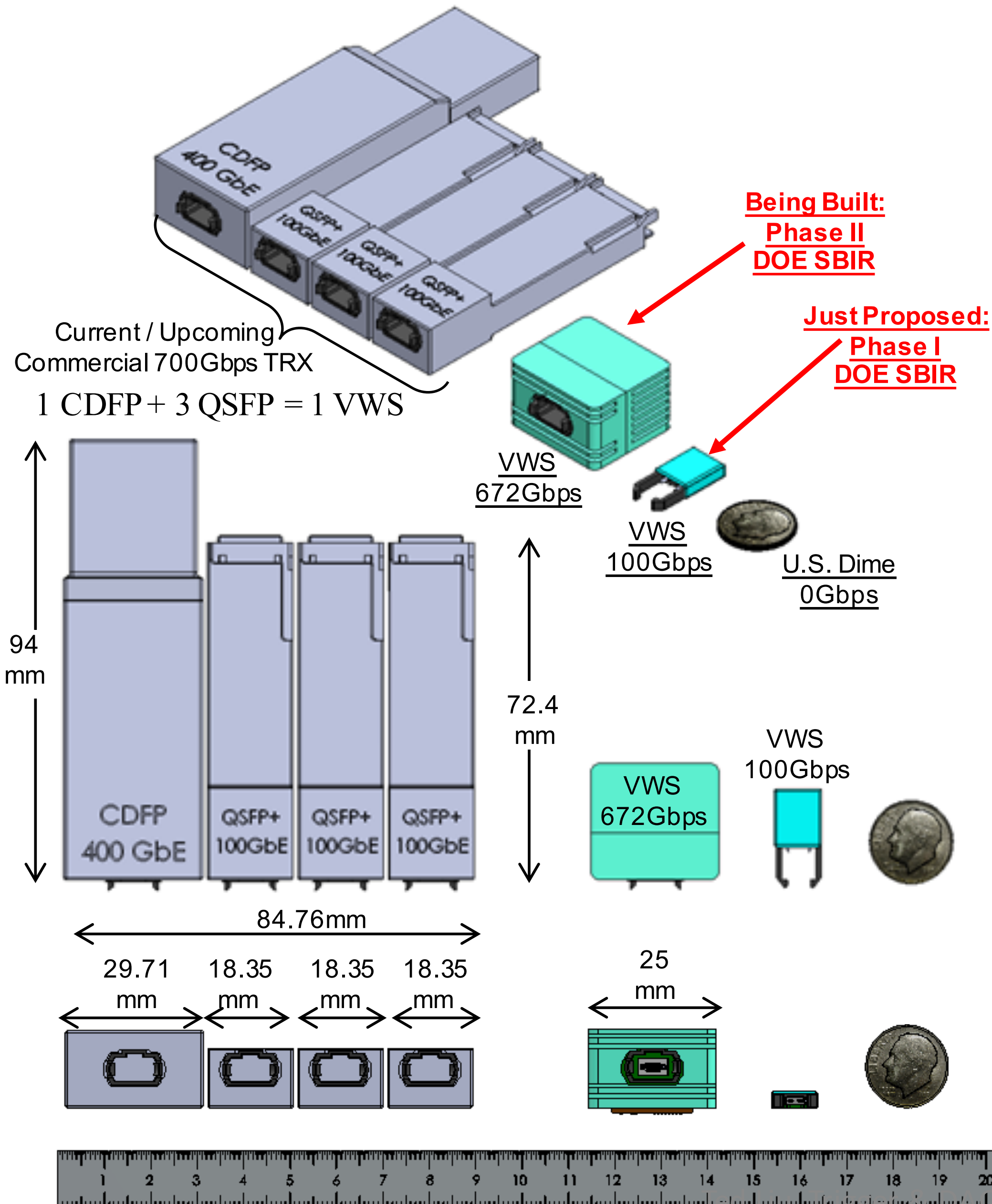


Measurement	Norm
OMA	-1.6 dBm*
Ext. Ratio	3.0 dB
Tx. Eye Opening	60% of OMA
Tx Rise Time	70 ps
Tx Fall Time	70 ps
Tx Total Jitter	0.25 of UI
Tx Deterministic Jitter	0.12 of UI

*Tracker Grade Spec

Performance Measurements/Comparative Analysis

Vega Wave Systems, Inc. Work with Fermilab (via SBIR): Increasing Bandwidth in Smaller Volume



- Vega Wave Systems, Inc. has been working with Fermilab to make high-bandwidth, rad-hard optical links for HEP.
- We have increased bandwidth/volume ratio by a factor of >20x. This is at least 4-5 years ahead of current commercial markets.
- This innovation is driven by Fermilab's input and has or will result in many new patents in high-speed optical links and advanced 3D integrated circuit packaging.
- Currently funded under Phase II SBIR.
- 5 new SBIR proposals submitted to continue variations and elements of this work.
- Current Program: Optical transceiver
  - >10X more bandwidth/volume than current market solutions
  - 48 channels – Terabit class
  - Platform Technology
  - Designed for low-cost manufacturing
- Proposed Program:
  - >2x additional reduction in bandwidth/volume

Detector design for triggering

AM + FPGA based Tracking Trigger

Data transfer

~ 100Tbps

Data formatting

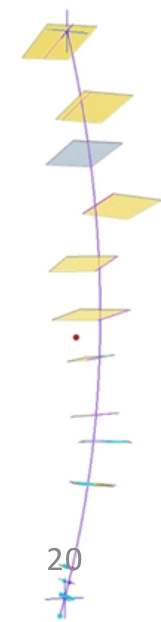
Partition detector into trigger towers/sectors

Associative Memory

Pattern Recognition — AM

Finer pattern recognition

Track Fitting — FPGA



- *Full Chain:*

(1) Data Reduction at detector/sensor stage
(2) Data Transfer (rad hard, high bandwidth, low power link)
(3) Data Formatting
(4) Pattern Recognition
(5) Track Fitting …

} Tracking Trigger

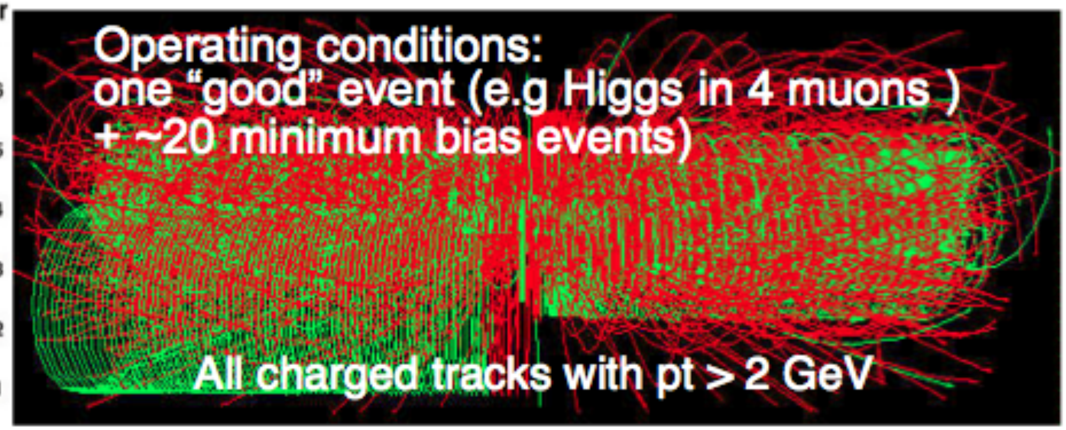
Core R&D for AM + FPGA approach:
High performance Data Delivery
High performance Pattern Recognition (ASIC) and Track Fitting

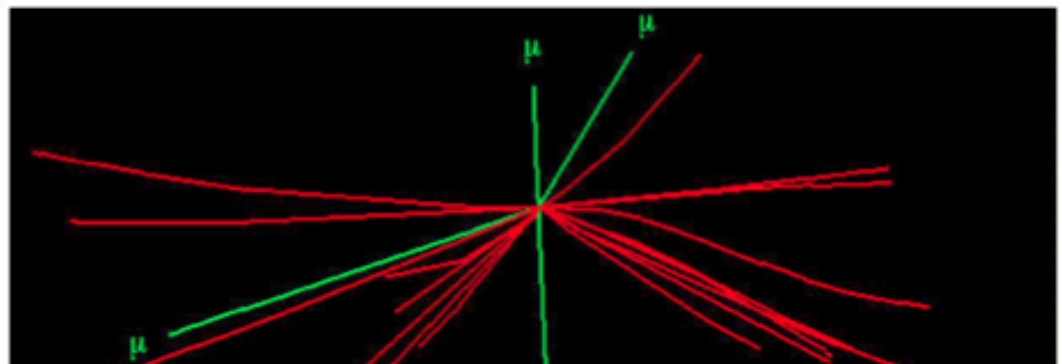
CMS L1 Tracking Trigger:

Will need to reconstruct charged particle trajectories "on-the-fly" for every beam crossing (25 ns, or 40 Million beam crossings per second), from an ocean of input data (bandwidth required to transfer up to ~ 100Tb/s)

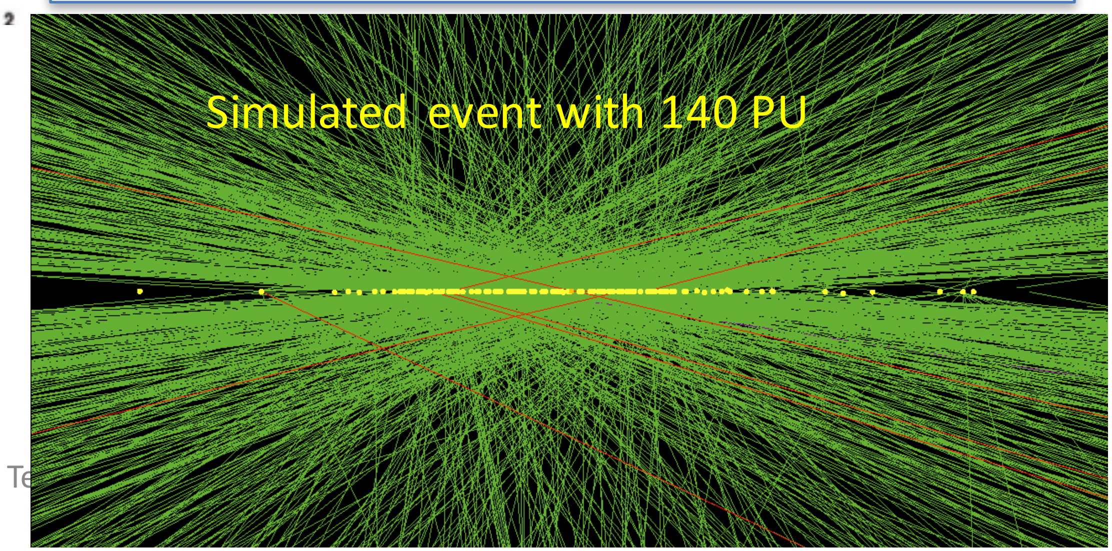
This requires extremely fast high bandwidth data communication as well as massive pattern recognition power.
AM approach requires millions known patterns to be compared against the multiple input data streams simultaneously and perform track fitting with near zero latency (~ few μs total)
This is challenging!

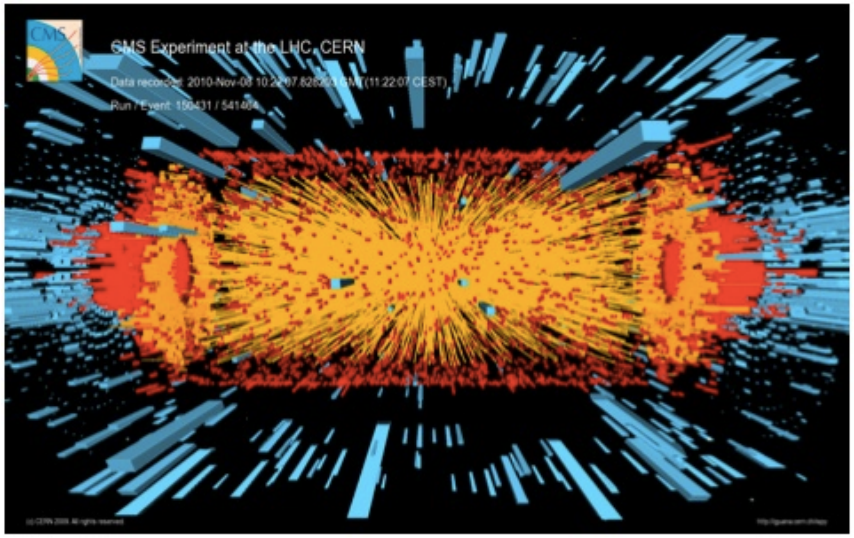
Pileup at HL-HC: ~ 200 (only 20 shown here)



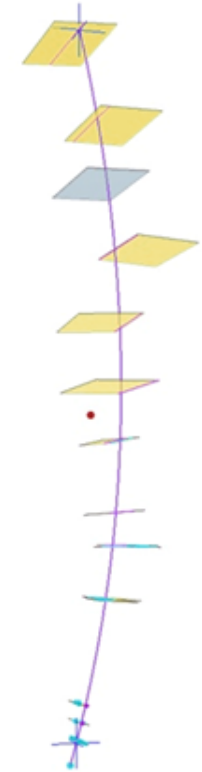


Impact of track reconstruction at L1

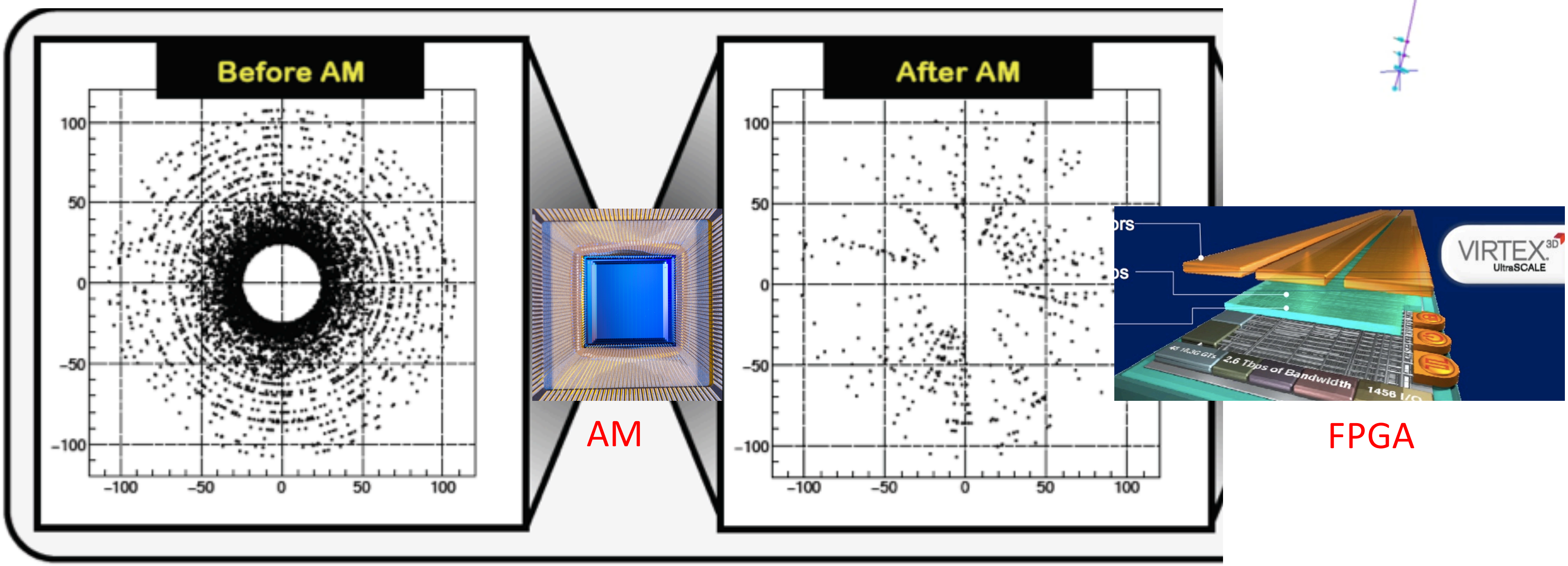




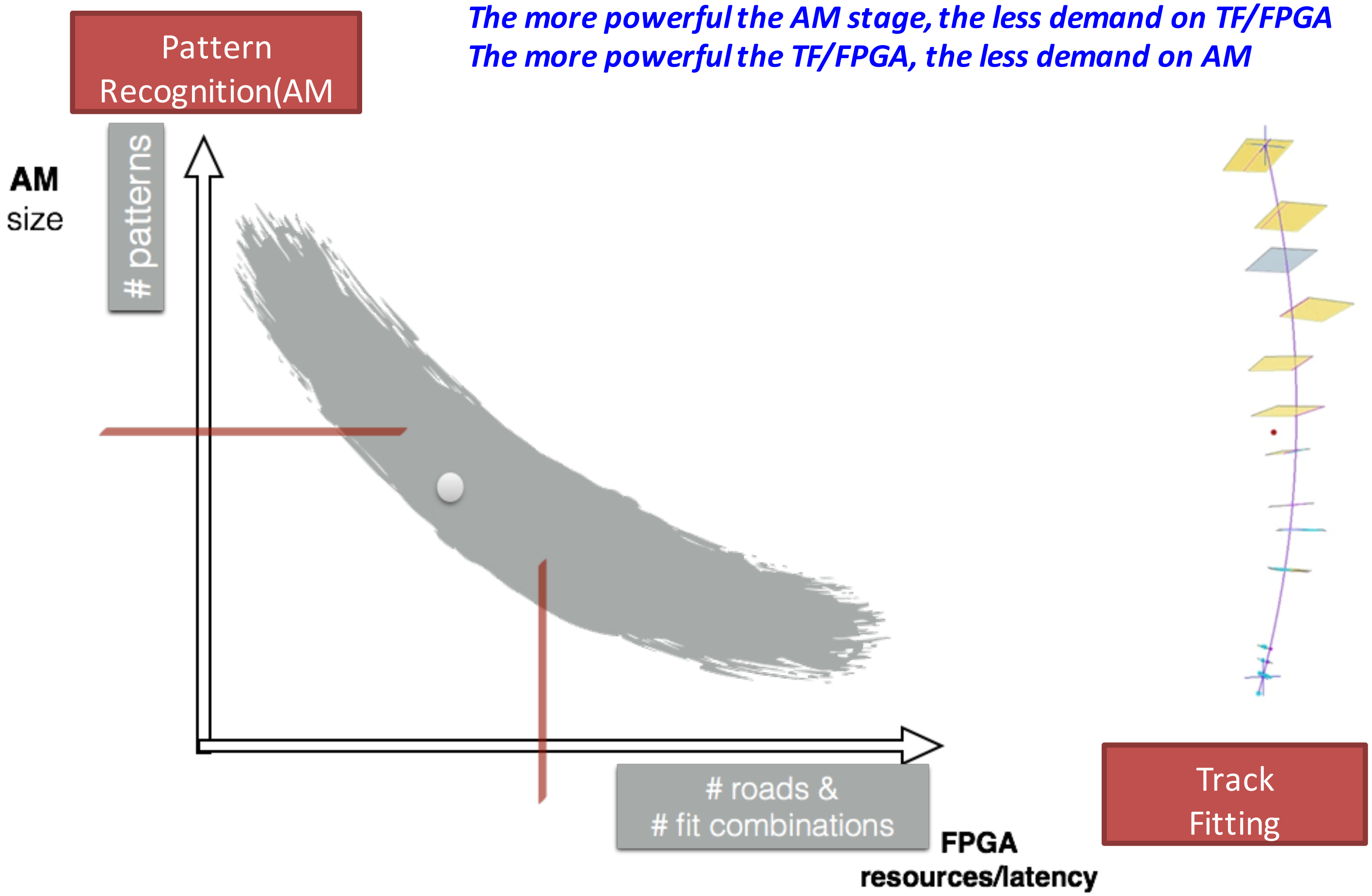
AM + FPGA



- Data delivery into AM
- Pattern Recognition (AM+FPGA)
- Track Fitting (FPGA)



The more powerful the AM stage, the less demand on TF/FPGA
The more powerful the TF/FPGA, the less demand on AM

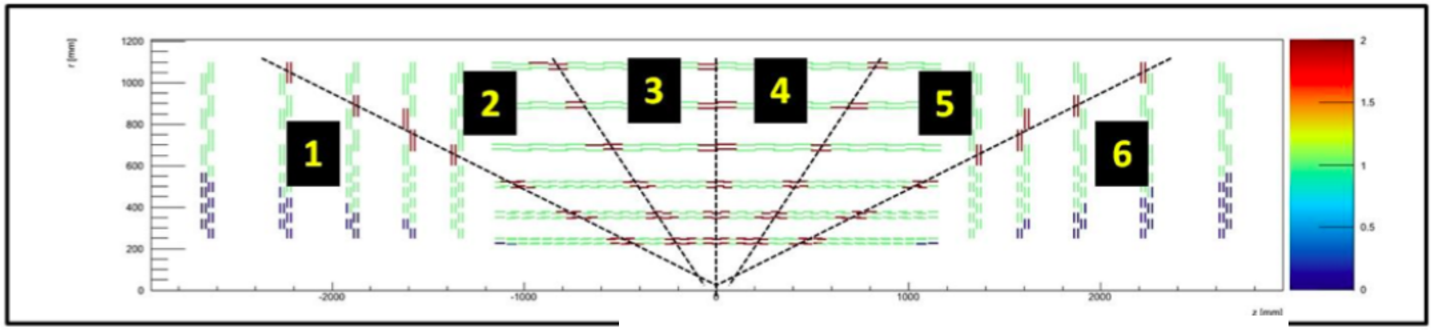


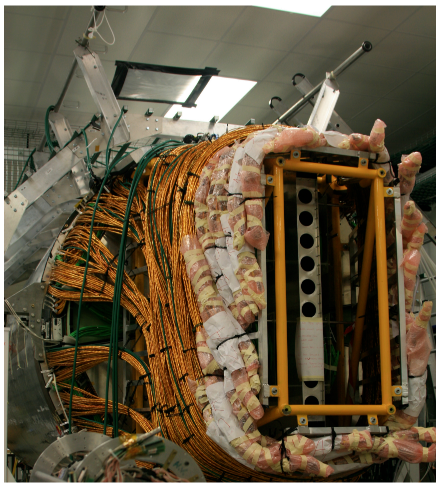
A good working point: as a compromise between the size of the AM and the number of roads and fits to perform per beam crossing

Extensive simulation work has been done

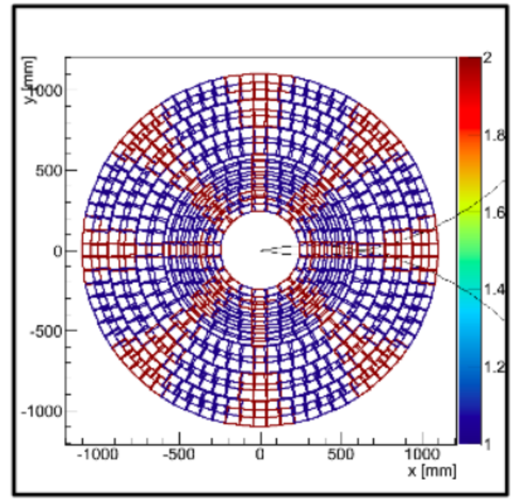
Use regional multiplexing => divide the detector into 6x8=48 trigger towers

6 regions in η





8 regions in r-phi



~15k modules/fibers ~ 100Tbps

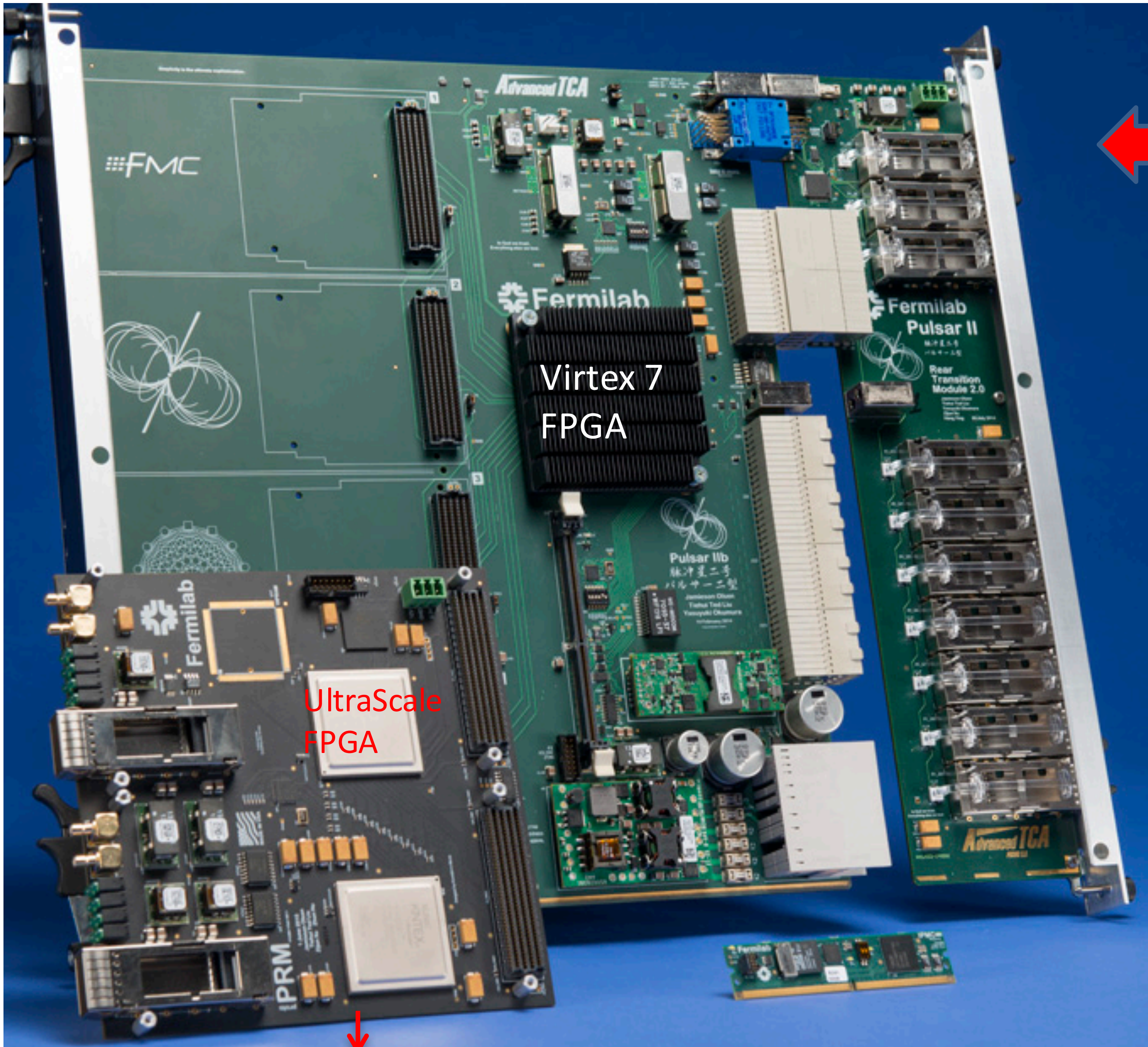
The need for divide and conquer

Divide and Conquer approach

AM+FPGA System Architecture

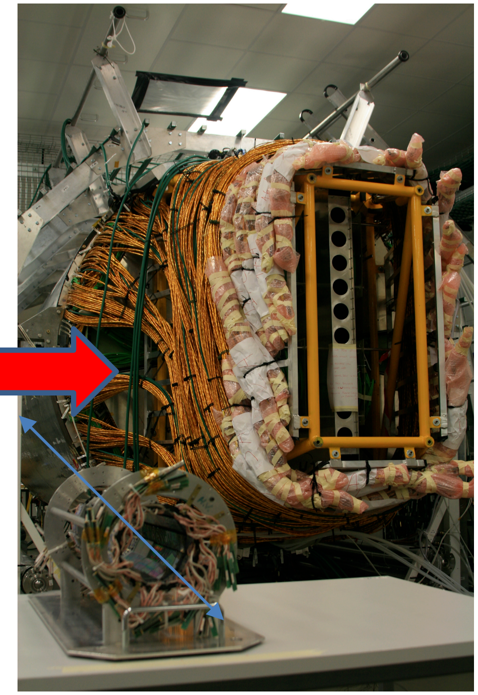
In space: 6 (eta) x 8 (phi) = 48 trigger tower
In time: time multiplexing

ATCA Pulsar 2b: Total ~ 1Tbps I/O capability for data delivery

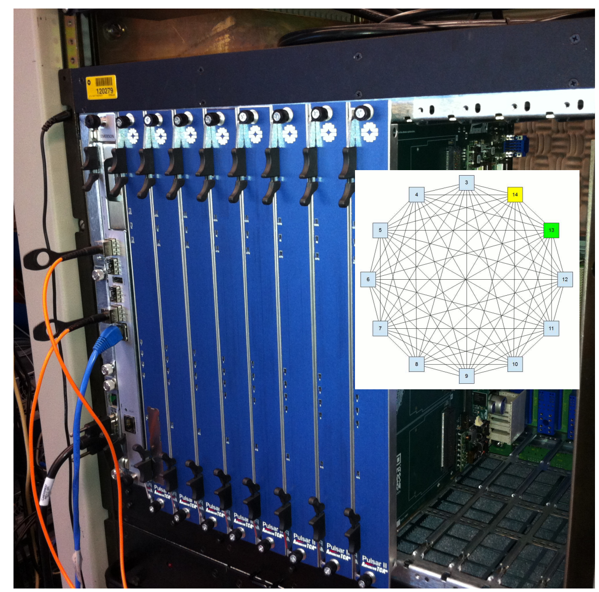


Pattern recognition mezzanine

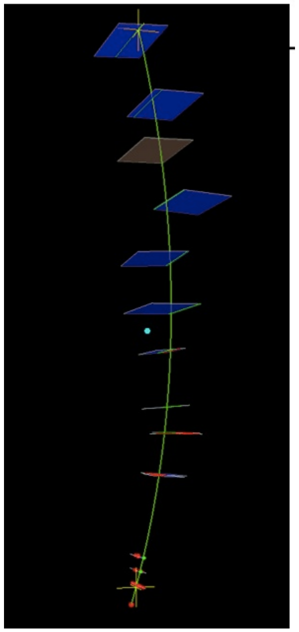
RTM:
400Gbps

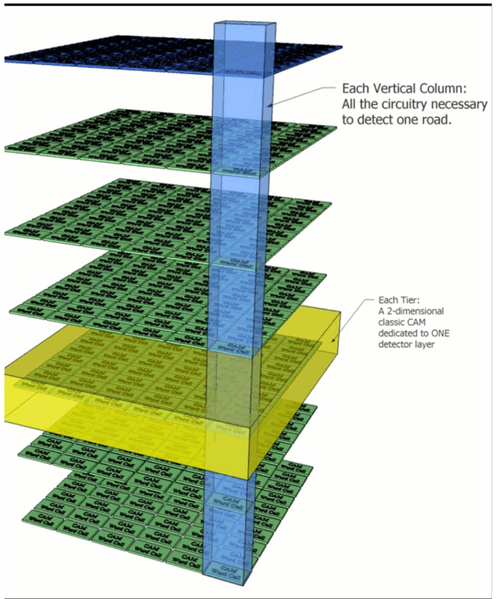


Full-mesh (40G+):



FNAL VIPRAM R&D Status Summary





The past: with steady progress

Initial Idea: ~2010

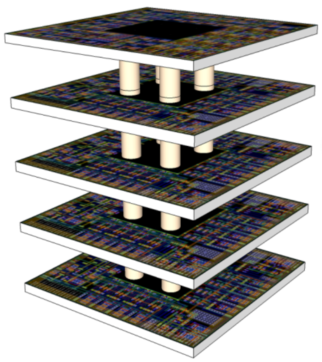
VIPRAM concept paper: 2011

CDRD award: 2012

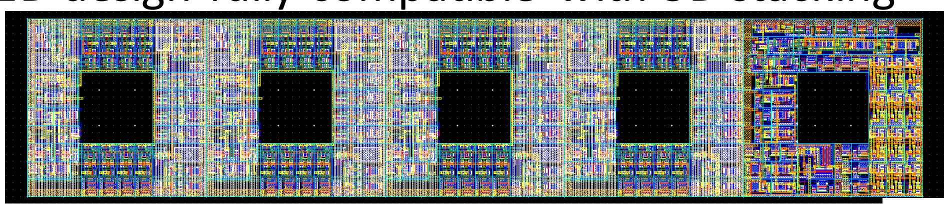
First pure 2D Design submission: 2013

First ProtoVIPRAM00 chip successfully tested: 2014

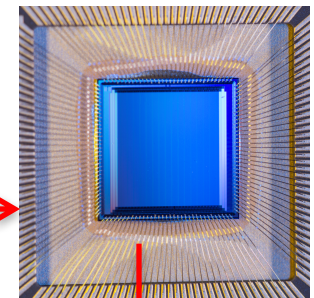
→ ***Design building blocks are ready for 3D stacking***

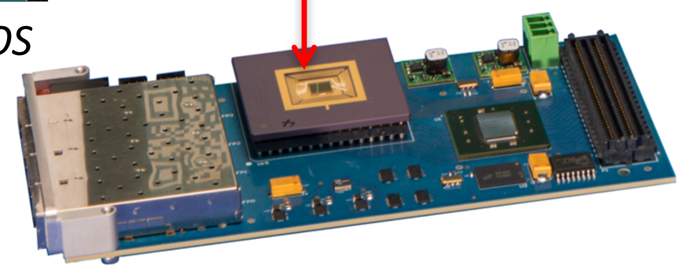


2D design fully compatible with 3D stacking



CAM cell size: 25 um x 25 um, @ 130nm GF CMOS





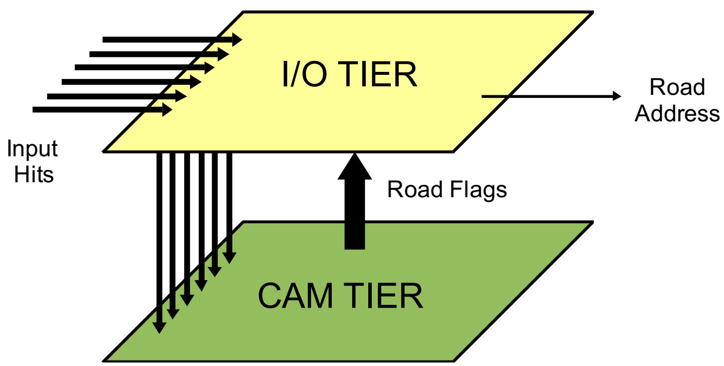
The generic 3D multi-tier design (protoVIPRAM01)

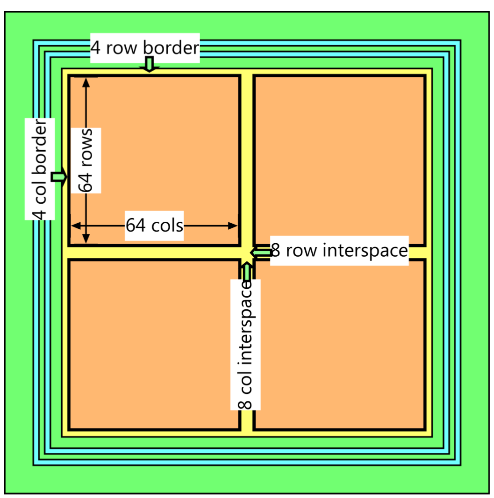
The 2-tier design for CMS L1 tracking trigger (protoVIPRAM02)

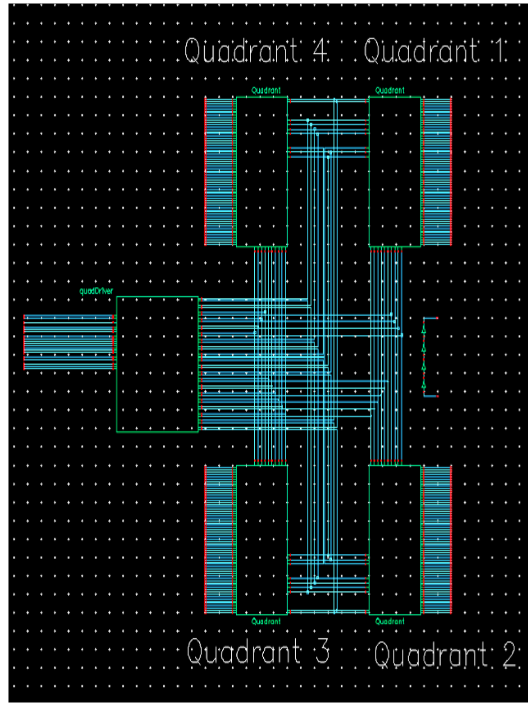
Both designs submitted in 2016, expect chips for testing early 2017

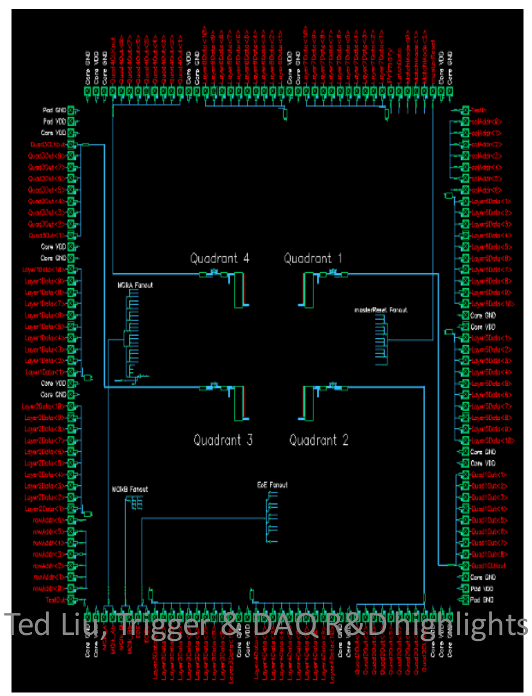
The L1CMS "CAM Tier and I/O Tier" Schematic and Layout

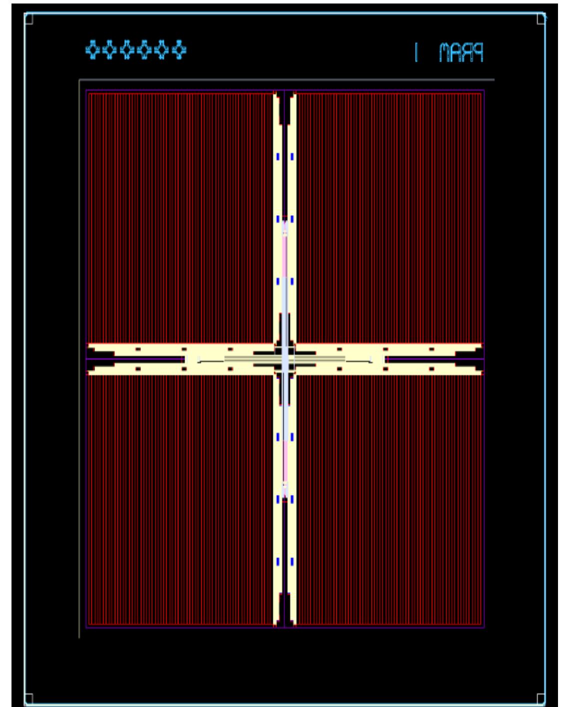
submitted in 2016

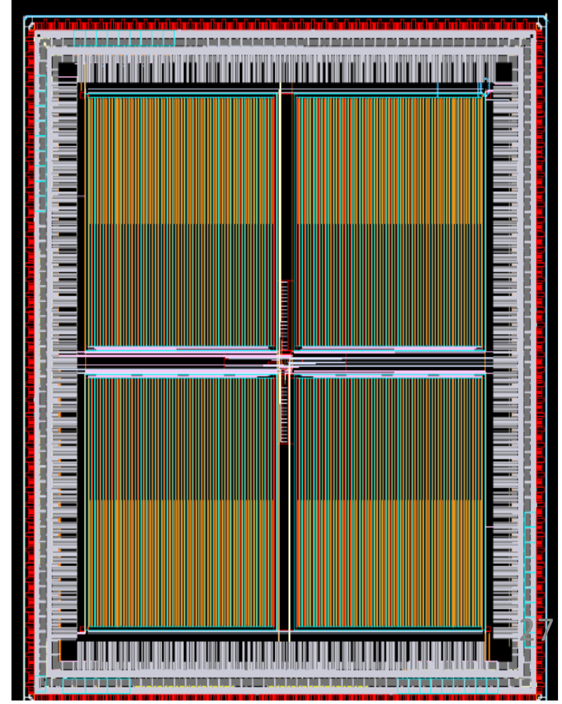






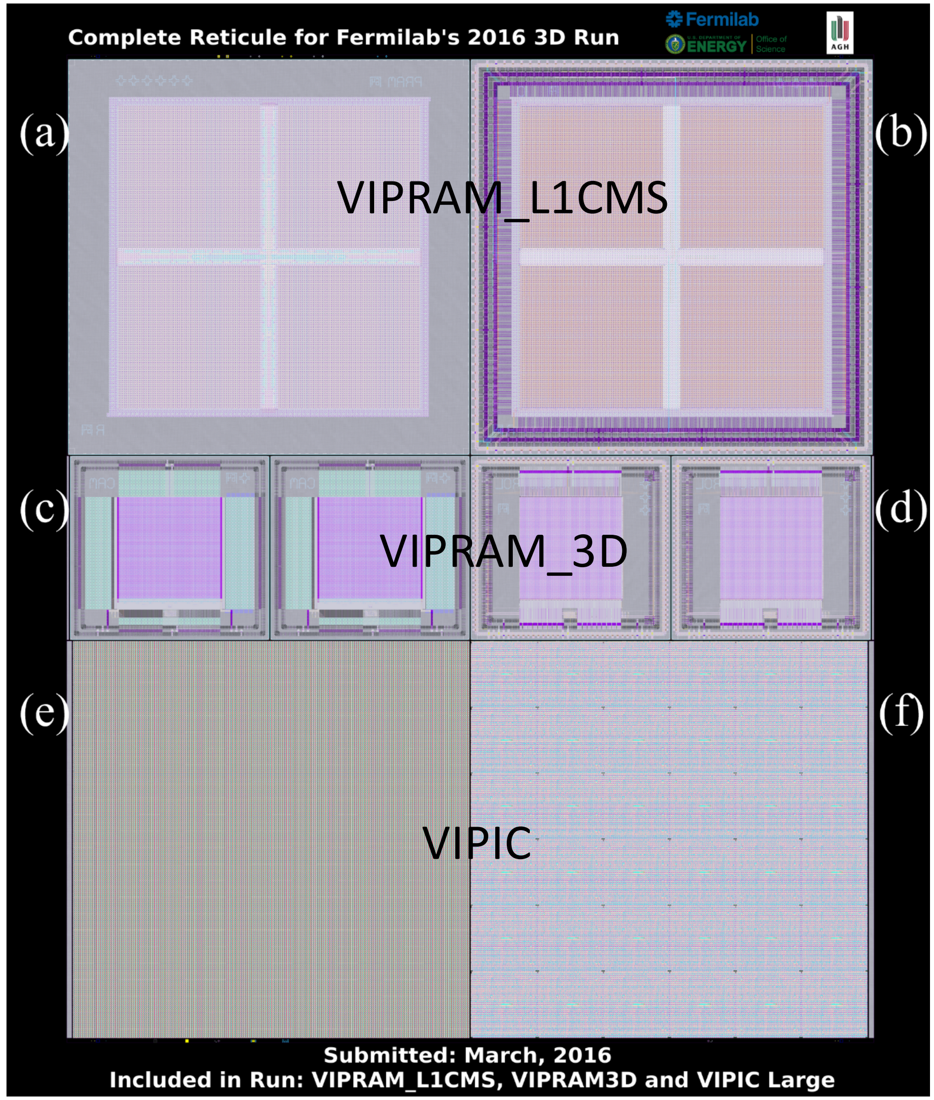






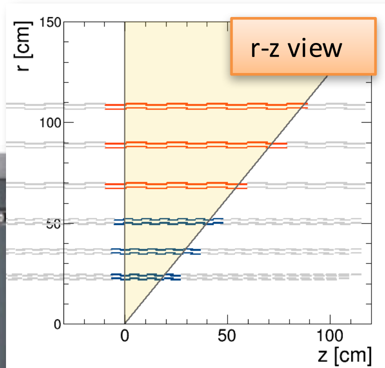
The 2016 3D MPW Reticule

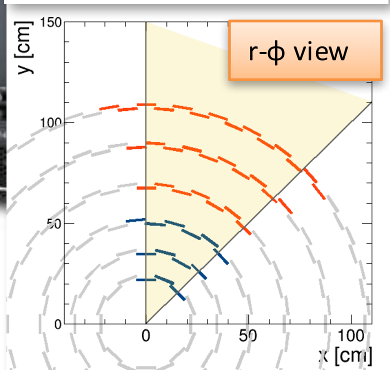
- The reticule was submitted for fabrication in March of 2016.
- The wafers were returned from Global Foundries in August of 2016.
- The wafers have been cored for 3D processing, and have been sent to Novati for further 3D processing.
- Expect VIPRAM_L1CMS chips for testing early 2017 (also first 2-tier VIPRAM_3D chips)



Demonstration data flow (single trigger tower)

Data sourcing using Pulsar 2b





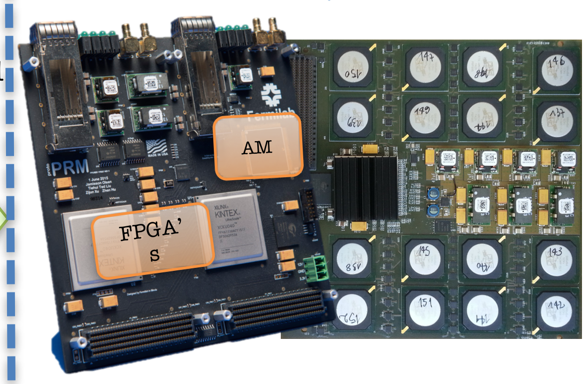
stubs from modules

Data processing using Pulsar 2b + PRM

~400 modules involved

formatted stubs

PRM



Now all relevant data arrived at the door of PRM. Next is pattern recognition (AM) and track fitting stage…

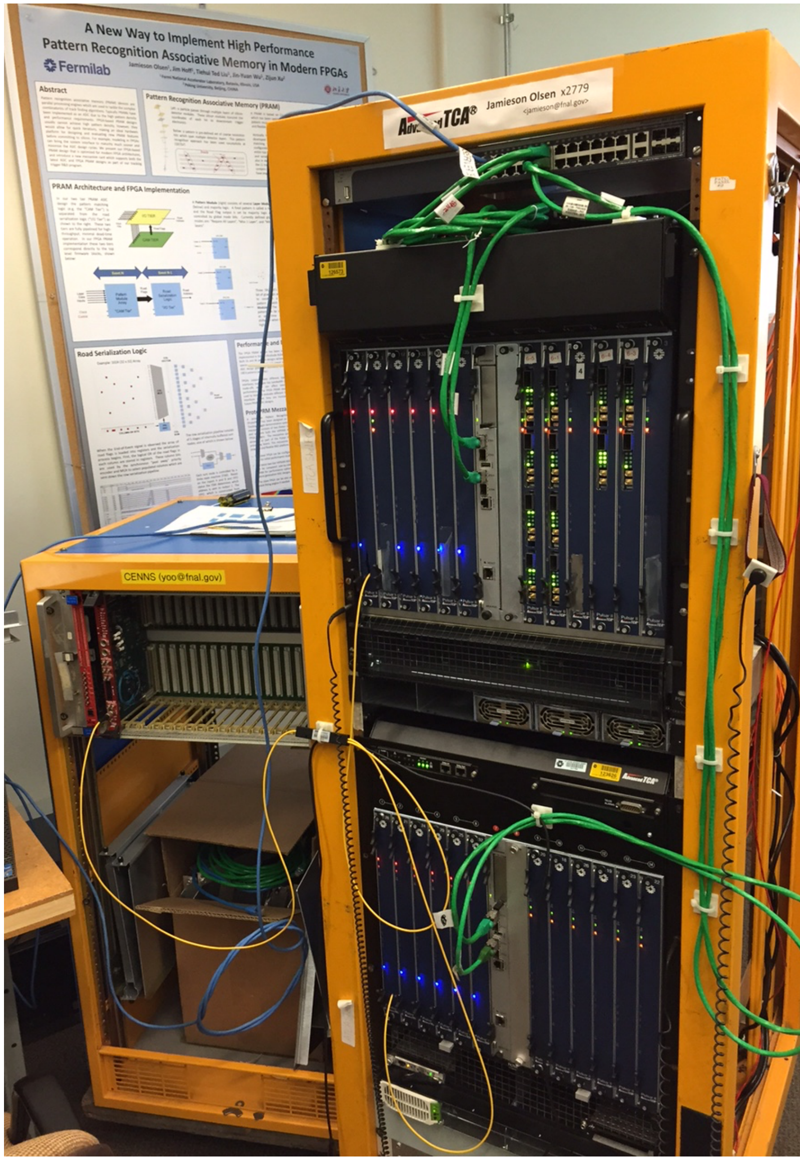
Data delivery latency: < 2 us

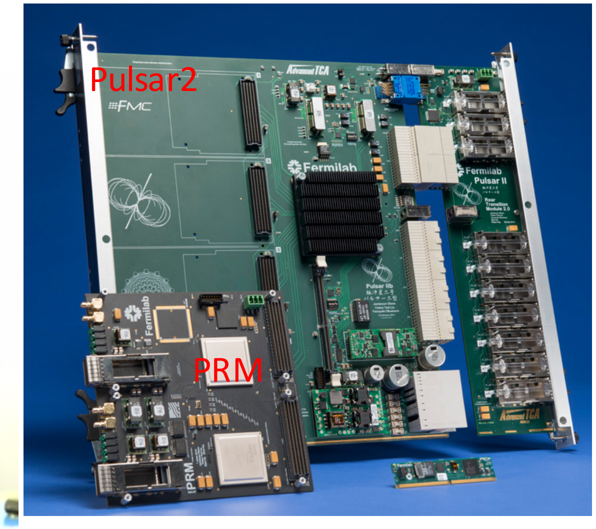
Data delivery stage

PR+TF < 2 us

PR + TF stage

CMS L1 Tracking Trigger System Demonstration at FNAL/LPC





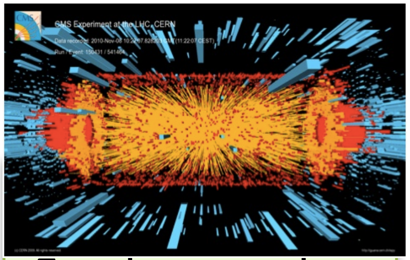
One shelf contains Pulsar 2
Data Source Boards (DSB)
Emulating ~400 detector modules (one trigger tower)

One shelf contains Pulsar2 as
Pattern Recognition Boards (PRB)

Each PRB hosts two
Pattern Recognition Mezzanines (PRM)

VIPRAM_L1CMS emulated in FPGA

Close collaboration among: FNAL, Northwestern, Florida, Texas A&M, SPRACE(Brazil) and Peking



What we have learned so far

Emulate tracker output using HL-LHC simulation data

The latency target is ~ 4 micro-seconds

Based on what we have done so far: simulation+hardware+firmware

That target is in sight …

Processing Latency Δ t

Goal: ~4 μs

Data formatting /delivery — ~ 1.7μs

Pattern Recognition (PR) — ~ few x 100ns (overhead+roads)

Track Fitting — ~ < 1 μs (one engine)

Tracks out

Δt1

Δt2

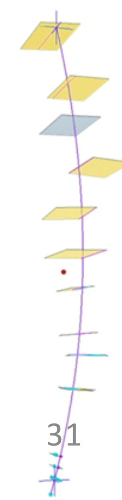
Δt3

performance

cost

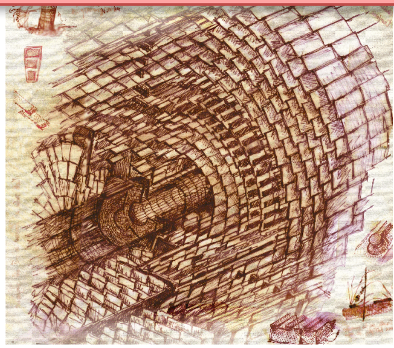
latency

(system/board/chip) design optimization

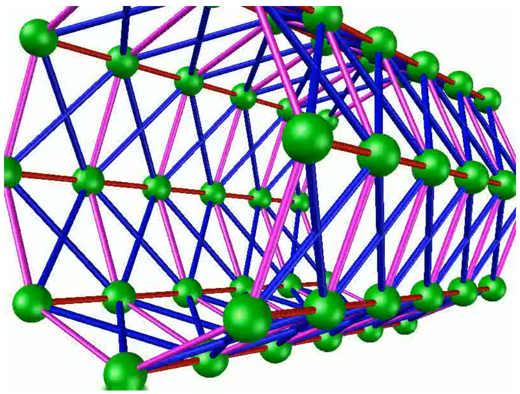


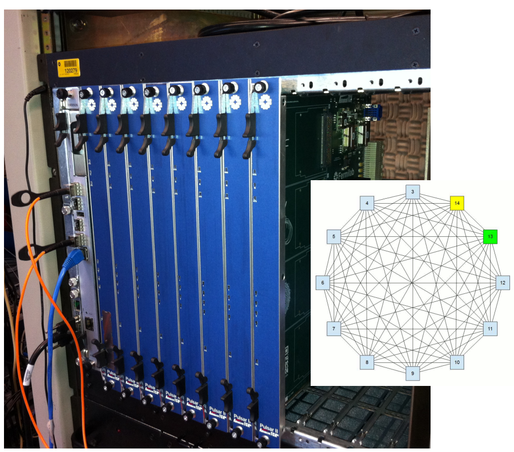
AM-based Tracking Trigger R&D for HL-LHC

Detector design for triggering



L1 Track Trigger architecture



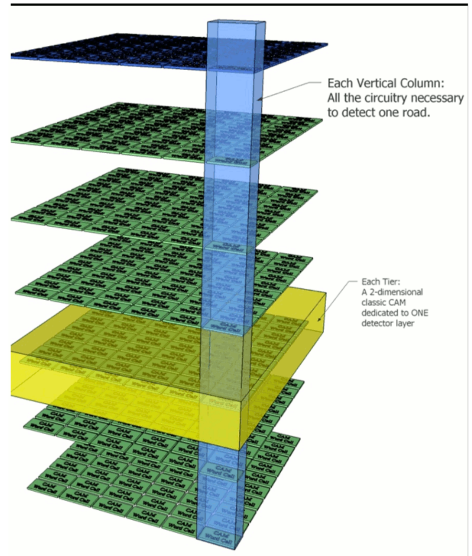


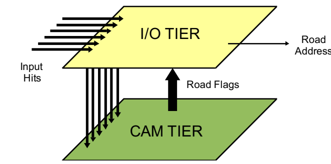
Data transfer

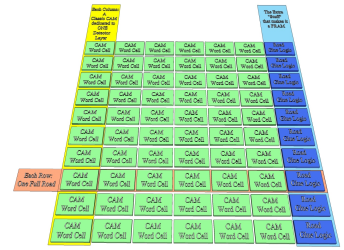
Data formatting

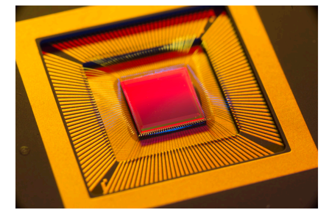
Custom ASIC

VIPRAM in 3D (DOE CDRD)





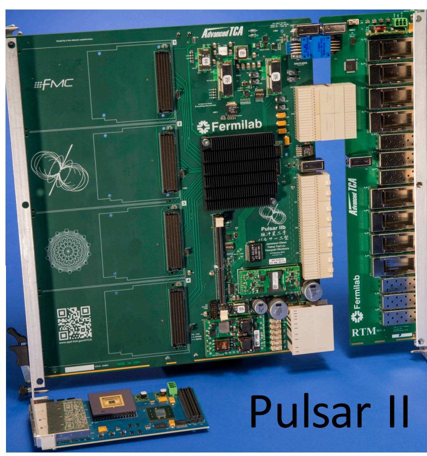




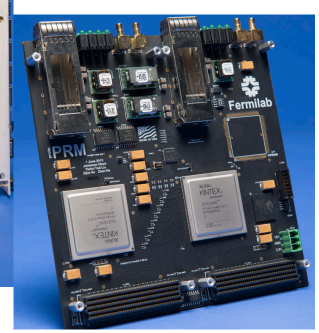
Pattern Recognition

VIPRAM: Vertically Integrated Pattern Recognition Associative Memory

ATCA



Pulsar II



Track Fitting

Extensive simulation work

Pattern Recognition Mezzanine (PRM)

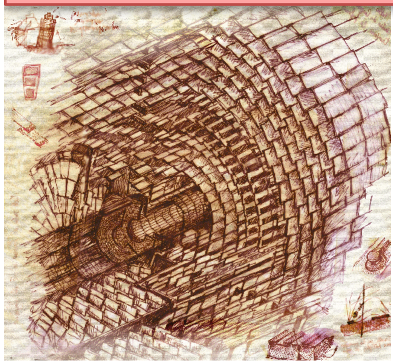
Tracking Trigger & Future Hadron Colliders

- Given the huge cost associated with any future higher energy hadron collider (such as VLHC), *it is crucial to push for higher luminosity* (similar to HL-LHC or beyond). This is to maximize the new physics reach of the huge investment already made, before a new higher energy collider can be proposed or built.
- Because tracking information is the most effective means for high pile-up mitigation, *a high performance, real time tracking trigger will be mandatory.*

In general, for all the on going HL-LHC tracking trigger R&D projects: not only is important for the success of LHC physics program in the HL-LHC era, it also lays some of the technological foundations for the future of the field.

Comment on Trigger @ future hadron collider → beyond HL-LHC

Detector design for triggering



Emerging 3DIC Technology promising

Data transfer (rad hard) high bandwidth low power data link

Data formatting

Telecommunication technology

Pattern Recognition

Emerging 3DIC Technology promising

Track Fitting

Modern FPGAs

There are new challenges:

(0) what kind of detector?

(1) Data Reduction at detector/sensor stage with much more intelligence integrated

(2) Data Transfer (rad hard, high bandwidth, low power link)

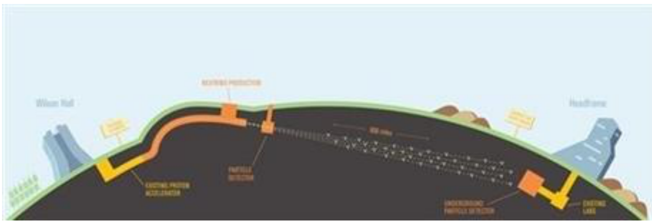
(3) Data Formatting

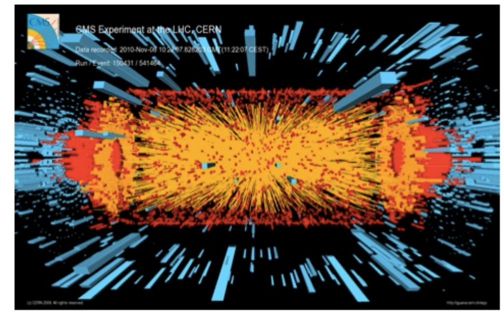
(4) Pattern Recognition

(5) Track Fitting …

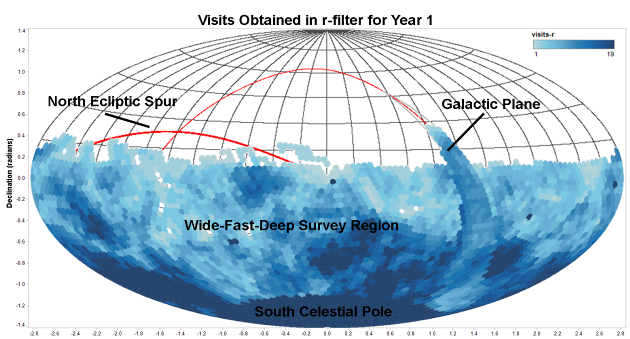
Open question: when/can fast timing be used for pattern recognition in tracking trigger? (pattern recognition in 4D: both space and time)

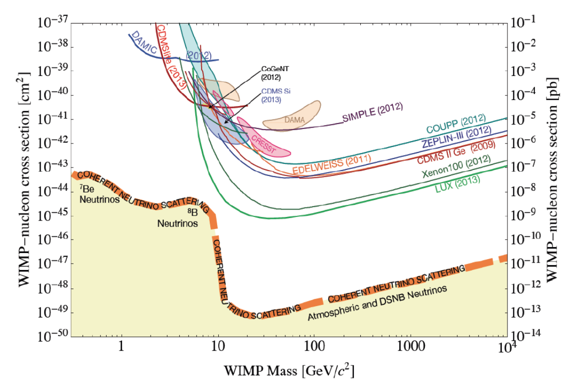
Highlights of activities on Trigger & DAQ R&D at FNAL





- Only a few R&D highlights shown today, didn't cover on going work for current experiments
- A few R&D projects to address future Trigger& DAQ challenges
- For both near term and long term scientific needs
- The R&D work has been done with close collaboration with university groups/labs
  - Example: FNAL LPC (LHC Physics Center) with many students and postdocs involved





Backup slides

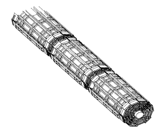
Detectors for astronomy

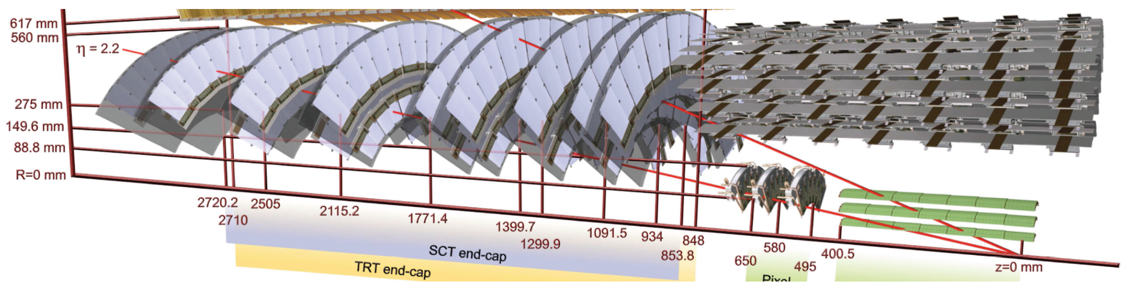
	sensitivity	Noise	Time resolution	Energy resolution	Array size	Cost/unit
Eyes	Poor	Good	msec	Poor	Good	Free
Photographic plates	Fair	Poor	minutes	none	Good	Moderate
Photomultipliers	Fair	Good	msec	none	Poor	High
CCDs	Excellent	Good	seconds	none	Excellent	Moderate
CMOS	Excellent	Fair	seconds	none	Excellent	Moderate
APD	Fair	Good	msec	none	Poor	High
STJ	Fair	Excellent	μ sec	Fair	Poor	High
TES	Fair	Excellent	μ sec	Fair	Poor	High
MKIDs (2020)	Excellent	Excellent	μ sec	Fair	Good	Moderate

MKID DAQ R&D is important to reach the system performance goals …

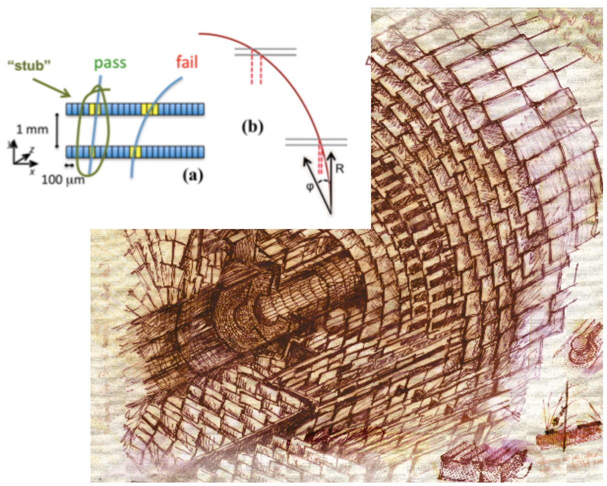
A sense of scale: Atlas FTK vs CDF SVT vs CMS AM TT

CDF SVX II





CMS Phase 2
Outer Tracker
Stub Finding
(extra early Pattern Recognition helps: x ~10)



CDF SVT
Channels involved: ~0.2M
SVT patterns: 6M (upgraded)
SVT towers: 12
Patterns/tower: 0.5M
AMchip03: 4K/chip(180nm)
Luminosity:~10^32 /1.8TeV

Atlas FTK
Channels involved:
PIXELS 80M + SCT 6 M =86M
FTK patterns: ~1 Billion
FTK towers: 64
Patterns/tower: 16M
AMchip06: 128K/chip (65nm)
Luminosity: ~3x10^34 /13TeV

CMS TT (AM)
Channels involved:
2S 48M + PS 217M ~ 260M
AM patterns needed: <~50M
Trigger Towers: 48
Patterns/tower: <~ 1M
AMchip desired: ~few x 100K/chip
Luminosity: ~10^35 /13TeV

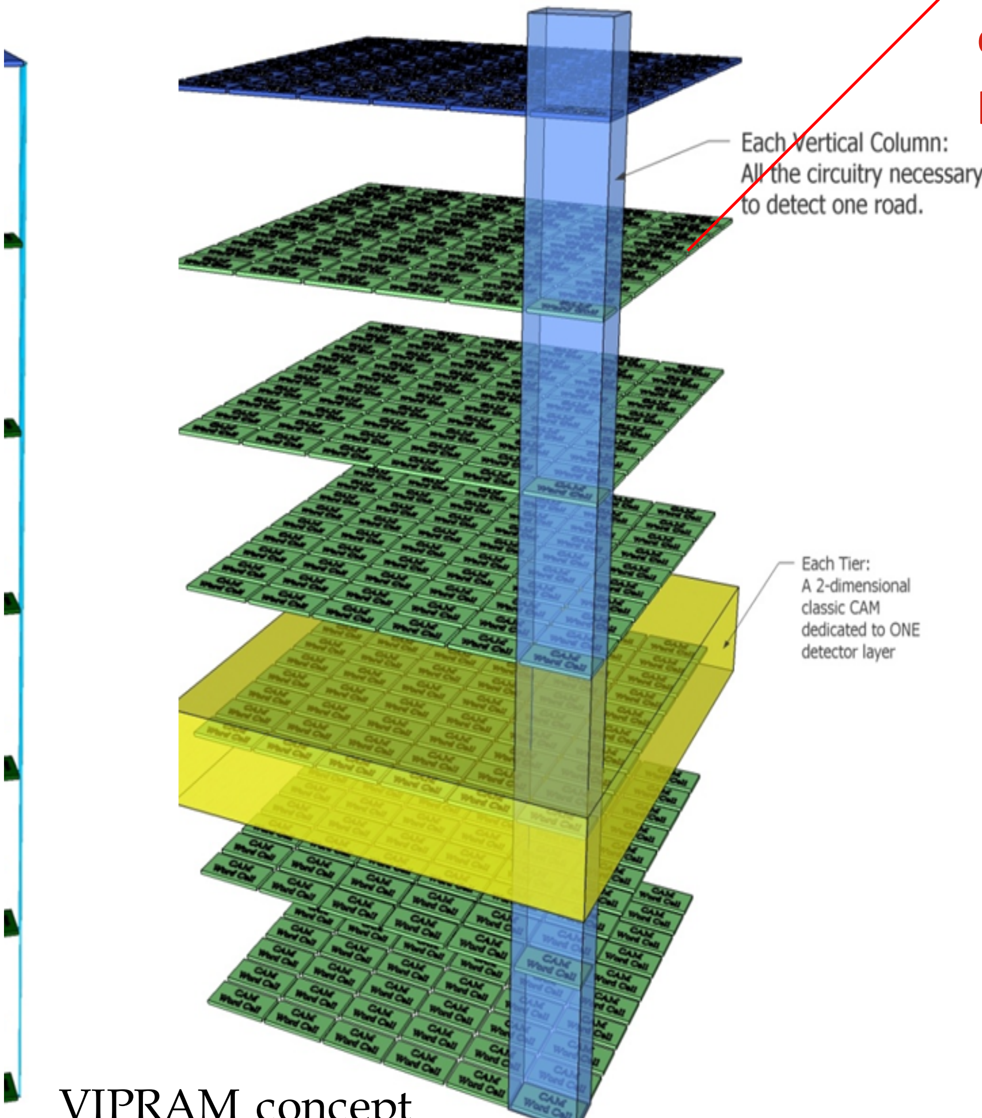
3D Architecture intrinsically open/flexible:

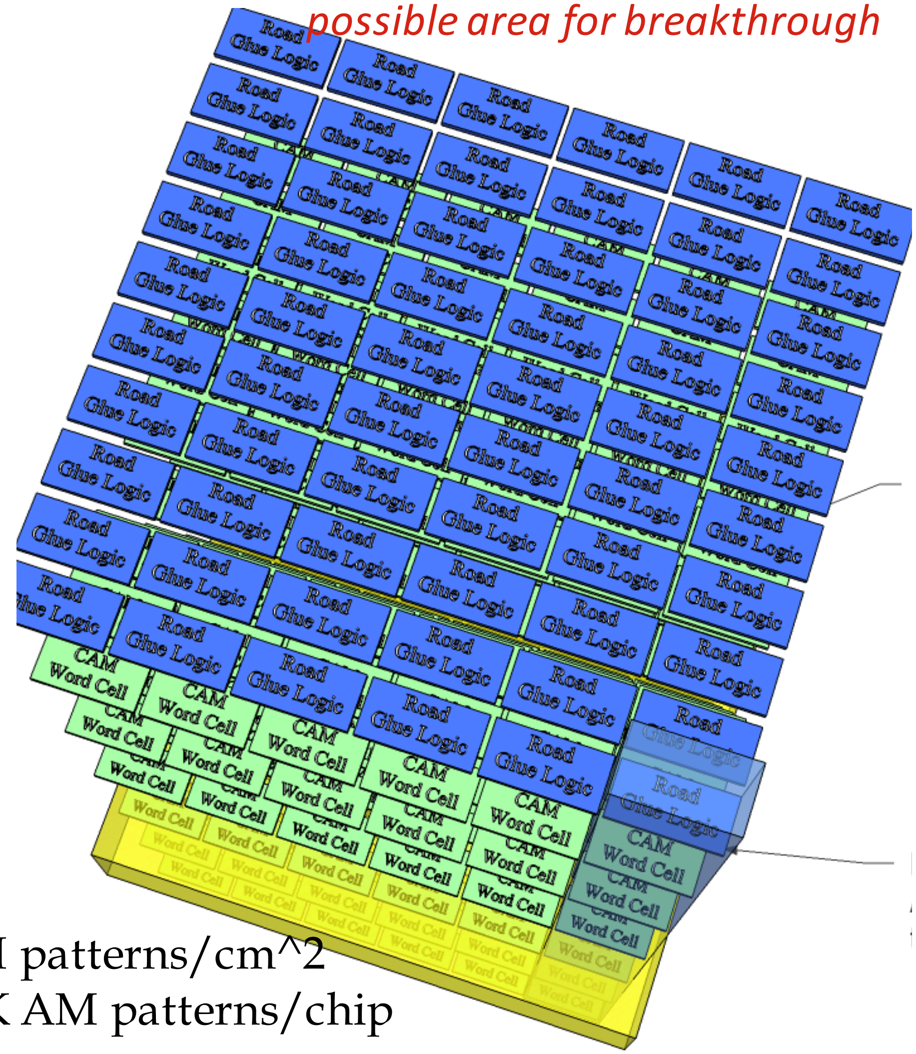
"CAM cell" doesn't have to be CAM

e.g. simple algorithm or even NN …

platform to implement more advanced/fast pattern recognition algorithm…

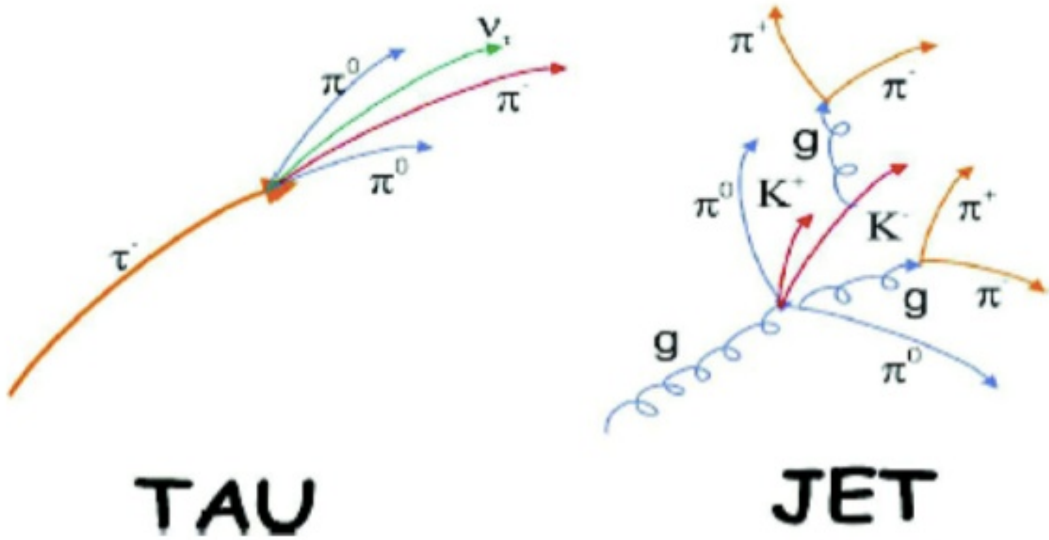
possible area for breakthrough





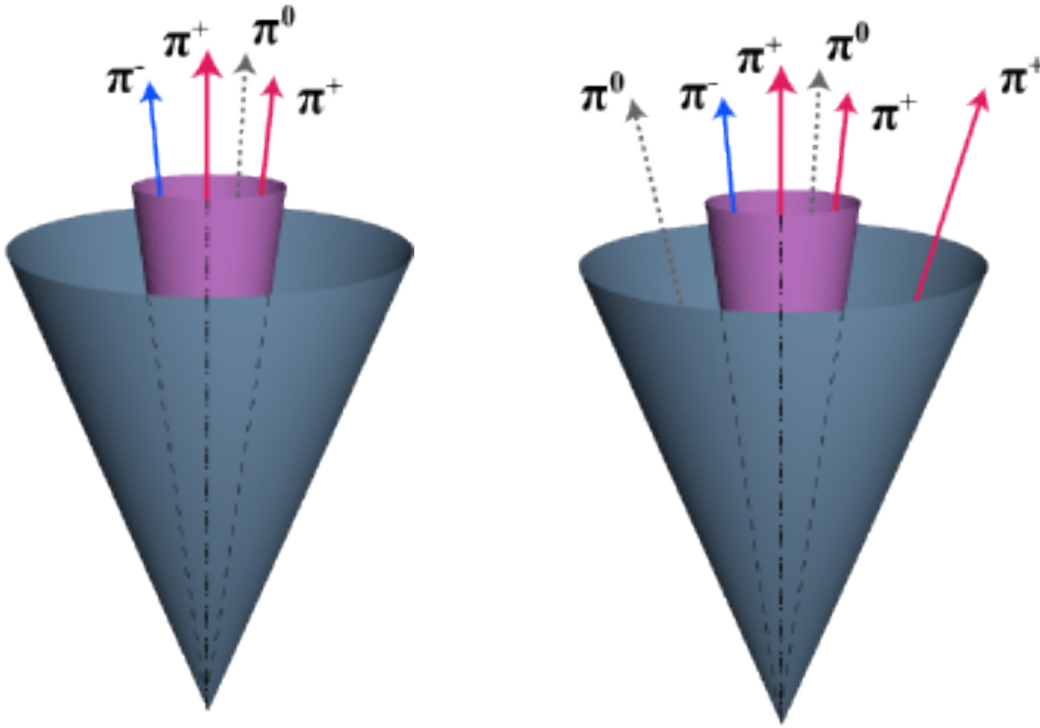
VIPRAM concept

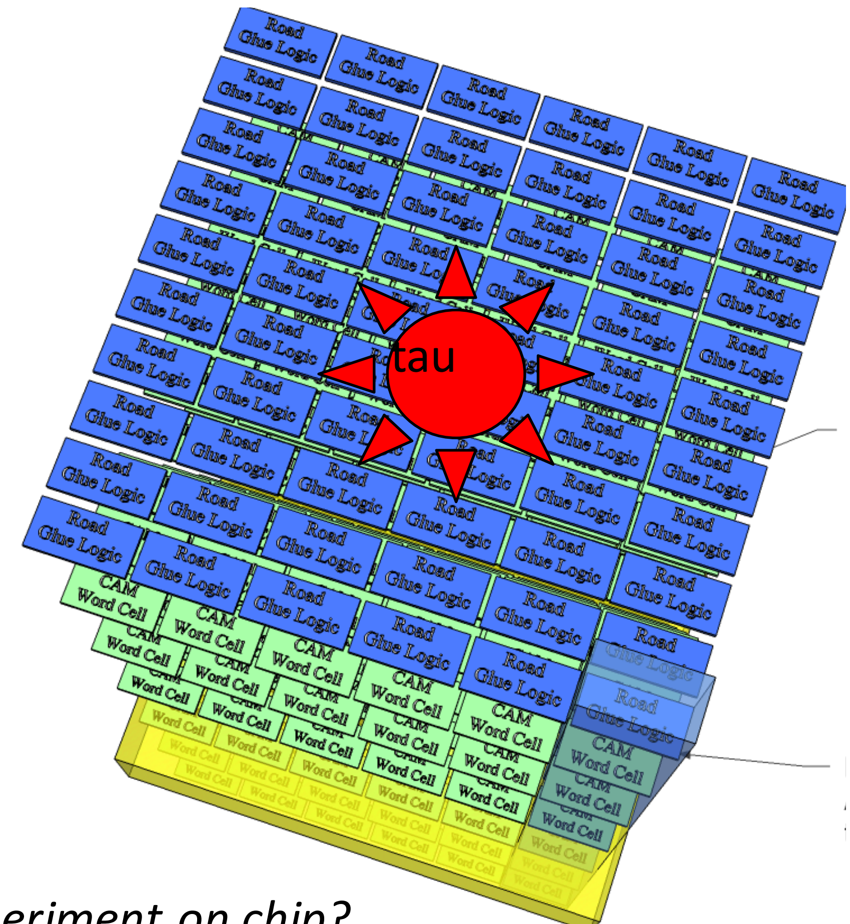
- In 3D, with 130 nm, VIRPAM ~160K AM patterns/cm^2
- CDF AMchip03: 180 nm, standard cell, 4K AM patterns/chip



What if one could implement much more patterns with 3D?

Triggering Taus at L1?





Experiment on chip?

(Food for thoughts)