CPAD Instrumentation Frontier Meeting 2016
Trigger & Data Acquisition

SLAC Roadmap

Ryan Herbst
Department Head, Advanced Electronics Systems

(rherbst@slac.stanford.edu)

SLAC TID-AIR
Technology Innovation Directorate
Advanced Instrumentation for Research Division

U.S. DEPARTMENT OF **ENERGY**
Office of Science

SLAC NATIONAL ACCELERATOR LABORATORY

Overview of SLAC Structure

LSST

LCLS

LCLS-II
John Galayda, Project Director

LSST
Steve Kahn, Project Director
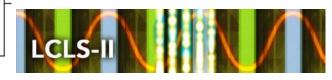
SuperCDMS SNOLAB
Blas Cabrera, Project Director

LABORATORY DIRECTOR'S OFFICE

Chi-Chang Kao
Laboratory Director

Norbert Holtkamp
Deputy Director

LCLS-II

| **Accelerator**
Lia Merminga
Associate Lab Director | **LCLS**
Mike Dunne
Associate Lab Director | **Science**
Chi-Chang Kao
Associate Lab Director | **SSRL**
Kelly Gaffney
Associate Lab Director | **Technology Innovation**
Michael Fazio
Associate Lab Director |

Biosciences, Chemical Science, Computer Science
Elementary Particle Physics, High Energy Density Science
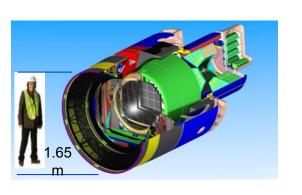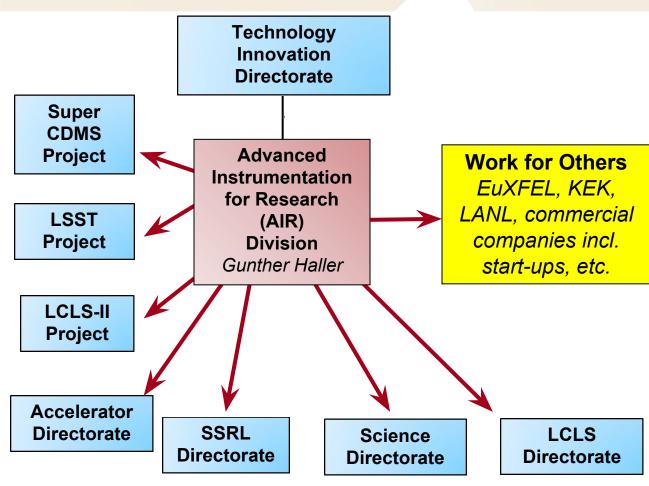Material Science, Particle Astrophysics & Cosmology

Business & Operations

ATLAS

Fermi-GLAST Gamma-Ray Telescope

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SLAC's Core Instrumentation R&D Capability in AIR provides Systems & Components for SLAC & National/International Projects

SLAC

- Provides engineering for SLAC directorates
- All *SLAC developed* LCLS/LCLS-II detectors
- HEP: ATLAS, CDMS, HPS, etc.
- LSST, CMB, Fermi …
- **Non-SLAC Projects**

Technology Innovation Directorate

Super CDMS Project

LSST Project

LCLS-II Project

Advanced Instrumentation for Research (AIR) Division
Gunther Haller

Work for Others *EuXFEL, KEK, LANL, commercial companies incl. start-ups, etc.*

Accelerator Directorate

SSRL Directorate

Science Directorate

LCLS Directorate

1.65 m

LSST: World's largest digital camera

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High Density / High Performance Processing In ATCA

High performance platform with 9 clustered processing elements (SOC)
- Dual core ARM A-9 processor
- 1GB DDR3 memory
- Large FPGA fabric with numerous DSP processing elements

Application specific RTM for experiment interfaces
96 High Speed bi-dir links to SOCs

Data processing daughter board with dual Zynq 045 FPGAs (modular for camera integration)

On board 10G Ethernet switch with 10G to each processing FPGA Supports 14 slot full mesh backplane interconnect!

Deployed in numerous experiments
- LSST
- Heavy Photon Search, LDMX
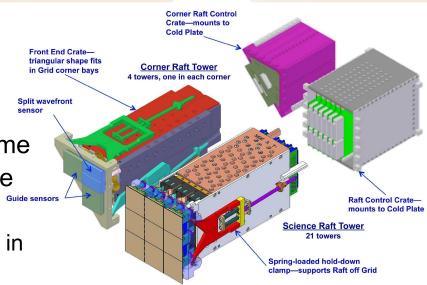- DUNE
- ATLAS Muon
- KOTO
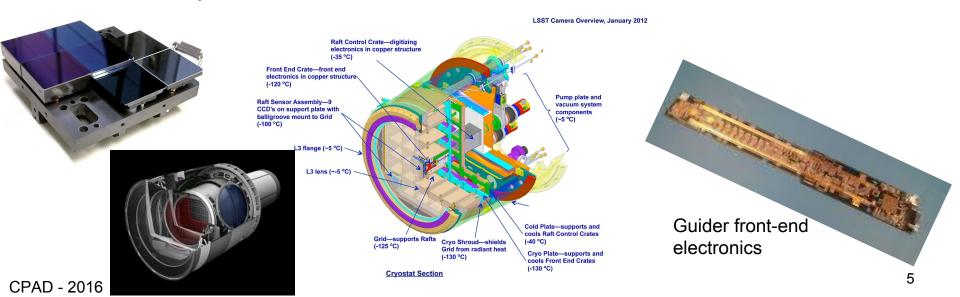- ITK Development

Front panel Ethernet 2 x 4, 10-GE SFP+

SOC platform combines stable base firmware / sw with application specific cores
- HLS for C++ based algorithms & compression
- Matlab for RF processing

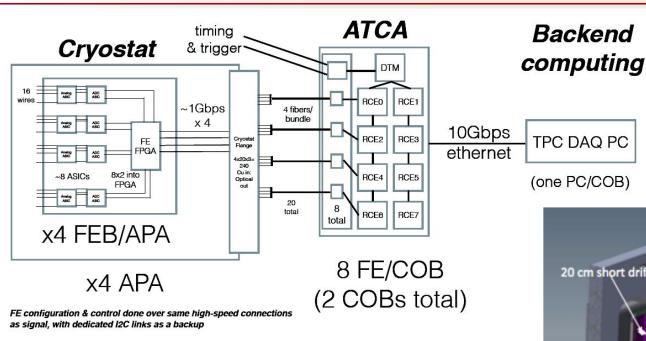CPAD - 2016

LSST Camera Development

- Overall lead of electrical / electronics engineering
- Development of high-performance guiding electronics system
- Development of low-latency, high data-volume data acquisition system hardware & software
  - SLAC ATCA RCE Platform
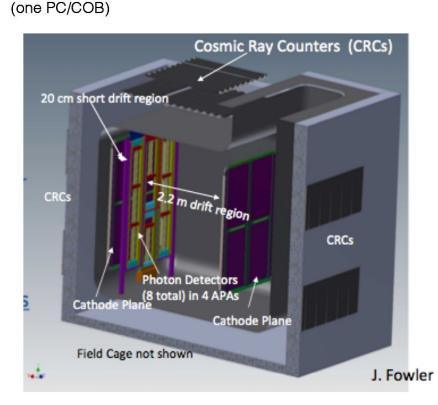 - Includes data-processing & 3 day data cache in flash memory

Corner Raft Control Crate—mounts to Cold Plate

Front End Crate—triangular shape fits in Grid corner bays

Corner Raft Tower
4 towers, one in each corner

Split wavefront sensor

Guide sensors

Raft Control Crate—mounts to Cold Plate

Science Raft Tower
21 towers

Spring-loaded hold-down clamp—supports Raft off Grid

LSST Camera Overview, January 2012

Raft Control Crate—digitizing electronics in copper structure (-35 °C)

Front End Crate—front end electronics in copper structure (-120 °C)

Raft Sensor Assembly—9 CCD's on support plate with ball/groove mount to Grid (-100 °C)

Pump plate and vacuum system components (~5 °C)

L3 flange (~5 °C)

L3 lens (~-5 °C)

Grid—supports Rafts (-125 °C)

Cryo Shroud—shields Grid from radiant heat (-130 °C)

Cold Plate—supports and cools Raft Control Crates (-40 °C)

Cryo Plate—supports and cools Front End Crates (-130 °C)

Cryostat Section

Guider front-end electronics

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DUNE 35-Ton

Cryostat — timing & trigger — **ATCA** — **Backend computing**

x4 FEB/APA

x4 APA

8 FE/COB
(2 COBs total)

FE configuration & control done over same high-speed connections as signal, with dedicated I2C links as a backup

- SLAC RCE Platform is readout for 35Ton detector
- Fully integrated with timing system
- Integrated with ARTDAQ backend system
- Successful deployment of zero suppression algorithm
  - Written in C++ via Vivado HLS design flow
  - Support for 128 channels with 25% FPGA utilization
  - Fully adjustable to optimize performance depending on S/N conditions
  - Successful handling of data quality issues
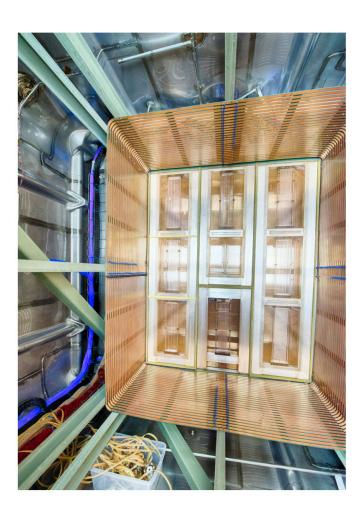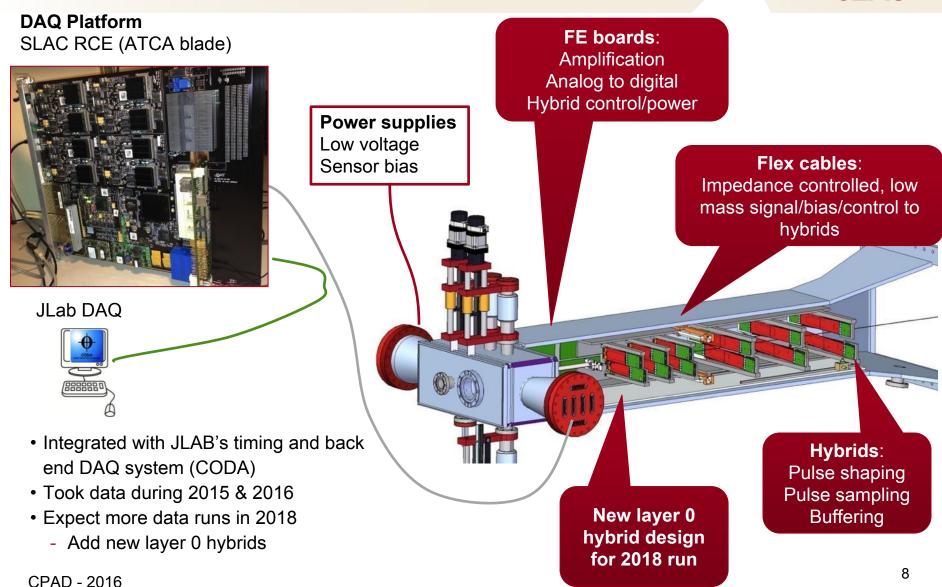   Noisy front end data links
    Cold ASIC stuck bit problem

J. Fowler

ProtoDUNE & DUNE

- Single phase detector data acquisition
- Data path processing of 256 channels per RCE
  - 2048 channels per COB
      Possible to grow to 384 channels
  - Compression algorithm written in C++ via Vivado HLS
  - Dynamic compression table for each channel using channel specific statistics
  - Algorithmic Probability Encoding
  - Best lossless compression without manual tuning
  - Remaining FPGA processing power can be used to remove correlated noise
- Fully integrated timing system for reliable start, stop and triggering

- Moving toward full integration of ArtDAQ board reader software
  - Moving from external PC to RCE ARM processor
  - Hardware offload of data path using SLAC RSSI protocol

- Looking forward to full DUNE detector
  - Optimize channel processing density
  - DAQ platform upgrade & cost reduction
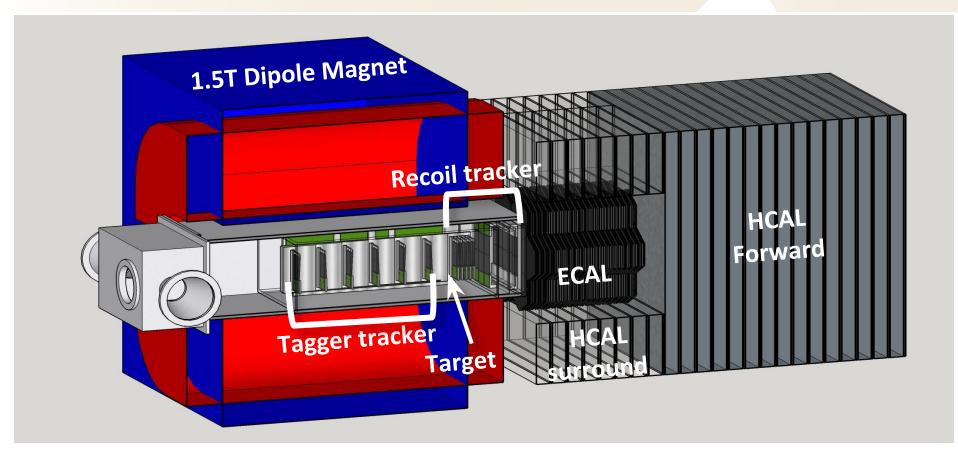 - Proposal for RCE based NOVA trigger contribution (J. Russell)

Heavy Photon Search

DAQ Platform
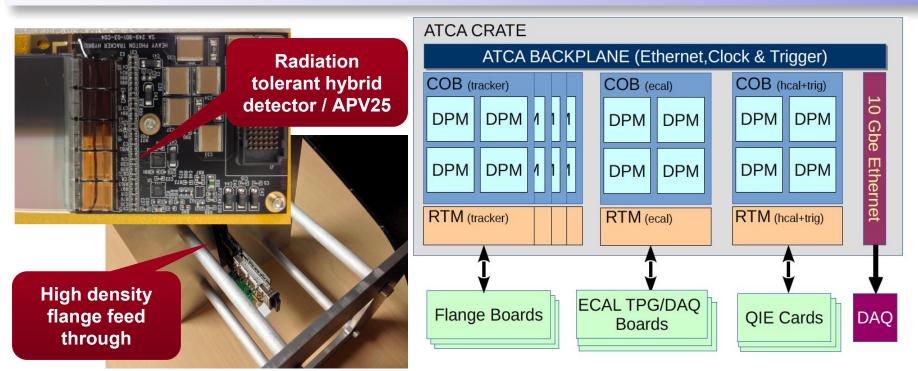SLAC RCE (ATCA blade)

JLab DAQ

- Integrated with JLAB's timing and back end DAQ system (CODA)
- Took data during 2015 & 2016
- Expect more data runs in 2018
  - Add new layer 0 hybrids

Power supplies
Low voltage
Sensor bias

FE boards:
Amplification
Analog to digital
Hybrid control/power

Flex cables:
Impedance controlled, low mass signal/bias/control to hybrids

Hybrids:
Pulse shaping
Pulse sampling
Buffering

New layer 0 hybrid design for 2018 run

LDMX

- Light Dark Matter Experiment planned for End Station A
  - Uses residual dark current available in LCLS-2
  - Low energy electrons which exist between 1Mhz primary beam pulses
- SLAC providing tagger tracker (HPS clone) and facility DAQ
  - Back end DAQ, event building, online analysis and offline storage based upon LCLS-2 DAQ
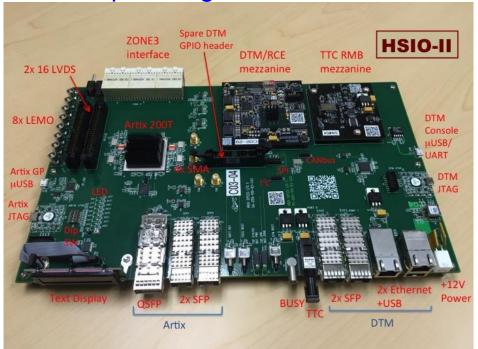
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LDMX Electronics & DAQ

- Common off-detector electronics system based on the RCE platform developed at SLAC
  - System is powerful enough to implement the trigger, timing distribution, DAQ, and controls in one ATCA crate

Radiation tolerant hybrid detector / APV25

High density flange feed through

ATCA CRATE

ATCA BACKPLANE (Ethernet, Clock & Trigger)

COB (tracker)			COB (ecal)		COB (hcal+trig)	
DPM	DPM	M I I	DPM	DPM	DPM	DPM
DPM	DPM	M I I	DPM	DPM	DPM	DPM
RTM (tracker)			RTM (ecal)		RTM (hcal+trig)	

10 Gbe Ethernet

Flange Boards → ECAL TPG/DAQ Boards → QIE Cards → DAQ

ATLAS ITk Readout Test Systems with HSIO+RCE

- Compact bench-top test stand multi-channel readout with RCE mezzanine
- Zynq Z030 based RCE + Artix FPGA for both gate logic and CPU
- Varieties of I/O banks: SFP/QSFP/LVDS/SMA/USB/LEMO, Ethernet ports and TTC interface. Further extended user I/O via zone 3 interface.
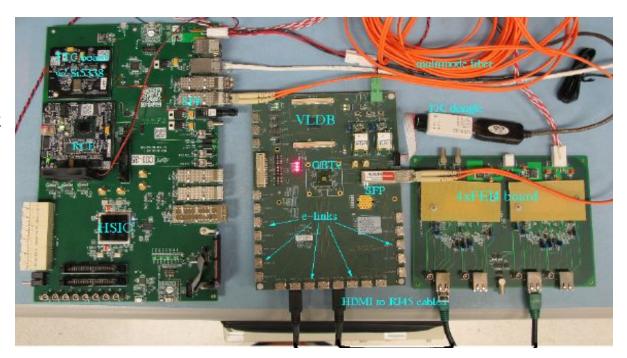- Boot-up management with flash and remote control J-tag

- Previous version of HSIO served critical IBL Q/A and commissioning readout and many ATLAS strip and pixel upgrade test stands and test beams worldwide (~50 boards)
- Current HSIO-II version with 40+ boards for 9 US and 23 international (1 CMS) institutions and systems.

A validated and evolved concept through extensive real applications
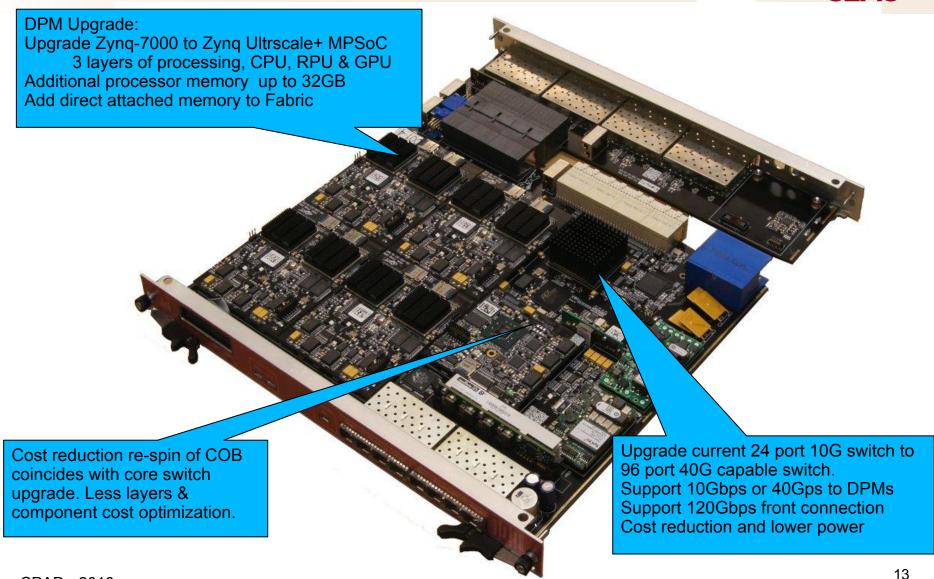
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HSIO & RCE GBT Integration

- RMB module available to support GBT communications
  - Plug in module to HSIO
  - Provides reference clock for all RCEs within a COB
- The VLDB is a test board with a GBTx chip and 20 e-links on HDMI connectors.
  - Available from CERN.
- GBT firmware is available for the Xilinx Kintex.

- Build an RCE test system for FEI4 chips using the GBT protocol.
  - Implementation directly on the RCE's Zynq rather than on the Artix on the HSIO because the Zynq has Kintex-like MGTs (GTX).
- Moved pixel firmware from Artix to Zynq.
- Connection via optical fiber (SFP).
- Next step is to port GBT firmware to the Artix FPGA fabric to run natively on the HSIO
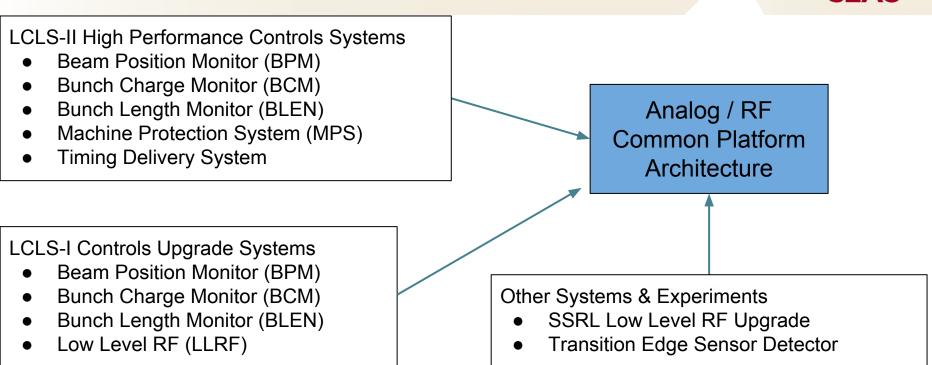
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Planned Upgrades To RCE Platform

DPM Upgrade:
Upgrade Zynq-7000 to Zynq Ultrscale+ MPSoC
    3 layers of processing, CPU, RPU & GPU
Additional processor memory up to 32GB
Add direct attached memory to Fabric

Cost reduction re-spin of COB coincides with core switch upgrade. Less layers & component cost optimization.

Upgrade current 24 port 10G switch to 96 port 40G capable switch.
Support 10Gbps or 40Gps to DPMs
Support 120Gbps front connection
Cost reduction and lower power

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SLAC LCLS-2 High Performance Accelerator Controls RF Detectors

LCLS-II High Performance Controls Systems
- Beam Position Monitor (BPM)
- Bunch Charge Monitor (BCM)
- Bunch Length Monitor (BLEN)
- Machine Protection System (MPS)
- Timing Delivery System

Analog / RF
Common Platform
Architecture

LCLS-I Controls Upgrade Systems
- Beam Position Monitor (BPM)
- Bunch Charge Monitor (BCM)
- Bunch Length Monitor (BLEN)
- Low Level RF (LLRF)

Other Systems & Experiments
- SSRL Low Level RF Upgrade
- Transition Edge Sensor Detector

- TID-AIR developed an ATCA based common platform for accelerator controls
  - LCLS-2, LCLS-1 and SSRL
  - Combines high performance digital processing with low noise RF design

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ATCA Based Platform For
LCLS-I & LCLS-II High Performance Controls
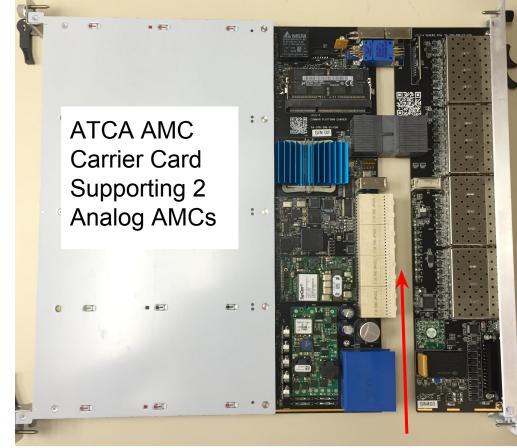
LCLS-1 LLRF Down Convert

ATCA provides the space, power & cooling required for LCLS-2!
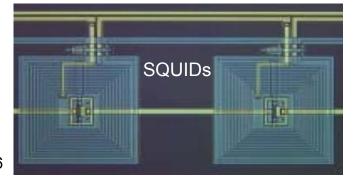

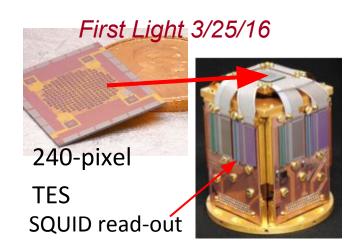ATCA AMC Carrier Card Supporting 2 Analog AMCs
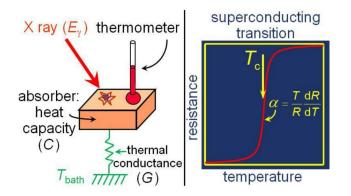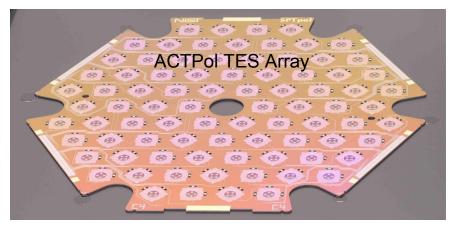
LCSL-2 BPM board

10/40Gbps Ethernet Backplane

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Superconducting Devices for Cosmology

- Seeking signs of cosmic inflation
- Measure polarization of cosmic microwave background
- Use Superconducting Quantum Interference Devices (SQUIDs)
- Transition-Edge Sensors (TES)
- Unprecedented sensitivity and energy resolution
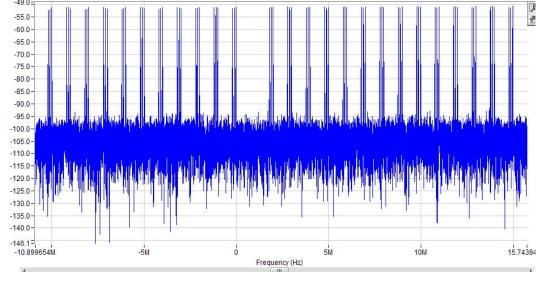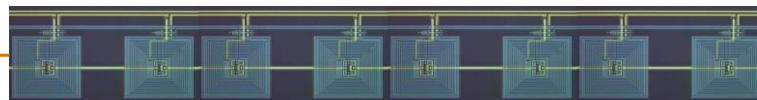- Megapixel arrays possible with spectroscopy on every pixel

First Light 3/25/16

240-pixel

TES

SQUID read-out

X ray (E_γ) thermometer

absorber: heat capacity (C)

T_{bath} — thermal conductance (G)

superconducting transition

T_c

$\alpha = \dfrac{T}{R}\dfrac{dR}{dT}$

resistance

temperature

SQUIDs

ACTPol TES Array

TES Readout Electronics

- Each TES element is coupled to a superconducting resonator with a SQUID that results in a resonant frequency dependent on current
  - Continuous current ramp induces sinusoidal frequency driver
  - TES sensor current modifies the frequency vs ramp current
- "Comb" of frequencies sent down to TES array
  - Triplett of frequencies per TES sensor
    - One below and above resonant frequency for reference

- ATCA based readout electronics generates comb of frequencies
  - 1 at TES resonant point (dip in received frequency)
  - 2 sideband frequencies for reference
- Design goal of 4K channels per FPGA
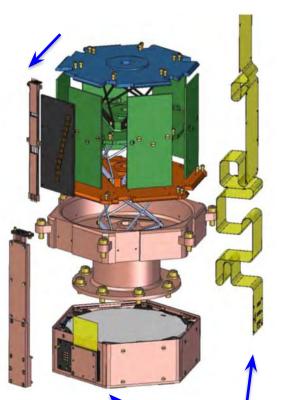 - 12K total tx and rx frequencies (resonant plus 2 reference)
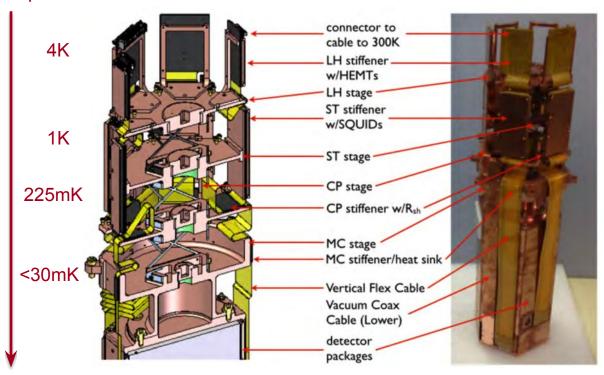
SuperCDMS Detector Tower Overview

TID-AIR responsible for tower cold electronics and 4K->300K readout wiring
⇒ Detect and amplify phonon and ionization signals in ultra-pure Ge/Si detectors
⇒ Tight requirements on radiopurity for all materials!

Tensioned NbTi wire cables

Temperature

4K

1K

225mK

<30mK

connector to cable to 300K
LH stiffener w/HEMTs
LH stage
ST stiffener w/SQUIDs
ST stage
CP stage
CP stiffener w/R_{sh}
MC stage
MC stiffener/heat sink
Vertical Flex Cable
Vacuum Coax Cable (Lower)
detector packages

Superconducting flex cables

Six Ge/Si detectors/tower operating at <30mK!

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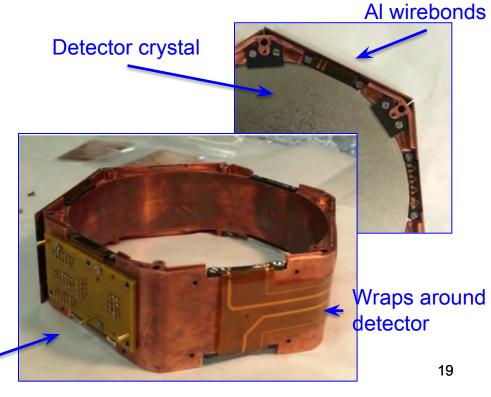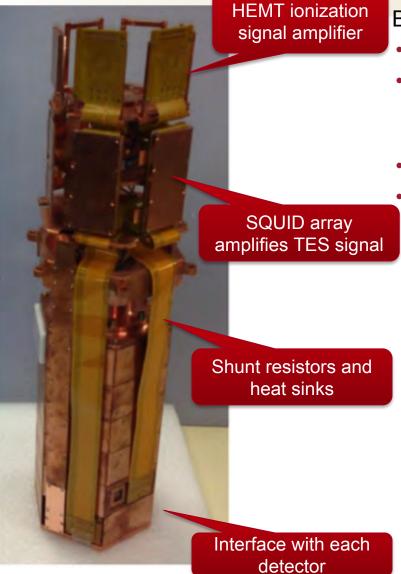
Superconducting Horizontal Flex Cable

Connects from detector wirebonds to vertical flex cable

- Superconducting traces (tin-copper) to minimize resistance
- Short run for ionization signals
- Low inductance for phonon signals
- LEDs for neutralizing ionization traps in crystal

Al wirebonds

Detector crystal

Wraps around detector

Rigid board connects to vertical flex cable

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Superconducting Vertical Flex Cable

HEMT ionization signal amplifier

SQUID array amplifies TES signal

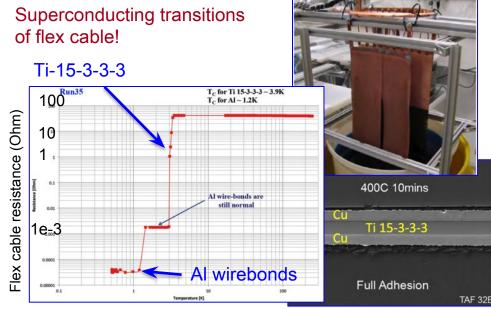Shunt resistors and heat sinks

Interface with each detector

Backbone of tower cold electronics

- Integrated cable with multiple rigid boards
- Challenging Titanium-based superconducting traces (Ti15-3-3-3-> NbTi); critical to minimize thermal load
- Low inductance for TES signal (phonon channels)
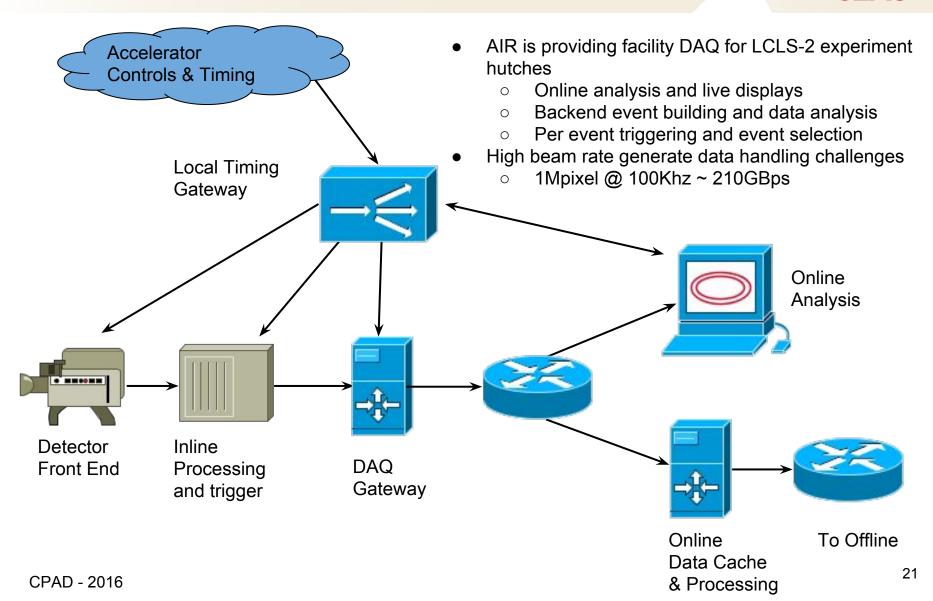- Exotic small signal/low noise amplifiers (HEMT transistors, SQUIDs)

Cu plating+annealing

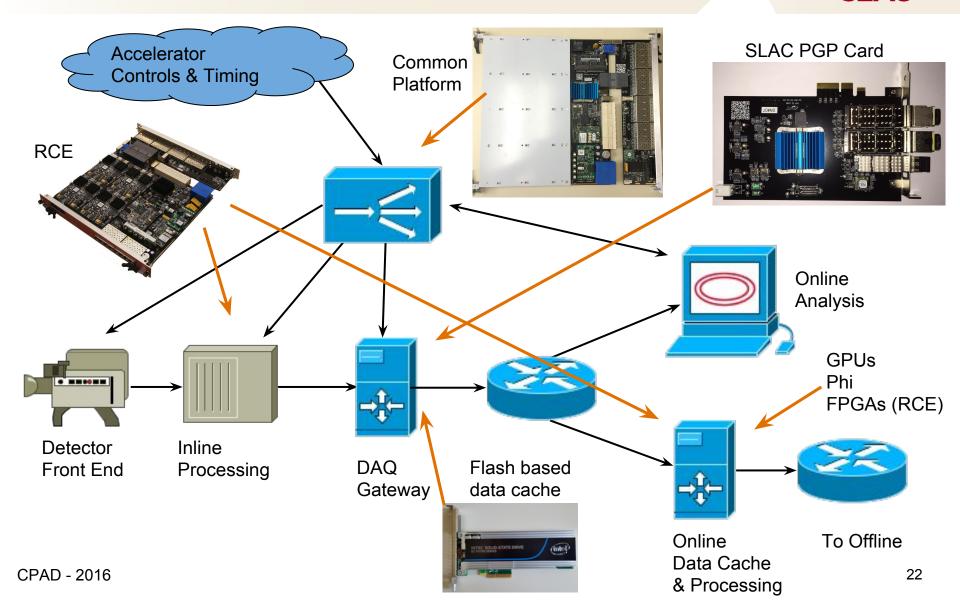Superconducting transitions of flex cable!

Ti-15-3-3-3

Flex cable resistance (Ohm)

Run35

T_C for Ti 15-3-3-3 ~ 3.9K
T_C for Al ~ 1.2K

Al wire-bonds are still normal

Al wirebonds

400C 10mins

Cu

Ti 15-3-3-3

Cu

Full Adhesion

TAF 32B

LCLS-2 Data Acquisition

Accelerator Controls & Timing

- AIR is providing facility DAQ for LCLS-2 experiment hutches
  - Online analysis and live displays
  - Backend event building and data analysis
  - Per event triggering and event selection
- High beam rate generate data handling challenges
  - 1Mpixel @ 100Khz ~ 210GBps

Local Timing Gateway

Online Analysis

Detector Front End

Inline Processing and trigger

DAQ Gateway

Online Data Cache & Processing

To Offline

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LCLS-2 Data Acquisition

Accelerator Controls & Timing

Common Platform

SLAC PGP Card

RCE

Online Analysis

GPUs
Phi
FPGAs (RCE)

Detector Front End

Inline Processing

DAQ Gateway

Flash based data cache

Online Data Cache & Processing

To Offline

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SLAC PCI-Express Generic DAQ Interface Card

Dual QUAD SFPs for 8 lanes of up to 6.125Gbps (upgrade to 12Gbps)

- Optical interface supports a number of detector protocols
  - PGP (SLAC)
  - Aurora
  - CameraLink
  - Raw Ethernet
  - User Custom!

LCLS-1 or LCLS-2 Timing Interface

- PCI-Express card supports bi-directional links to camera front end
  - Hardware handles protocol layers to reduce CPU loading
- Supports bi-direction timing interface supporting busy and trigger feedback
  - Timing receiver firmware built into FPGA
- Timestamp and trigger forwarded down optical link with PGP
  - Timestamp applied directly on camera
  - Round trip latency measurements and adustment
- Firmware can also apply trigger on incoming data
  - Gate event acceptance based upon event code / trigger information

- Most SLAC detectors uses SLAC developed PGP2 protocol
- High bandwidth data transport from camera to DAQ
- Supports timing and trigger delivery to front ends

AIR Integrated Circuits

Develop Application Specific Integrated Circuits (ASIC)
- 10+ ASIC designers

For any application, the following slides concentrate on:
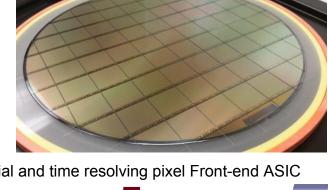- The processing of signals from detectors
- The control of detectors

Standard interfaces for control and readout
- SLAC SACI protocol for SPI like control
- 8B10B and 10B12B cores for 1Gbps streaming data readout
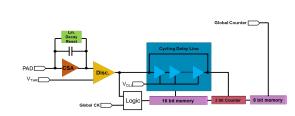
Areas of expertise:
- mixed-signal architectures
- low noise analog front end
- noise filtering optimization
- high speed, mixed mode blocks
- ADC's, DAC's
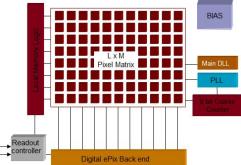- high-speed digital data transmission

Some of the technologies

Variety of vendors (TSMC, IBM, L-Foundry, AMC, setc: 250nm to 65nm technologies

tPix a spatial and time resolving pixel Front-end ASIC

	tPix
Mode of Operation	Time of Arrival + ToT
Pixel Size (µm)	100 x 100
Tile size (pixels)	352 x 384 (2x2 ASICs)
Timing resolution	~ 100ps / 1ns
Time depth	1µs / 10µs

FGPA SERDES Diagnostics And Tuning

- DCP interface to FPGA serializers allows full dynamic reconfiguration and monitoring of SERDES
    - Monitor eye diagrams for link diagnostics
    - Reconfigure operating mode
        - No need to IP core gen for every application
        - Drop down generic VHDL module with default mode and reconfigure as needed
    - We currently use this to switch between LCLS-1 and LCLS-2 timing modes on our internal receiver
- Console based eye diagram testing with Microblaze:

Lane0 ES with 715 pixels: Lane1 ES with 715 pixels:

Additional Areas Of Development

- RSSI (Reliable SLAC Streaming Interface)
  - Reliable layer on top of UDP for FGPA-FPGA and FPGA-SW interfaces
  - Allows firmware to firmware intercommunication for distributed data processing
  - Integration with our PCI-Express board host protocol offload
- BSP (Board Support Package) software layer auto inferring from VHDL firmware
  - Adding hooks to register definition procedures in VHDL to generate Python code describing register space in parallel to RTL definition
  - BSP can be output of FPGA build process.
  - Eliminates errors when translating register space to software
  - Quick prototyping
- Putting the DNA in the hardware
  - Python code generated from VHDL can be integrated into FPGA image
  - Compressed file next to bitfile image
  - Generic software can learn the hardware and auto populate the BSP upon connection
  - Plug and play detectors and front end boards
- Reliable boot loader for failsafe image download
  - BIOS like initial boot and jump to application image

The End