ATLAS TRIGGER UPGRADES

WADE FISHER
MICHIGAN STATE UNIVERSITY
On behalf of the ATLAS Collaboration

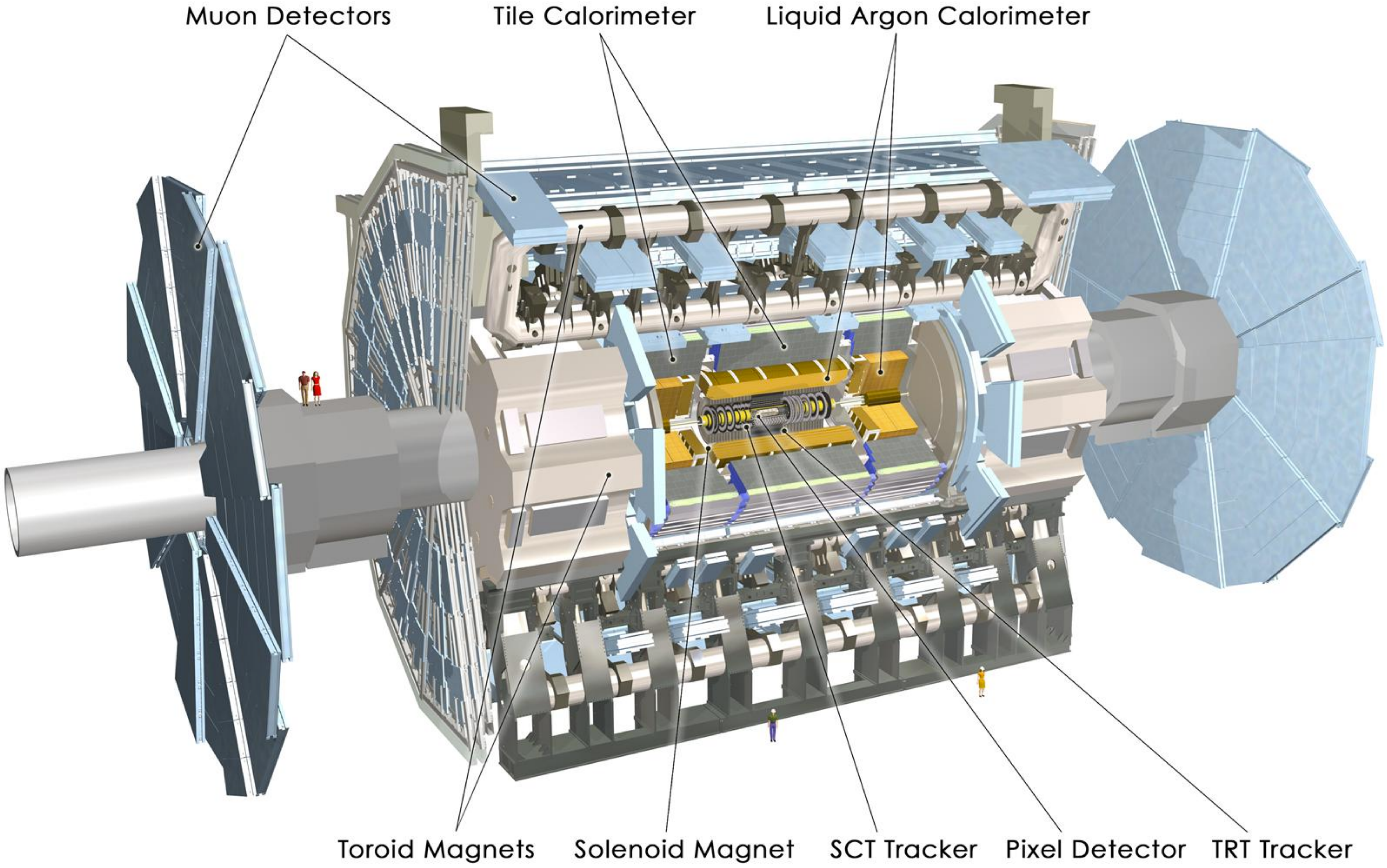
CPAD Meeting, 9 October 2016

Overview

ATLAS & LHC
Status and plans

Phase-1 Upgrades
Strategy & Goals
Construction Progress

HL-LHC Upgrades
a.k.a. Phase-2 Upgrade
Strategy & Goals
Current plans and options



LHC Longterm Schedule

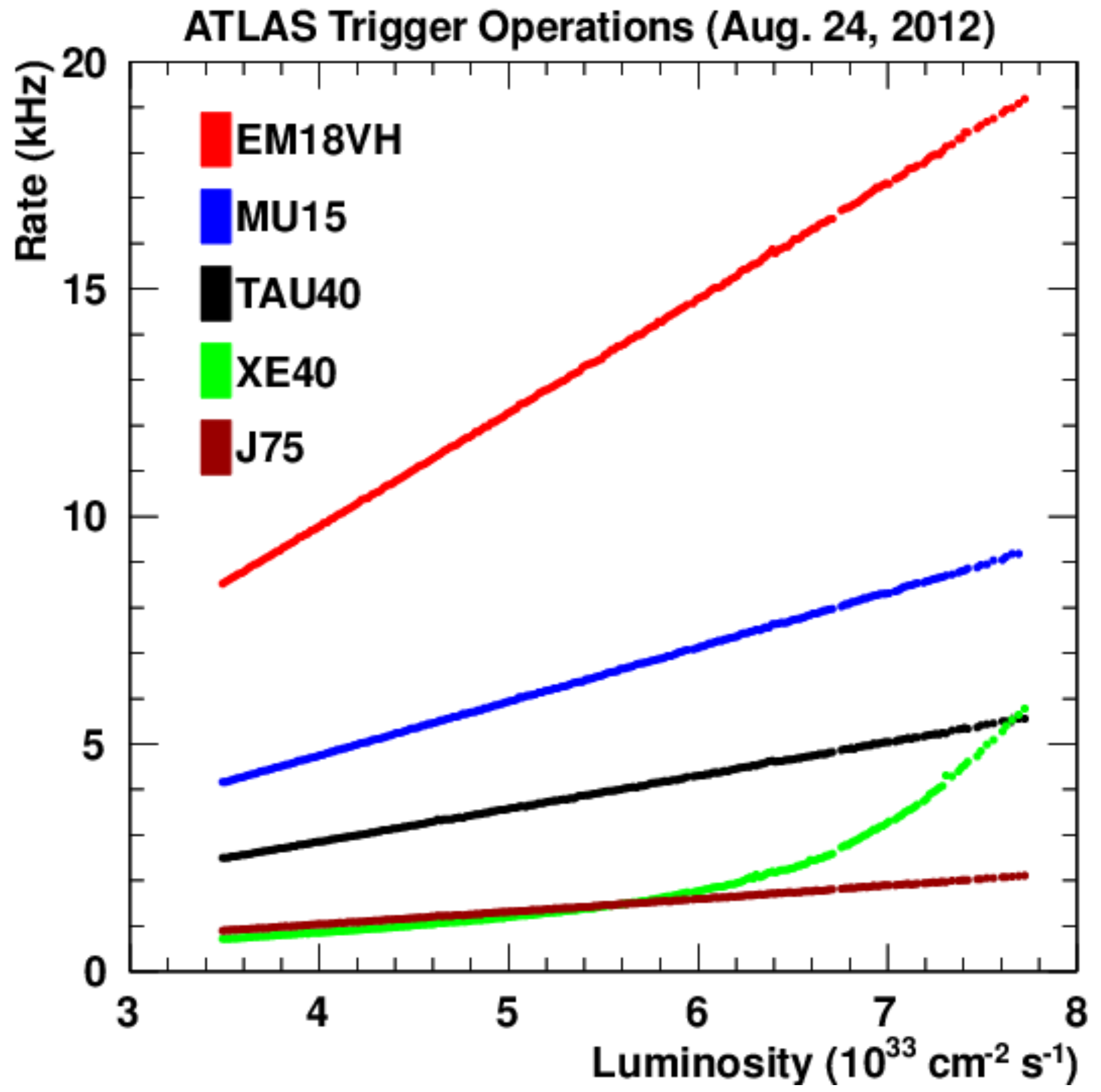
Upgrade Motivations

Lepton trigger rates linear with luminosity & Jet/MET triggers can be highly non-linear

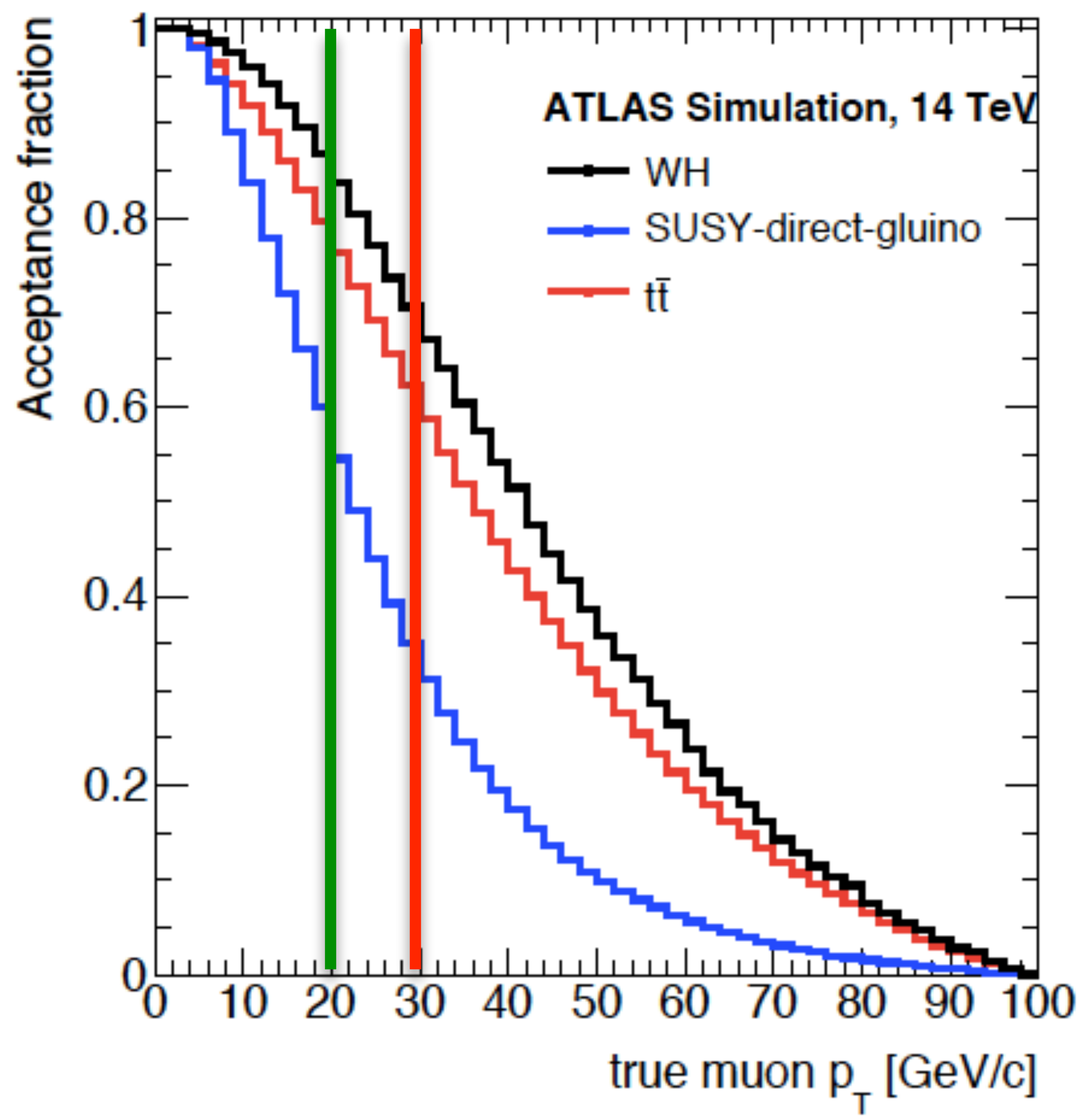
- Extrapolation to high lumi yields rates incompatible with current hardware

Strong desire to maintain low trigger thresholds

- Even modest reductions in thresholds can yield significant physics gains
- Eg, lowering muon pT from 30→20 GeV gains 30-80% in acceptance for core physics interests



		2012 (50 ns, 7.8×10^{33})	Phase I No Upgrade (25 ns, 3×10^{34})
Trigger*	Offline Thresh	Rate	Rate
EM18VH	24 GeV	22 kHz	130 kHz
MU15	25 GeV	12 kHz	150 kHz
TAU40	100 GeV	7 kHz	52 kHz
Rate Limit		~75 kHz	100 kHz

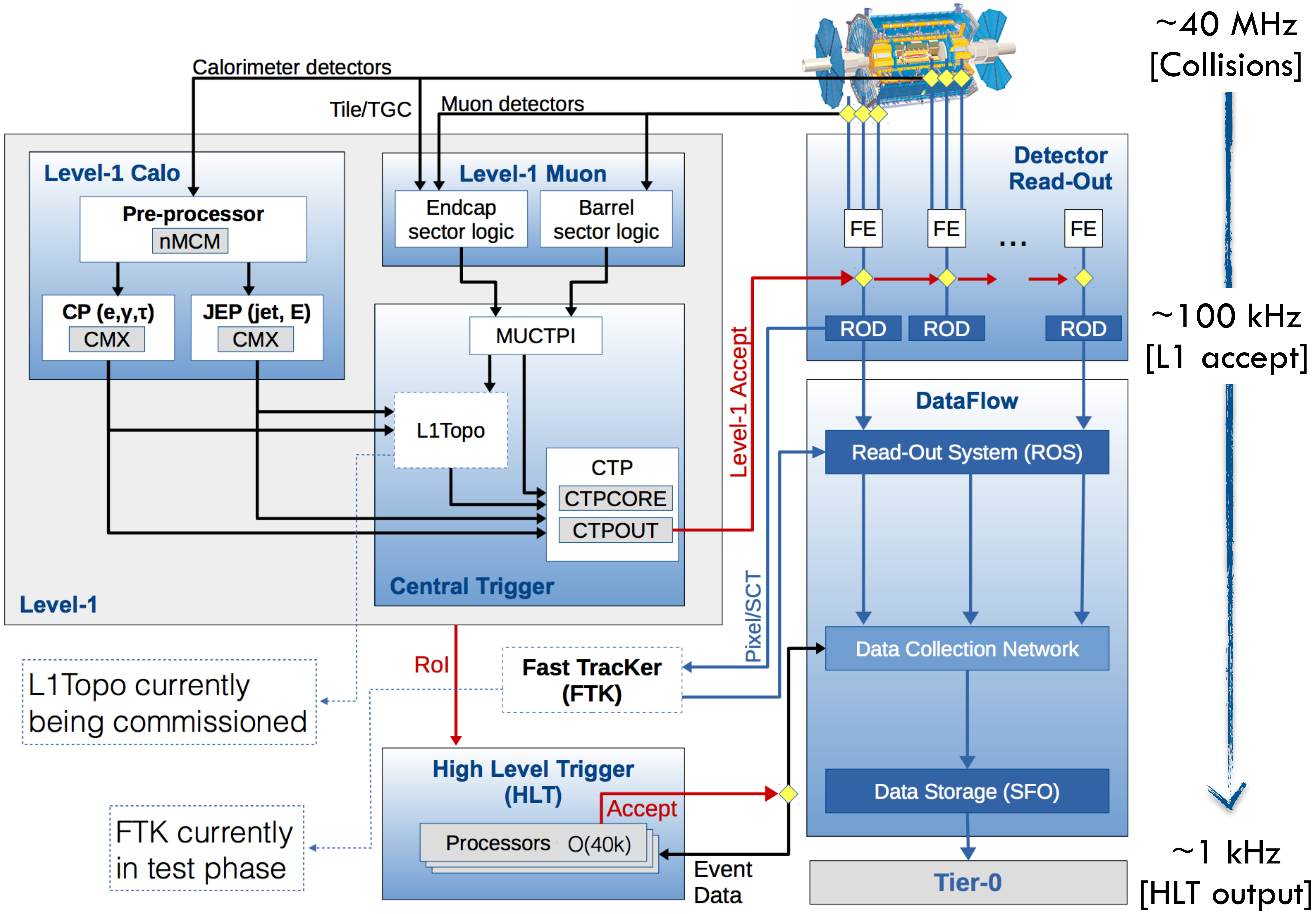


ATLAS Run-2 Trigger/DAQ

Run-2 Trigger
- New L1 Topological Processor
- New Fast TracK (FTK) Trigger

Phase-1 Upgrades
- Improve calorimeter trigger granularity
- Additional forward muon trigger detectors

HL-LHC Upgrades
- New TDAQ system
- Upgraded calorimeter & muon detectors
- New Inner TracKer - silicon strips and pixels



Phase-1 Trigger Upgrade

Run-2 Trigger

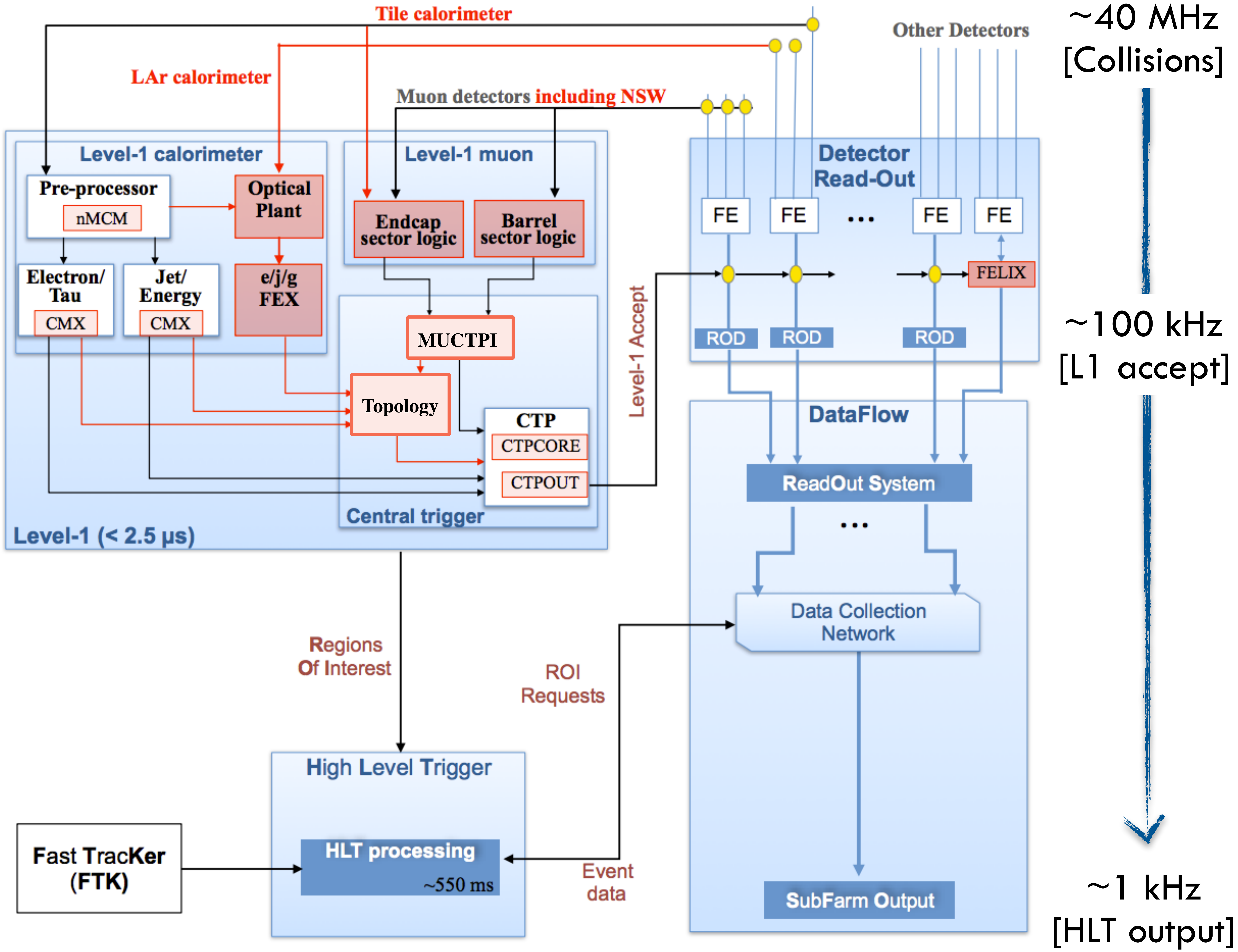
- New L1 Topological Processor
- New Fast TracK (FTK) Trigger

Phase-1 Upgrades

- Improve calorimeter trigger granularity
- Additional forward muon trigger detectors

HL-LHC Upgrades

- New TDAQ system
- Upgraded calorimeter & muon detectors
- New Inner TracKer - silicon strips and pixels



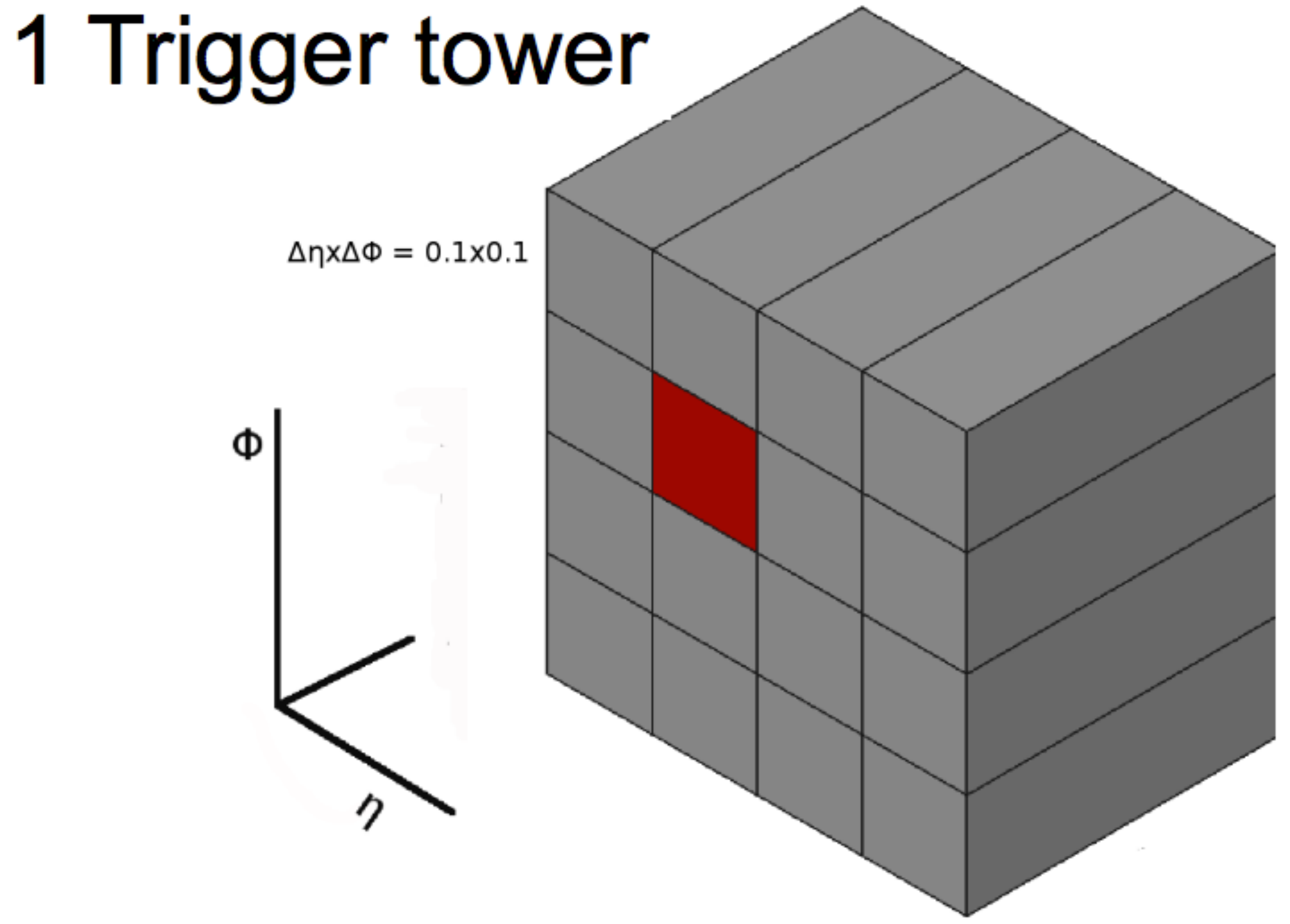
Phase-1 Strategy: Calorimeter

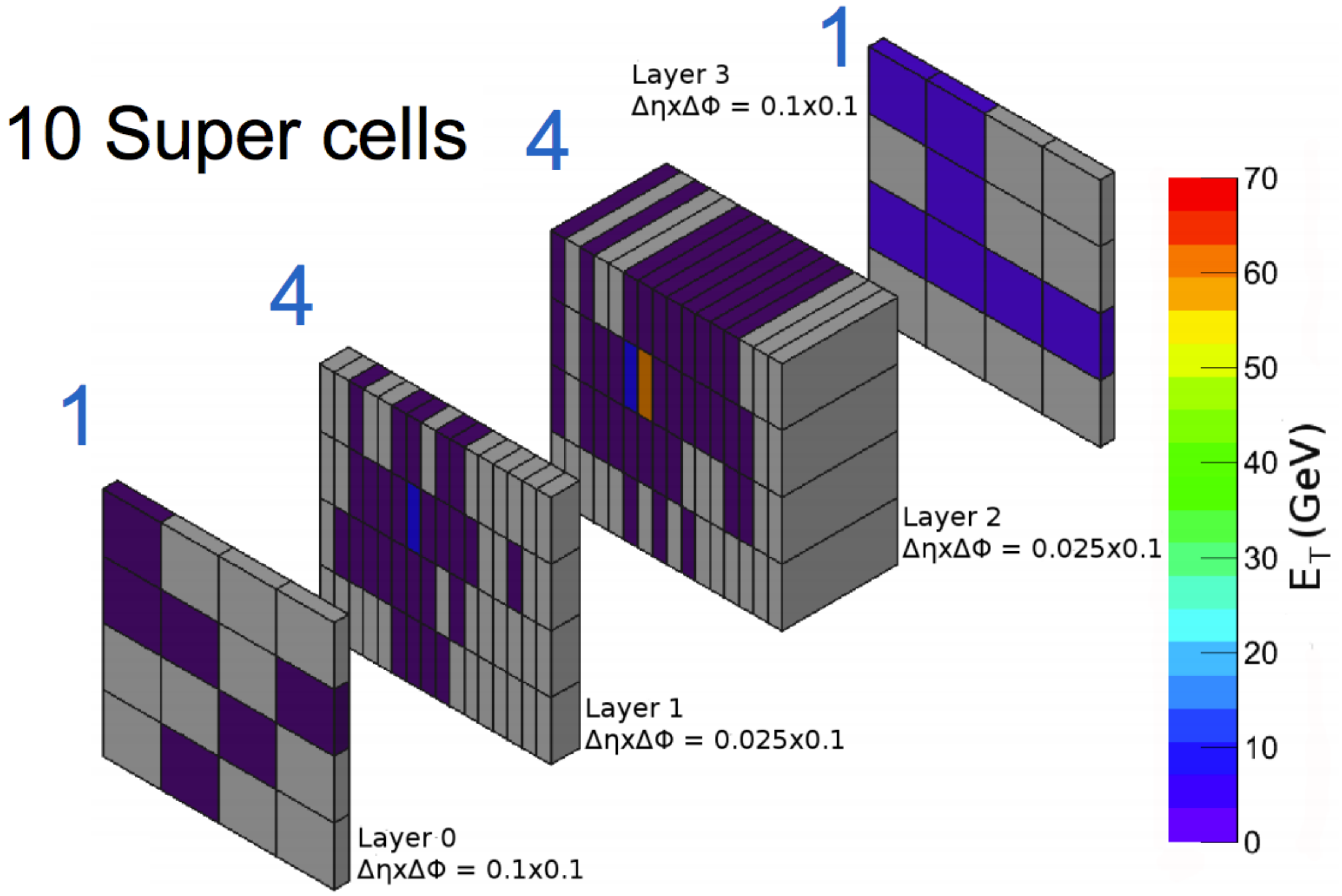
Current L1 Calorimeter Trigger

- Analog sums over sliding window algorithms in FPGAs
- 0.1x0.1 towers for electrons, photons, taus (EM Calo)
- 0.2x0.2 towers for jets, MET (EM+Had Calo)

Phase-1 strategy

- Increase granularity of calorimeter information available
- Migrate HLT-style algorithms to L1 trigger
- Lower energy thresholds, improve isolation capability
- Implemented in Feature Extraction (FEX) processors





Example of potential gain via increase in granularity

70 GeV ET electron as seen in current & upgraded L1Calo trigger

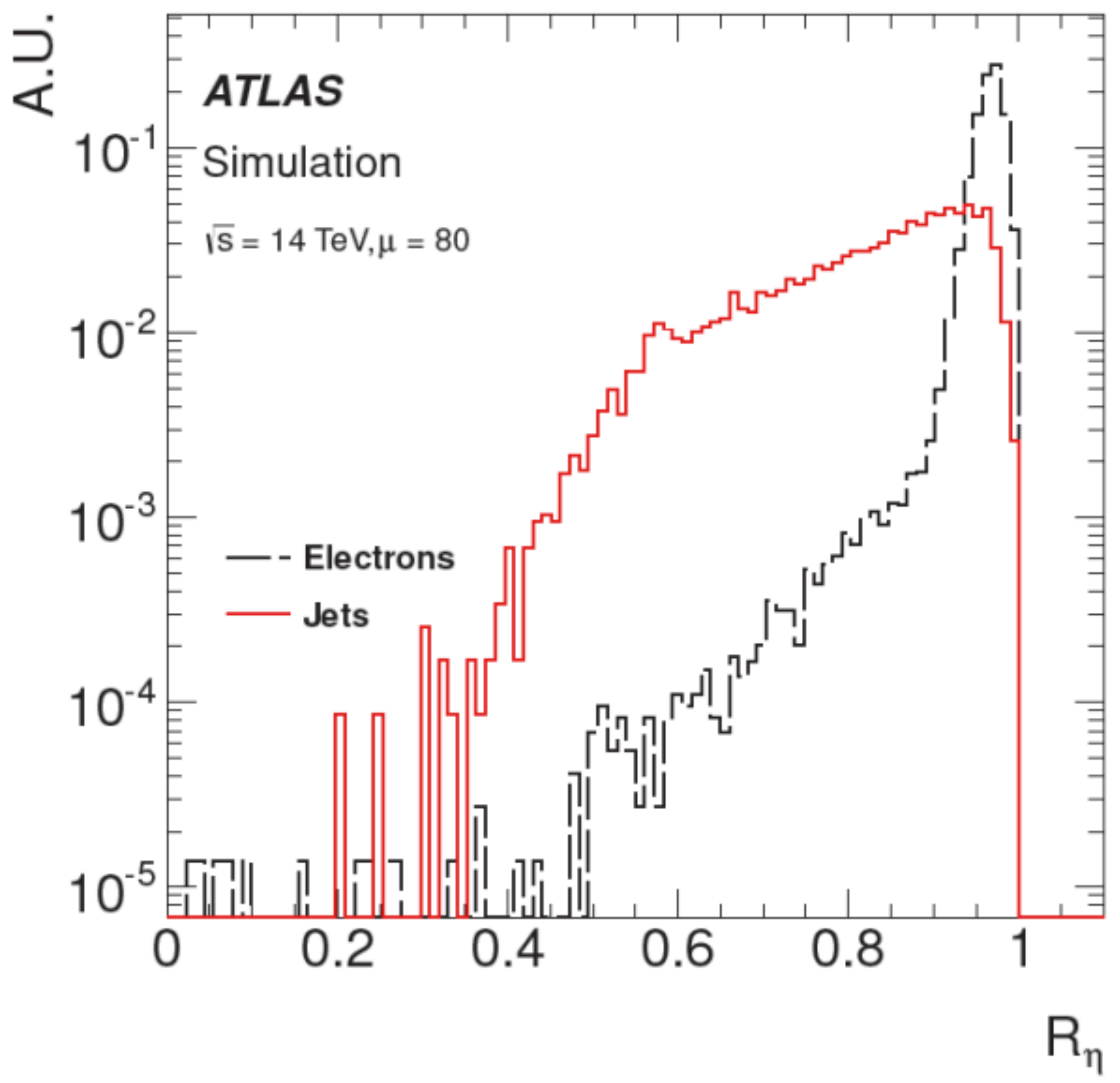
Phase-1 Upgrade: eFEX

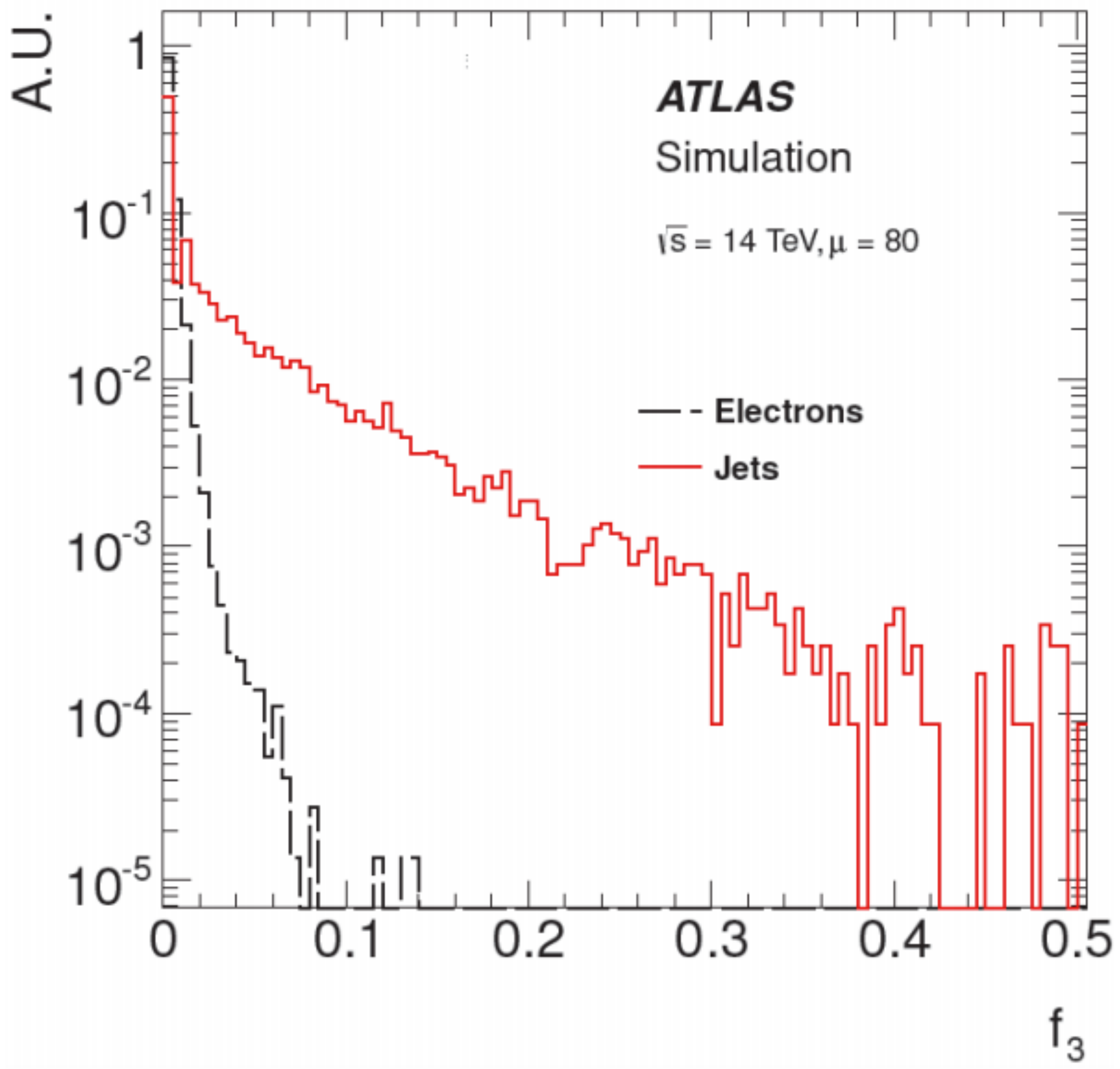
Electron Feature Extraction (eFEX) module

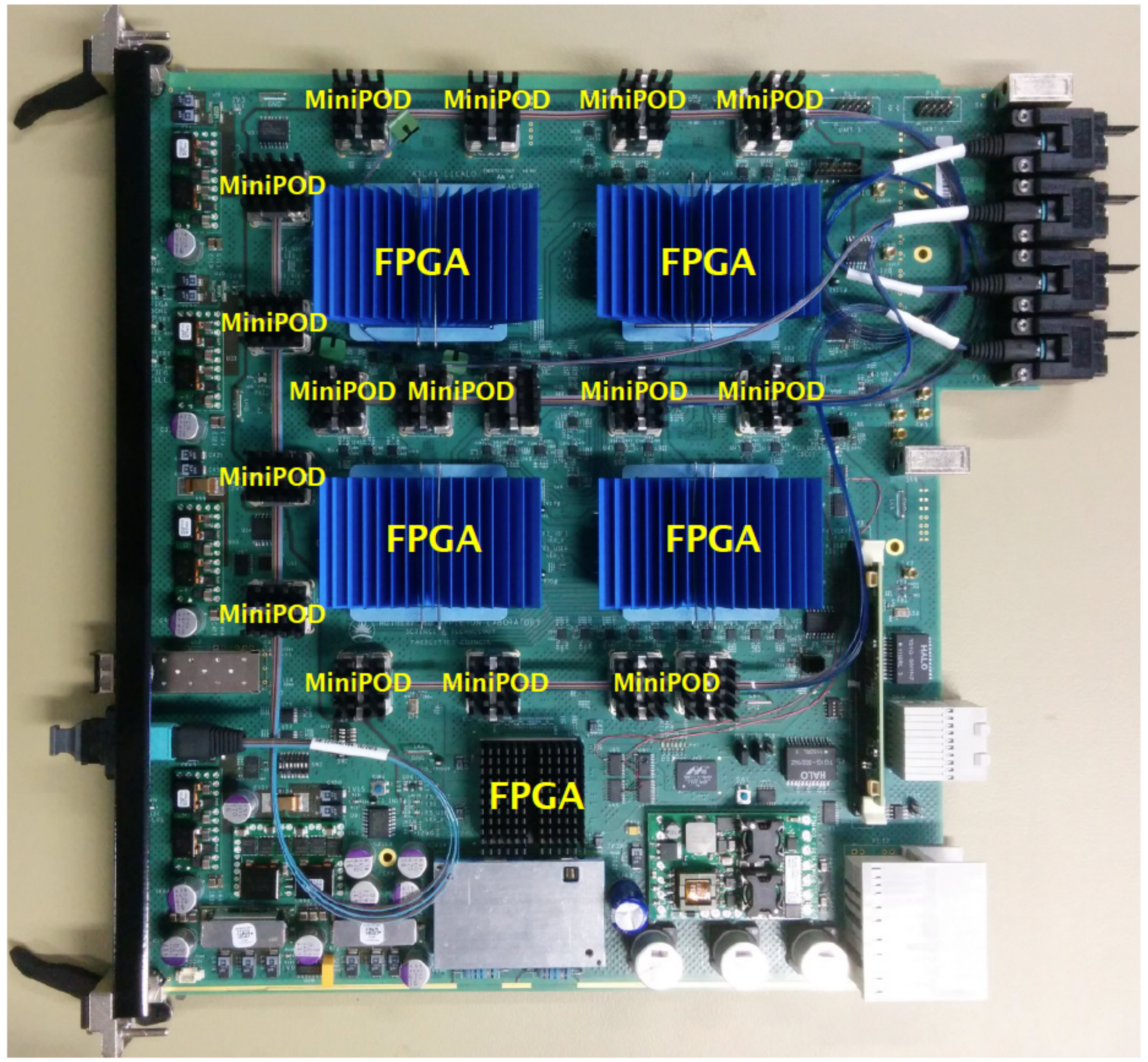
- Designed to utilize more of the calorimeter shower shape information
- Migration from 0.1x0.1 trigger towers to Super-Cells with depth information

Electron-jet separation

- Lateral R_η - relate energy in central core to immediate surroundings
- Depth f_3 - relate back sampling to whole cluster







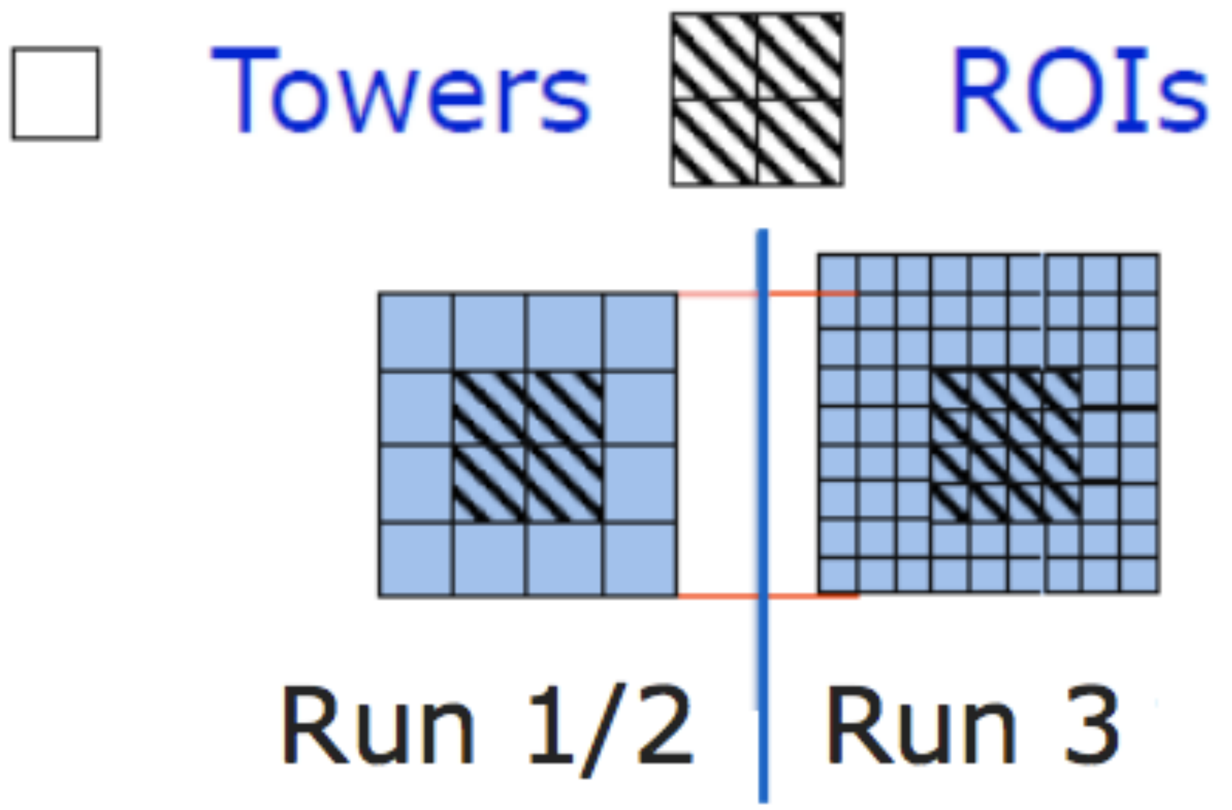
Above: eFEX prototype

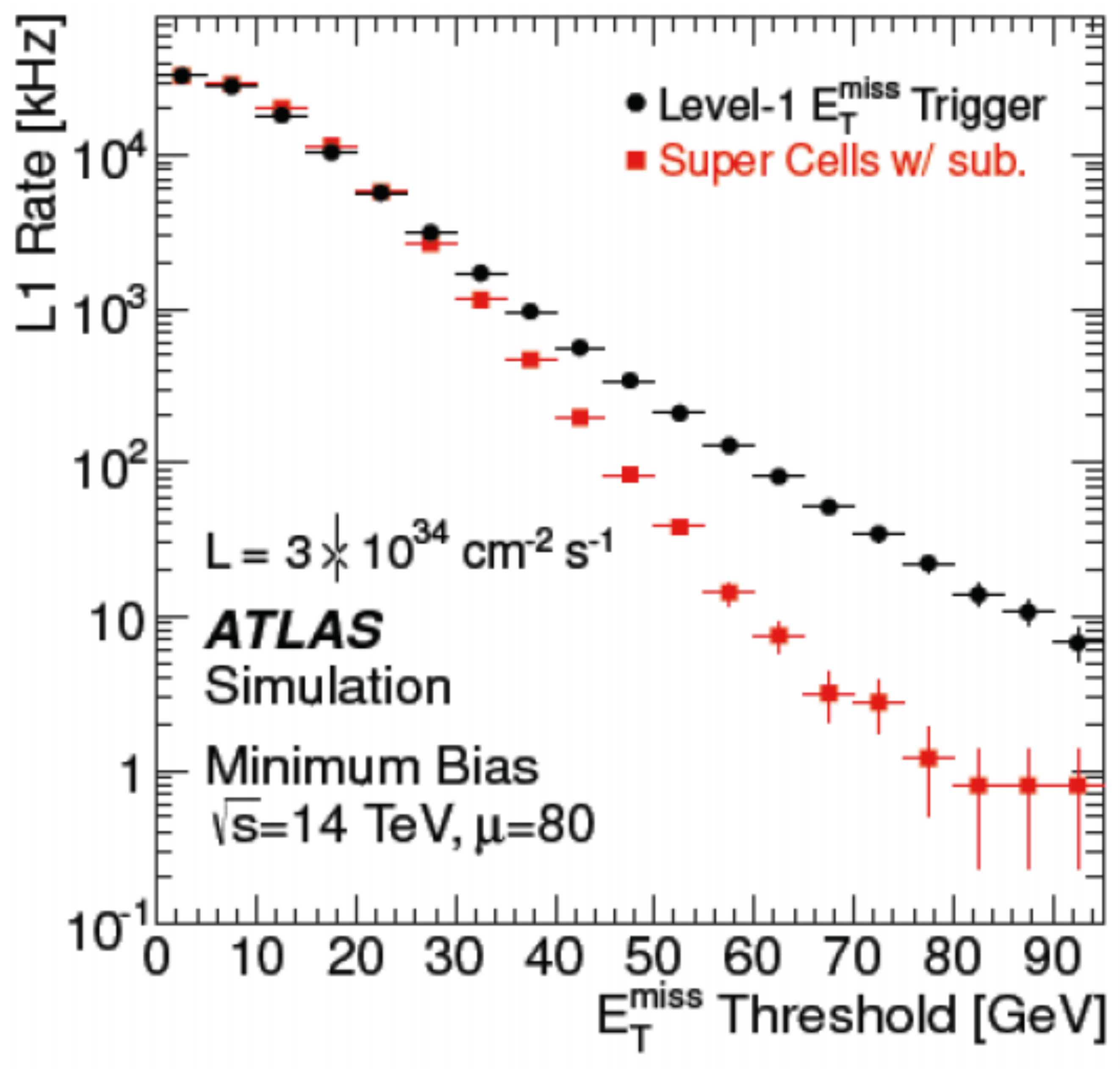
Phase-1 Upgrade: jFEX

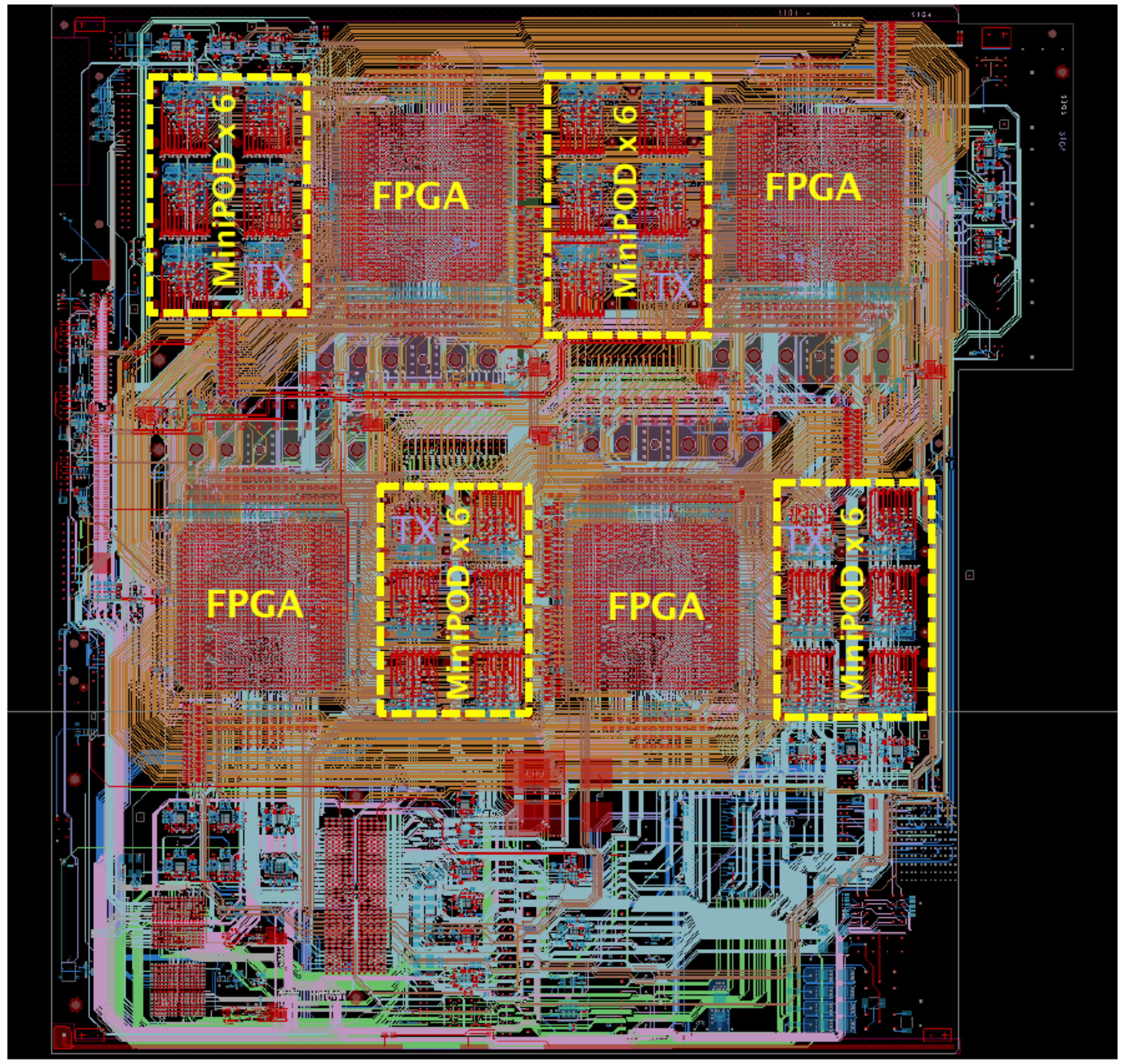
Jet Feature Extraction (jFEX) module
- Designed to cluster and identify jets/τ and calculate MET and HT
- Brings HLT-like jet algorithms to L1 hardware

Better trigger turn-on for jet and missing ET triggers
- Pileup suppression, improved jet reconstruction

Increased granularity (x4 vs Run-2)
- 0.1x0.1 trigger towers, 0.9x0.9 window
- allows flexibility in jet definition (non-square, Gaussian filter, …)







Above: jFEX prototype design

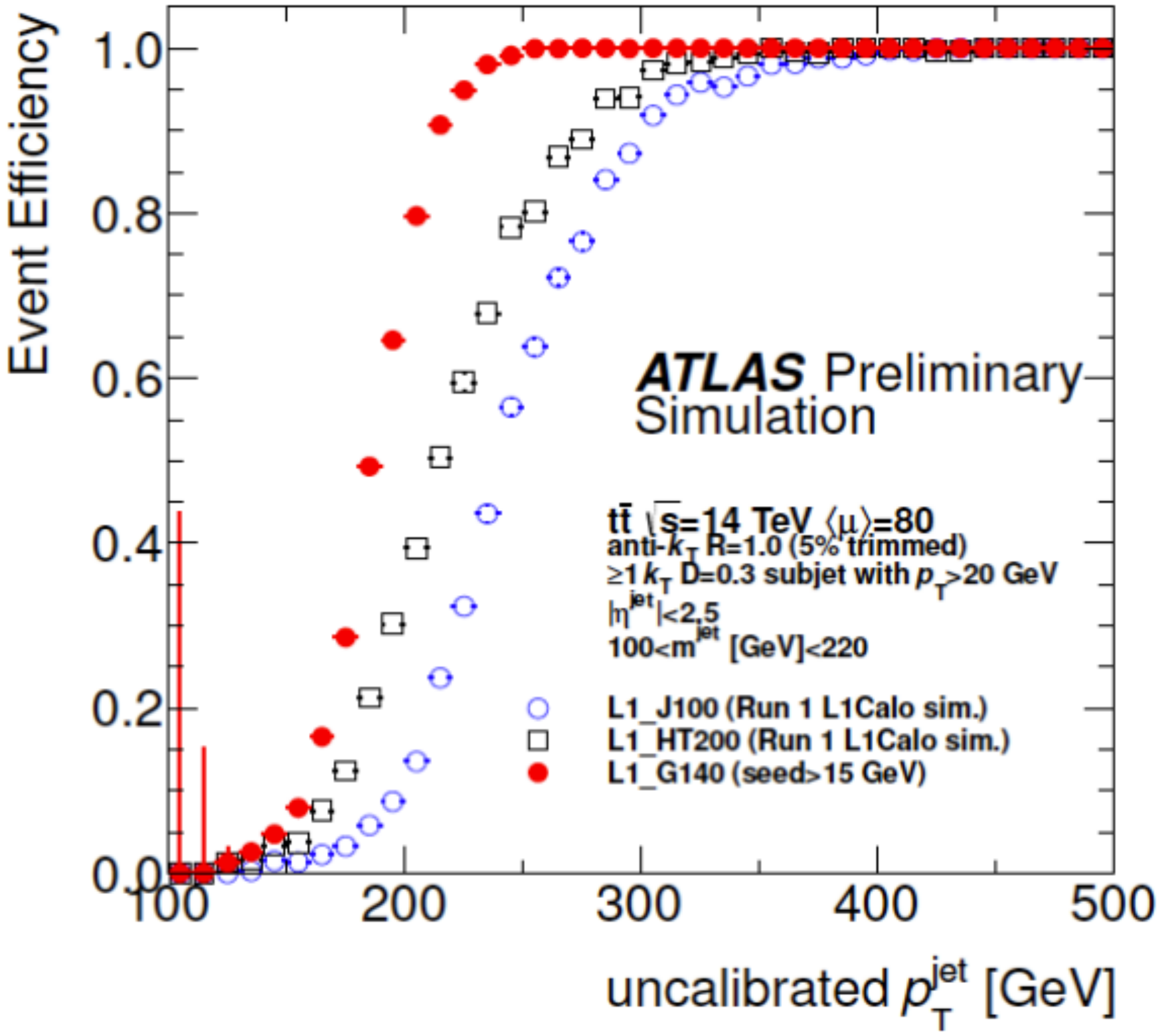
Phase-1 Upgrade: gFEX

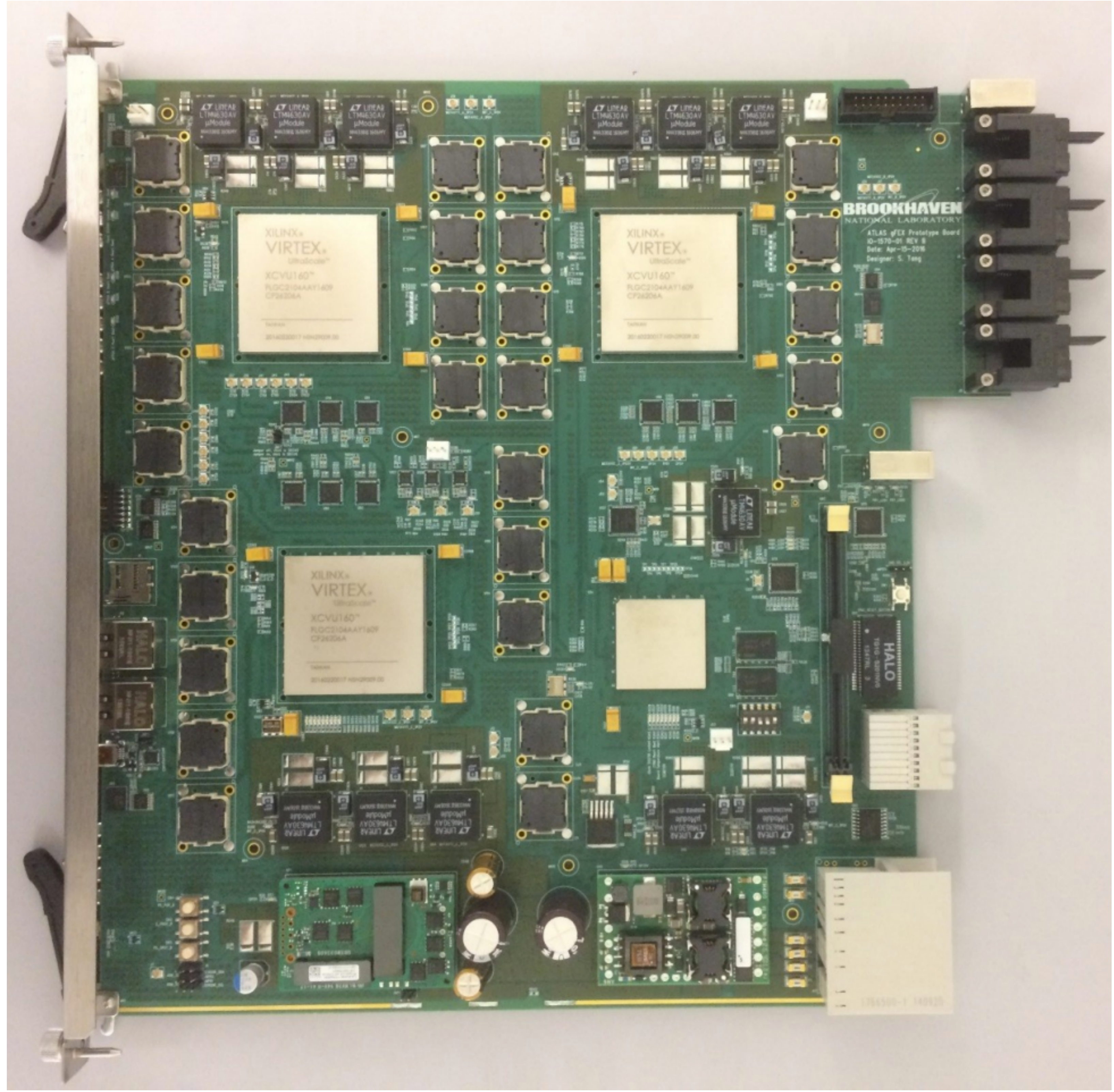
Global Feature Extraction (gFEX) module

- Inputs from entire calorimeter to provide global view
- Per-event calorimeter-wide pileup estimation for energy subtraction
- Run anti-kT like algorithms on 0.2x0.2 jet elements (R=1.0 fat jets)

Large-area jets for dedicated physics cases

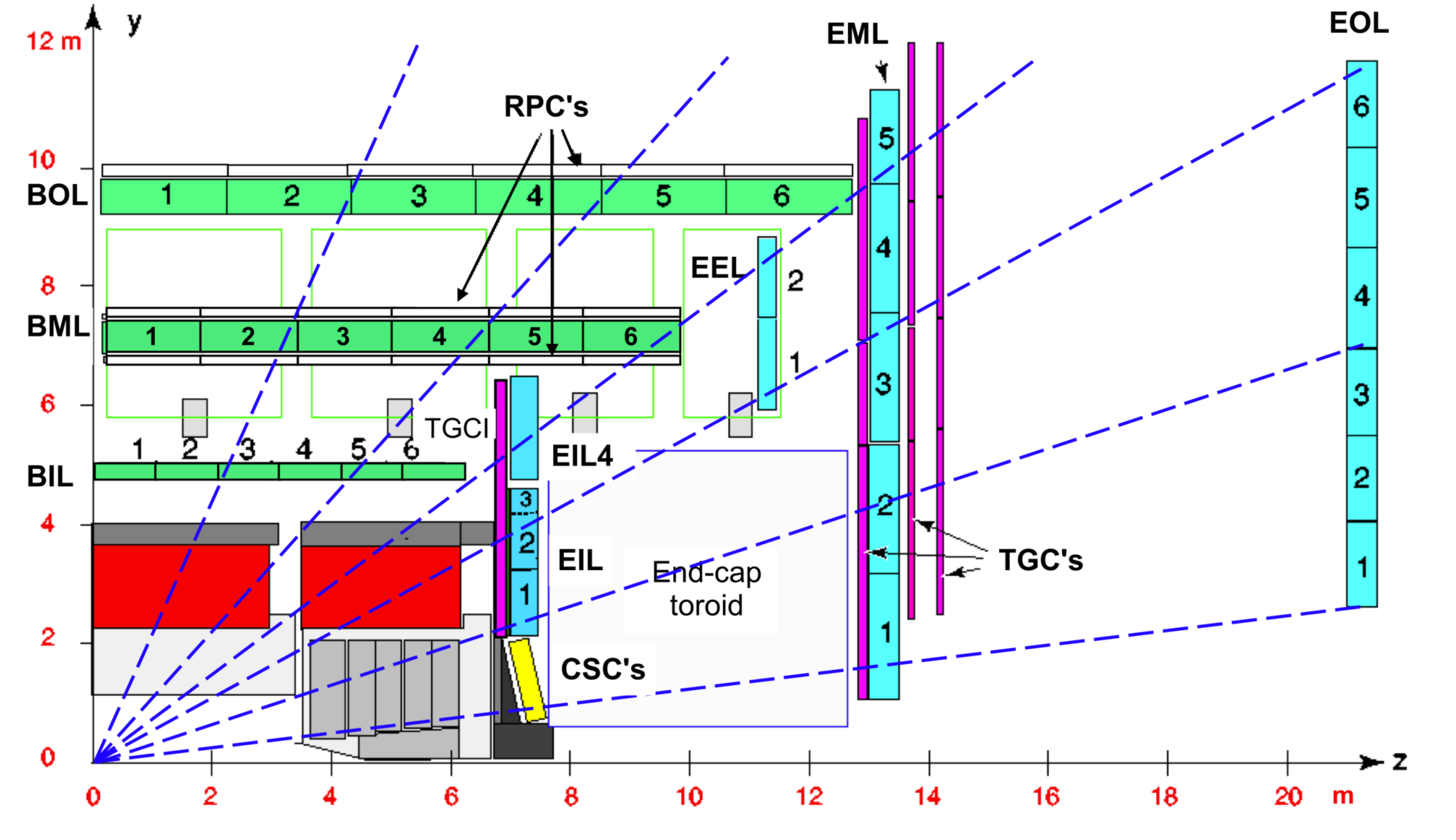
- Larger trigger acceptance for boosted heavy objects
- Opens the possibility to look for jet sub-structure at the trigger level

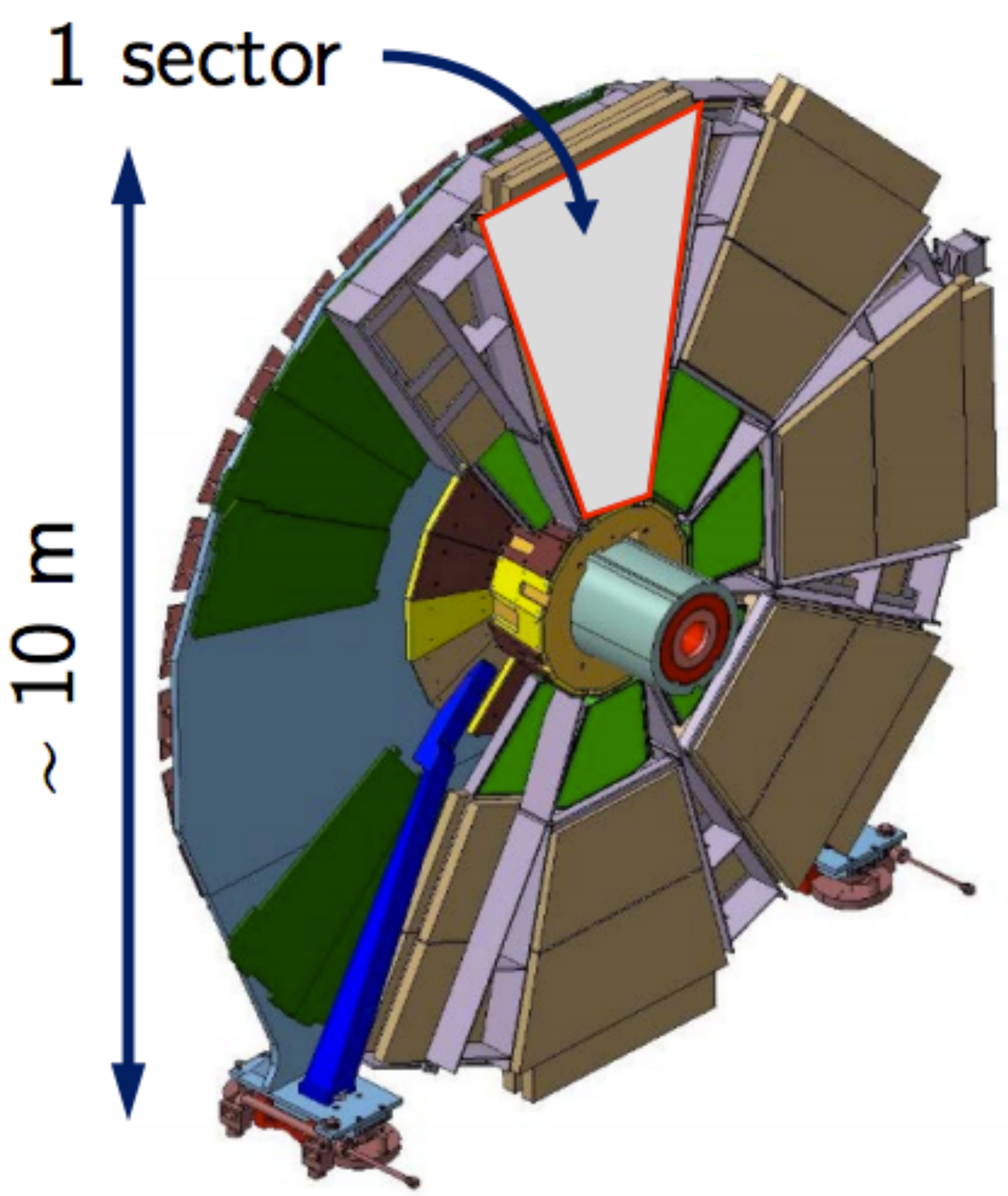


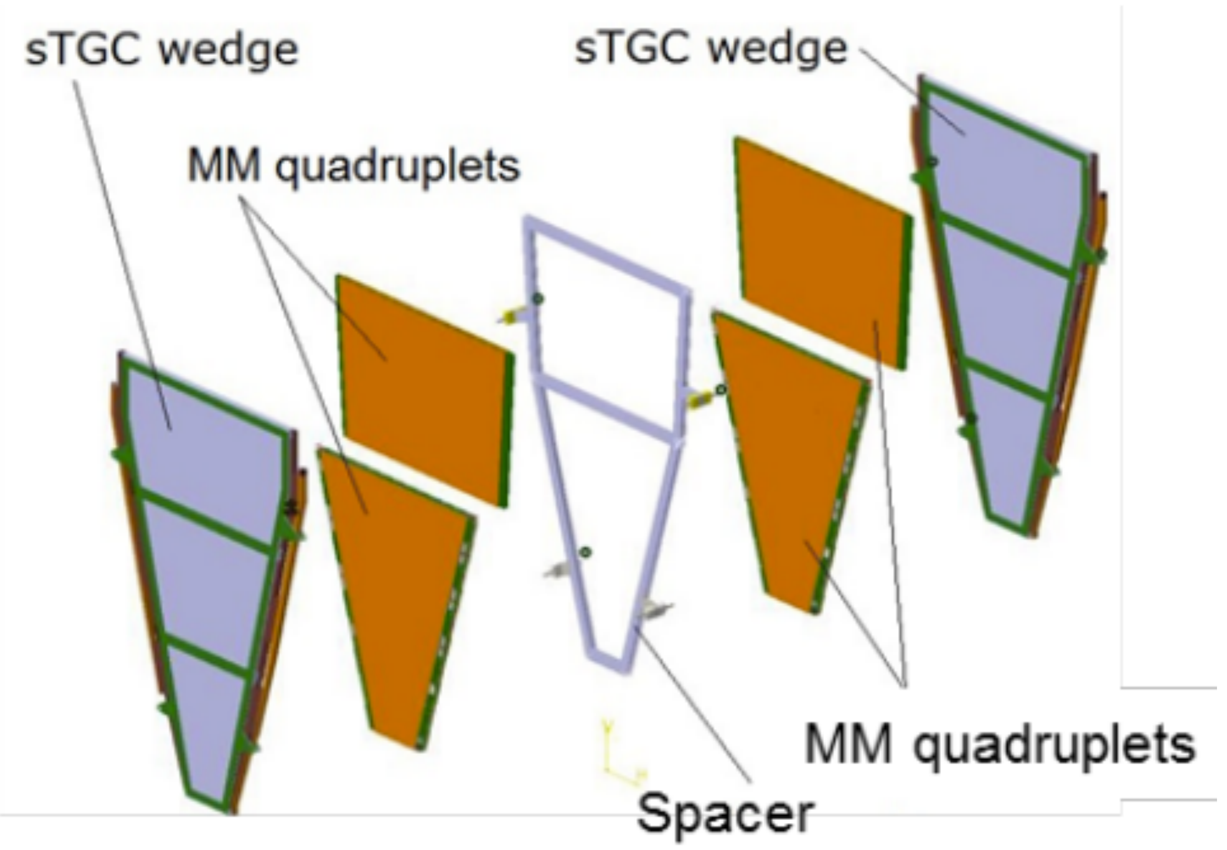


Above: gFEX Prototype v2

Phase-1 Strategy: Muons







Readout channels:

- MM: ~ 2.1 M
- sTGC: 280k (strip) + 46k (pads) + 28k (wires)

Current L1 Muon Trigger

- Fast Resistive Plate (RPC) and Thin Gap Chambers (TGC)
- Hardware (FPGA) pattern recognition

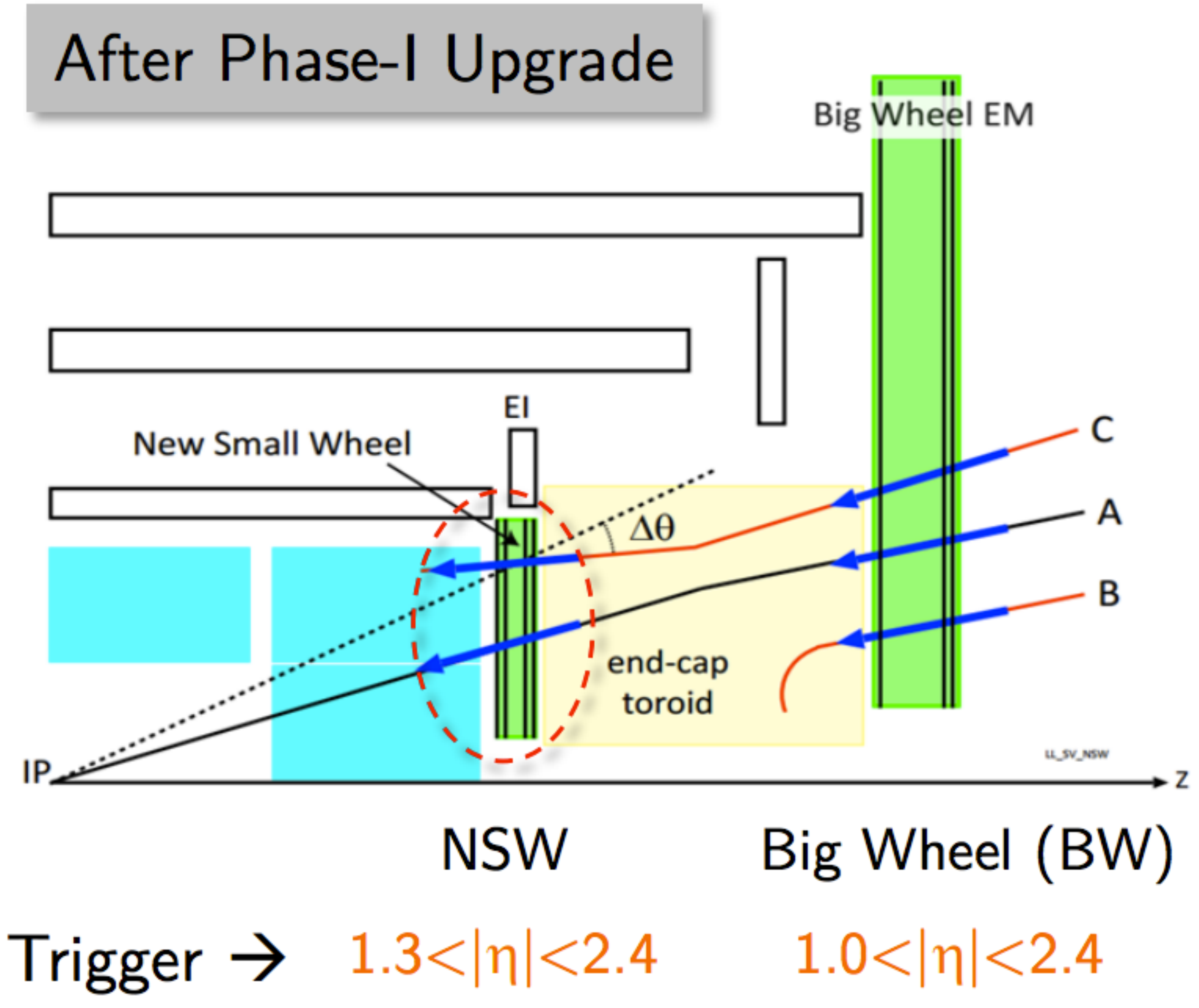
Trigger Rates driven by

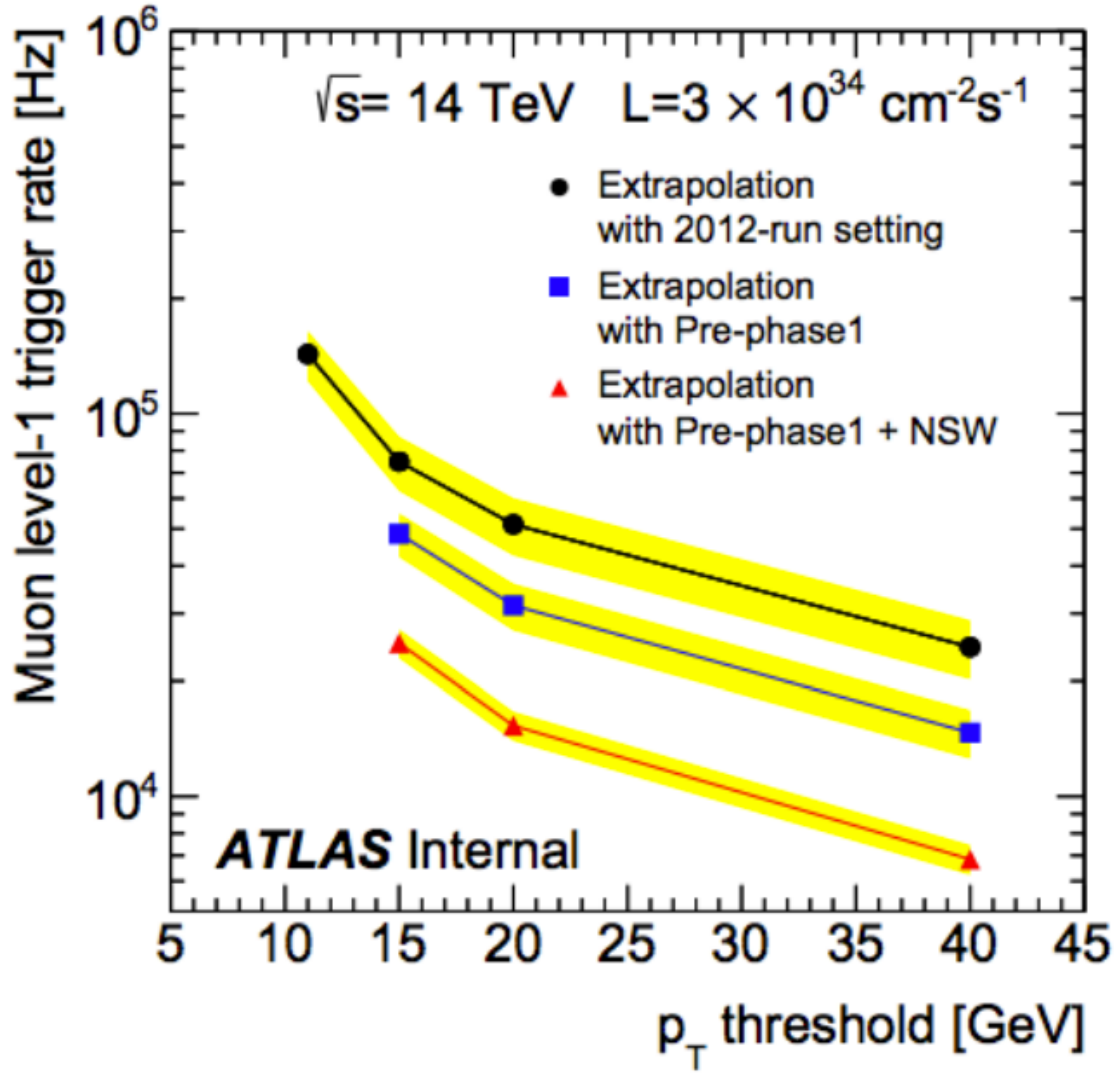
- Resolutions (muons below the nominal threshold)
- Fakes (charged particles not associated with the collision)

Phase-1 strategy

- Add new forward trigger chambers
  - New Small Wheel = Small-strip TGC + Micromegas
- Migrate HLT-style algorithms to L1 trigger
- Counteract increased forward fake rate

Phase-1 Upgrade: Muon System





Current L1 Muon Trigger

- Fast Resistive Plate (RPC) and Thin Gap Chambers (TGC)
- Hardware (FPGA) pattern recognition

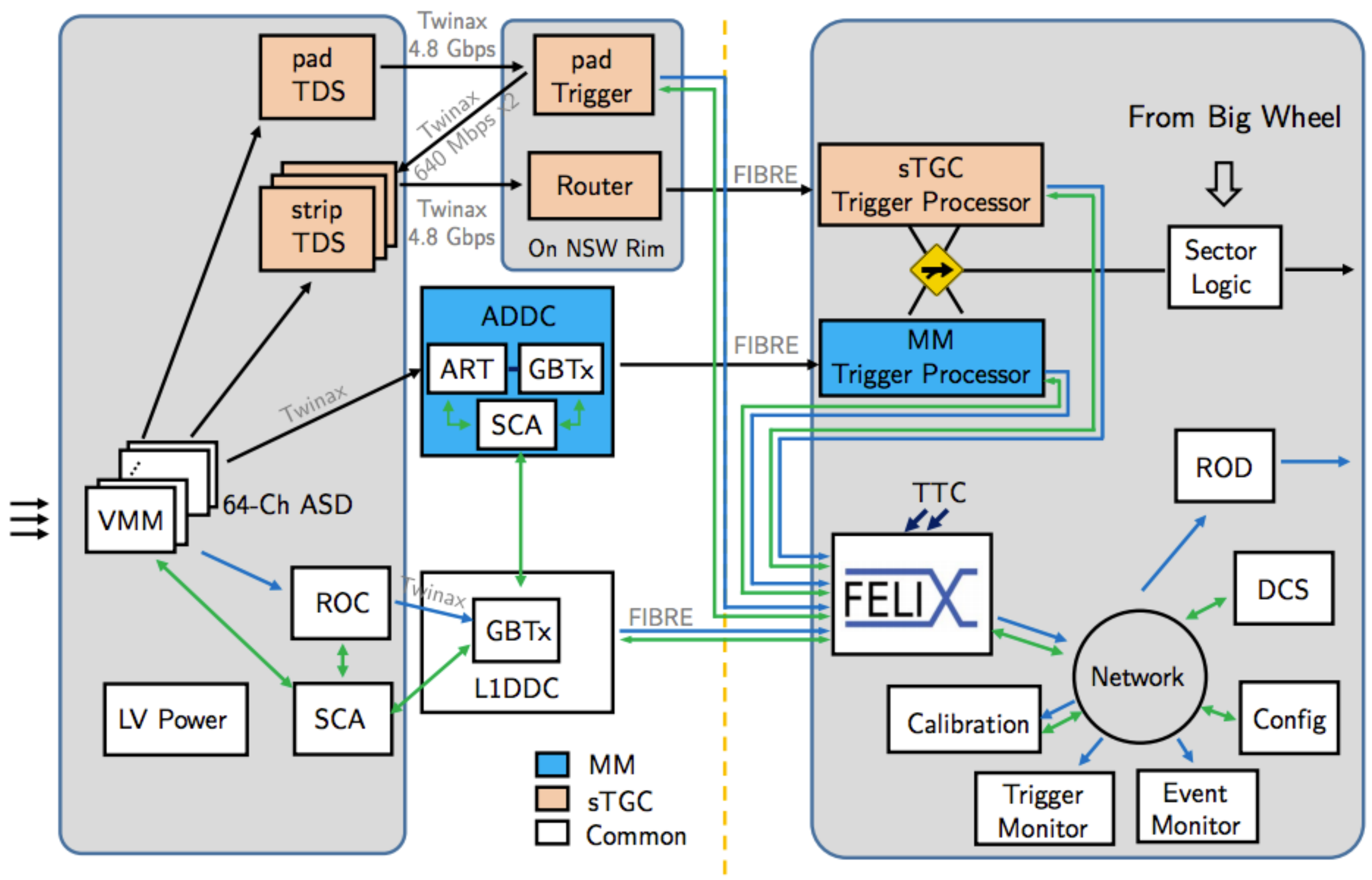
Trigger Rates driven by

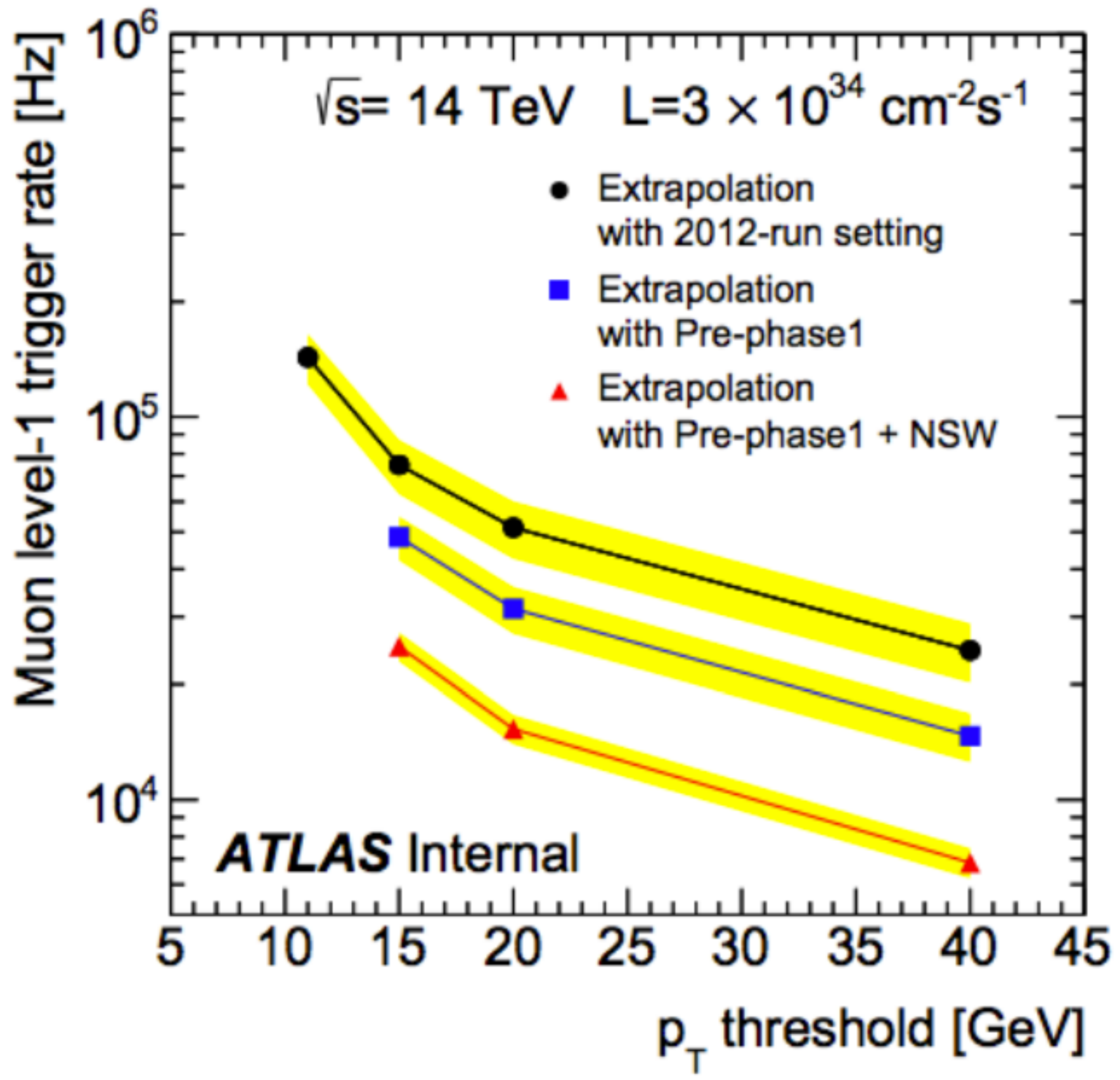
- Resolutions (muons below the nominal threshold)
- Fakes (charged particles not associated with the collision)

Phase-1 strategy

- Add new forward trigger chambers
  - New Small Wheel = Small-strip TGC + Micromegas
- Migrate HLT-style algorithms to L1 trigger
- Counteract increased forward fake rate

Phase-1 Upgrade: Muon System





Current L1 Muon Trigger

- Fast Resistive Plate (RPC) and Thin Gap Chambers (TGC)
- Hardware (FPGA) pattern recognition

Trigger Rates driven by

- Resolutions (muons below the nominal threshold)
- Fakes (charged particles not associated with the collision)

Phase-1 strategy

- Add new forward trigger chambers
  - New Small Wheel = Small-strip TGC + Micromegas
- Migrate HLT-style algorithms to L1 trigger
- Counteract increased forward fake rate

HL-LHC Upgrade Motivations

Studies of the light Higgs require precision at electroweak scale
- Higgs couplings are a window into new physics

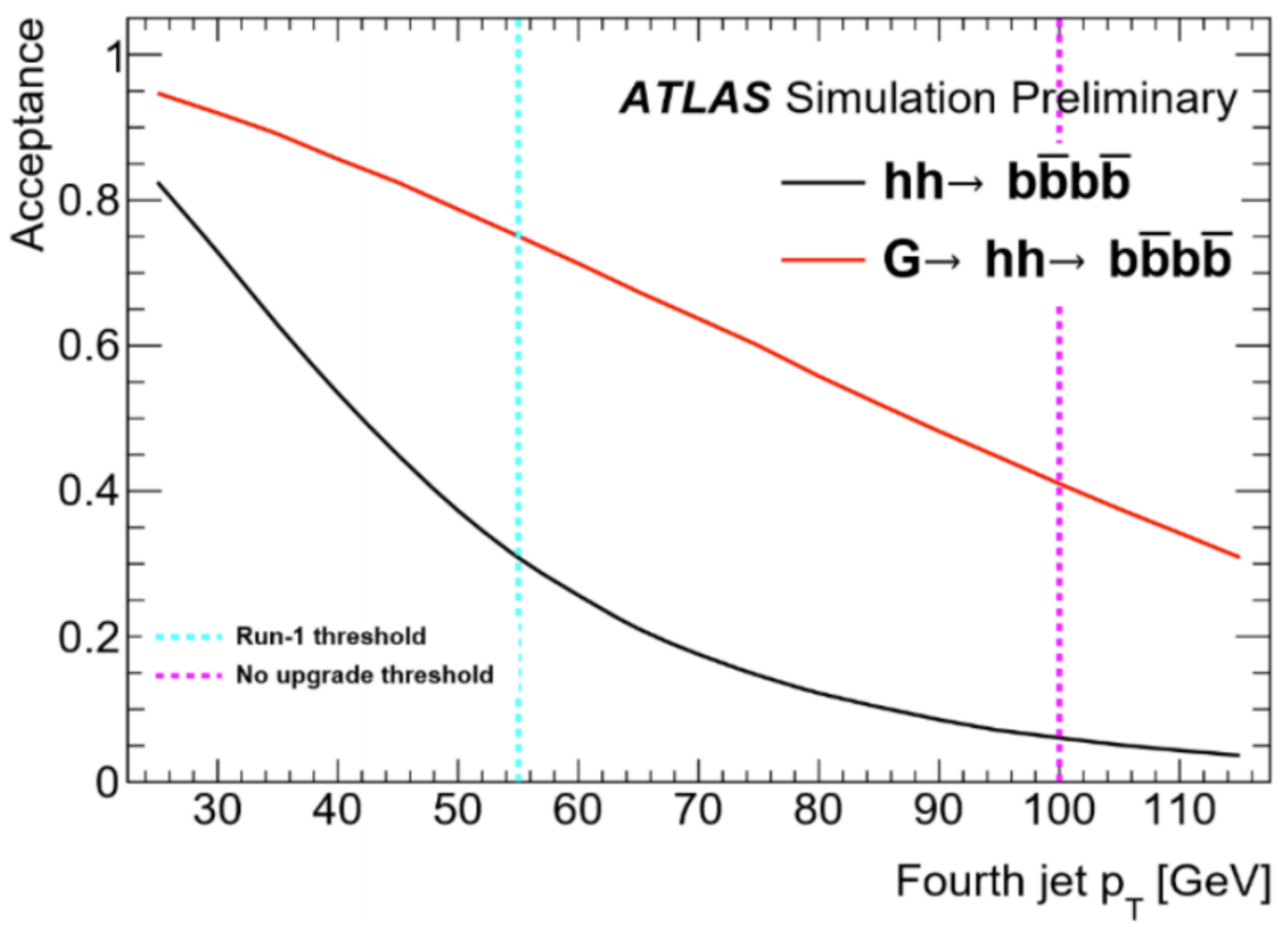
Subtle BSM physics can only be found if the SM is well understood
- Searches for physics may require low cross section processes with large backgrounds, e.g. SUSY

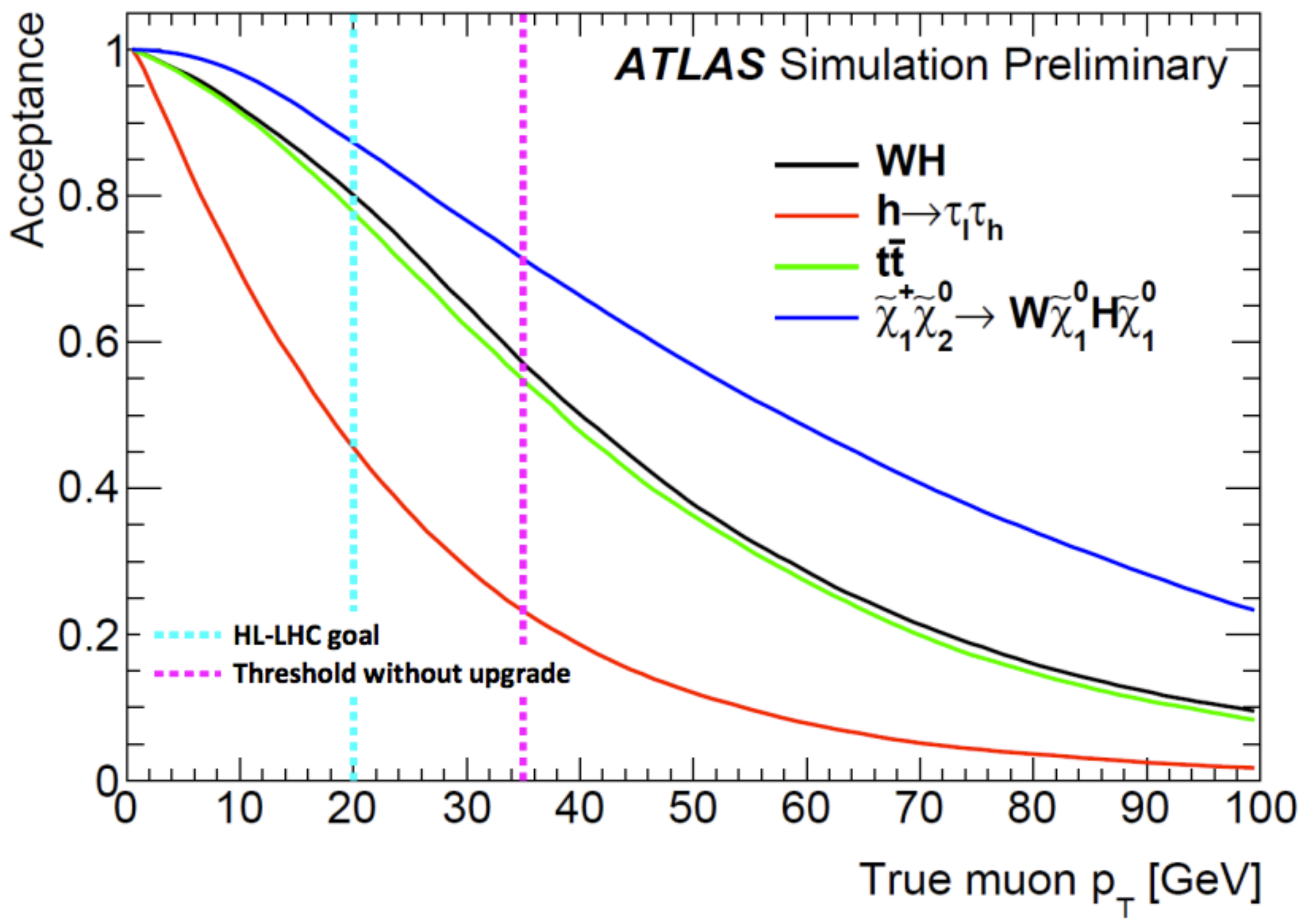
European Strategy report (ECFA), P5 (DOE/NSF)
- HL-LHC needs at least 3000 fb^{-1}
- 10 years at $L = 7.5\times10^{34}$ $cm^{-2}s^{-1}$

Target thresholds at or better than Run 2
- Single electron 22 GeV
- Single muon 20 GeV
- Compare to 25 GeV in Run 2

Setting thresholds to keep total rate to 100 kHz incompatible with physics aims
- for single leptons would imply 32 GeV electron and 40 GeV muon

Item	Run 1 Offline p_T Threshold [GeV]	Phase-I Level-1 system performance at $L = 7.5 \times 10^{34}$ cm^{-2}s^{-1}: Offline Threshold for Phase-II Goal [GeV]	Level-1 Rate [kHz]
isolated Single e	25	22	200
single μ	25	20	40
di-γ	25	25	8
di-e	17	15	90
di-μ	12	11	10
$e-\mu$	17,6	17,12	8
single τ	100	150	20
di-τ	40,30	40,30	200
single jet	200	180	60
four-jet	55	75	50
E_T^{miss}	120	200	50
jet + E_T^{miss}	150,120	140,125	60



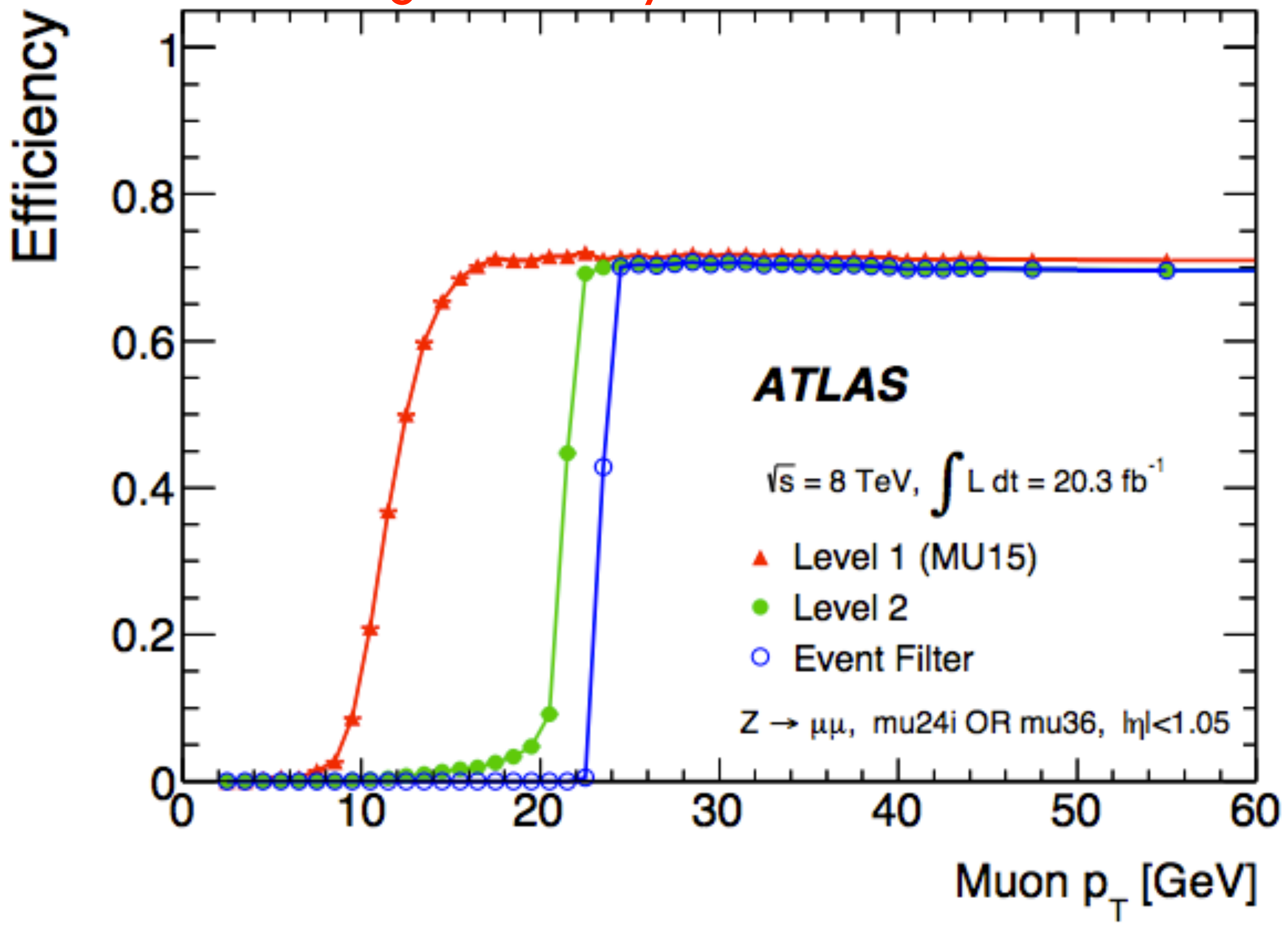


HL-LHC Upgrade Motivations

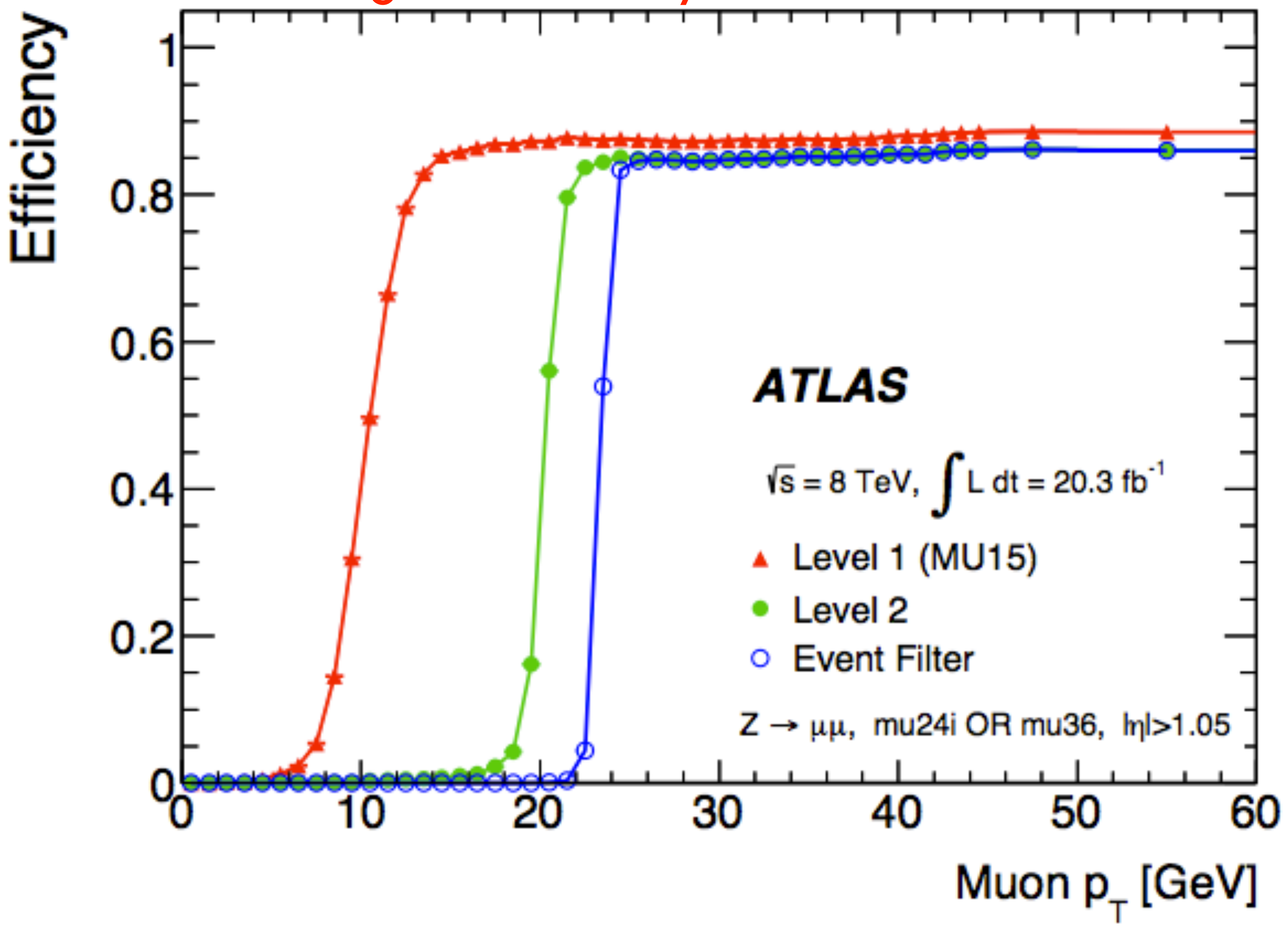
Muon barrel efficiency and acceptance are crucial trigger issues for ATLAS

- Largely driven by geometrical acceptance
- Purity cannot be relaxed because of high background rates

Existing Barrel System ~70% efficient



Existing Forward System ~90% efficient



Without changes barrel efficiency likely to be worse due to trigger chamber aging

Strategy: Redundancy added into hardware trigger

- in barrel add new muon trigger chambers and include precision muon detectors
- in forward region include precision muon detectors (& don't forget NSW Phase-1 upgrade)

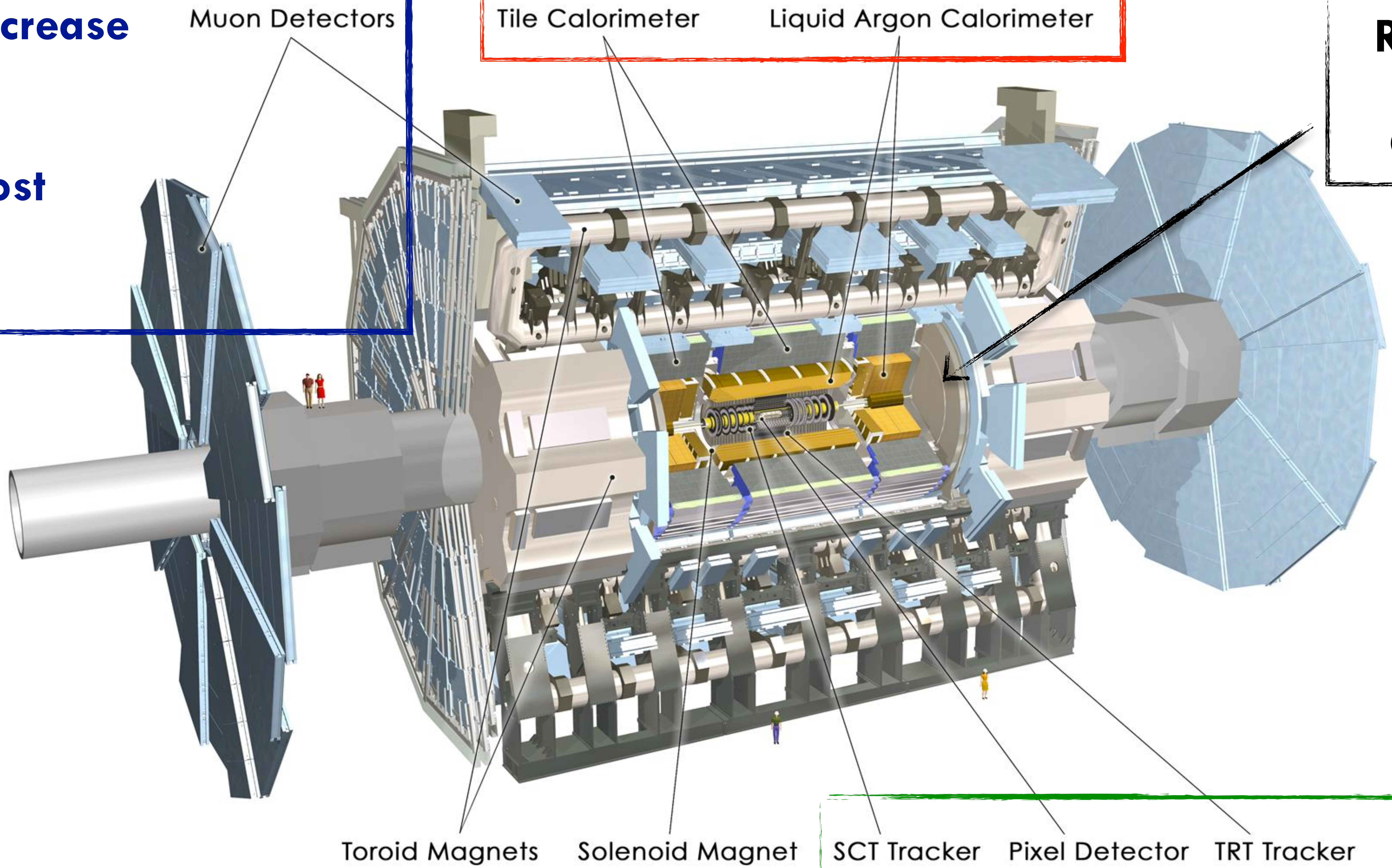
ATLAS HL-LHC Upgrade Overview

Add new readout to improve coverage and increase efficiency

Replace Innermost Forward Muon Chambers

New Calorimeter Electronics

Replace Some Forward Calorimeters



New Inner TracKer - silicon strips and pixels

TDAQ System Design Options

Level-0 Muon & Calo used to make initial fast rejection and identify Regions of Interest

- 1 MHz accept rate, trigger latency 6 μs, minimum detector latency 10 μs

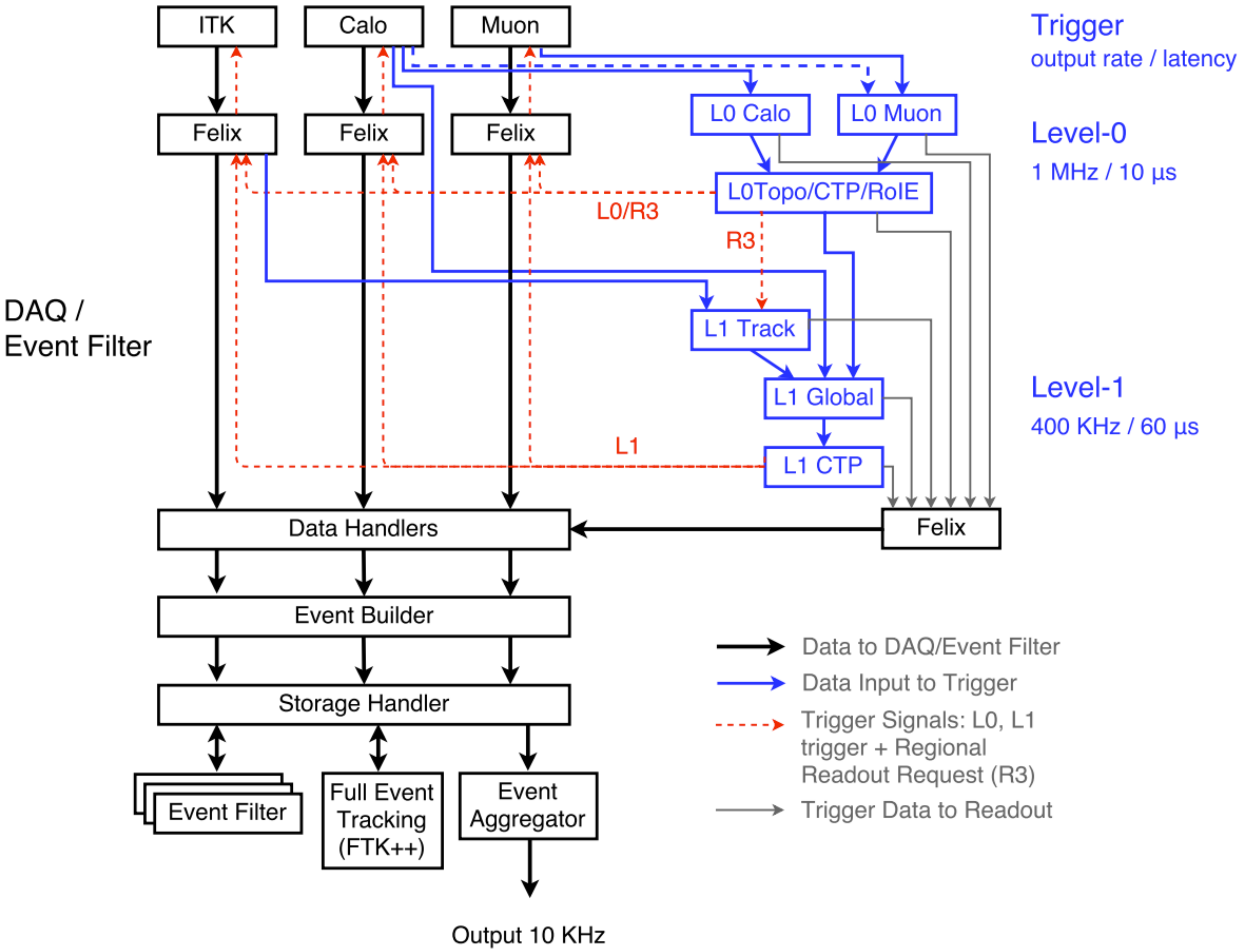
Level-1 hardware track trigger and high resolution calo data provide further rejection

L1Track and L0Calo/L0Muon feed to L1Global processor

- 400 kHz accept rate, trigger latency 30 μs, minimum detector latency 60 μs

Event Filter (commodity farm + HW tracking) delivers a factor 40 reduction down to output rate of 10 kHz

- FTK++ full event tracking processor down to p_T > 1 GeV at 100 kHz



TDAQ System Design Options

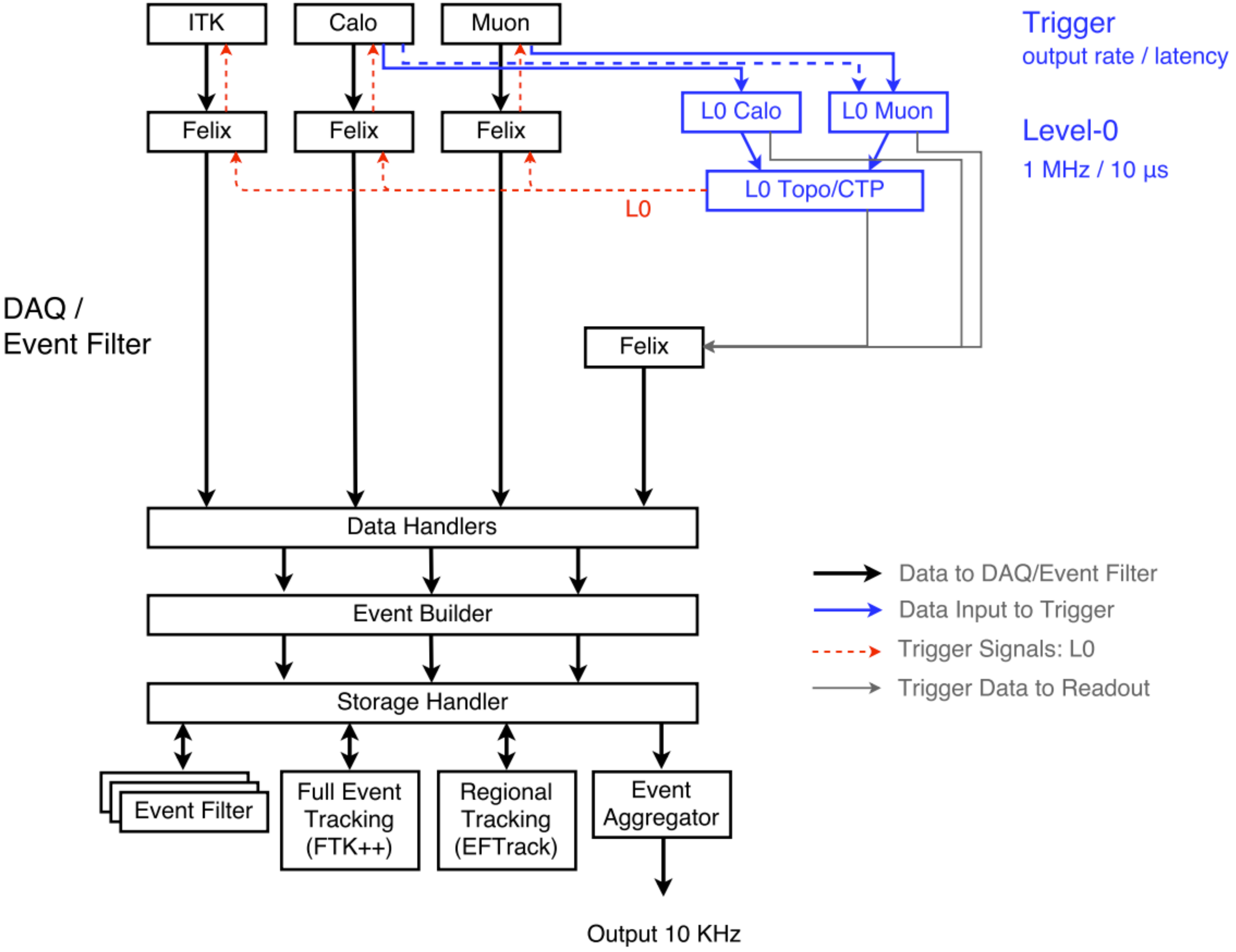
Single level hardware trigger straight into Data Handler

- L1 hardware trigger and RoI Engine relocated to EF hardware & software
- Readout less complex but less flexible
- 1 MHz accept rate, trigger latency near 6 μs, minimum detector latency around 10 μs

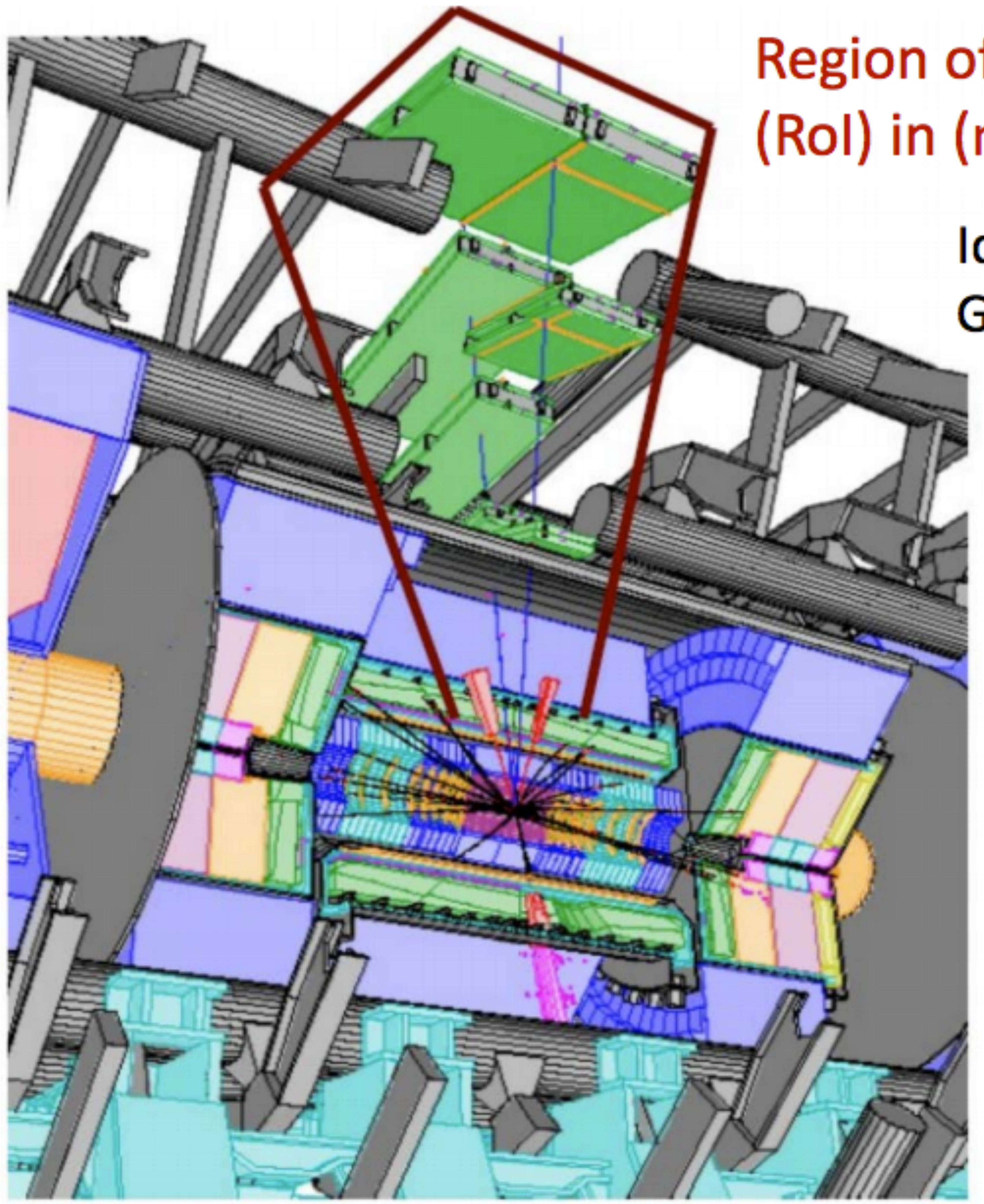
Event Filter now delivers a factor 100 reduction down to output rate of 10 kHz

- Naively a factor 2.5 larger than in two level system, at least 10 times larger than Phase-1
- EFTrack regional tracking processor alongside FTK++ full event tracking

Also looking at L0+L1 options in which lower latency is traded for higher L0 accept rate



HL-LHC Level-0 Trigger



L0 Calo:

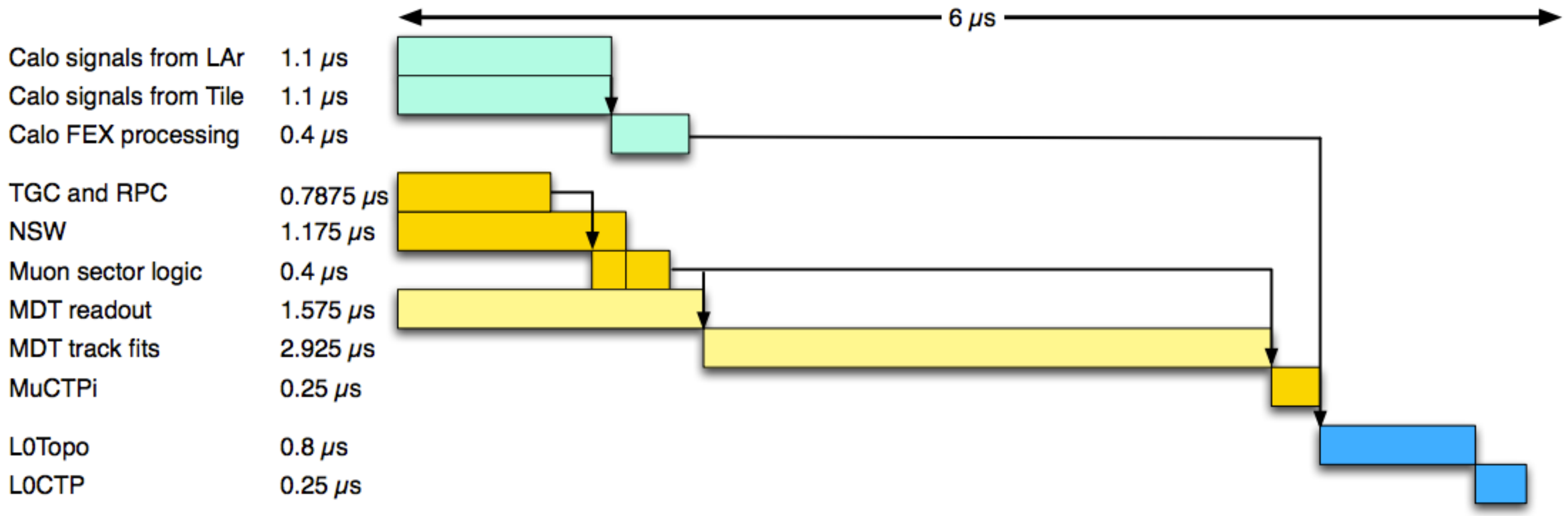
- Existing Phase-1 L1Calo trigger system becomes L0Calo trigger for HL-LHC
- FEX system receives firmware upgrade; largely same hardware as Run 3

L0 Muon:

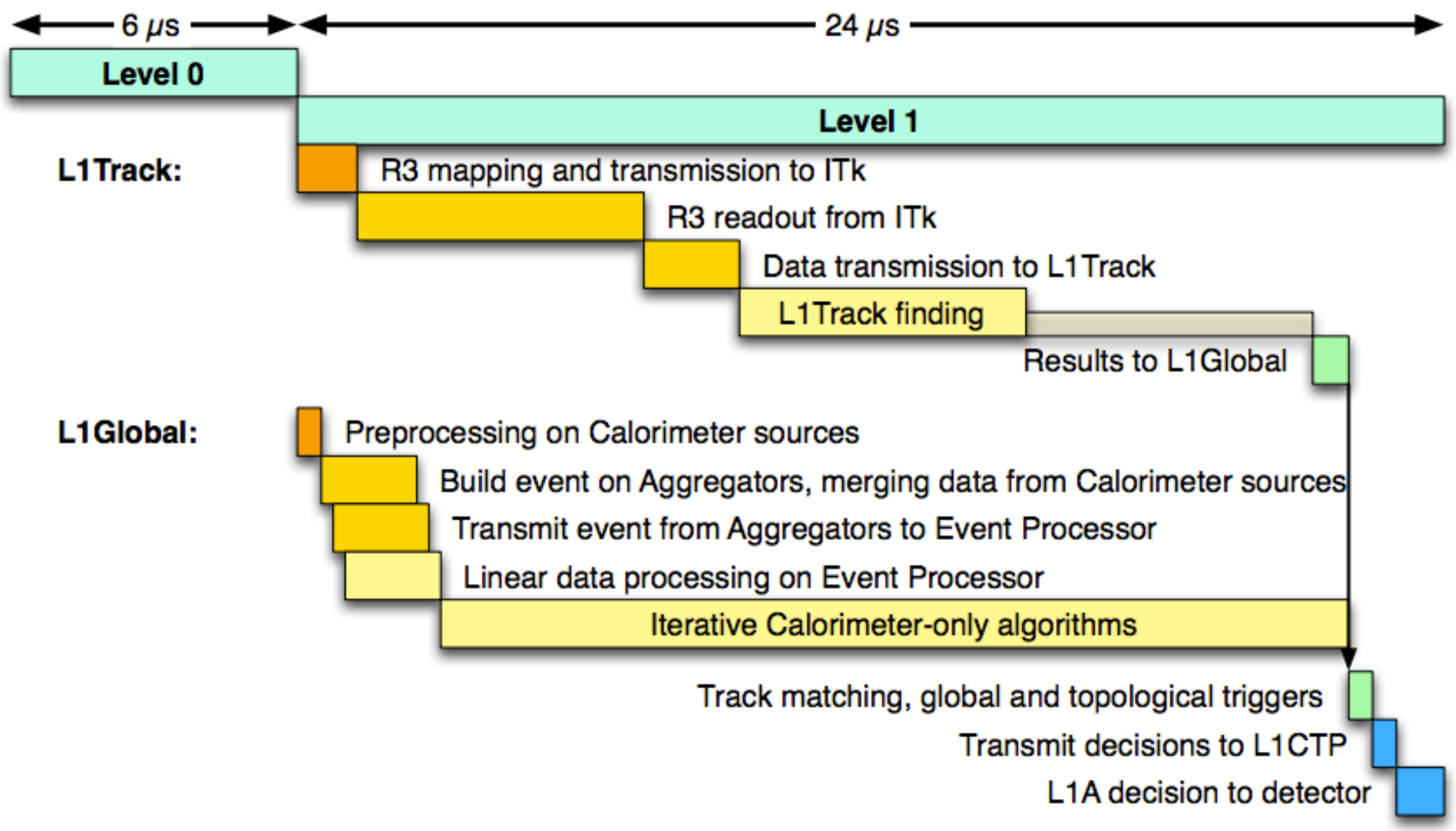
- New readout and improved coverage to increase efficiency
- Latency now long enough to use precision MDTs for sharper turn on

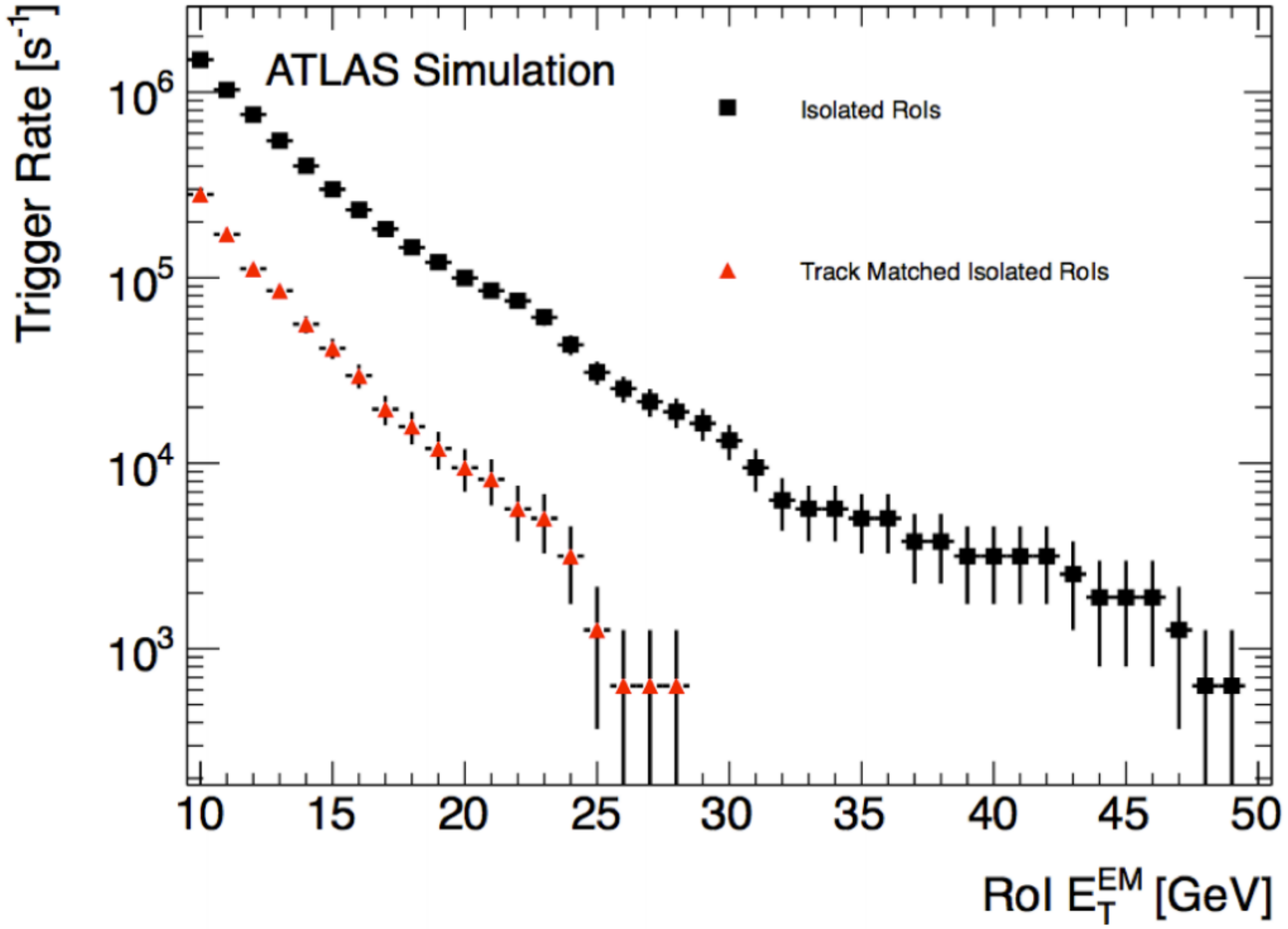
L0Topo/Central Trigger Processor/RoIEngine

- Receives trigger objects from L0Calo and L0Muon
- Performs complex trigger selections (invariant mass, missing transverse energy, etc.)
- On L0-Accept, the RoIEngine calculates the Regional Readout Requests to send back to the detectors
- RoIs cover at most 10% of detector => 100 kHz equivalent rate for readout



HL-LHC Level-1 Track Trigger





Level-1 Track Trigger receives ITk data from regions around RoIs contributing to L0-Accept

- Finds tracks in those regions above 4 GeV pT cut
- Quasi-offline resolution, reconstruction efficiency at least 95% for offline tracks
- Rejection factor of 5 for single lepton triggers, pileup track resolution < ~10 mm

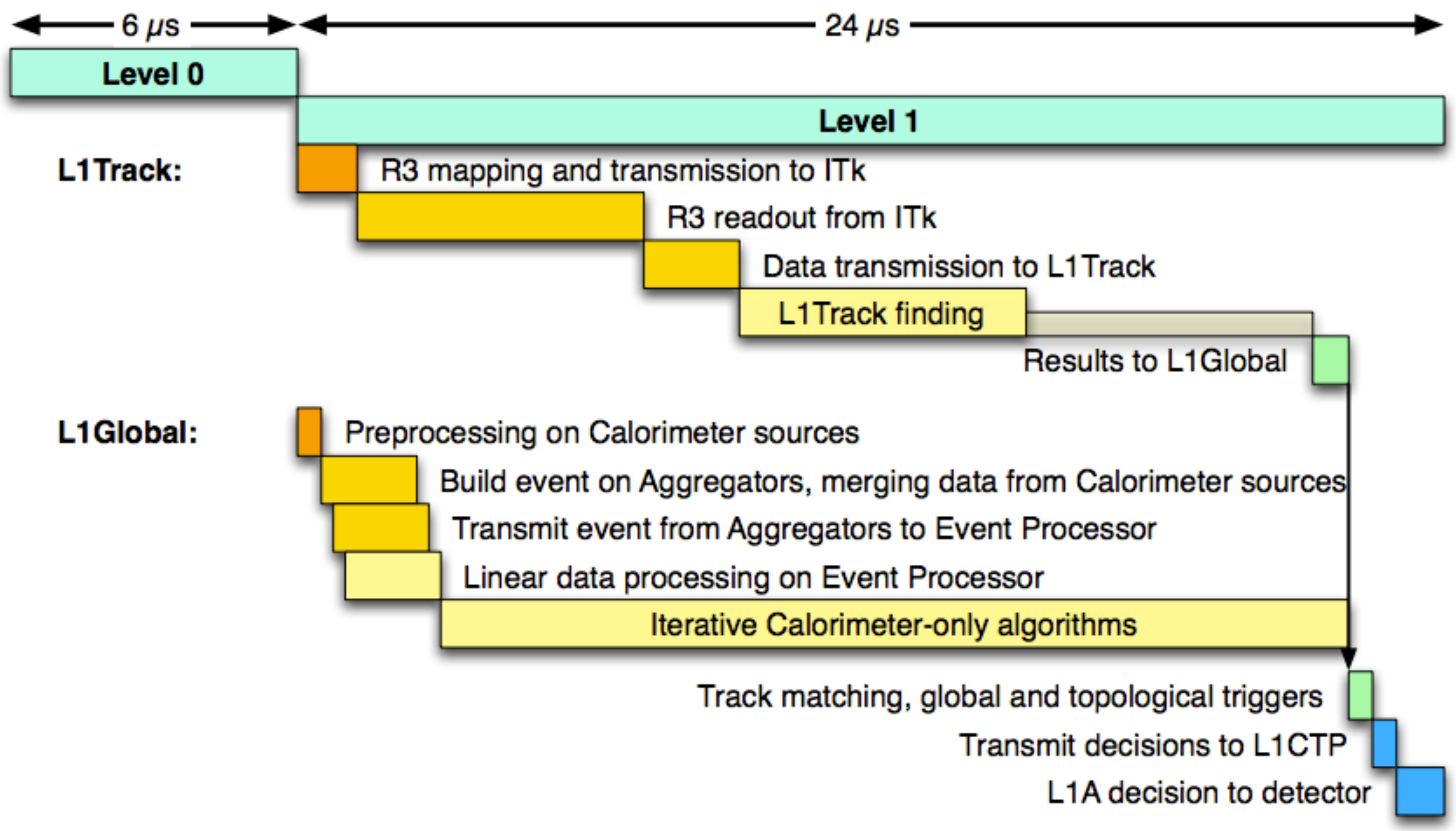
Regional readout of 10% ITk in ~6 μs

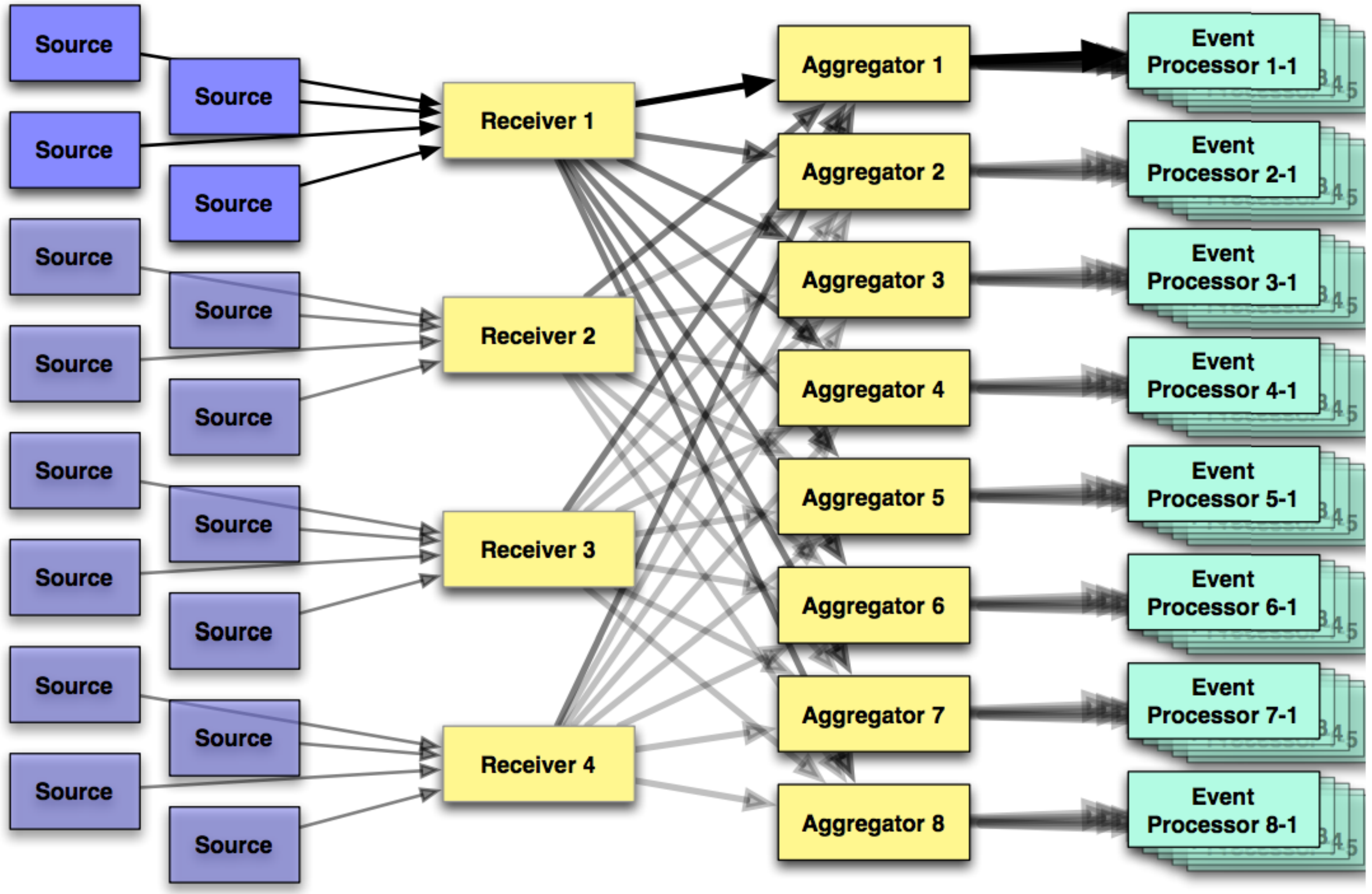
- Strip front-end readout chips with double-buffer capability
- Full pixel readout at 1 MHz

FTK next-gen associative memory chip and track-fit on FPGA

- 500k track patterns per AM chip at 200 MHz
- 4 fit/ns on modern FPGA

HL-LHC Level-1 Global Trigger





40 Event Processor time-multiplexed system, better than 0.1% dead time at 1 MHz
- Receives calorimeter information from every cell, L0Muon objects, L1 tracks

Input up to 8 events in parallel each taking 2 μs to arrive
- Linear processing of calorimeter data on arrival, Iterative processing for calorimeter jets and MET

Global and topological selections: Tracks vital for taus and pileup suppression

HL-LHC Trigger Strategy

Reduction in two hardware level system at Level-1 mainly using tracks from L1Track

Lower rate triggers for multiple low-pT leptons, taus, jets and missing transverse energy

- e.g. single electron 200 kHz Level-0, 40 kHz Level-1, 2.2 kHz output
- also improvements from individual cell information for calorimeter at Level-1

In single level system Level-0 rates feed directly into Event Filter

Item	Offline p_T Threshold [GeV]	Offline $\|\eta\|$	L0 Rate [kHz]	L1 Rate [kHz]	EF Rate [kHz]
isolated single e	22	< 2.5	200	40	2.20
forward e	35	$2.4 - 4.0$	40	8	0.23
single γ	120	< 2.4	66	33	0.27
single μ	20	< 2.4	40	40	2.20
di-γ	25	< 2.4	8	4	0.18
di-e	15	< 2.5	90	10	0.08
di-μ	11	< 2.4	20	20	0.25
$e - \mu$	15	< 2.4	65	10	0.08
single τ	150	< 2.5	20	10	0.13
di-τ	40,30	< 2.5	200	30	0.08
single jet	180	< 3.2	60	30	0.60*
large-R jet	375	< 3.2	35	20	0.35*
four-jet	75	< 3.2	50	25	0.50*
H_T	500	< 3.2	60	30	0.60*
E_T^{miss}	200	< 4.9	50	25	0.50*
jet + E_T^{miss}	140,125	< 4.9	60	30	0.30*
forward jet**	180	3.2 - 4.9	30	15	0.30*
Total			$\sim$1000	$\sim$400	$\sim$10

Summary

ATLAS has a plan to meet the challenges of HL-LHC

- Higgs, BSM and SM physics all benefit from low thresholds

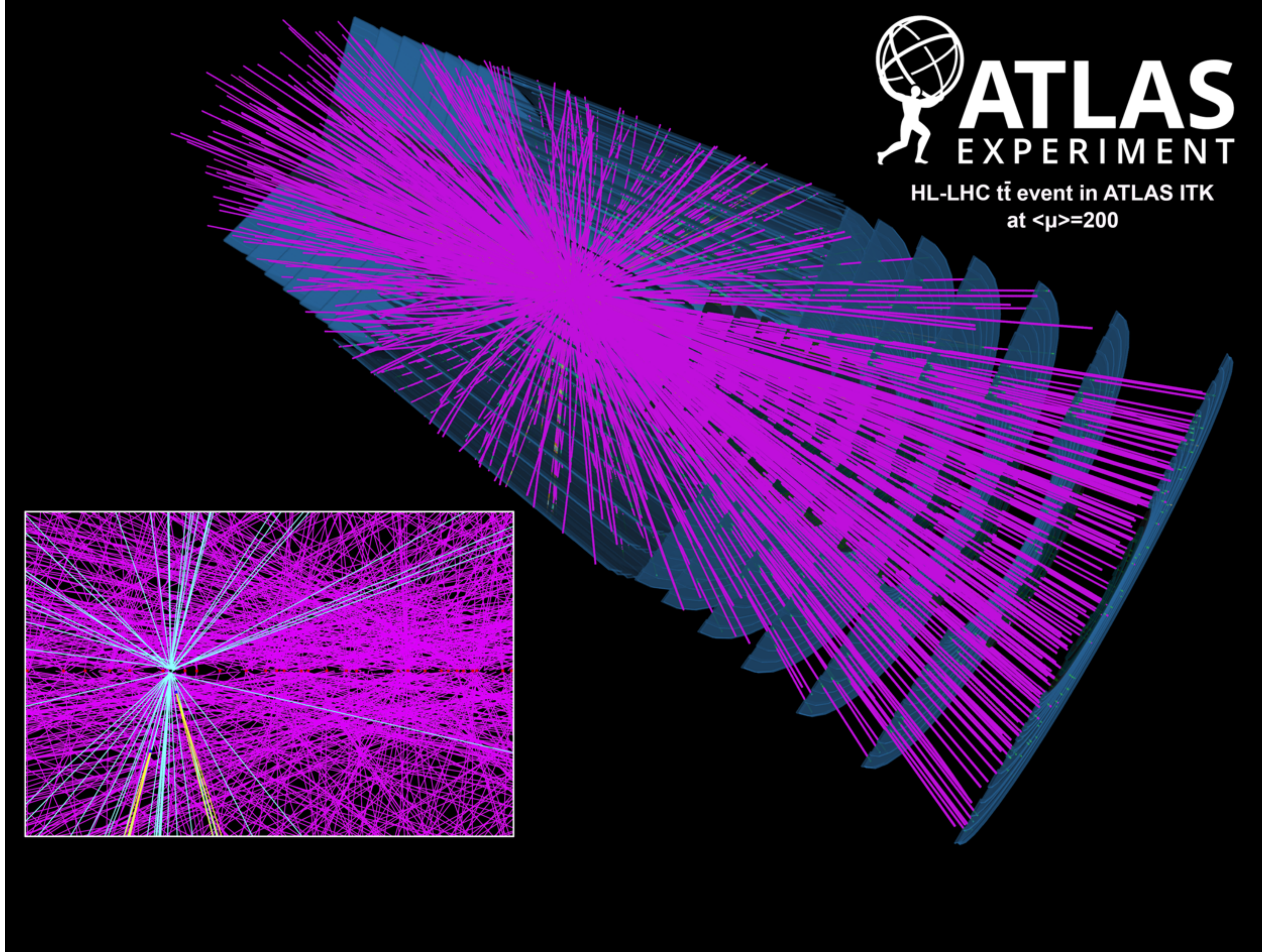
Two-level hardware trigger based on Regions of Interest, also a single level option.

- Phase-I trigger provides basis for Phase-II system

Track info from inner tracker crucial in subsequent levels

- Factor 5 reduction in single lepton triggers, also vital for taus and pileup suppression
- Regional tracking in either second hardware level or as coprocessor to Event Filter

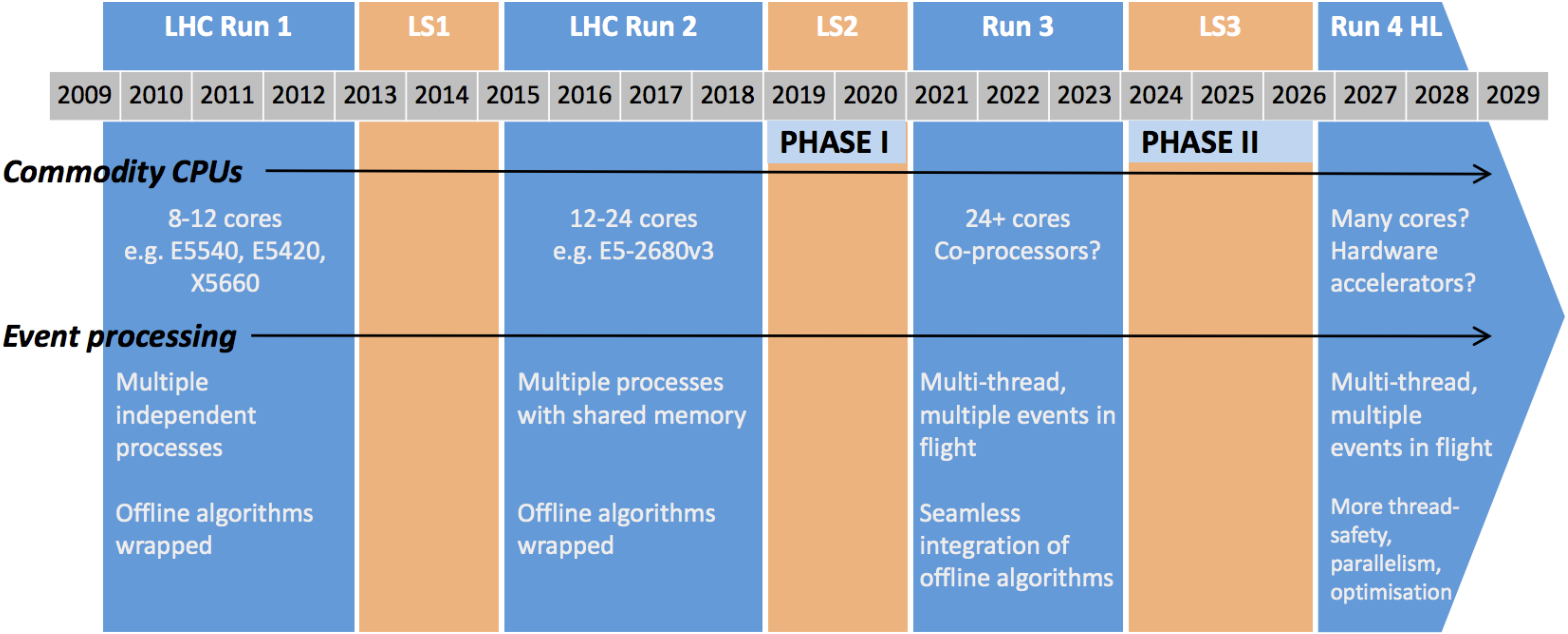
Baseline will be documented in a TDR, due Q4/2017



https://twiki.cern.ch/twiki/bin/view/AtlasPublic/UpgradeEventDisplays

The End

High Level Trigger Evolution



HL-LHC Upgrade Motivations

Studies of the light Higgs boson require precision at electroweak scale

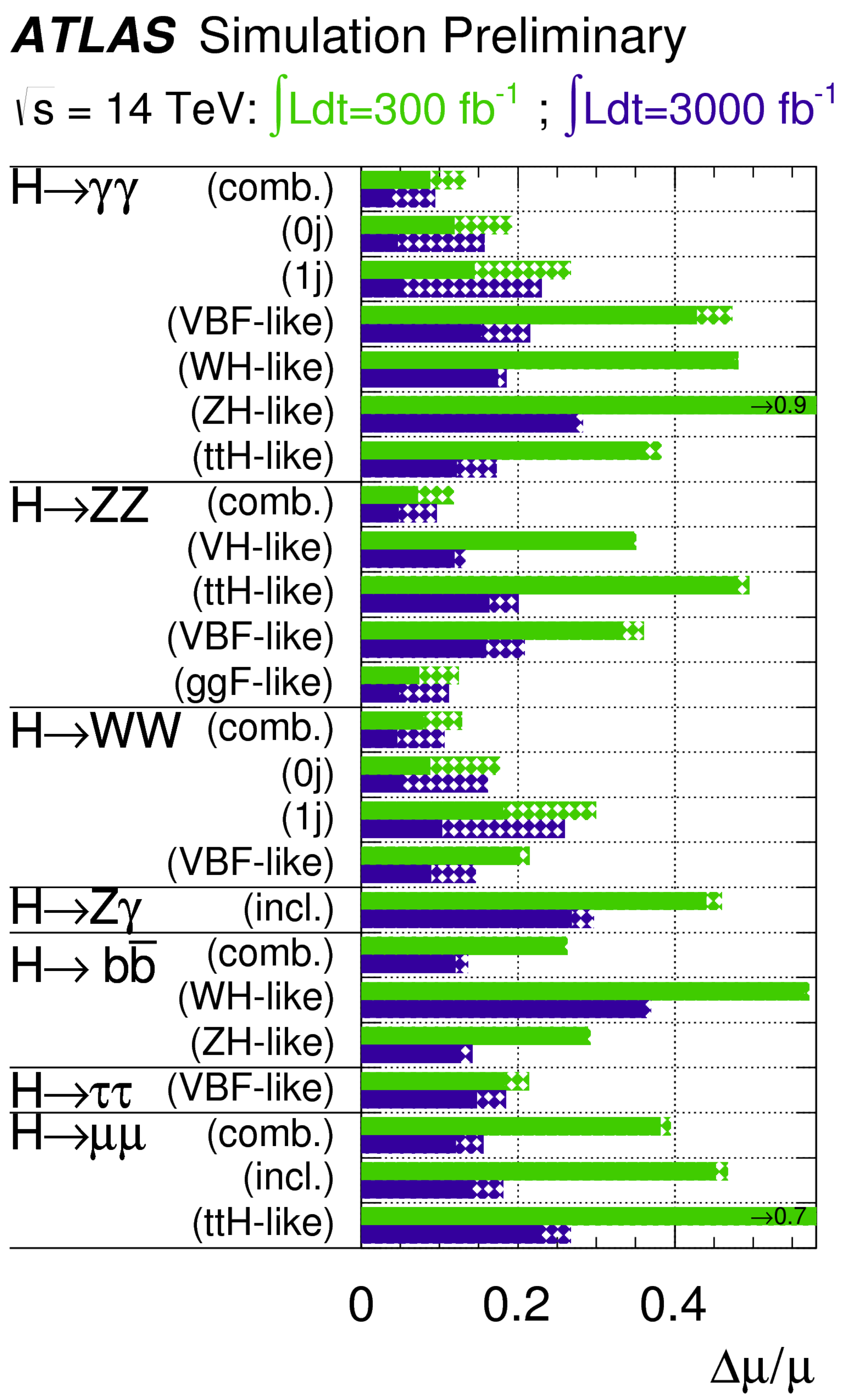
- Higgs couplings are a window into new physics

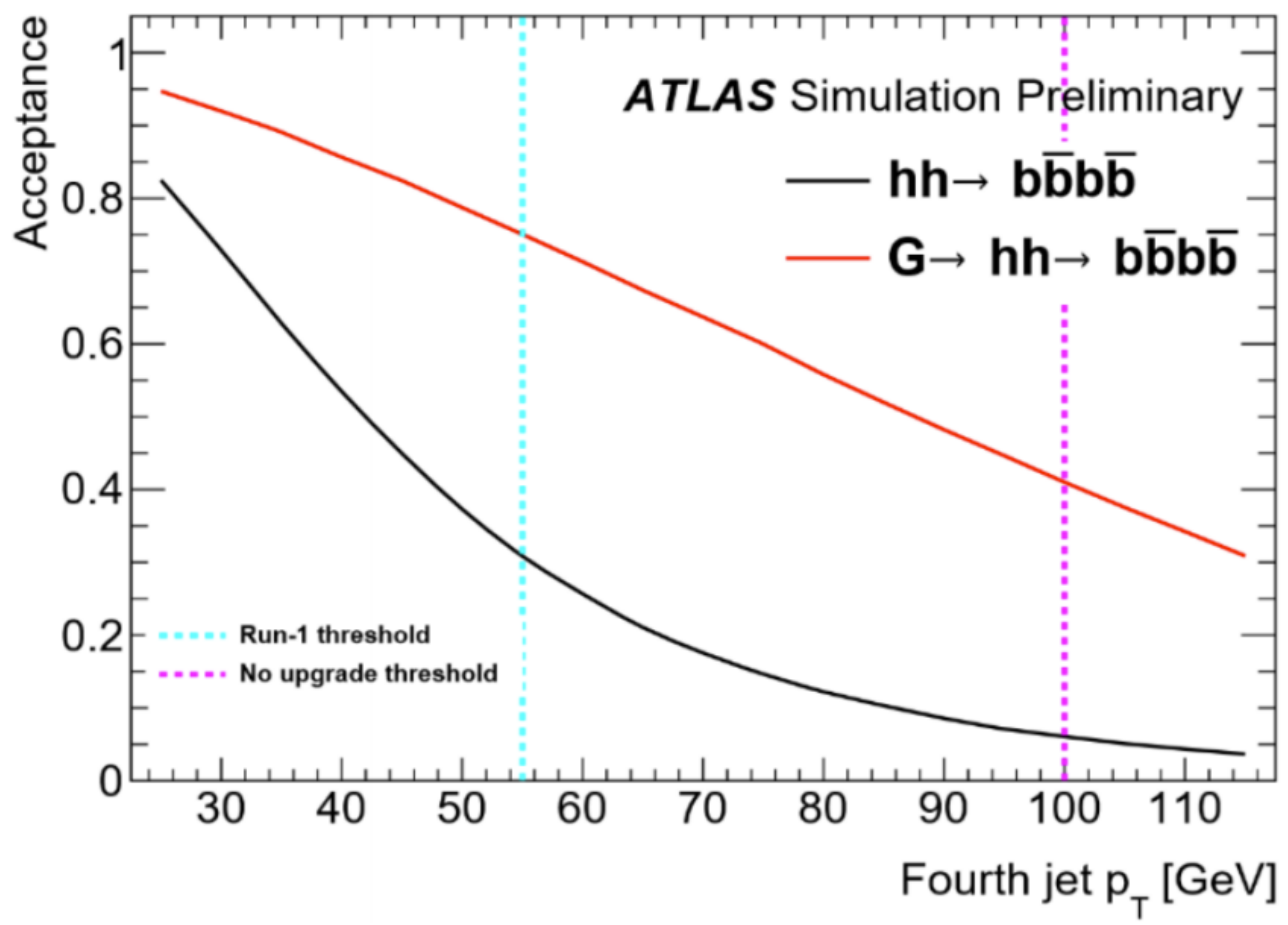
Subtle BSM physics can only be discovered if the SM is well understood

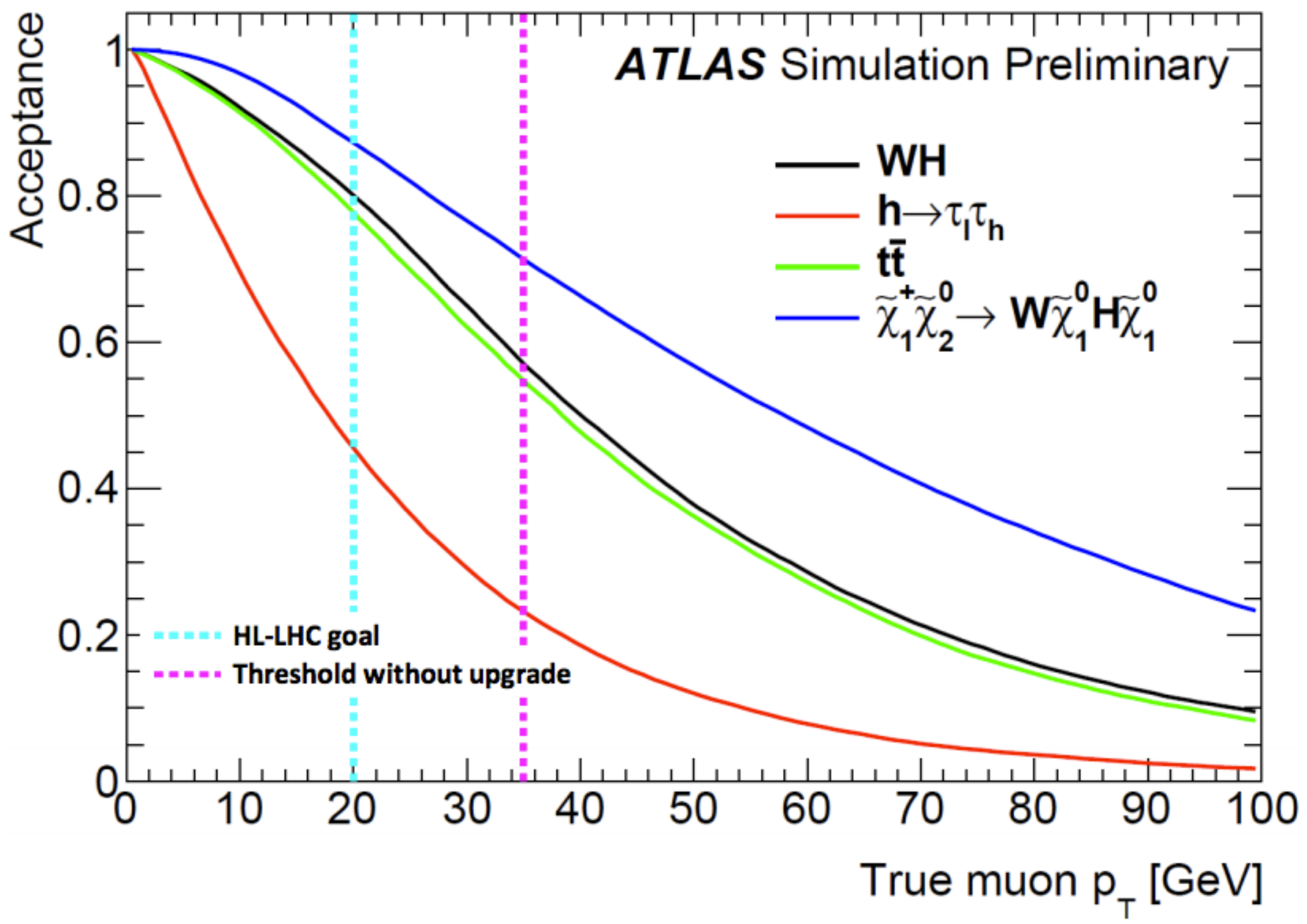
- Searches for physics may require low cross section processes with large backgrounds, e.g. SUSY

European Strategy report (ECFA), P5 (DOE/NSF)

- HL-LHC needs at least 3000 fb^{-1} (10 years at $L = 7.5\times10^{34}\ cm^{-2}s^{-1}$)







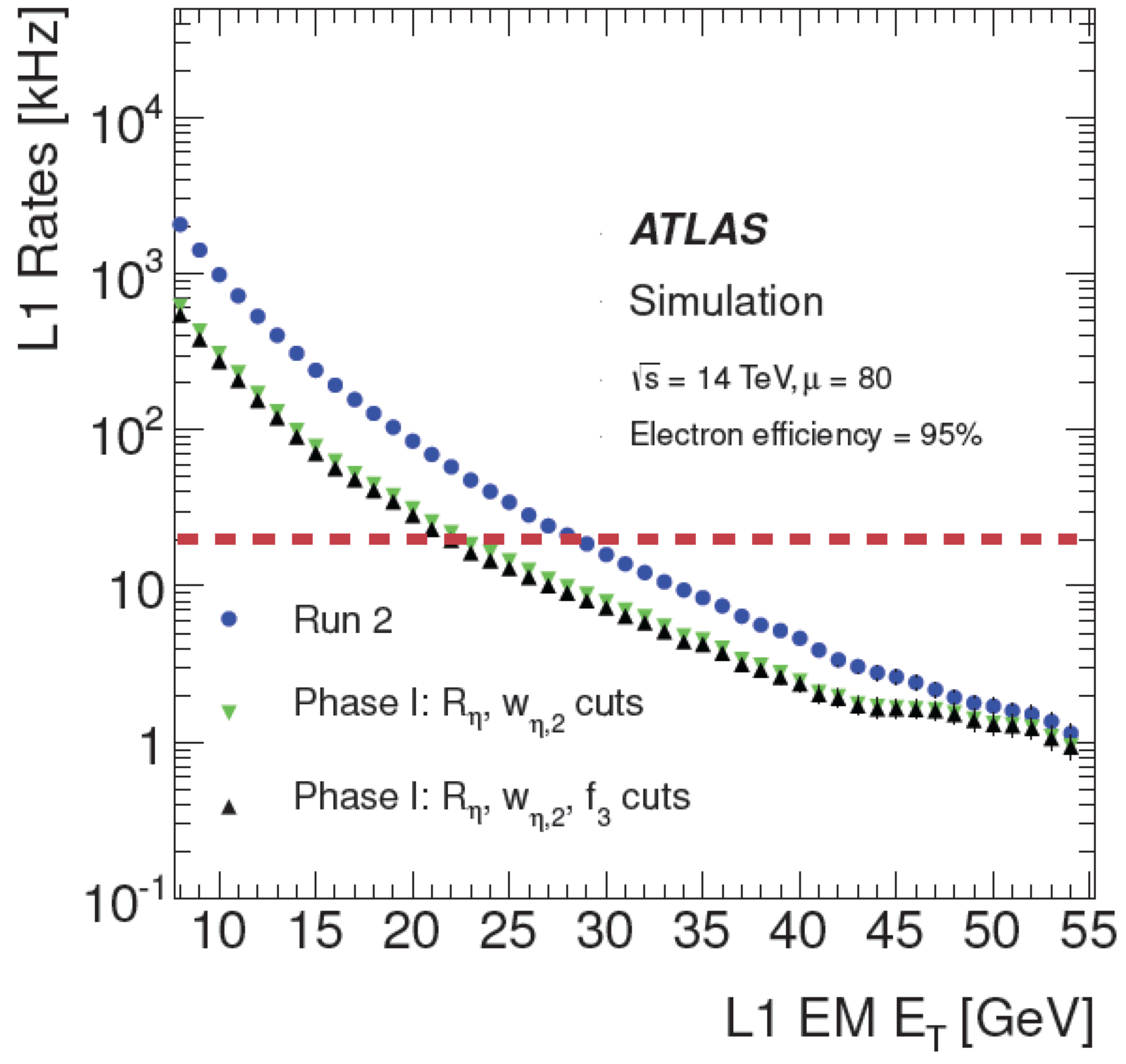
Phase-1 Performance

Phase-I Upgrade Expected Performance:

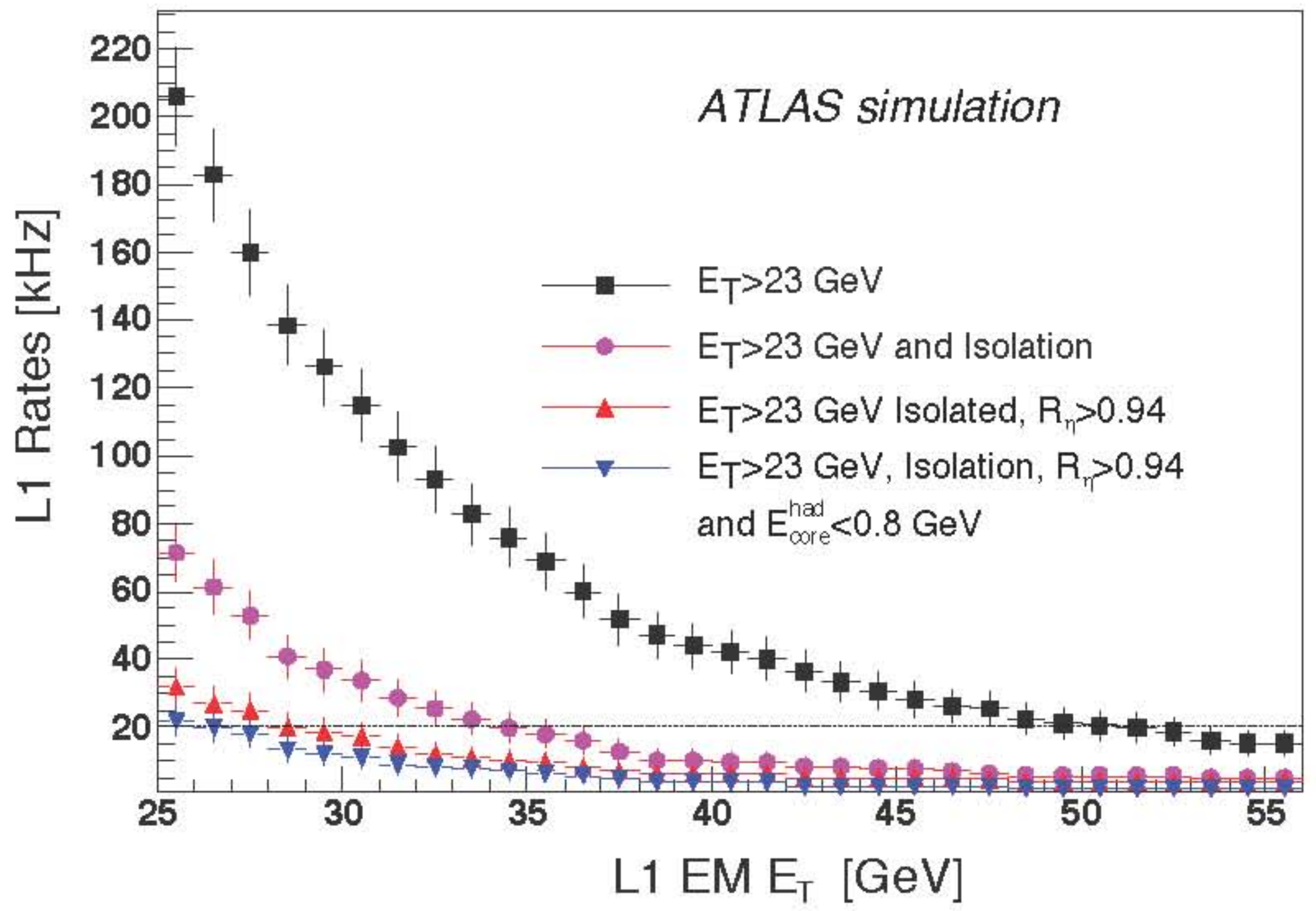
	2012 Menu+Hardware at Phase-I Luminosity		Phase-I 2018 Menu+Hardware at Phase-I Luminosity	
Trigger	Offline Usable Threshold	L1 Rate	Offline Usable Threshold	L1 Rate
Single Electron	25	130 KHz	32	14 KHz
Single Muon	25	150 KHz	25	15 KHz

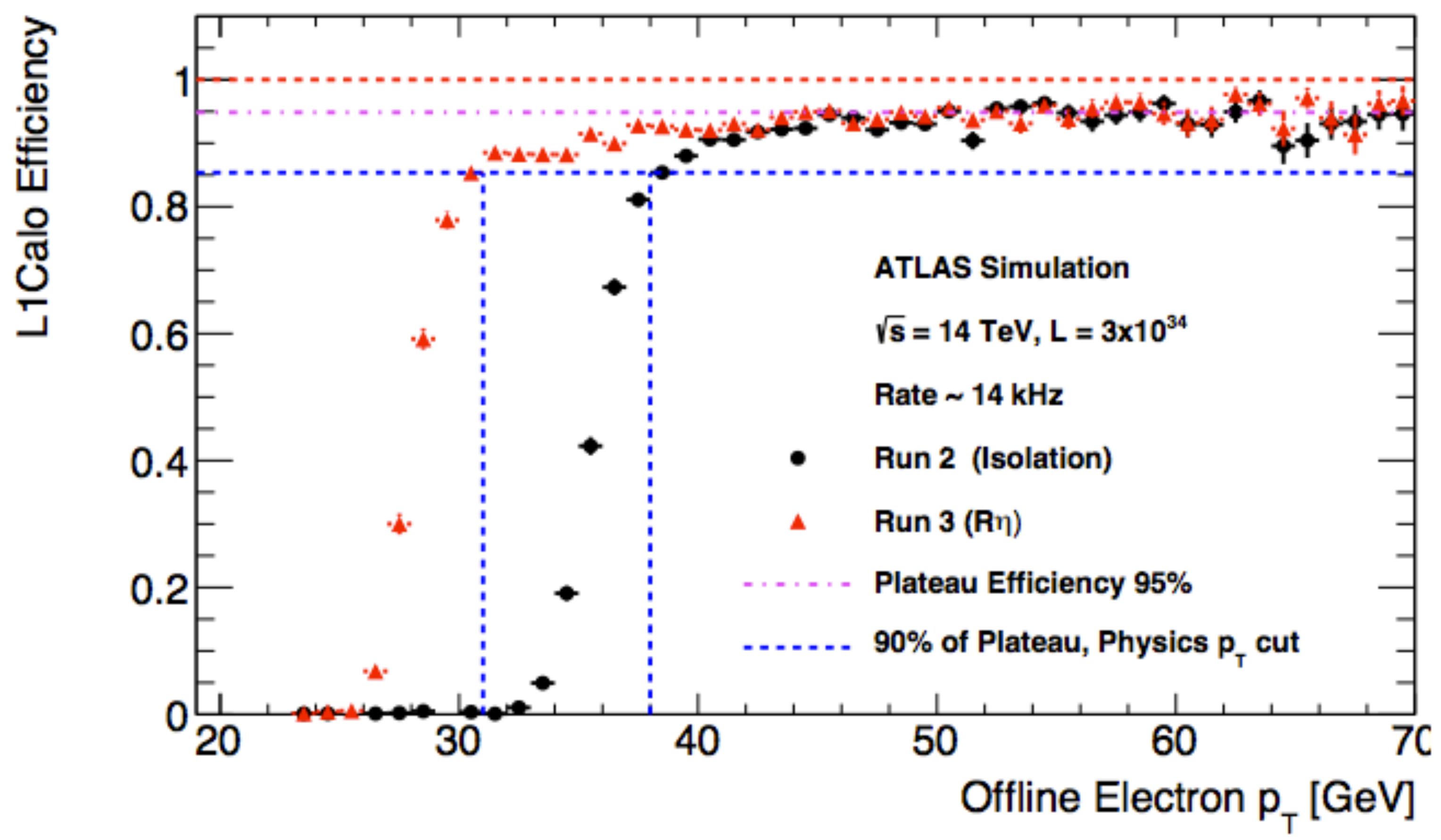
Rates for $3x10^{34}cm^{-2}s^{-1}$ (from ATLAS Phase-I TDR)

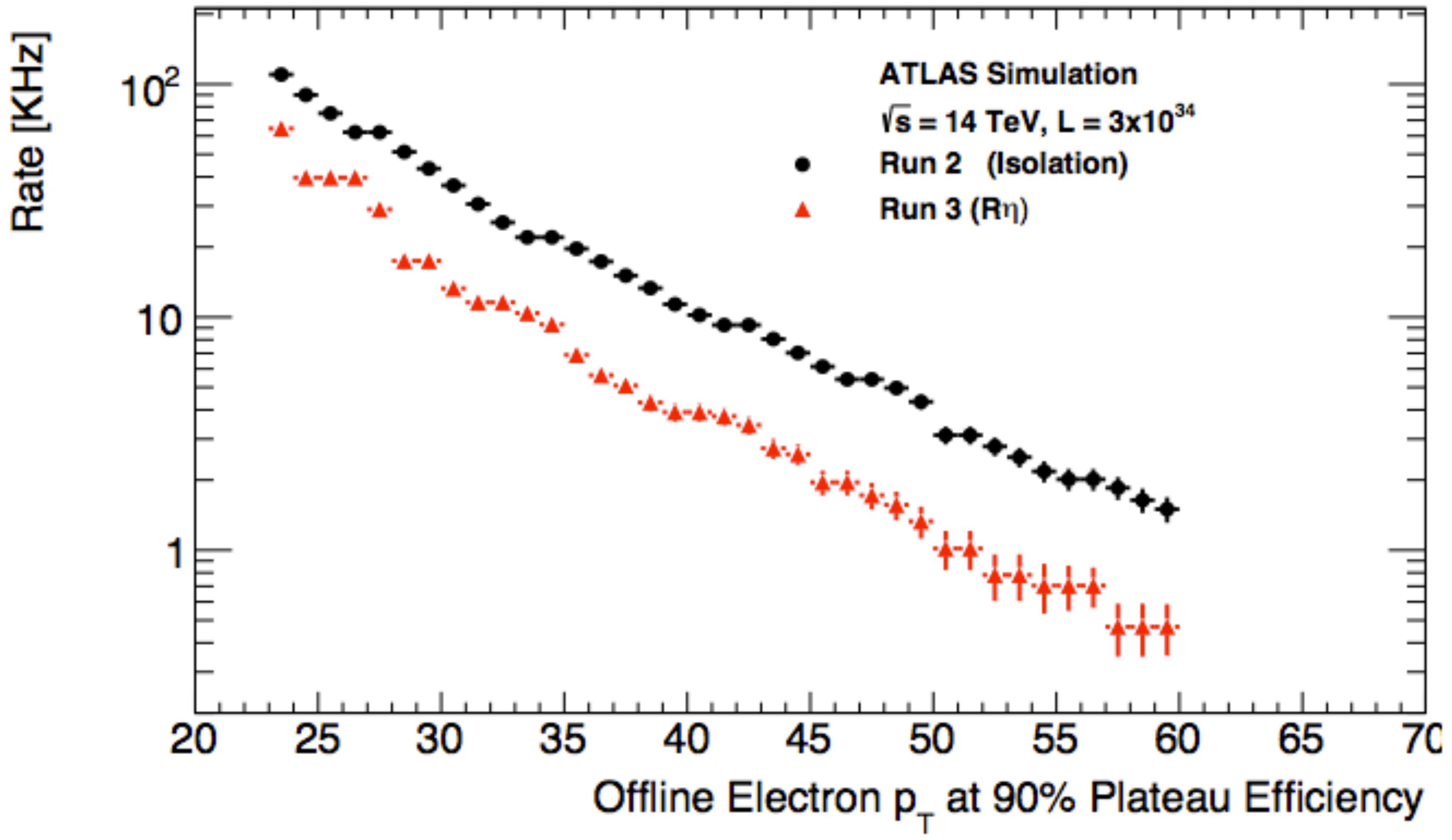
Note: Single electron threshold is a bit high



Now single lepton trigger fits in 100 KHz







HL-LHC Level-0 Muon Trigger

L0Muon

Information from precision muon chambers (MDT) and additional muon trigger chambers added to significantly improve efficiency and purity

- building on existing muon trigger system and Phase-I NSW

New RPCs + MDT gives ~95% efficiency

Increased resolution also gives ~4-5 additional rejection