

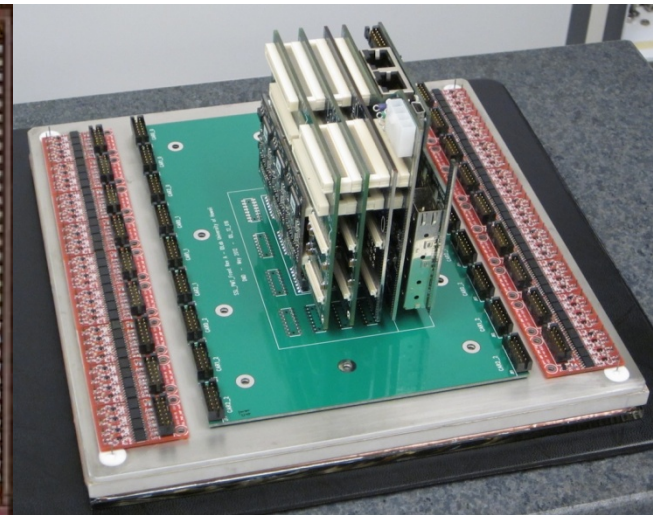
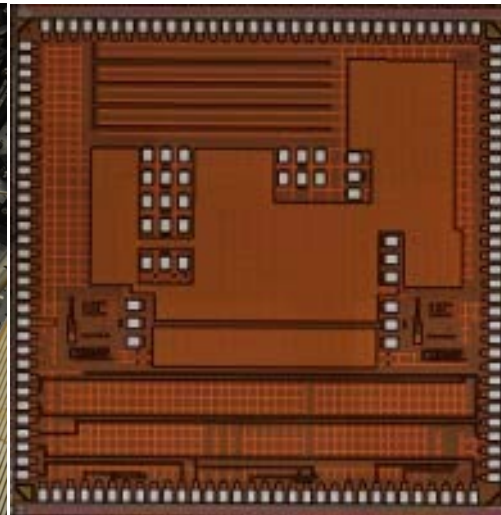
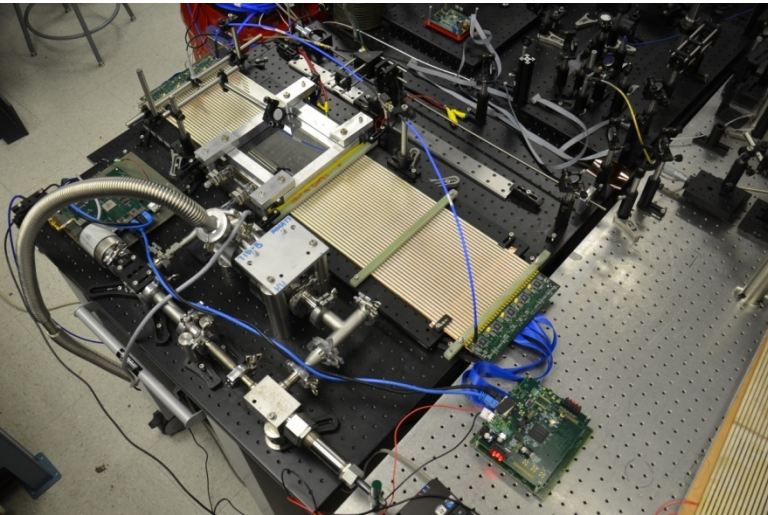
LAPPD2 Electronics

Mircea Bogdan, Henry Frisch, Craig Harabedian,
Razib Obaid, Mary Heintz, Eric Oberla
University of Chicago

Matt Andrew, Sergey Butsyk, Gary S. Varner
University of Hawai'i at Manoa

Jean-Francois Genat, Herve Grabas
Universite Pierre et Marie Curie – Paris VI, France
for the LAPPD2 Collaboration

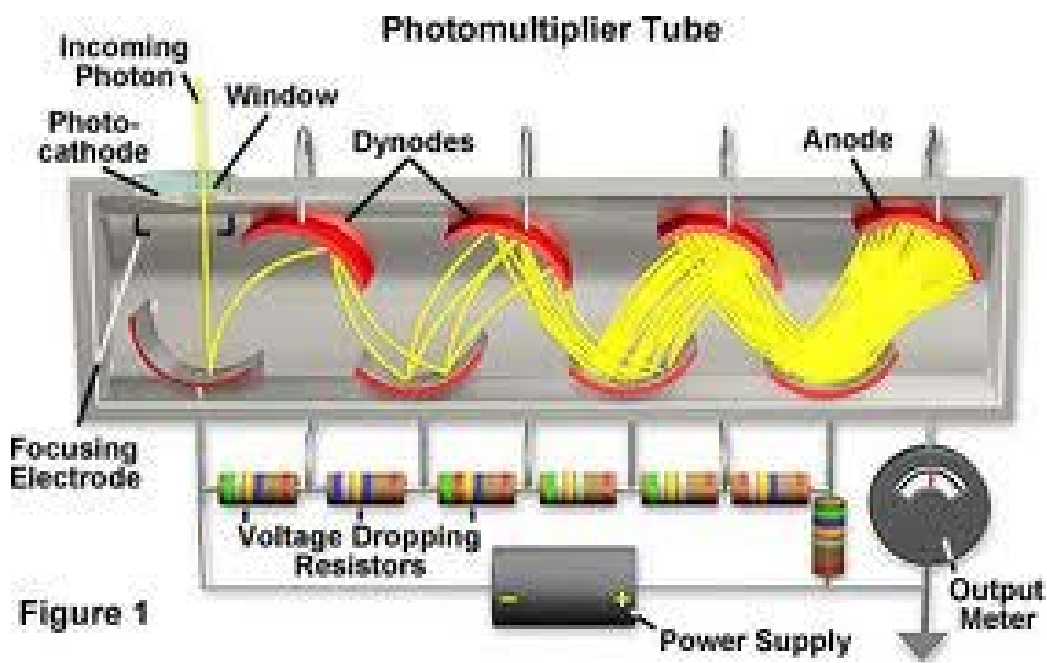
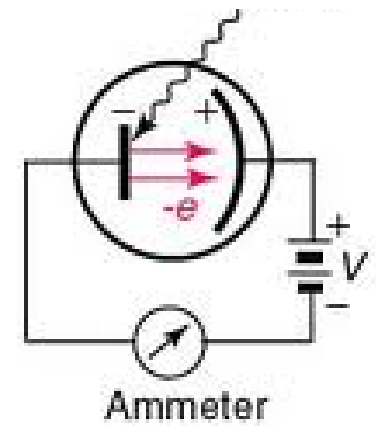
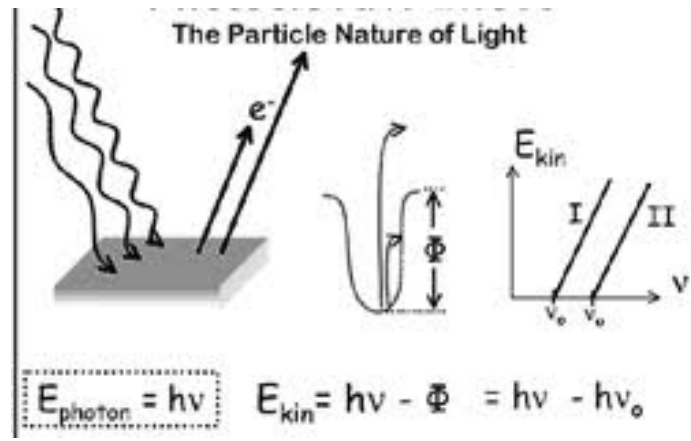
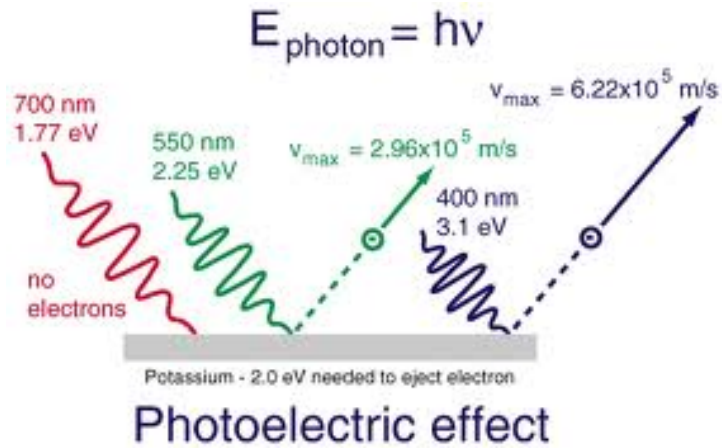
6-APR-2013 == godparent Review at ANL



LAPPD2 Project Overview

- **Brief Introduction to the project:**
 - **Goals/dreams**
 - **Brief history**
 - **Current status**
- **Integrated Electronics as an enabling technology to facilitate use by first adopters**

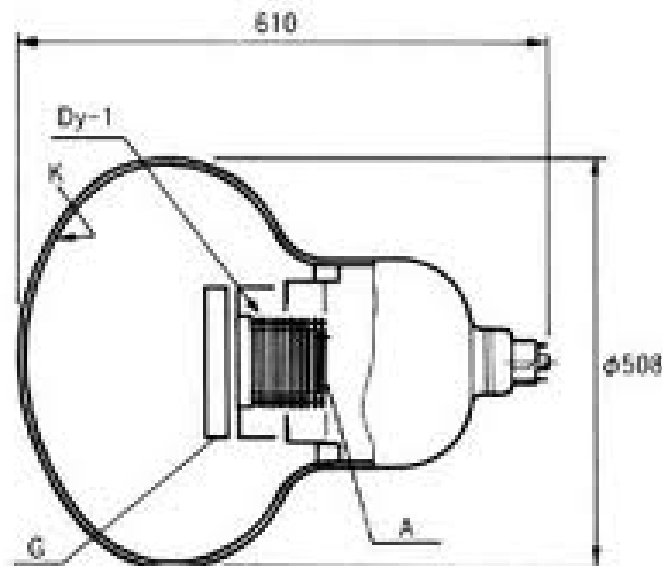
Photo-multipliers -- a very fundamental detector building block



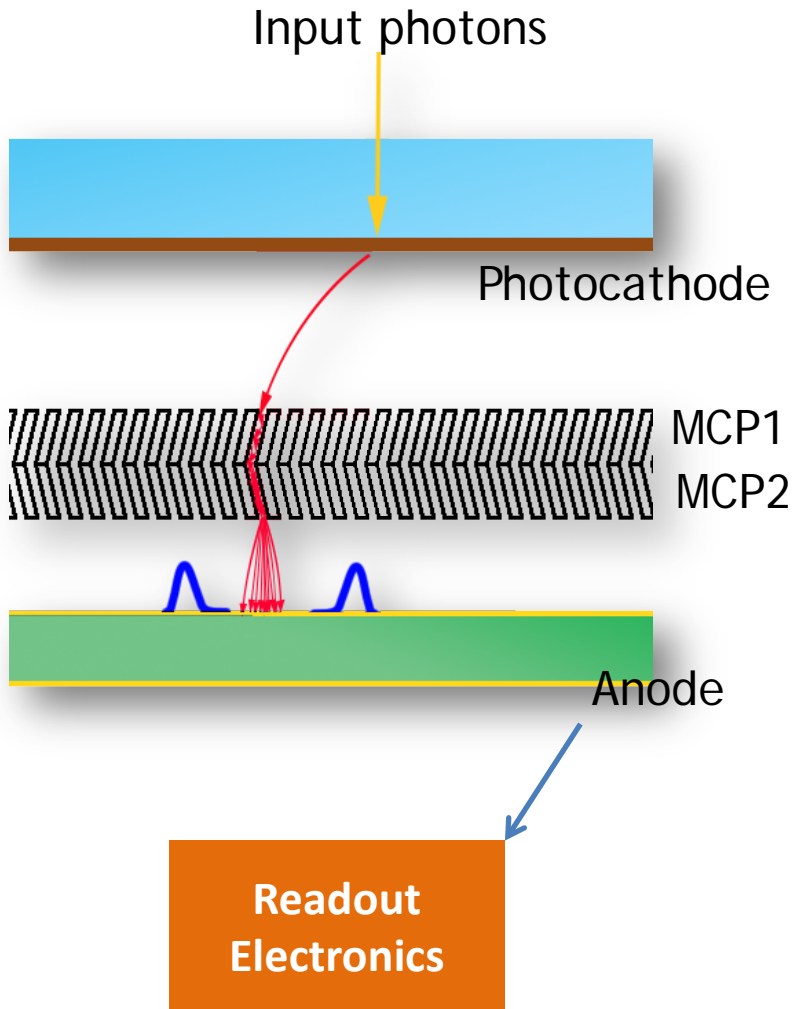
An almost ideal amplifier!

$(G \cdot BW \sim 10^{16})$
[as noted by H. Frisch]

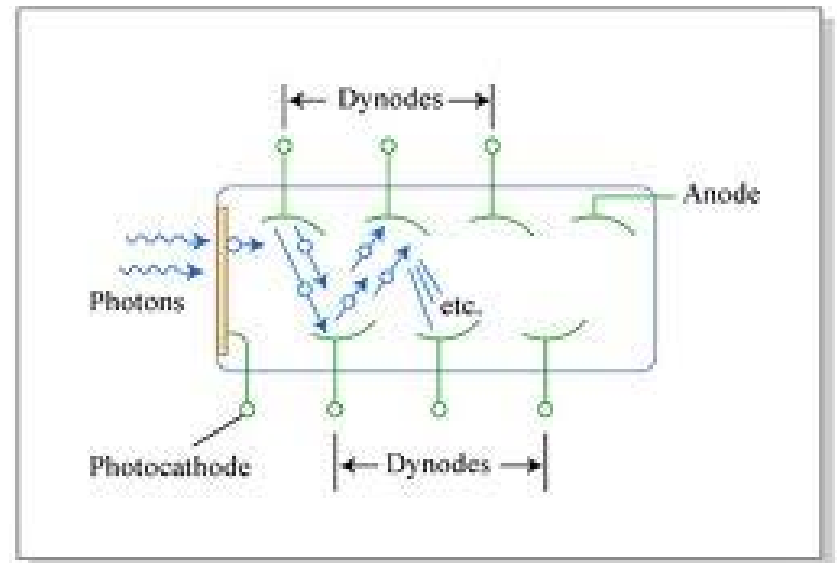
Old ways die hard...



“Flat panel display” vs. CRT



Starting point is a
Micro-Channel
Plate Photo-
Multiplier Tube



LAPPD Collaboration:

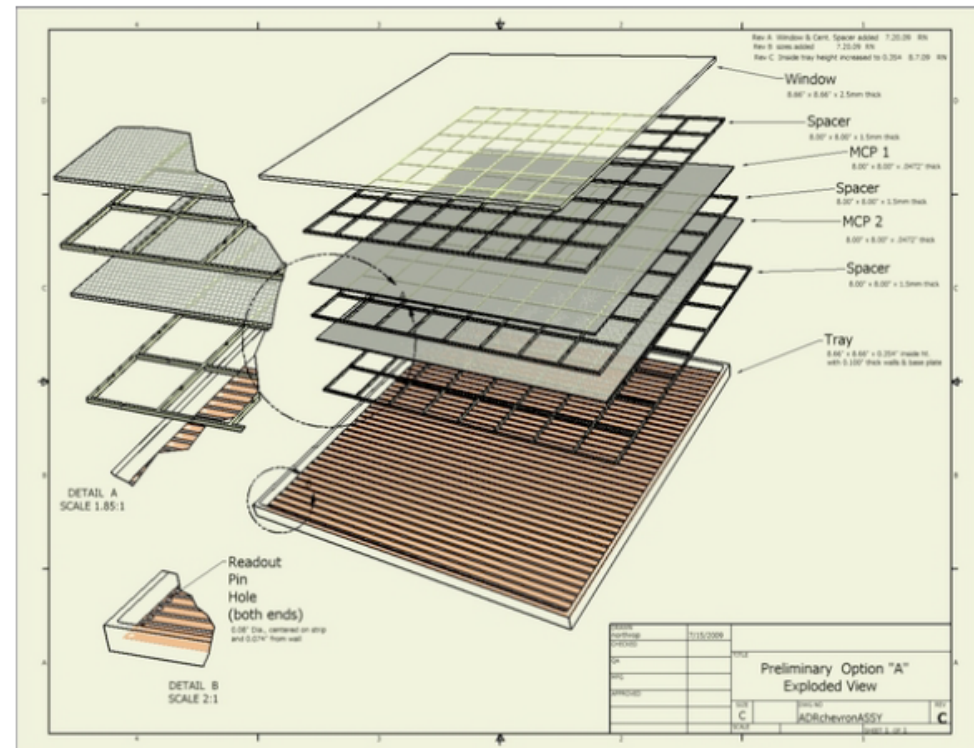
Pushing limits on multiple frontiers: timing, volume, & cost.

Microchannel Plates are an existing photo-multiplier technology known for:

- Picosecond-level time resolution
- Micron-level spatial resolution
- Excellent photon-counting capabilities
- Being expensive

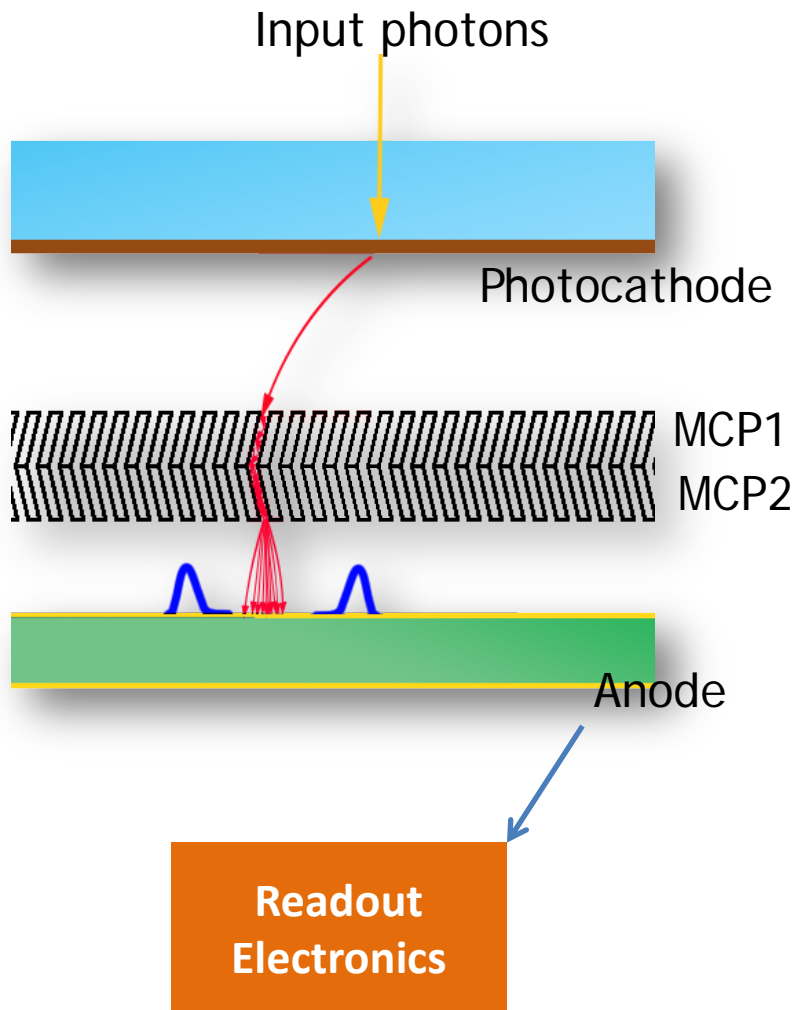
What if we could exploit advances in material science and electronics to develop new methods for fabricating:

- Large area (8"x8"), flat panel MCP-PMTs **(BIG)**
- Preserving that excellent time resolution **(FAST)**
- At competitive costs for particle physics scales **(CHEAP)**



How could that change the next-generation particle Detectors?

Elements of the LAPPD2* MCP-PMT



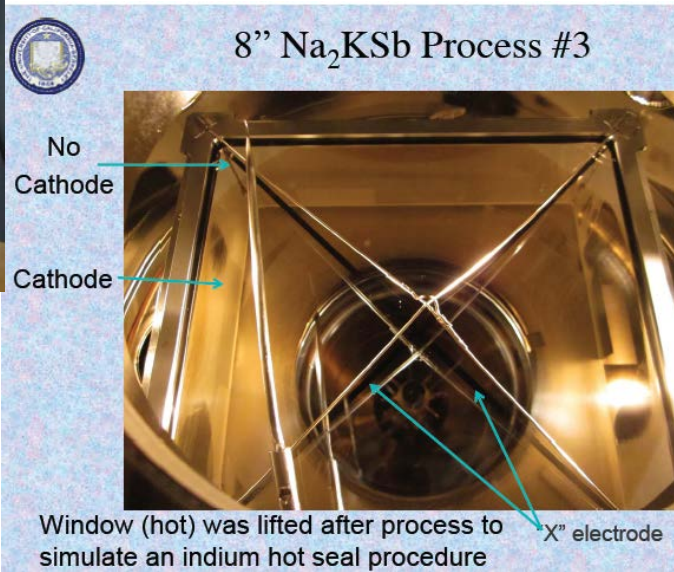
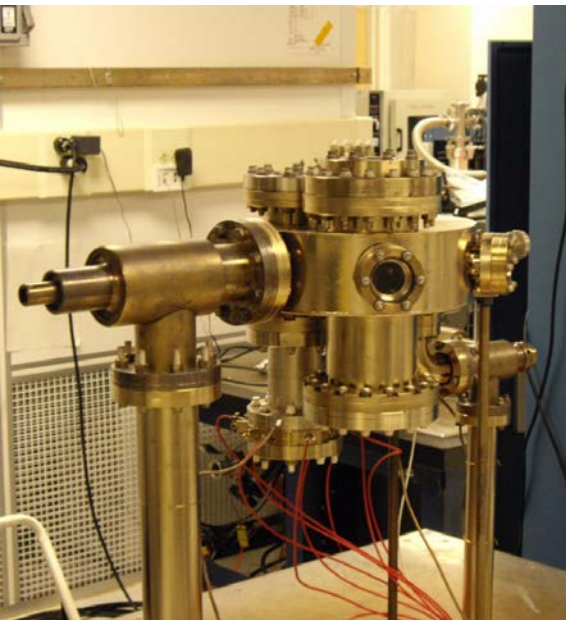
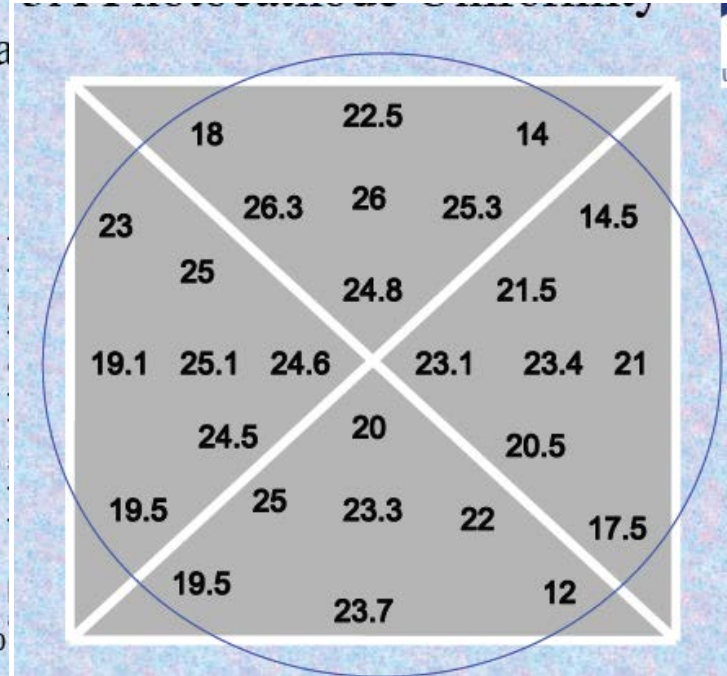
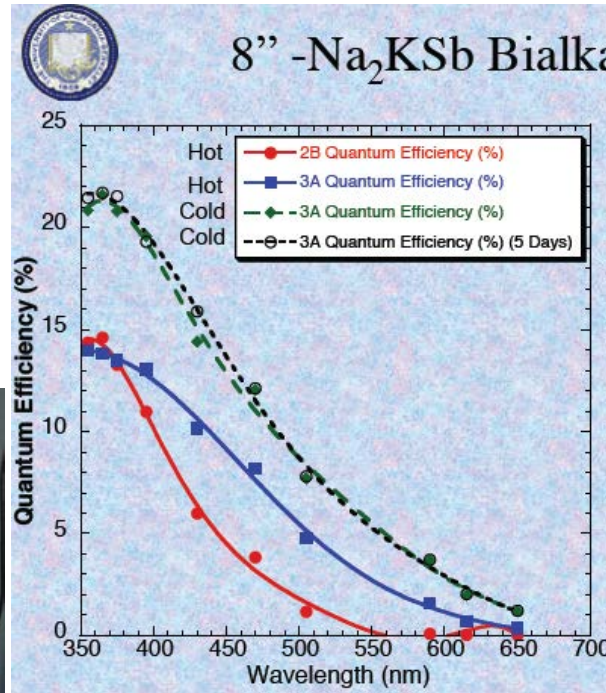
1. Photocathode
2. Micro-channel plates
 - Collection anode array
 - Readout electronics
3. Mechanical design / tile assembly.

→ Active research is ongoing for all elements... there are a lot of impressive achievements. Can only provide a brief snapshot/update

* = 2nd phase (first 8" tiles to first adopters)

Perfecting Standard PC: Scaling up to 8" @ SSL

Good Q.E., uniformity



Scale up to larger chamber

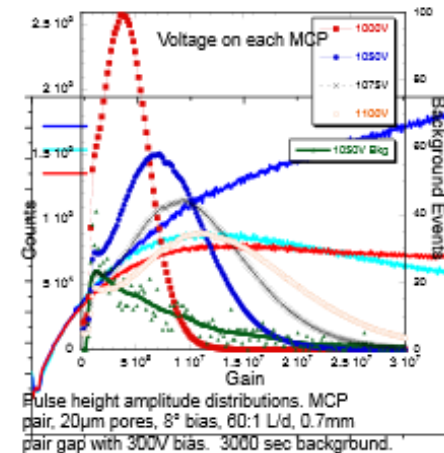


Microchannel Plates

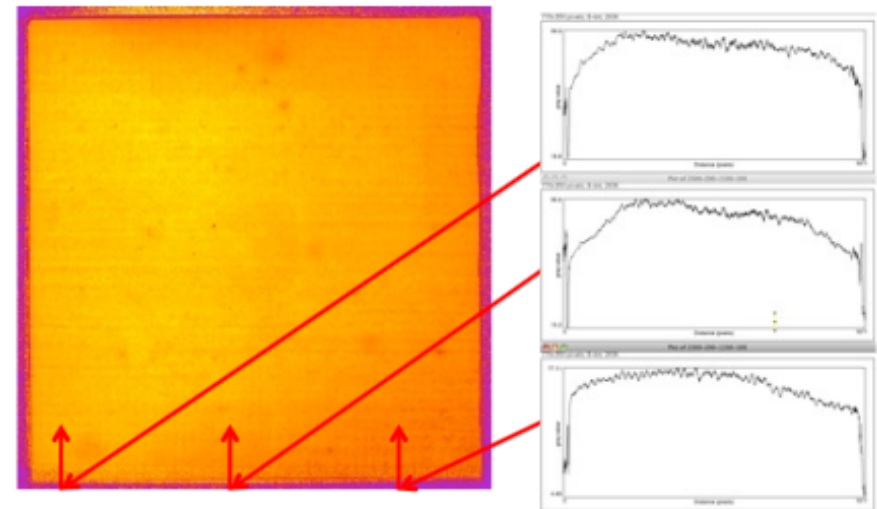
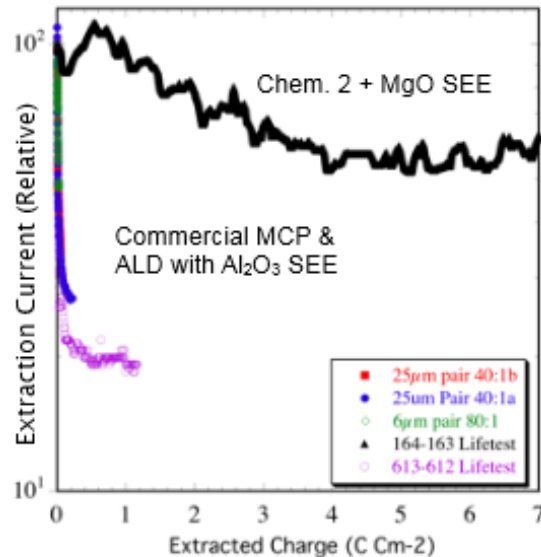
MCP Development Program - Impressive Success

- ▶ Routinely making 8"×8" MCPs with pairwise gain 10^{6-7} ($>10^{-3}$ per plate)
- ▶ Uniformity of gain has been greatly improved in recent months
- ▶ Gain stability of MgO SEY plates is far better than Pb glass MCPs after initial conditioning
- ▶ Recognized with R&D100 award in 2012

$G=4 \times 10^6$ @ 1000V



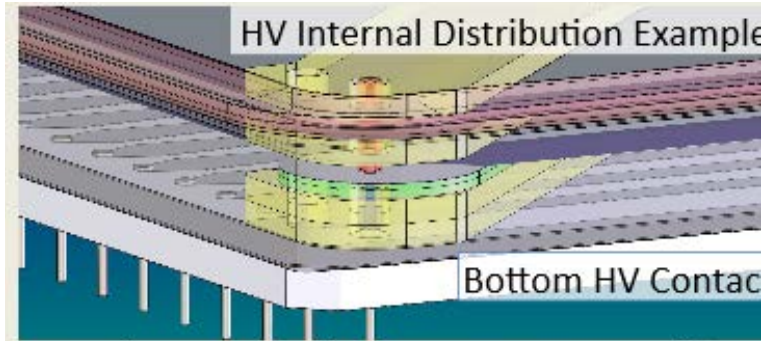
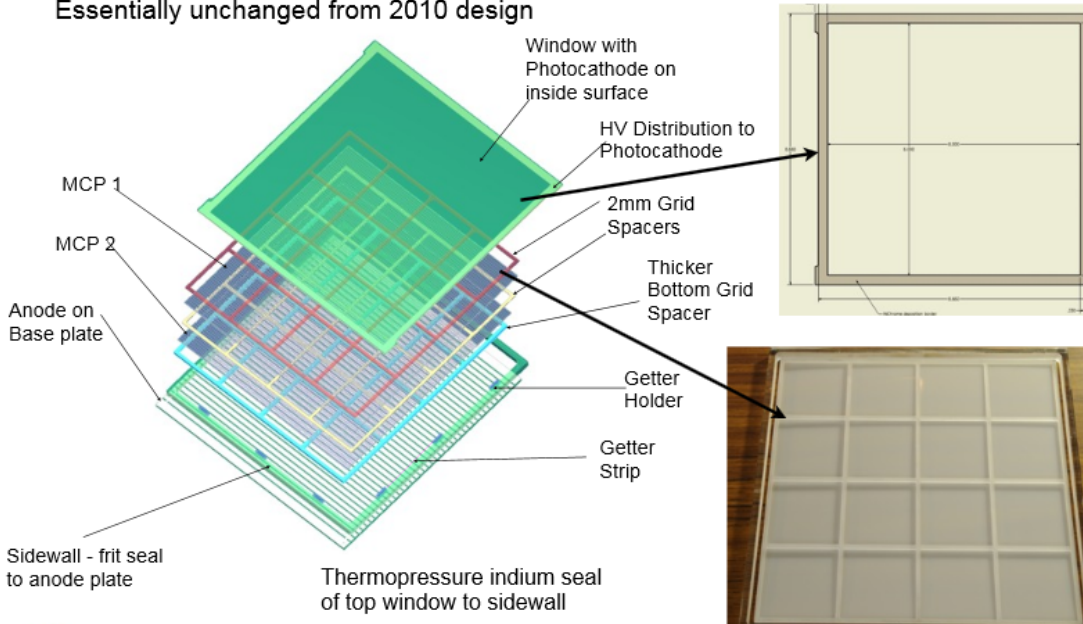
graphic: Ossy Siegmund, SSL



Sealed Tubes

All Glass Option --- ALD Coated Grid Spacer Design

Essentially unchanged from 2010 design

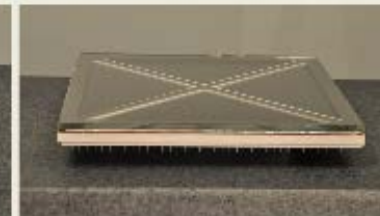


HV Internal Distribution Example

Bottom HV Contact

Anode Gap X-grids

Inter-MCP X-grid



Cathode Gap X-grid

Mech. Test Unit

There are a number of issues with ensuring vacuum, assembly of such large structures

Ceramic Option

Current LAPPD2* Status

1. Photocathode

- ✓ Ready to shoot 8" (test shots look good)
- ✓ Advanced PCs as separate task in LAPPD2 program

2. Micro-channel plates

- ALD-coated, 20um pore tubes in 8" format
- Excellent lifetime, robust mechanically

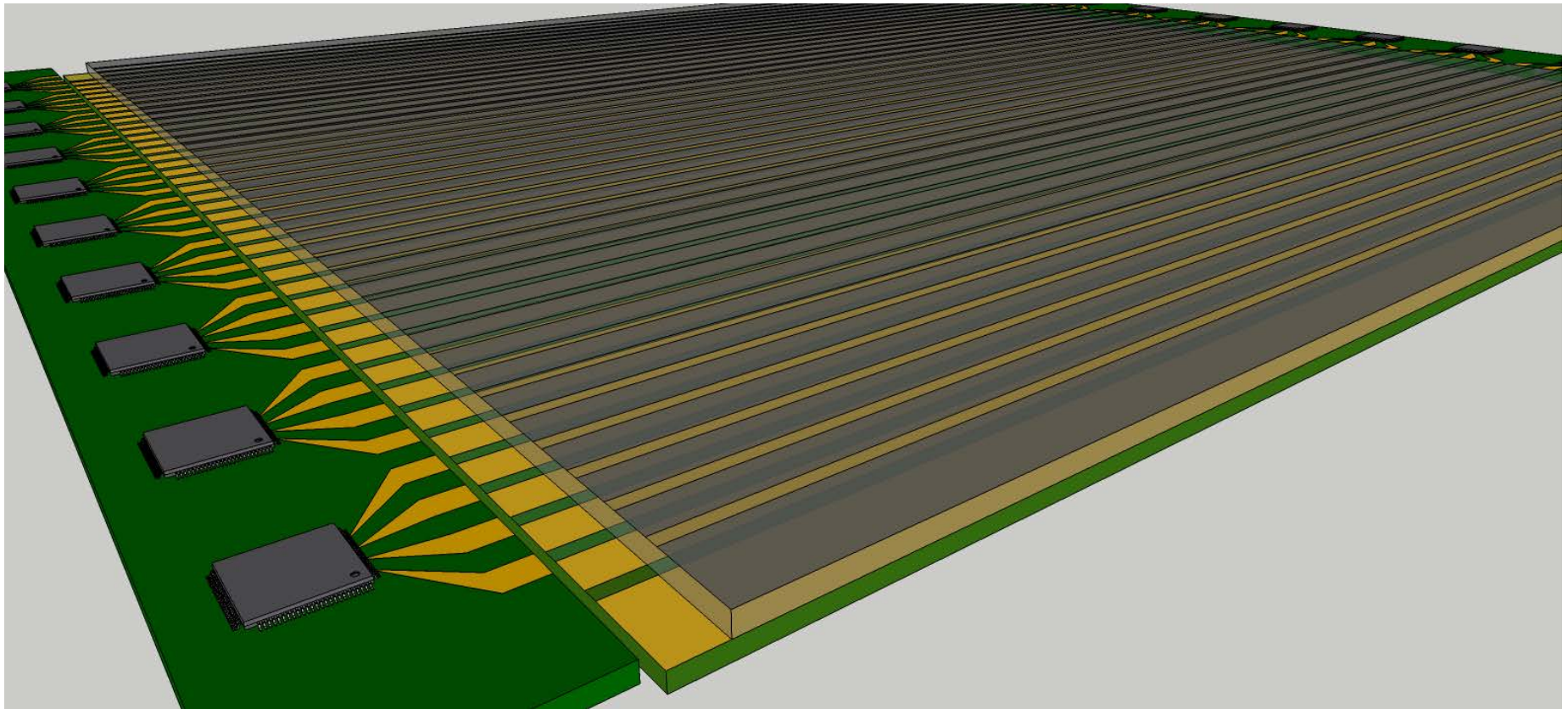
3. Mechanical design / tile assembly

- ✓ Need to demonstrate can make sealed tube
- ✓ Ceramic (pin-feed through) and Glass (anode strip) options

4. Signal coupling/readout

- Collection anode array
- Readout electronics

Electronics support for an ideal (integrated) Photodetector



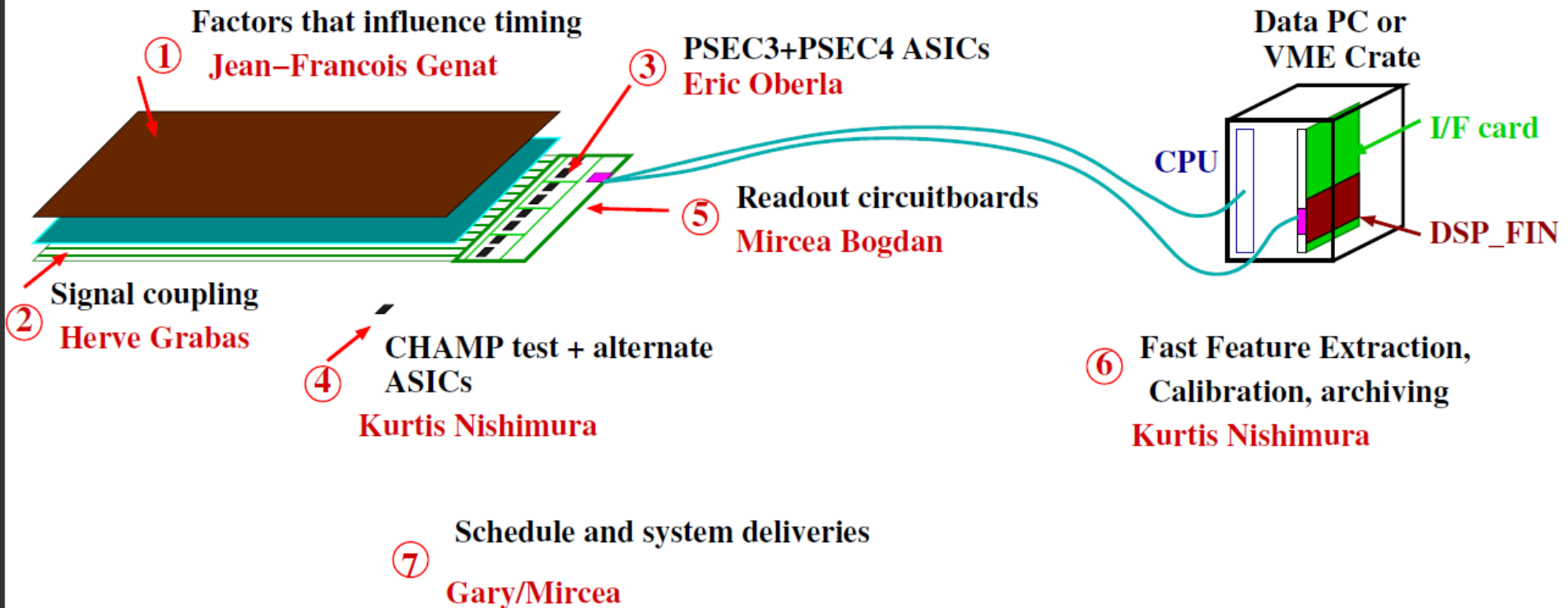
- DC power in, fiber optic out
- Integrated photon \rightarrow electrons \rightarrow T,Q \rightarrow data out

Electronics Overview

- Development of readout support for glass tile array and ceramic tiles
- Specific front-end and common back-end support
- **PSEC family ASIC for ultimate timing (spatial) resolution; portfolio of ASIC solutions (application-specific)**
- Field-test experience of readout systems at ANL, Chicago and Hawai'i
- Support of systems for first adopters

Many Aspects to the Electronics

LAPPD Electronics Overview



- Addressing all aspects needed to realize integrated PD goal
- Participants come and go... nature of university-led efforts

Many highlights

1. Deeper understanding of the processes that limit timing resolution
http://psec.uchicago.edu/workshops/fast_timing_conf_2011
2. A much more fundamental understanding of how to couple the charge signal into the readout anodes [publication, SBIR]
3. Understanding how to make a electrically and mechanically viable readout
4. Impressive results with the PSEC ASICs [publication]
5. Expanded significantly expertise with the IBM 130nm process and tested future subcircuits on the CHAMP ASIC
6. Fabrication of ASIC evaluation boards, as well as the first tile/module scale readout systems
7. Exploration of options for large-scale/high-speed readout, with a number of viable, application-specific ASIC solutions identified
8. Evaluation of calibration procedures, required constants, and data archiving

From Previous Review

- This has been great “generic” development – consider specific applications

Application	Market Need	Approach	Benefit	Competition
Non-cryogenic Tracking Neutrino Detectors	HEP-Fermilab	Very-large-area, bialkali-cathode	Bkgd rejection, Cost, Readiness	Liquid Argon
LE Neutron Detection	Neutron Diffraction	B or Gd Glass no cathode	Time and Position resolution, pulse shape γ/n differentiation, Large area	He3, B tubes
LE Neutron Detection	Transportation Security	B or Gd Glass no cathode	Large area pulse shape γ/n differentiation, Large area	He3, B tubes
LE Anti-Neutrino Detection	Reactor Monitoring	Large-area, bialkali-cathode	Efficiency, Cost	PMT's, SiPMs
HE Collider Vertex Separation	CERN	Psec TOF	Resolution, Radiation-Hard	Silicon Vertex
HE Collider Particle ID	CERN, Future Lepton Collider	Psec TOF	Resolution Reach in P_T	None
π^0/η Reconstruction and ID	Rare K Decays (JPARC), Fermilab	Psec TOF	Combinatoric Bkgd Rejection	Conventional TOF
Strange Quark ID	RHIC (BNL), ALICE (LHC) Collider	Psec TOF	Resolution Reach in P_T	dE/dx
Positron-Emission	Clinical Medical Imaging	TOF, Large Area	Lower Dose Rate, Faster throughput	SiPM

Focus on 5x Applications

1. TOF in the LArIAT Beam
2. Small (1-4 m³) water neutrino detector prototype
3. Pre-converter in KOTO
4. PET (positron-emission tomography)
5. High spatial resolution X-ray diffraction

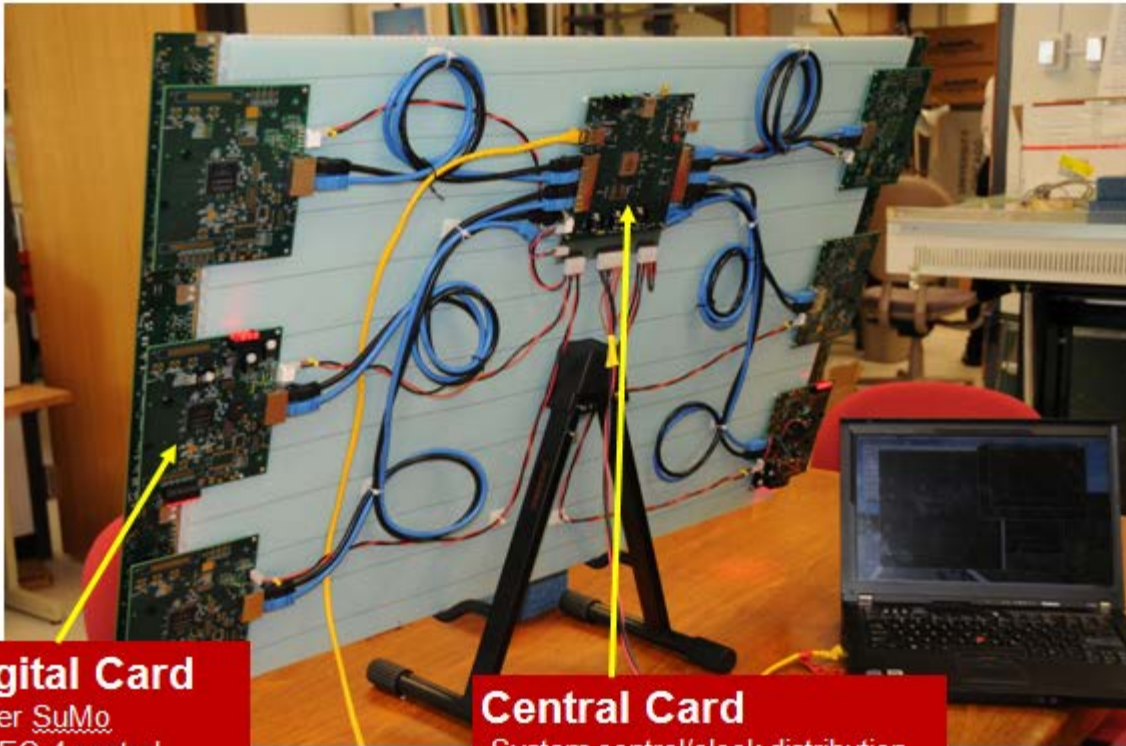
Chosen for mix of HEP and other applications where can have impact and well aligned to needs

Details subsequently

What does LAPPD2 mean for electronics?

- Readout support for glass tile array and ceramic tiles (job 1)
- Specific front-end and common back-end support [systems engineering!?!]
- PSEC family ASIC for ultimate timing (spatial) resolution; portfolio of ASIC solutions (application-specific)
- Field-test experience of readout systems at ANL, Chicago and Hawai'i
- Support of systems for first adopters?

System Engineering Issues



Digital Card

- 6 per SuMo
- PSEC-4 control, trigger handling, local data reduction & calibration

Central Card

- System control/clock distribution
- Feature extraction & event pairing
- CPU/GPU interface

(10 Gbit Ethernet & USB 2.0)



- **Current experience with Belle II iTOP development**
→ much firmware/infrastructure development required still

Today's Agenda

Saturday, 6 April 2013

- 08:30 - 08:35 Welcome & Introduction
08:30 **Welcome & Charge** 5'
- 08:35 - 10:55 Digitization
Convener: Kurtis Nishimura (SLAC)
- 08:35 **Overview: Goals, Specs for Five Applications, Resources, & Progress Since Last GP Review** 30'
Speaker: Gary Varner (UHawaii)
- 09:10 **What We Learned from PSEC-4** 20'
Speaker: Eric Oberla (UChicago)
- 09:35 **Can We Use IRS3b or Other Existing Chips** 20'
Speaker: Gary Varner (UHawaii)
- 10:00 **PSEC-5** 20'
Speaker: Eric Oberla (UChicago)
- 10:25 **Questions to Be Decided** 30'
Assignments of Chips to Applications?
IBM vs TSMC
Simulation of Blocks
Task Assignments?
Proposals, Schedule
Speaker: Ted & Kurtis, leaders Discussion
- 11:00 - 11:15 Coffee Break
- 11:15 - 13:30 Systems
Convener: Ted Liu (Fermilab)
- 11:15 **System Architecture for PSEC-4** 20'
Speaker: Eric Oberla (UChicago)
- 11:40 **Alternative Architectures I** 20'
Speaker: Gary Varner (UHawaii)
- 12:05 **Alternative Architectures II** 20'
Speaker: Mircea Bogdan (UChicago)
- 12:30 **Questions to Be Decided** 20'
Speaker: Ted & Kurtis, leaders Discussion
- 12:50 **Drafting of Recommendations & Working Lunch** 40'
Speaker: GP Committee & Proponents

Electronics jumping off point

- **Steady progress, resource (human) bounded**
- **Are learning much from first integrated readout tests**
- **Field-test experience of readout systems at ANL, Chicago and Hawai'i**
- **Building toward full system deployments with first adopters**
- **Obvious question is what comes next**

5x Targeted Applications

What limited number of applications would you target as priorities in the next stage of development and why?

Three HEP and two directed toward market expansion:

1. TOF in the LArIAT Beam

- a) Why: Simplest set-up that has a large impact on HEP programs**
- b) Straight-forward interface to experiment**
- c) Local, have collaborators in place;**
- d) Drop in for scintillators and PMTs at higher cost and better performance**
- e) Spec: 4 stand-alone single tile stations, 10 psec time resolution, 50KHz (needs checking)**

2. Small (1-4 m³) water neutrino detector prototype

- a) Why: Comparison to simulation; test of the optical TPC concept with track reconstruction**
- b) If successful, no competition**
- c) From 1 to 6 SuperModules;**
- d) Spec: Single pe resolution ~ 100psec, low rate**

3. Pre-converter in KOTO

- a) Why: Archetype for 3D localization and precise timing of high energy photons**
- b) Good access to management and technical expertise in the experiment**
- c) If successful, no competition**
- d) 1-4 SuperModules**
- e) Spec: Timing = 1 psec; Rate = 200 kHz; Position = several mm; Trigger latency = 5 μ sec**
- f) HEP benefit: Increased physics reach**

4. PET

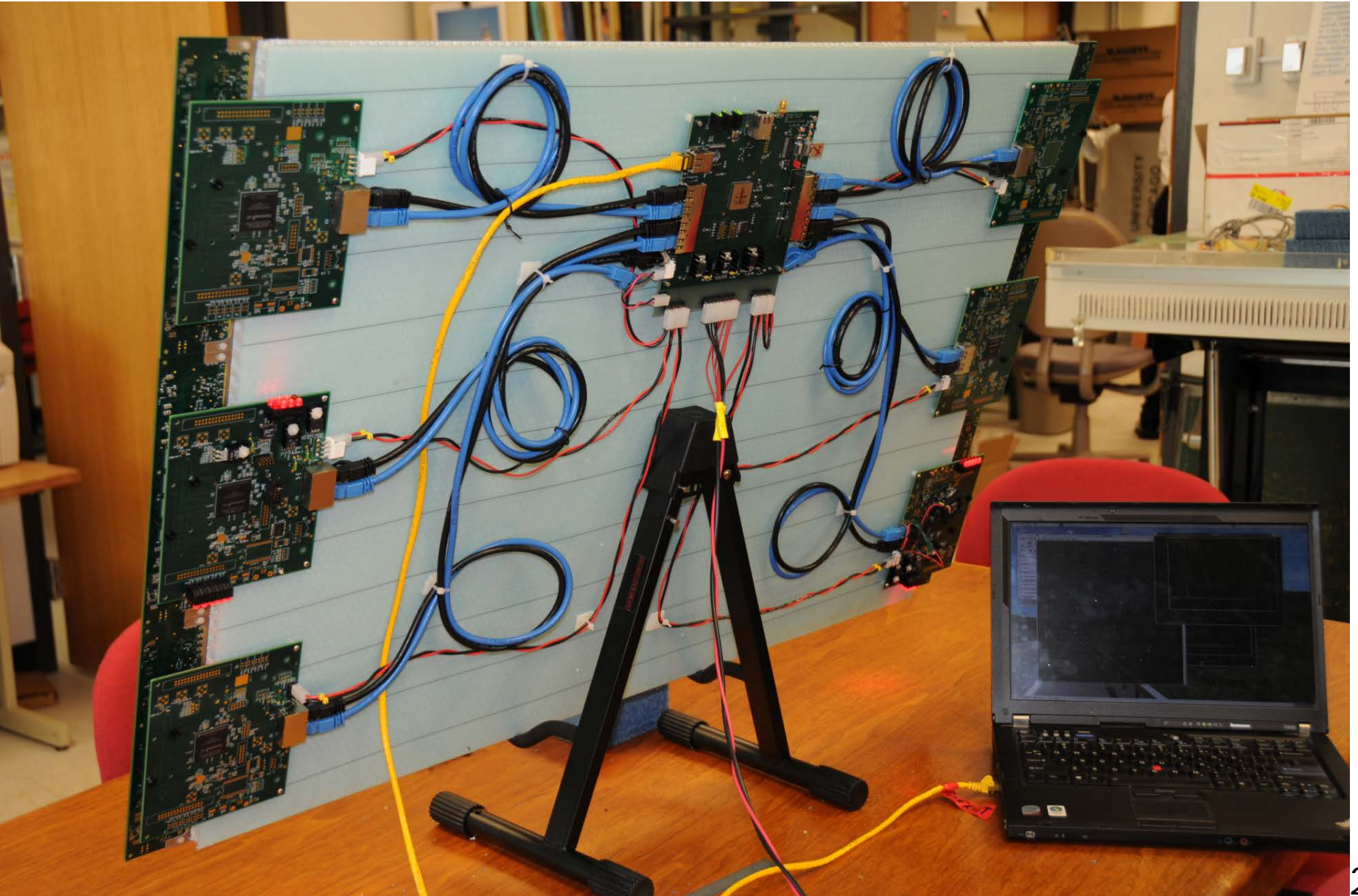
- a) Why: Potential to decrease patient dose rate by >10 or increase patient throughput**
- b) Current state of the art = 300 psec**
- c) Spec: 50 psec (FWHM) TOF-PET resolution**
- d) HEP benefit: Potentially large market drives the cost down**

5. High spatial resolution X-ray diffraction

- a) Why: Large area detector with high spatial resolution**
- b) Large area, high spatial resolution, multi-channel solid state detectors are very expensive and slow**
- c) Spec: 100 μm spatial**
- d) HEP benefit: Increase cross-disciplinary ties**

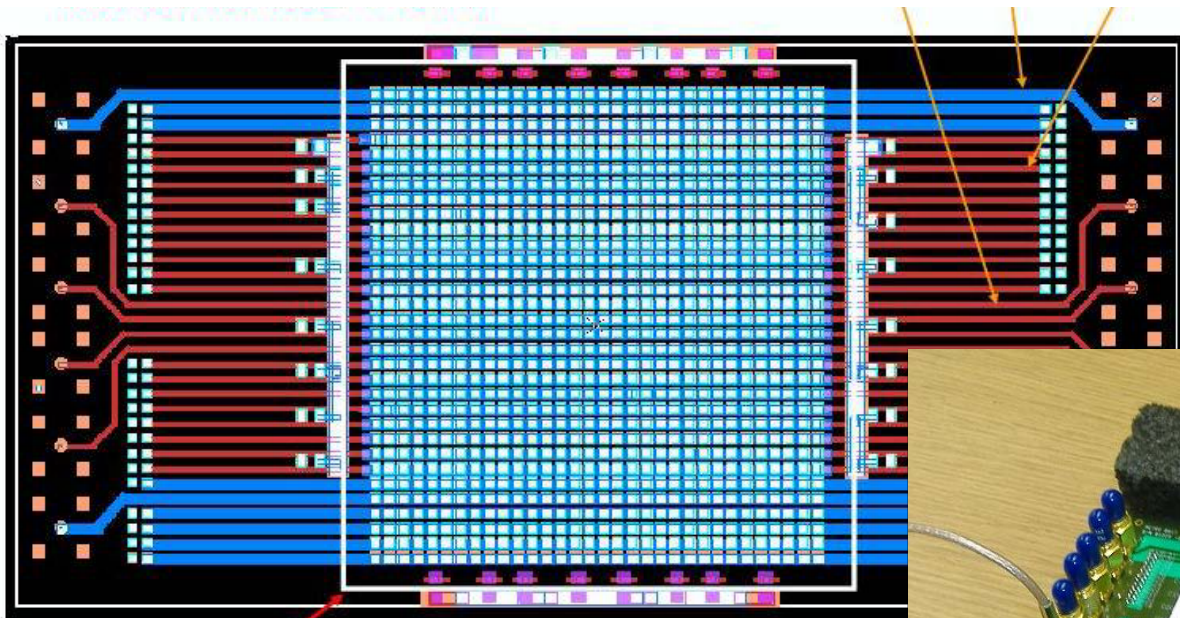
- 08:30 - 08:35 Welcome & Introduction
08:30 **Welcome & Charge** 5'
- 08:35 - 10:55 Digitization
Convener: Kurtis Nishimura (SLAC)
- 08:35 **Overview: Goals, Specs for Five Applications, Resources, & Progress Since Last GP Review** 30'
Speaker: Gary Varner (UHawaii)
- 09:10 **What We Learned from PSEC-4** 20'
Speaker: Eric Oberla (UChicago)
- 09:35 **Can We Use IRS3b or Other Existing Chips** 20'
Speaker: Gary Varner (UHawaii)
- 10:00 **PSEC-5** 20'
Speaker: Eric Oberla (UChicago)
- 10:25 **Questions to Be Decided** 30'
Assignments of Chips to Applications?
IBM vs TSMC
Simulation of Blocks
Task Assignments?
Proposals, Schedule
Speaker: Ted & Kurtis, leaders Discussion
- 11:00 - 11:15 Coffee Break
- 11:15 - 13:30 Systems
Convener: Ted Liu (Fermilab)
- 11:15 **System Architecture for PSEC-4** 20'
Speaker: Eric Oberla (UChicago)
- 11:40 **Alternative Architectures I** 20'
Speaker: Gary Varner (UHawaii)
- 12:05 **Alternative Architectures II** 20'
Speaker: Mircea Bogdan (UChicago)
- 12:30 **Questions to Be Decided** 20'
Speaker: Ted & Kurtis, leaders Discussion
- 12:50 **Drafting of Recommendations & Working Lunch** 40'
Speaker: GP Committee & Proponents

Backup



Stripline Anodes (Prototype)

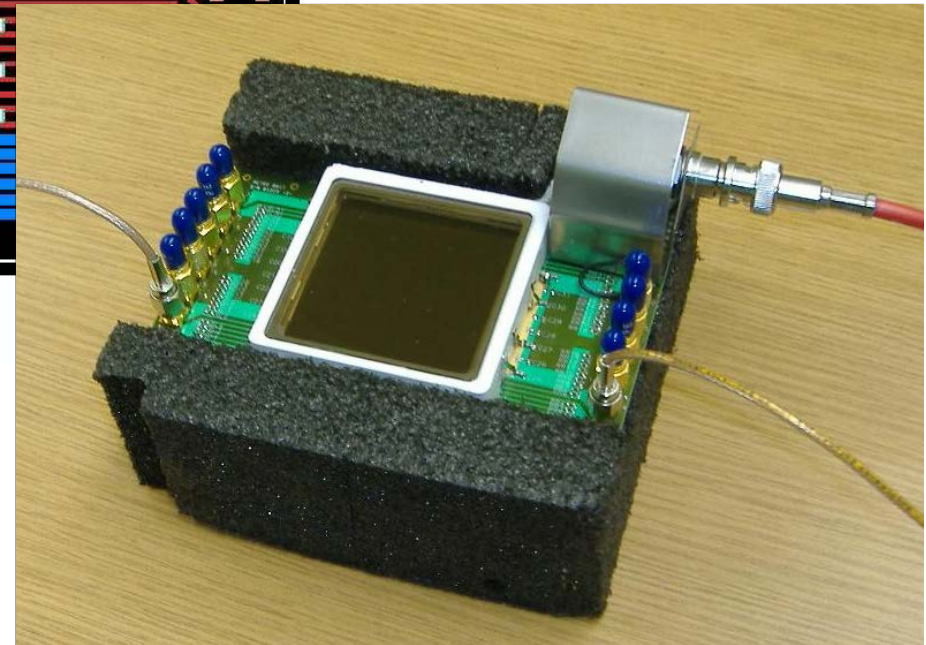
- Photonis-Planacon on transmission line PCB:



Tube Outline 58x58mm

F.Tang

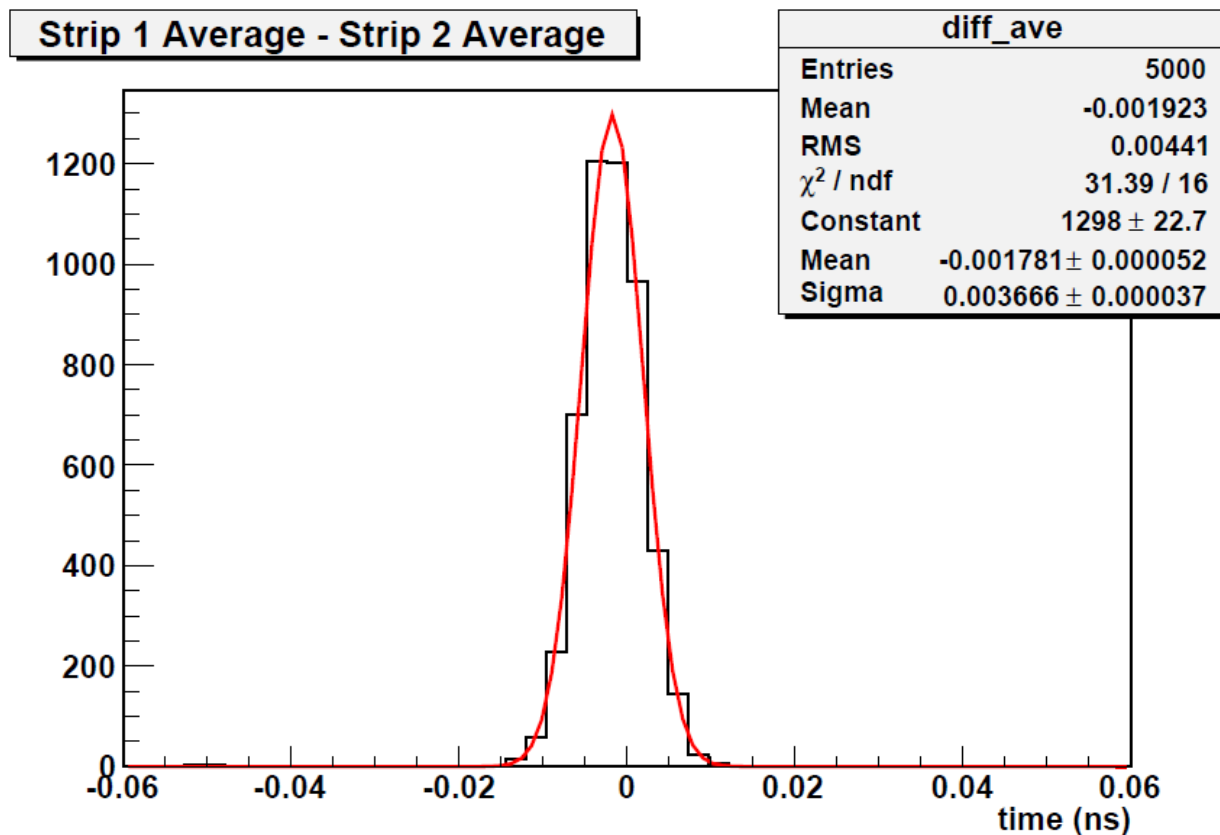
- Striplines allow coverage of a large area with a manageable number of channels.



Courtesy Fukun Tang, Greg Sellberg

Stripline Anodes Measurement

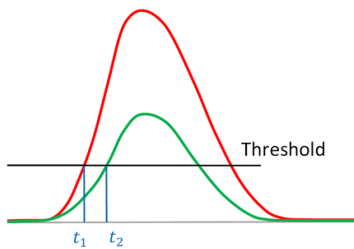
- Average time $((t_1+t_2)/2)$ along strip gives arrival time
- Time difference (t_1-t_2) gives the position



σ_t of order ps feasible for large N_{pe}

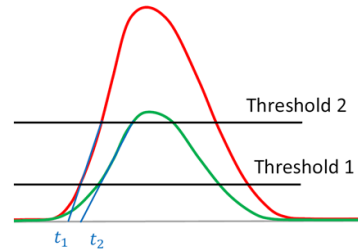
Timing Extraction Methods

Single threshold



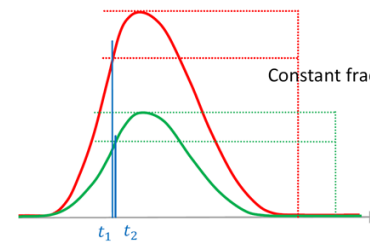
The single threshold is the least precise time extraction measurement. It has the advantage of simplicity.

Multiple threshold



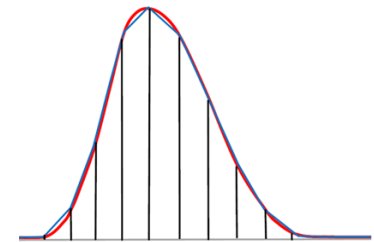
The multiple threshold method takes into account the finite slope of the signals. It is still easy to implement.

Constant fraction



The constant fraction algorithm is very often used due to its relatively good performance and its simplicity.

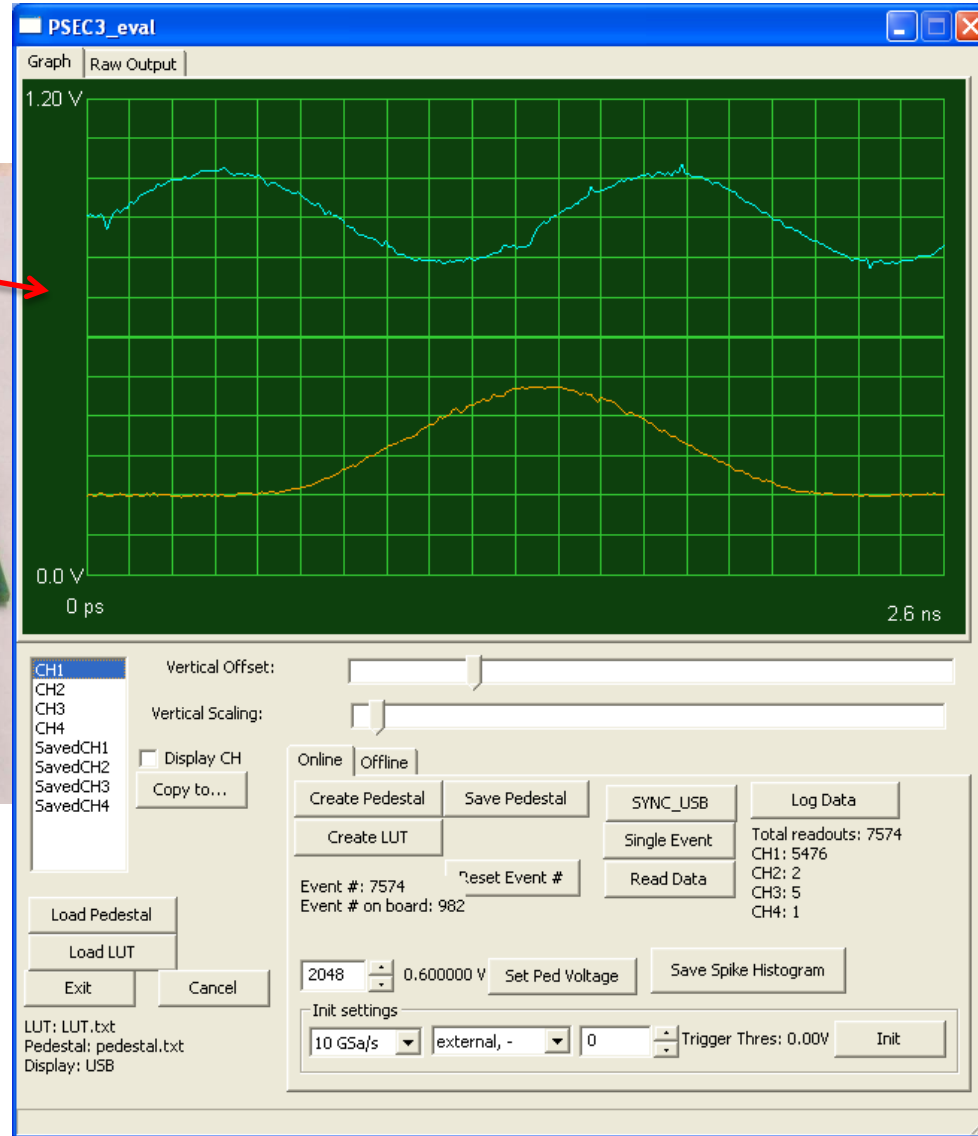
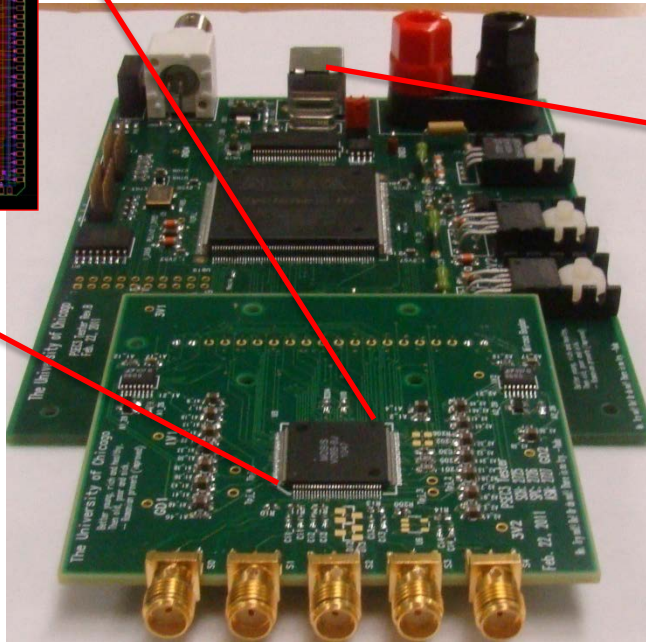
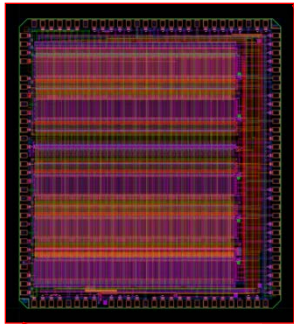
Waveform sampling



The waveform sampling above the Nyquist frequency is the best algorithm since it preserves the signal integrity.

In principle, sampling above the Nyquist-Shannon frequency and fully reconstructing the signal attains the best timing information.

Oscilloscope on a chip? → Calibration

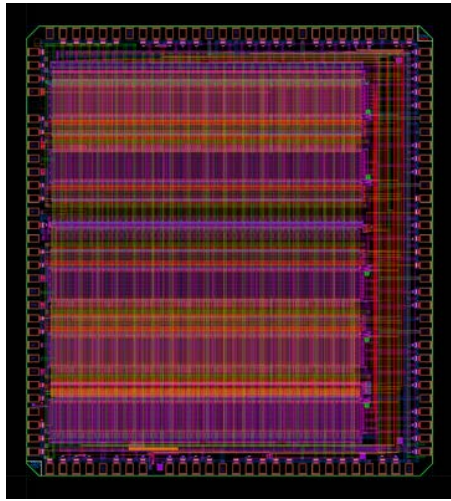


\approx ??



Oscilloscope on a chip? → Calibration

- Modified approximation:



+



+



+



+



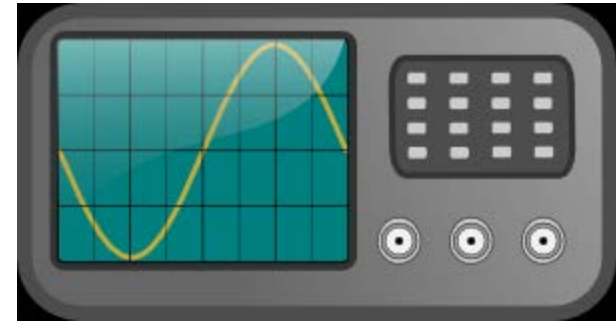
+



+

... ~

=



PSEC-4 measurements with an 8" MCP

