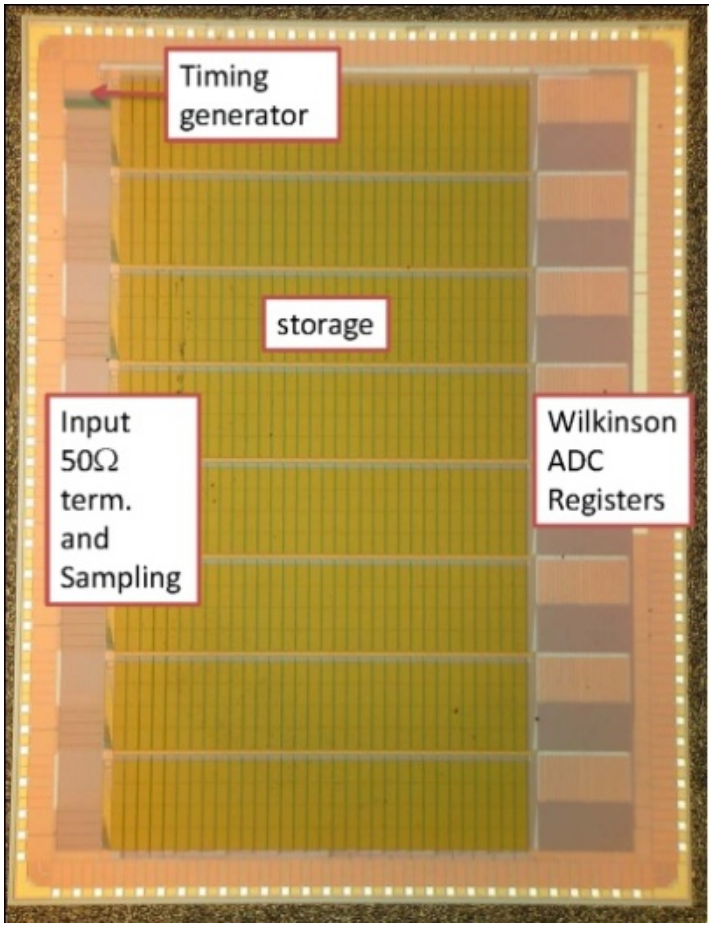
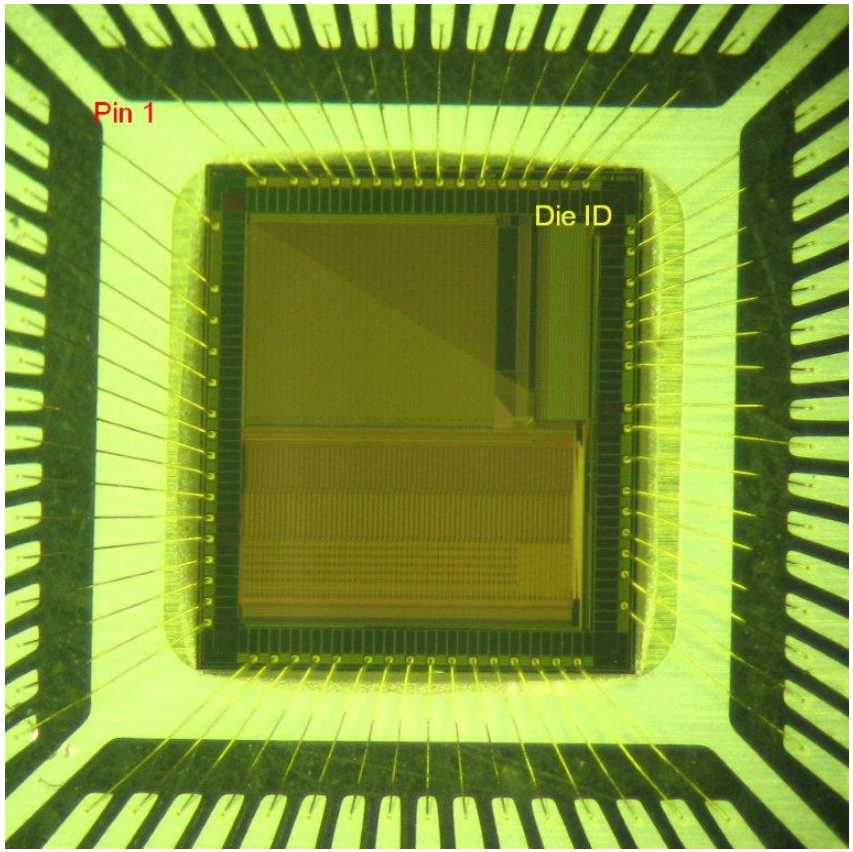
IRS3B & Other ASICs

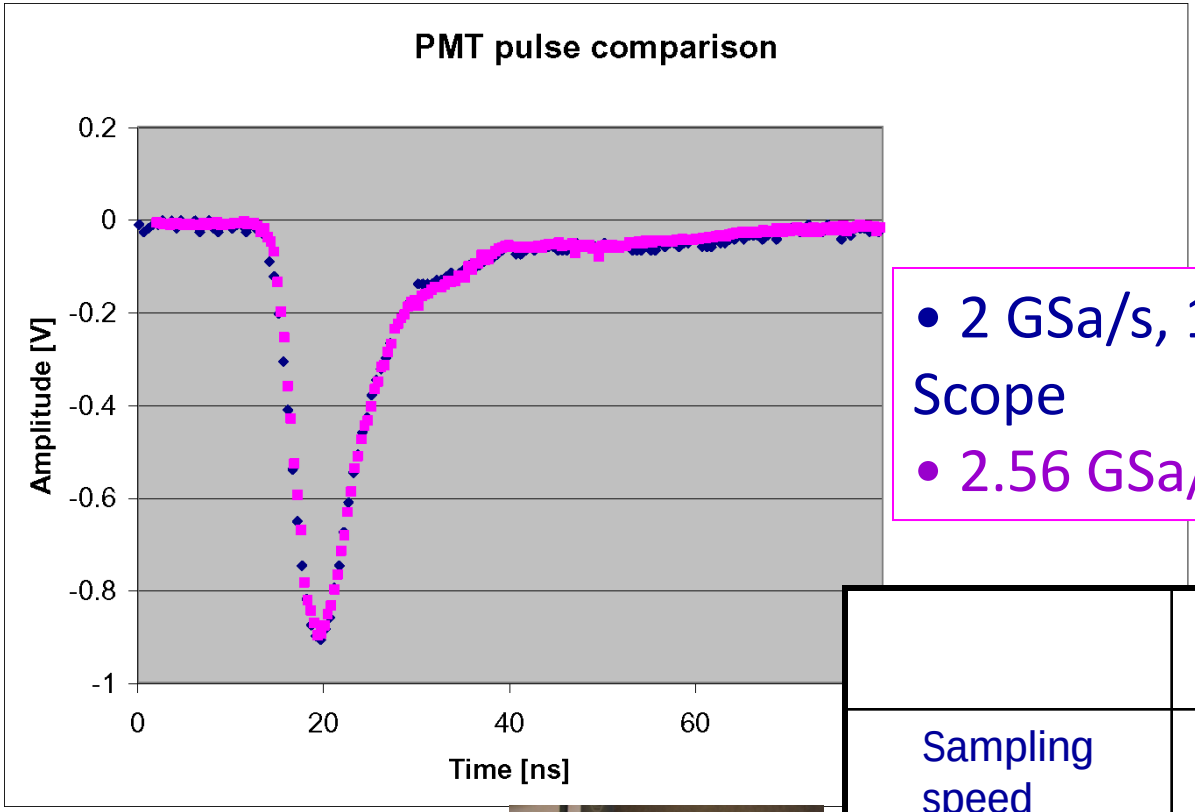
Gary S. Varner
University of Hawai'i at Manoa

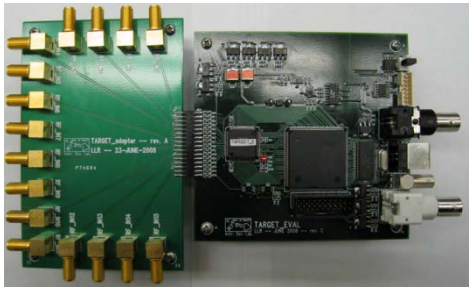




6-APR-2013 == godparent Review at ANL

A reminder of motivation

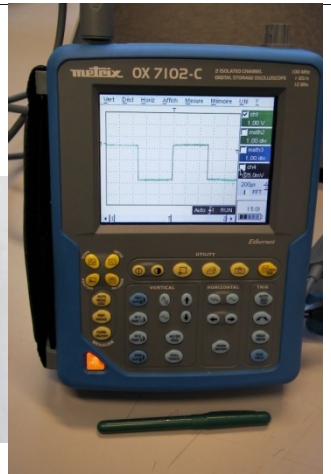




- 2 GSa/s, 1GHz ABW Tektronics Scope
- 2.56 GSa/s LAB

	WFS ASIC	Commercial
Sampling speed	0.1-6 GSa/s	2 GSa/s
Bits/ENOBs	16/9-13+	8/7.4
Power/Chan.	<= 0.05W	Few W
Cost/Ch.	< $10 (vol)	> 100$

"oscilloscope on a chip"



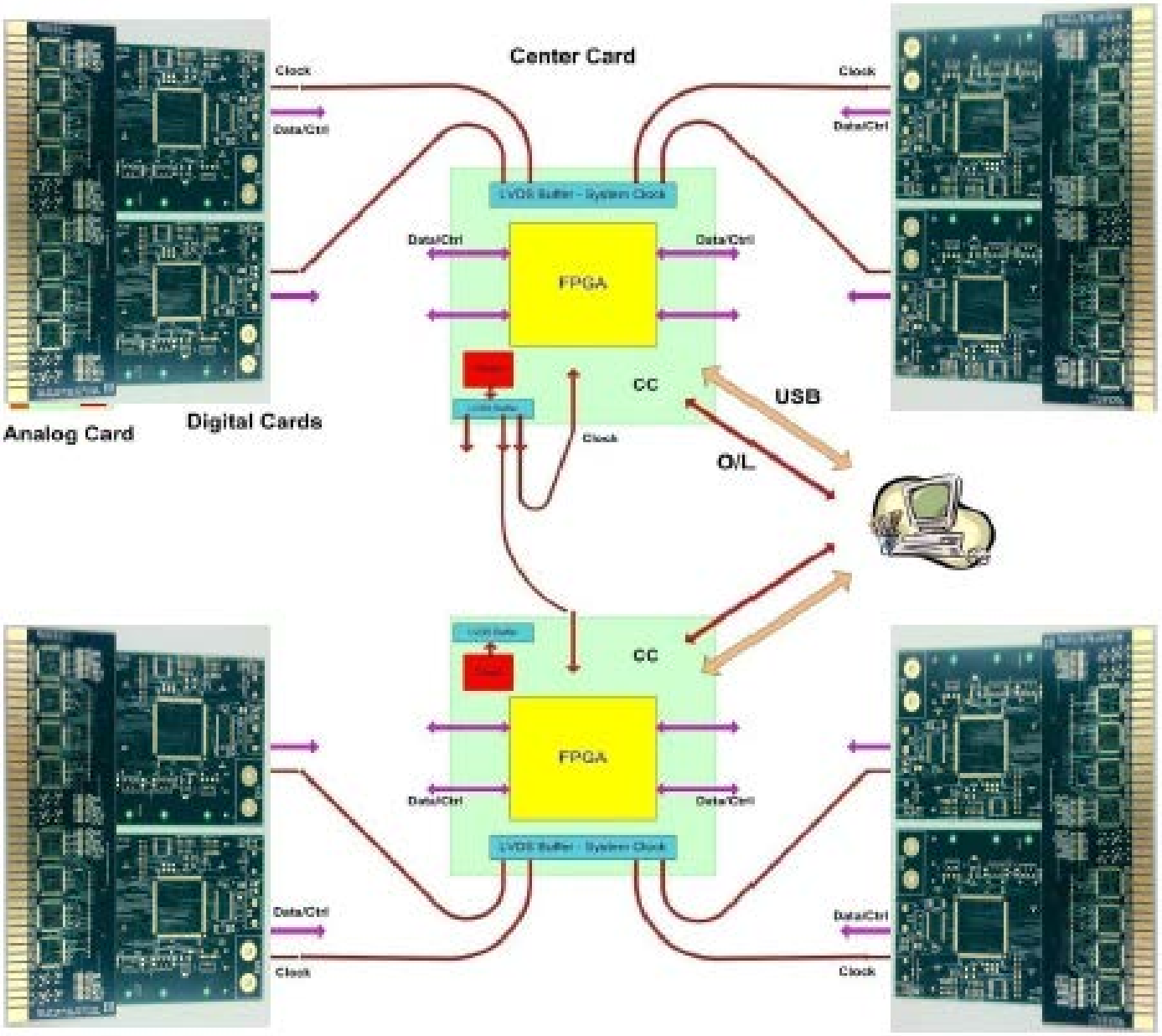
Portfolio of options, ever expanding

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2/3	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.

➔ **Success of PSEC: proof-of-concept of moving toward smaller feature sizes.**

- Next DRS plans to use 110nm; next SAM plans to use 180 nm.

Tile Assembly Readout System Overview

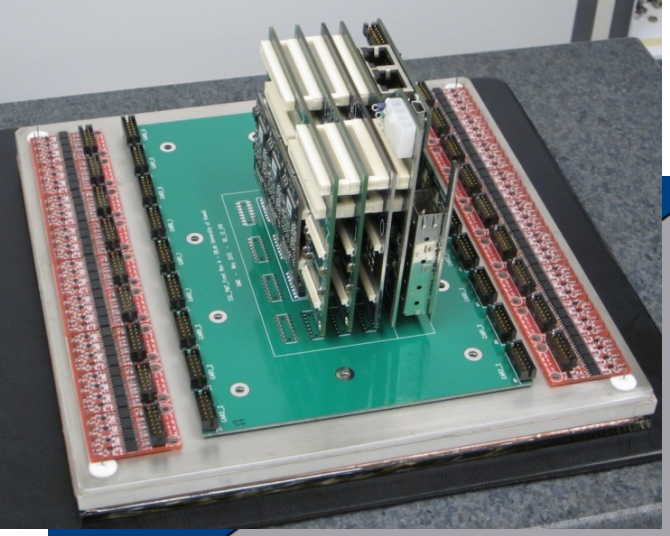


Respin Analog card only for different ASIC

A variety of data collection configurations possible

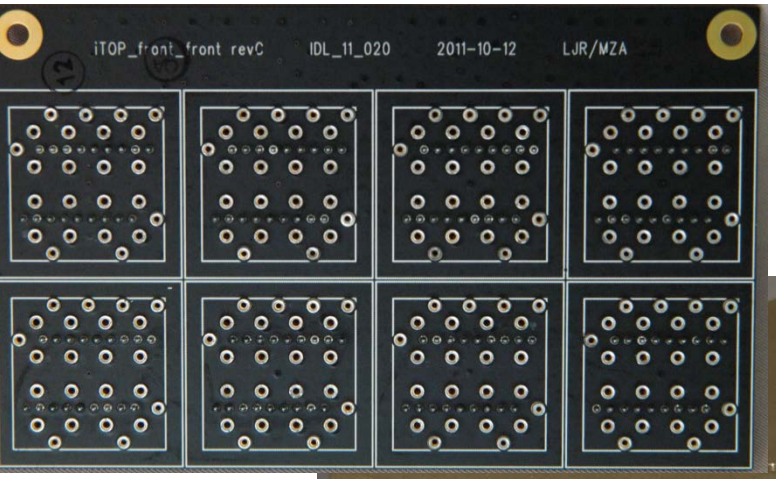
Demonstrate timing distribution @ ps level between modules

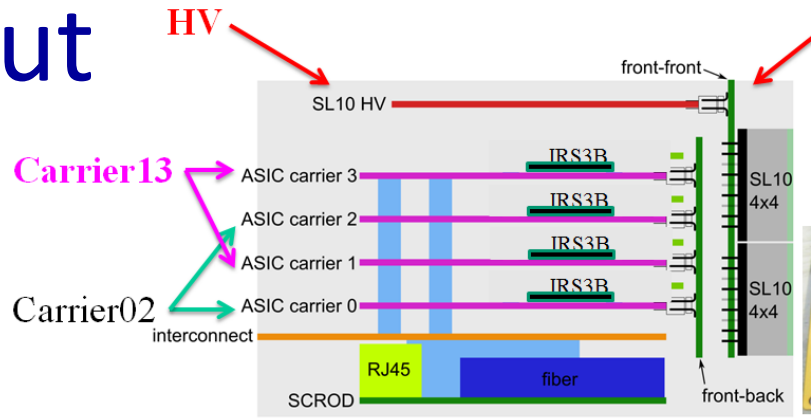
Ceramic 8” MCP design

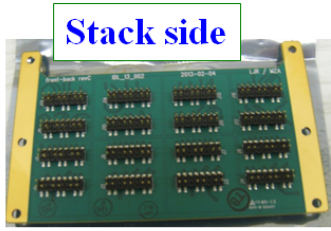


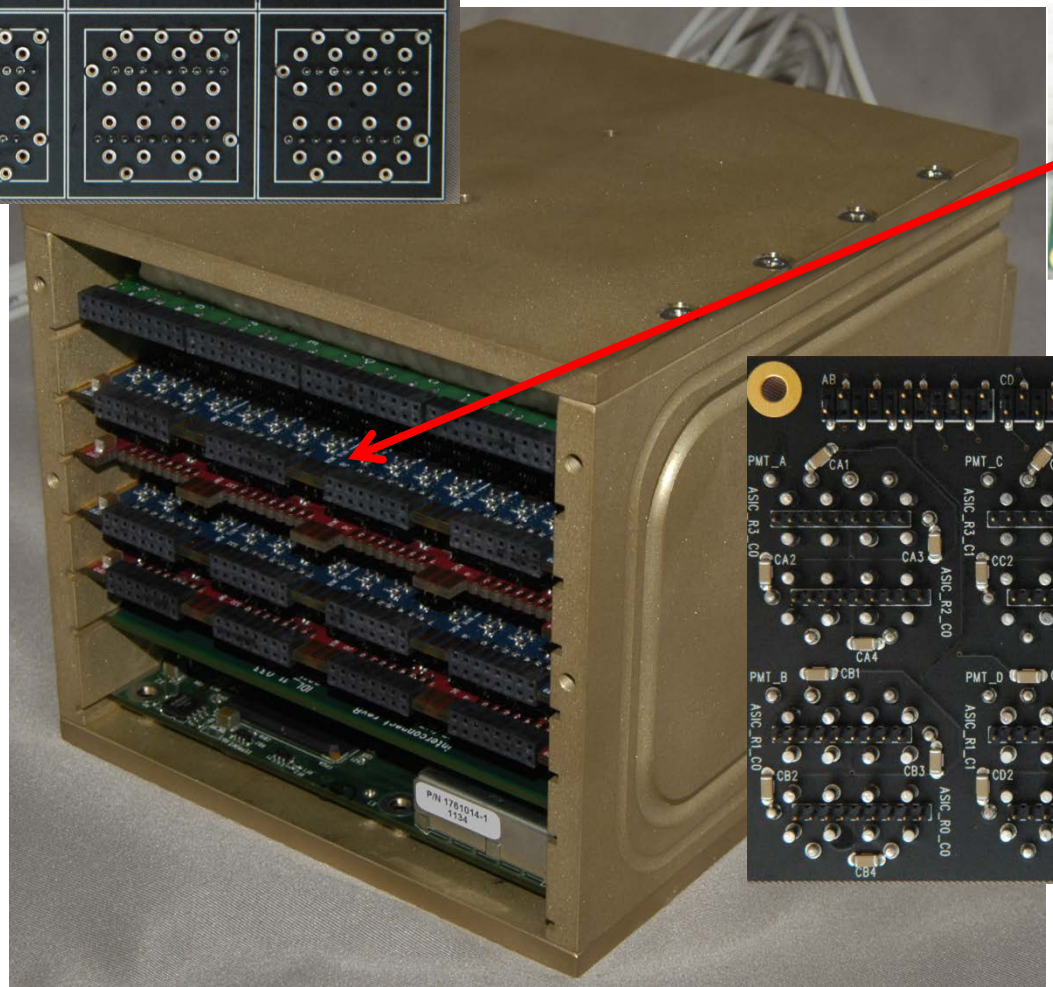
- Mechanically different configuration
- Leverage Belle II iTOP HW/FW development effort
- Single p.e. TTS limitation

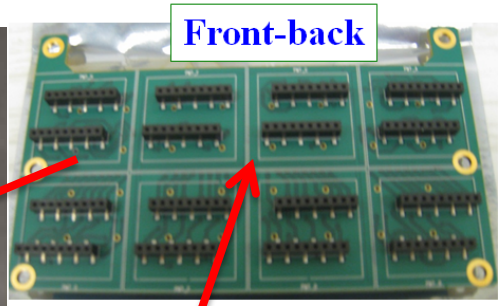
Pixellated Readout

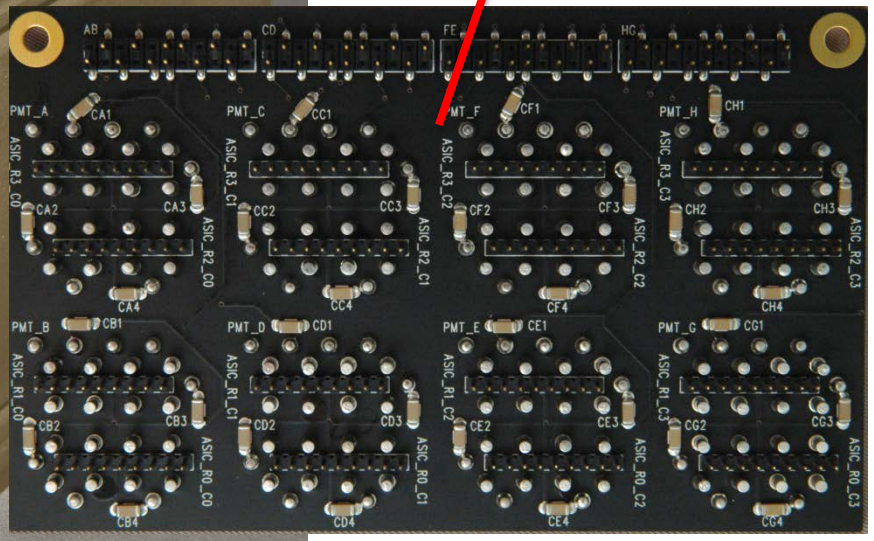












9

IRS3B ASIC Specifications

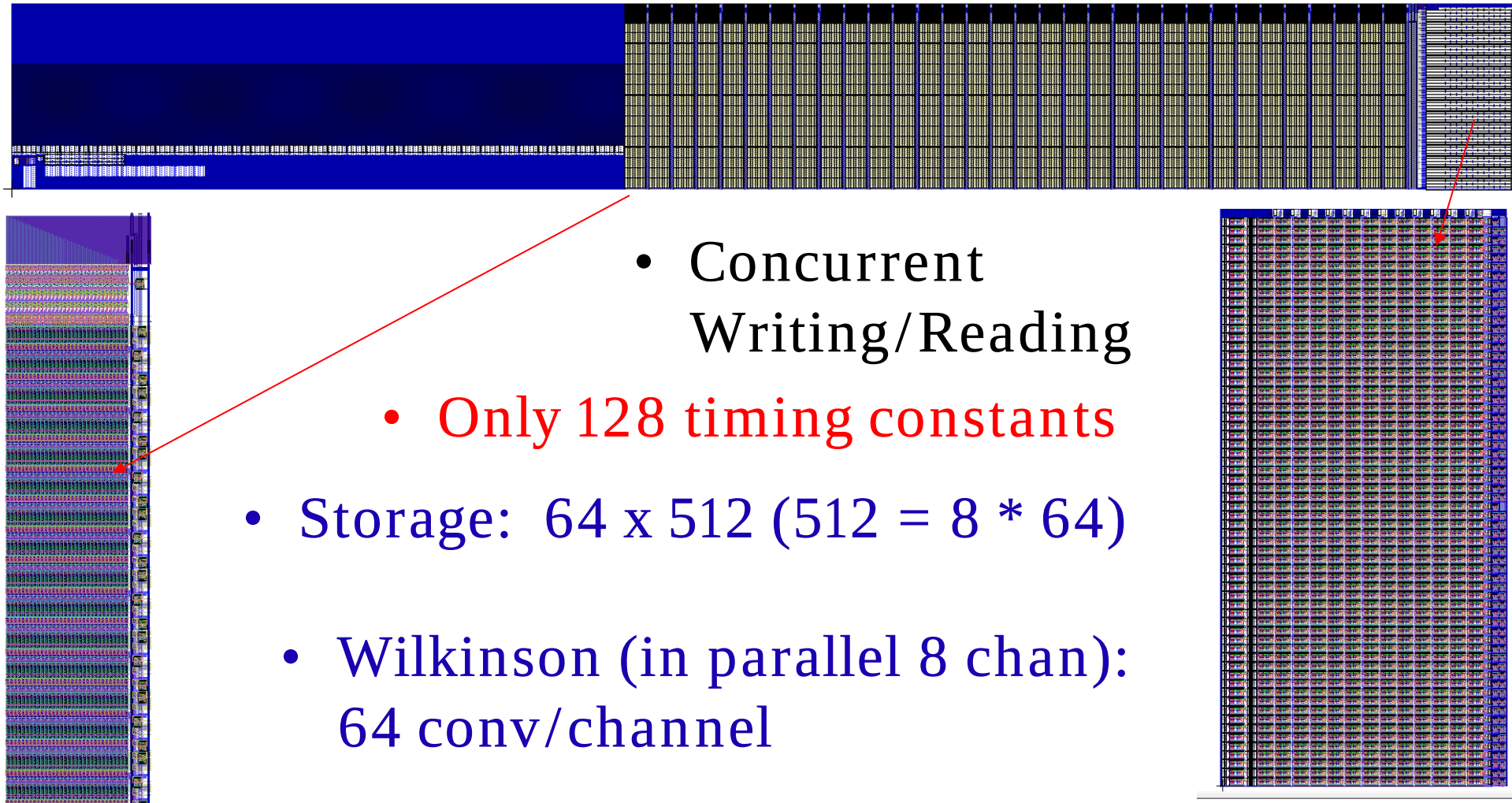
32768	samples/chan (>5.2μs trig latency)
8	channels/BLAB3 ASIC
8	Trigger channels
~9	bits resolution (12[10]-bits logging)
64	samples convert window (~16ns)
4	GSa/s
1	word (RAM) chan, sample readout
1+n*0.02	μs to read n samples (of same 64)
30	kHz sustained readout (multibuffer)

- Time alignment critical
  - Synchronize sampling to accelerator RF clock (Belle TOF)
  - >5μs buffer depth a must for trigger, since single photon rates high

Multi-stage transfer (single channel)

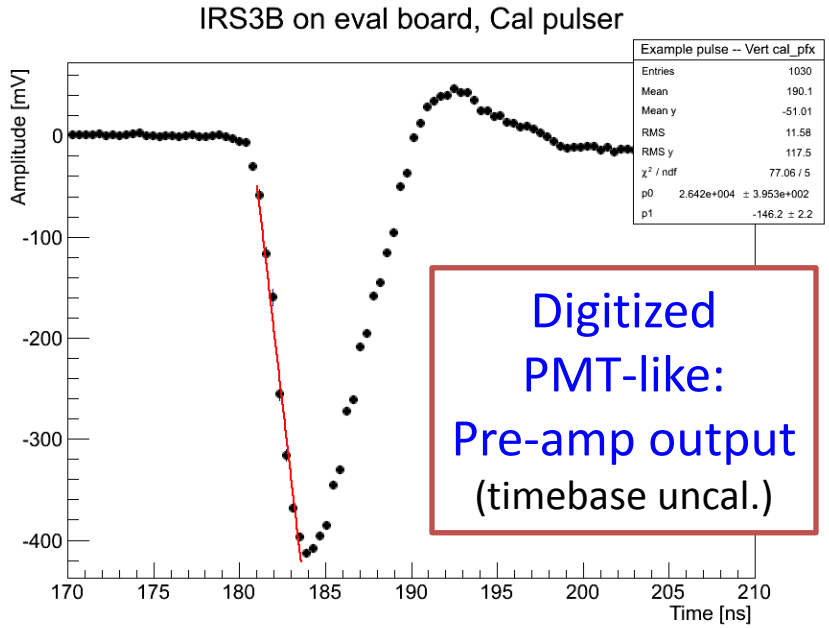
- Sampling: 128 (2x 64) separate transfer lanes

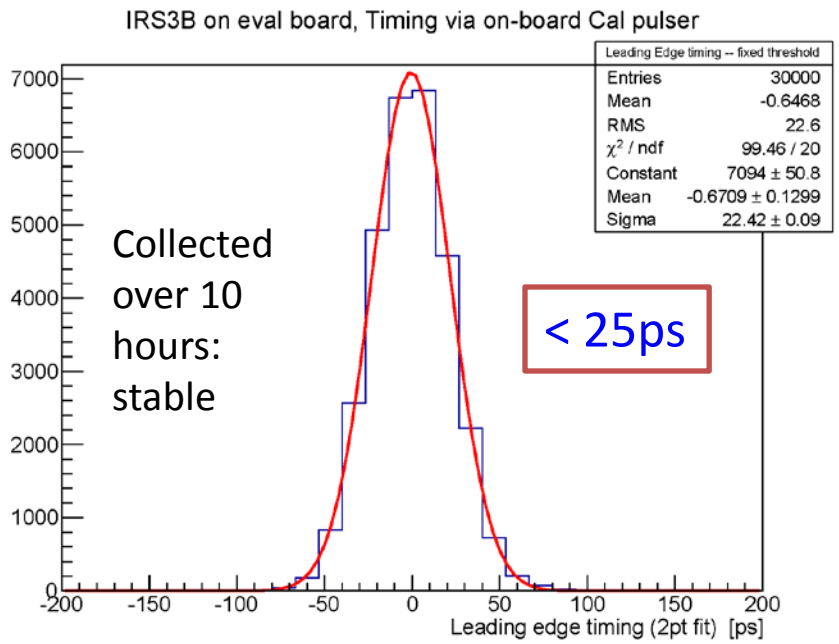
Recording in one set 64, transferring other ("ping-pong")

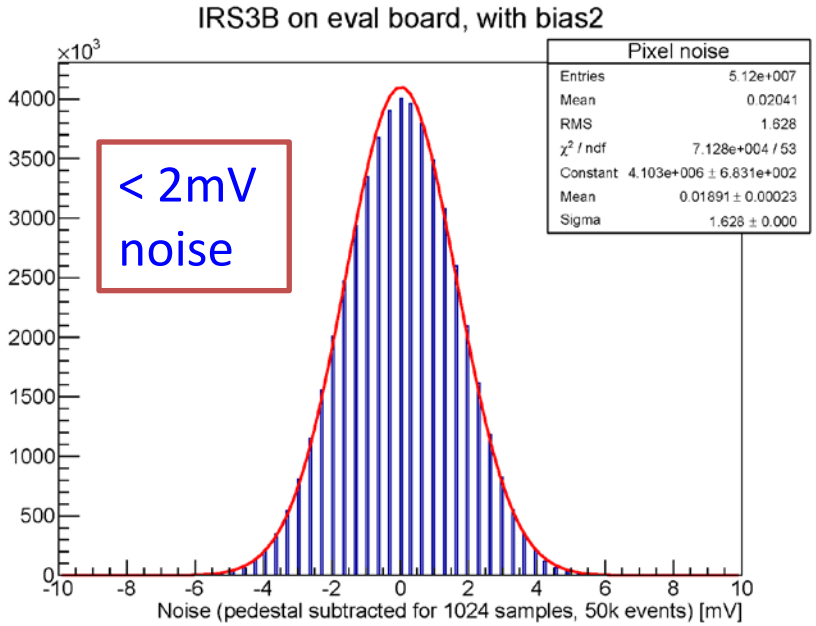


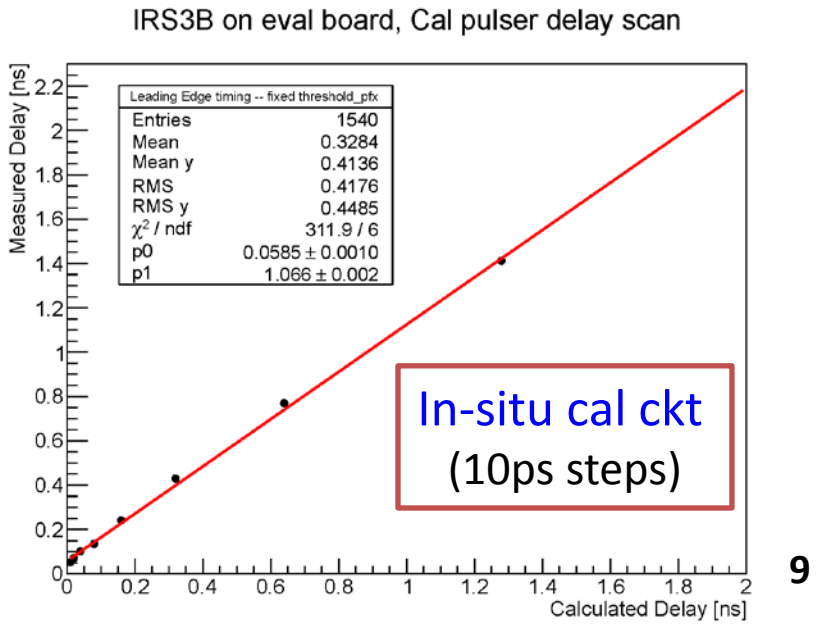
- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (512 = 8 * 64)
- Wilkinson (in parallel 8 chan): 64 conv/channel

IRS3B in system

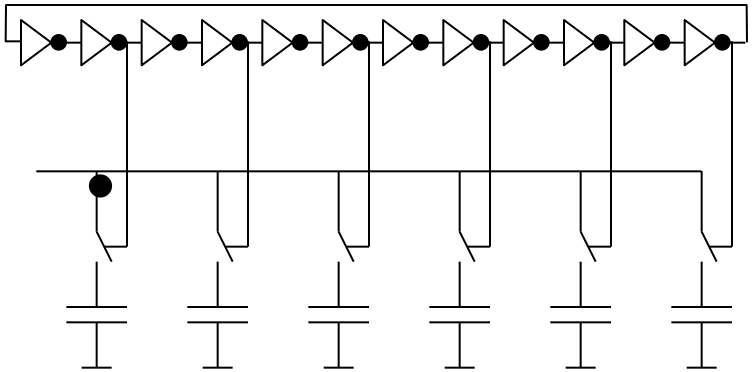


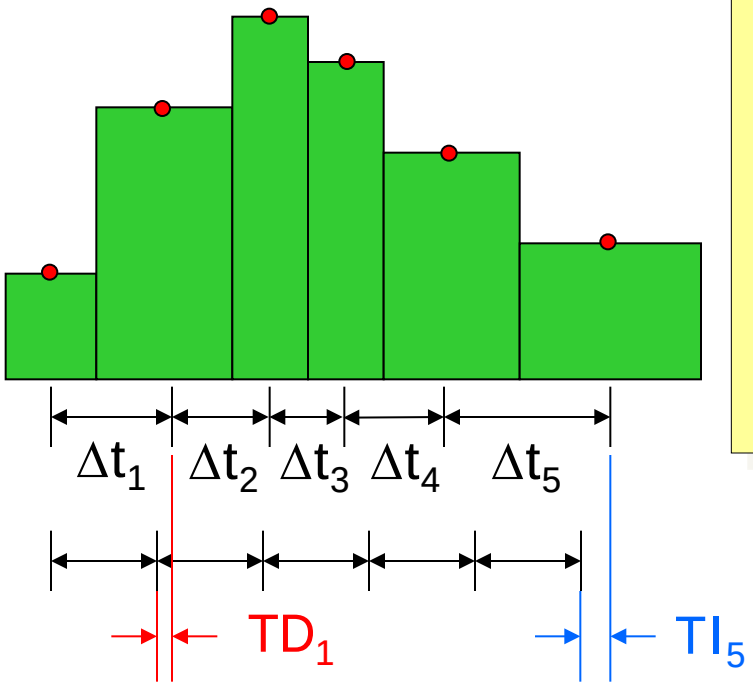






Non-uniform timebase

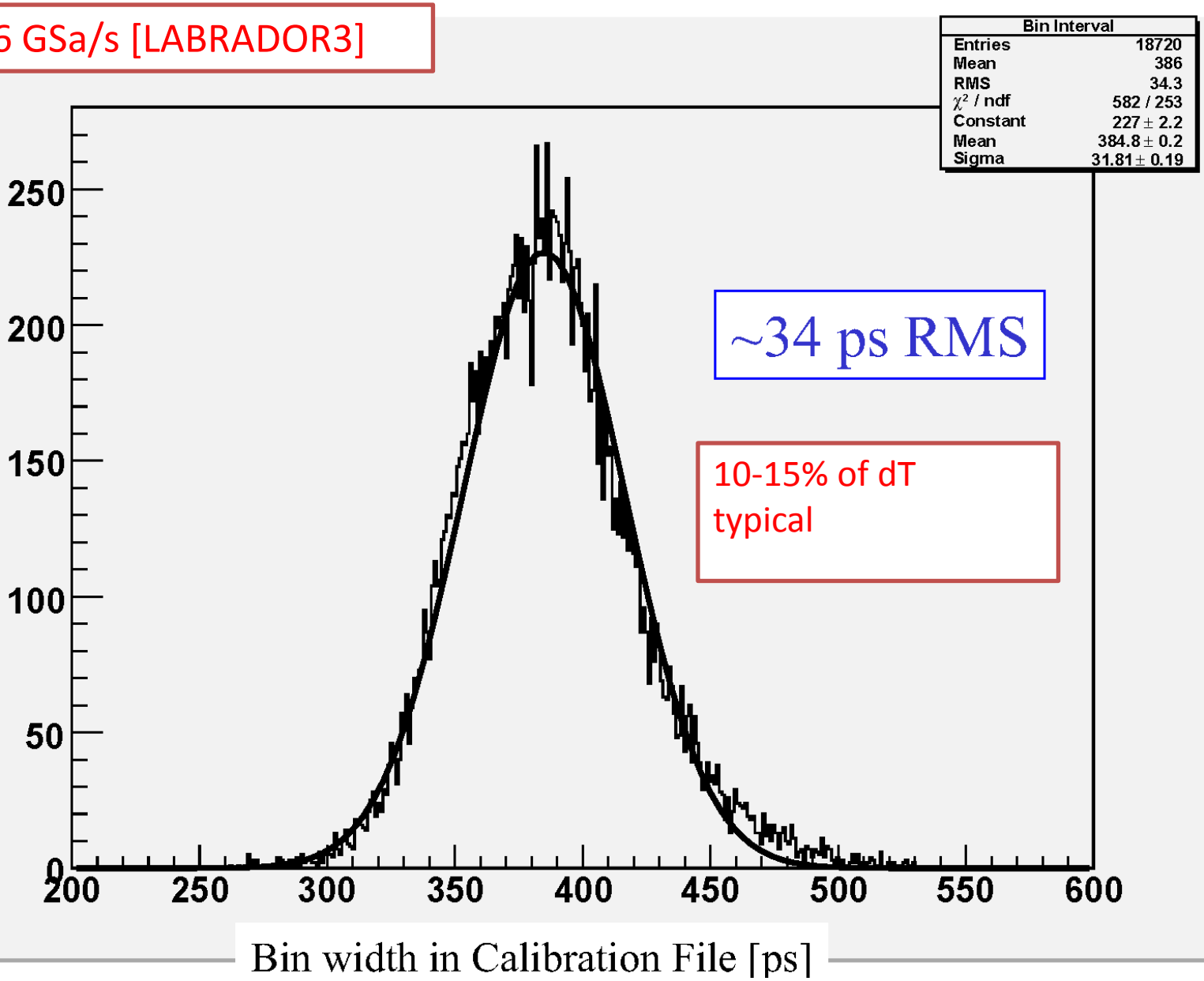




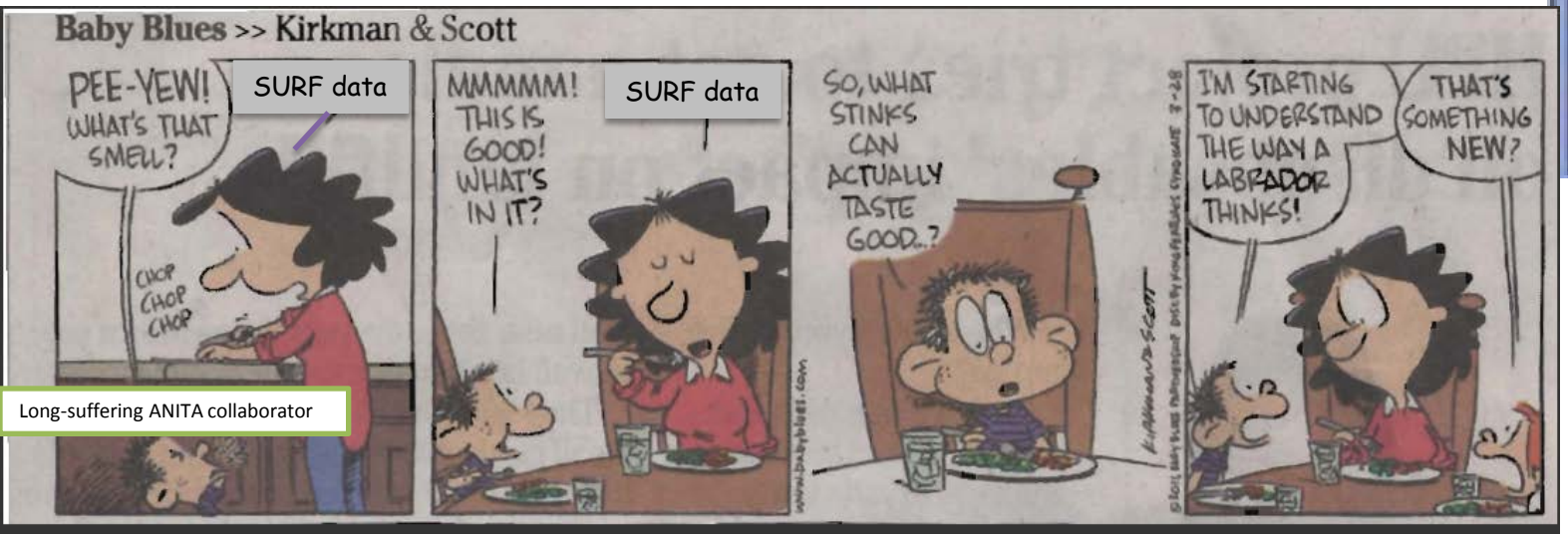
- Inverter chain has transistor variations
  → Δt_i between samples differ
  → "Fixed pattern aperture jitter"
- "Differential temporal nonlinearity"
  $TD_i = \Delta t_i - \Delta t_{nominal}$
- "Integral temporal nonlinearity"
  $TI_i = \Sigma \Delta t_i - i \cdot \Delta t_{nominal}$
- "Random aperture jitter" = variation of Δt_i between measurements

dT Spread

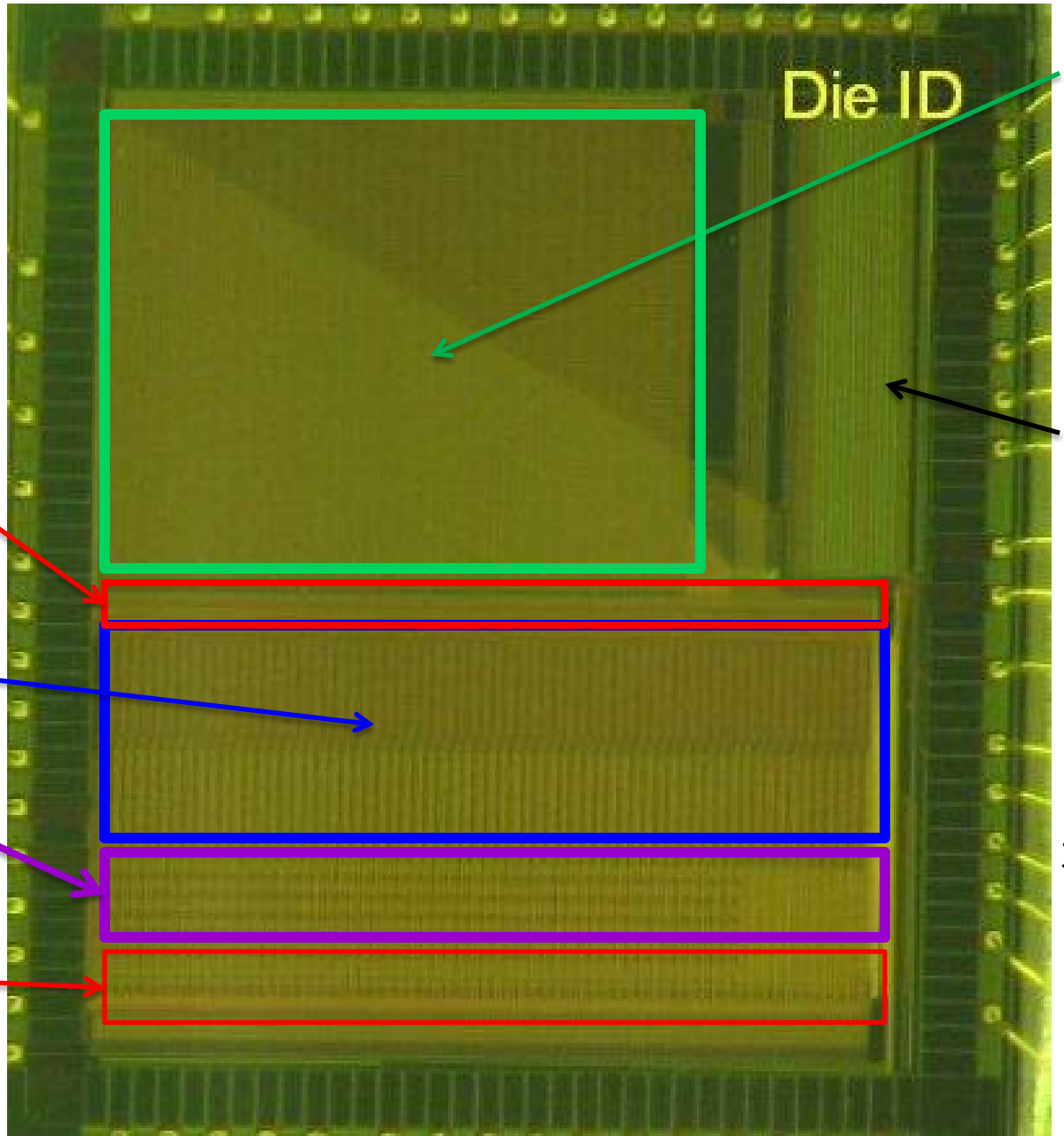
2.6 GSa/s [LABRADOR3]



Non-uniform sampling timebase



LAB4B: “fix timebase in hardware”



Storage Array

2nd stage transfer

Wilkinson Registers

dT trim DACs

Timing Generator

3.6 x 4.2mm

Sampling array

Even ASIC-less architectures

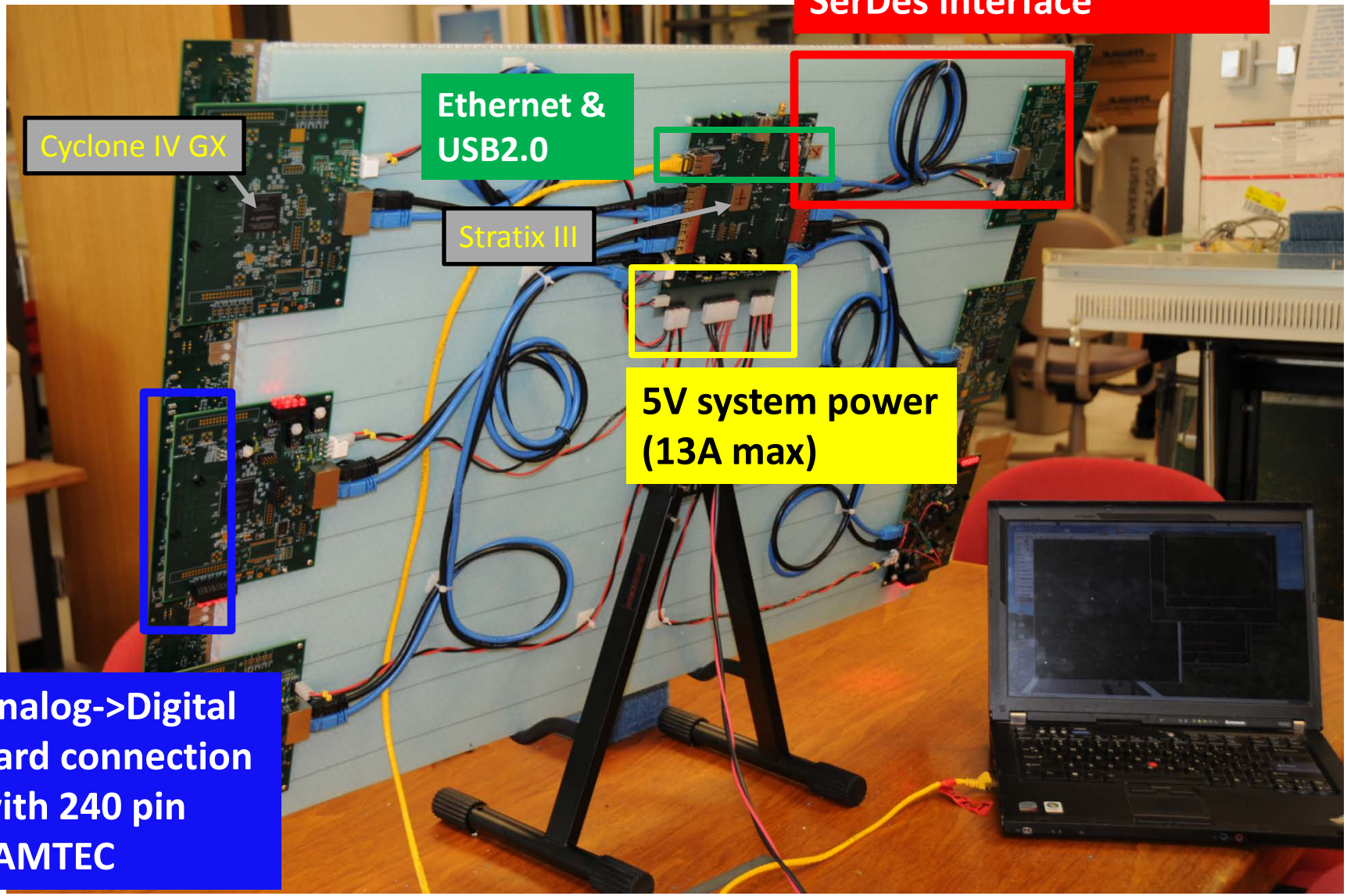
- **Going back to 2007, can use FPGAs**
  - **High-speed comparator**
  - **TDC**
  - **TOT for rough amplitude information**
  - **<100ps timing possible**
- **Low cost, high density, and need FPGA for data collection anyway**
- **If need DACs for thresholding, for large systems ASICs probably still preferred. Though not always.**

IRS3B or ASICs Summary

- A number of options now available – can be tailored to specific needs:
  - <= 1 ps timing (PSEC family)
  - High channel count
  - Long (10's of us) trigger latency
  - High trigger rate/througput
- Front-end and common back-end support a serious issue
- Reality of "large" systems is that a custom readout likely to be developed (gain, optimal information extraction, in-house control, etc)

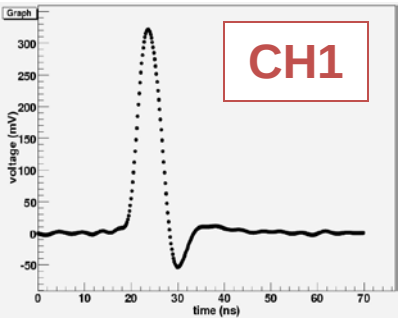
Backup

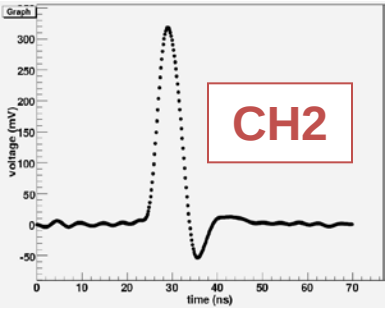
Super Module: features

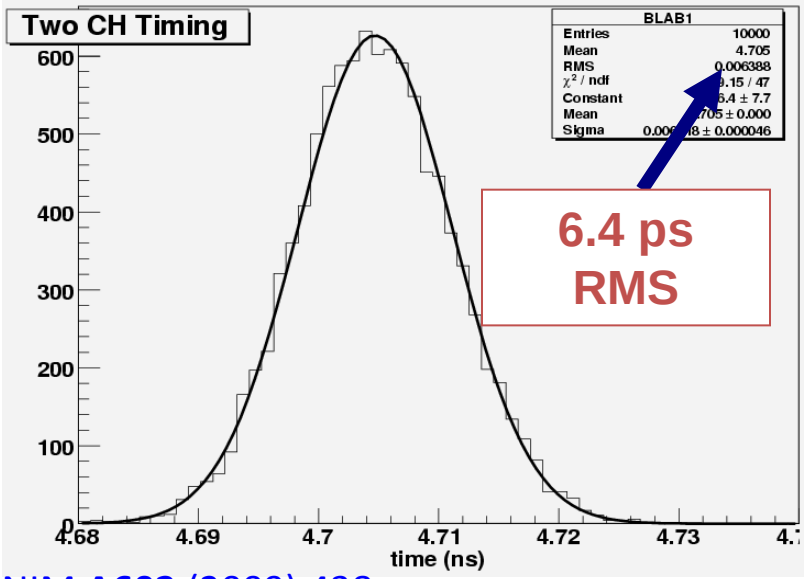


Readout Electronics

- Building on experience from existing devices & readouts.
  - Readout based on waveform sampling
  - Requirements of the readout vary significantly by application

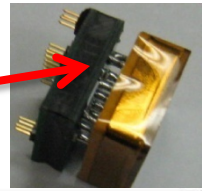


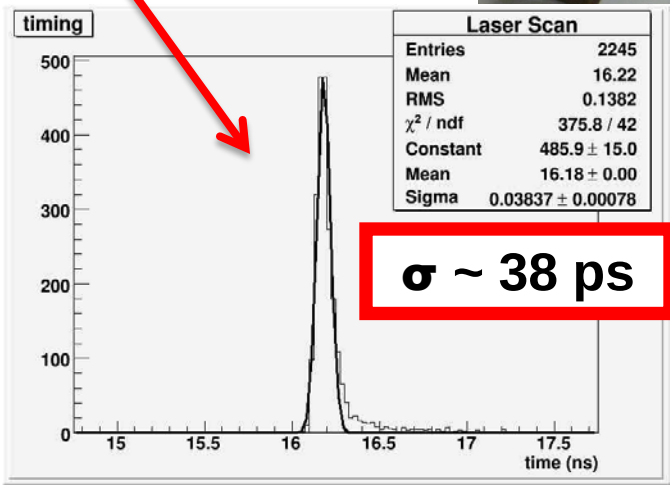




NIM **A602** (2009) 438

4x4 anode “1 inch”
MCP-PMT (HPK SL-10)





Single p.e. resolution