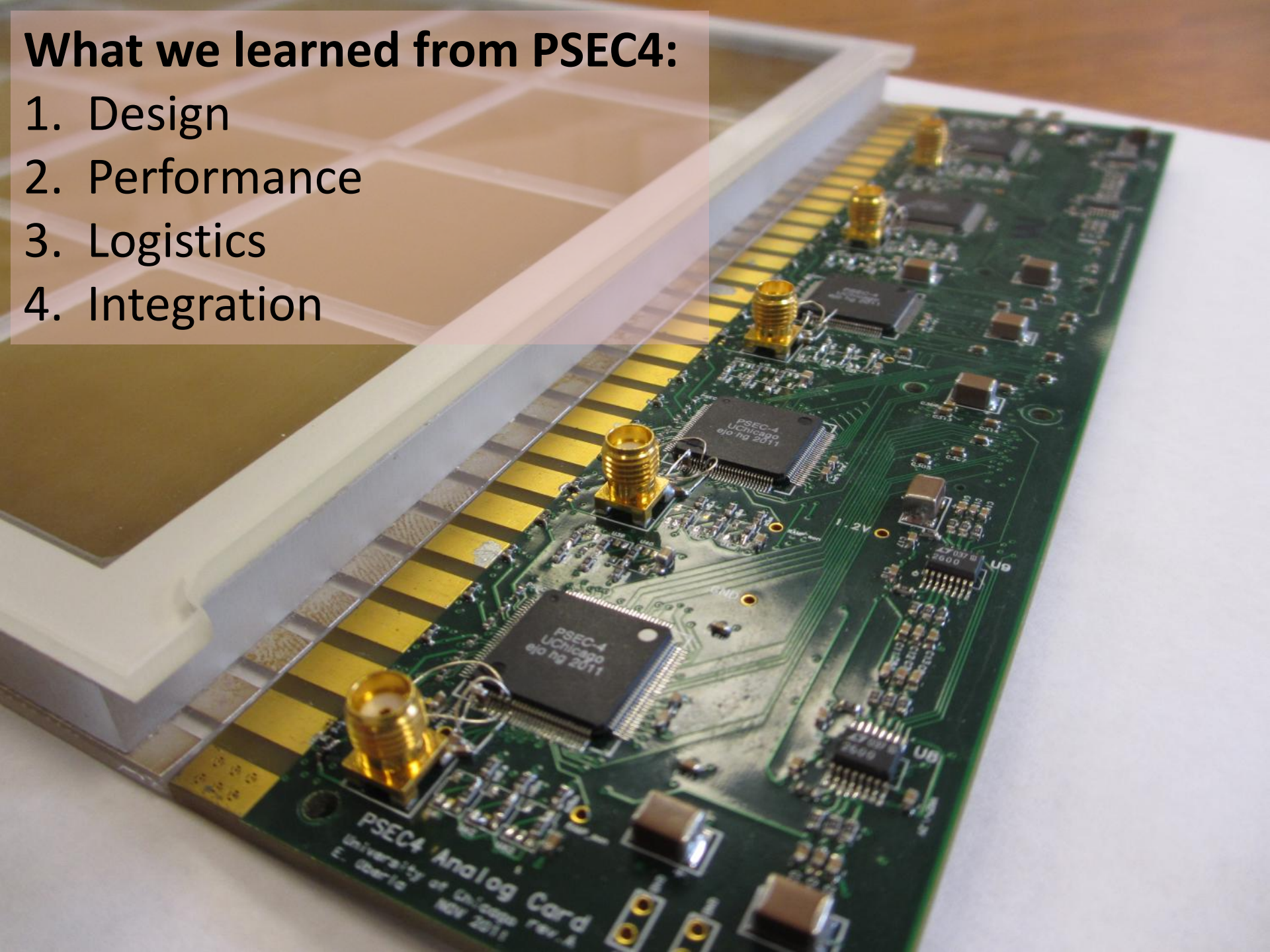
What We Learned from **PSEC4**

Eric Oberla

LAPPD2 Electronics Review

6-April-2013

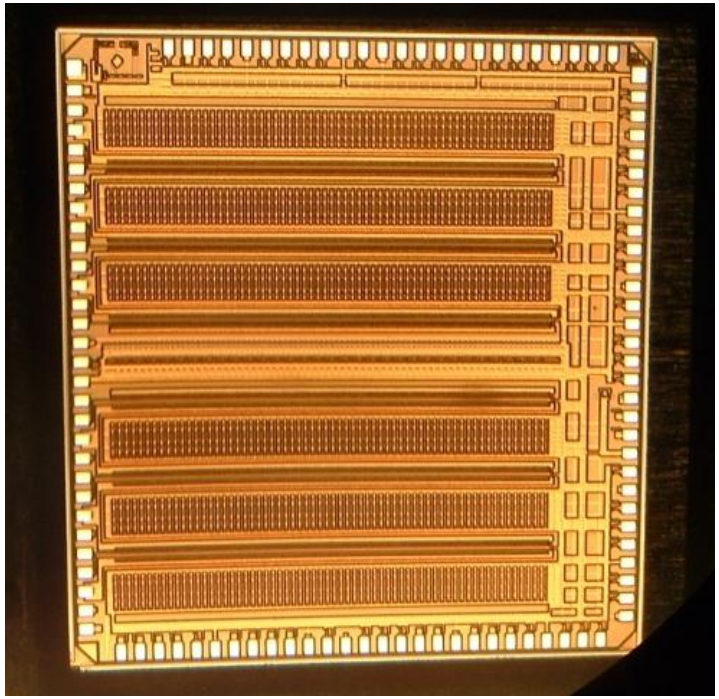

What we learned from PSEC4:
1. Design
2. Performance
3. Logistics
4. Integration
PSEC4 Analog Card

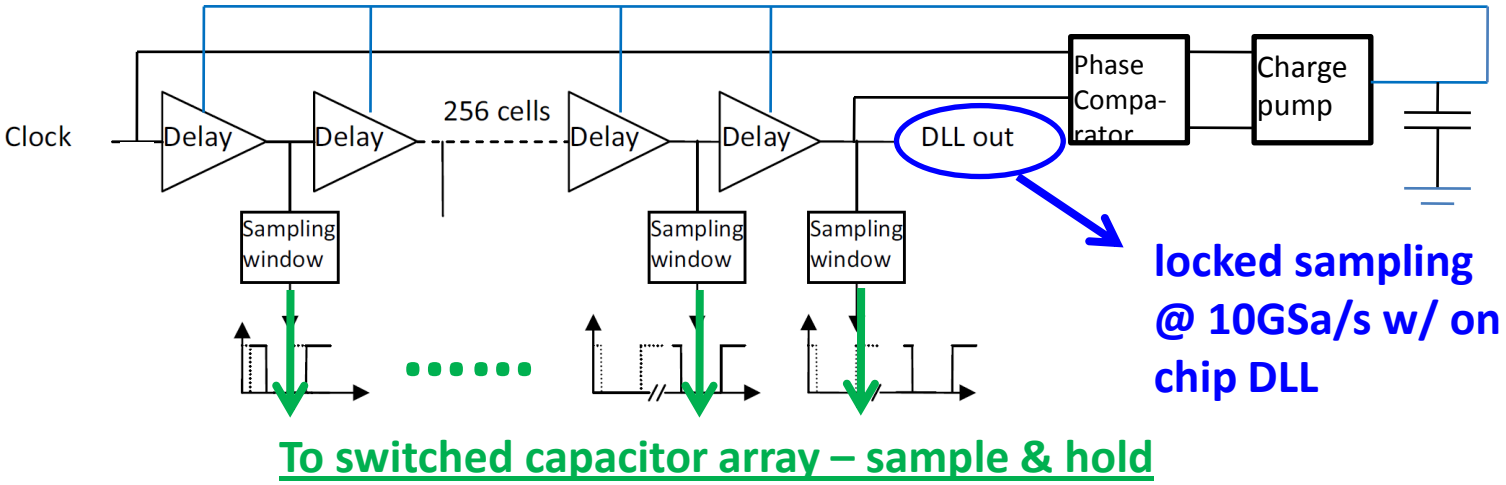
1) Design: PSEC4

10-15 Gsa/s Switched capacitor array sampling: ***'analog down-conversion'***

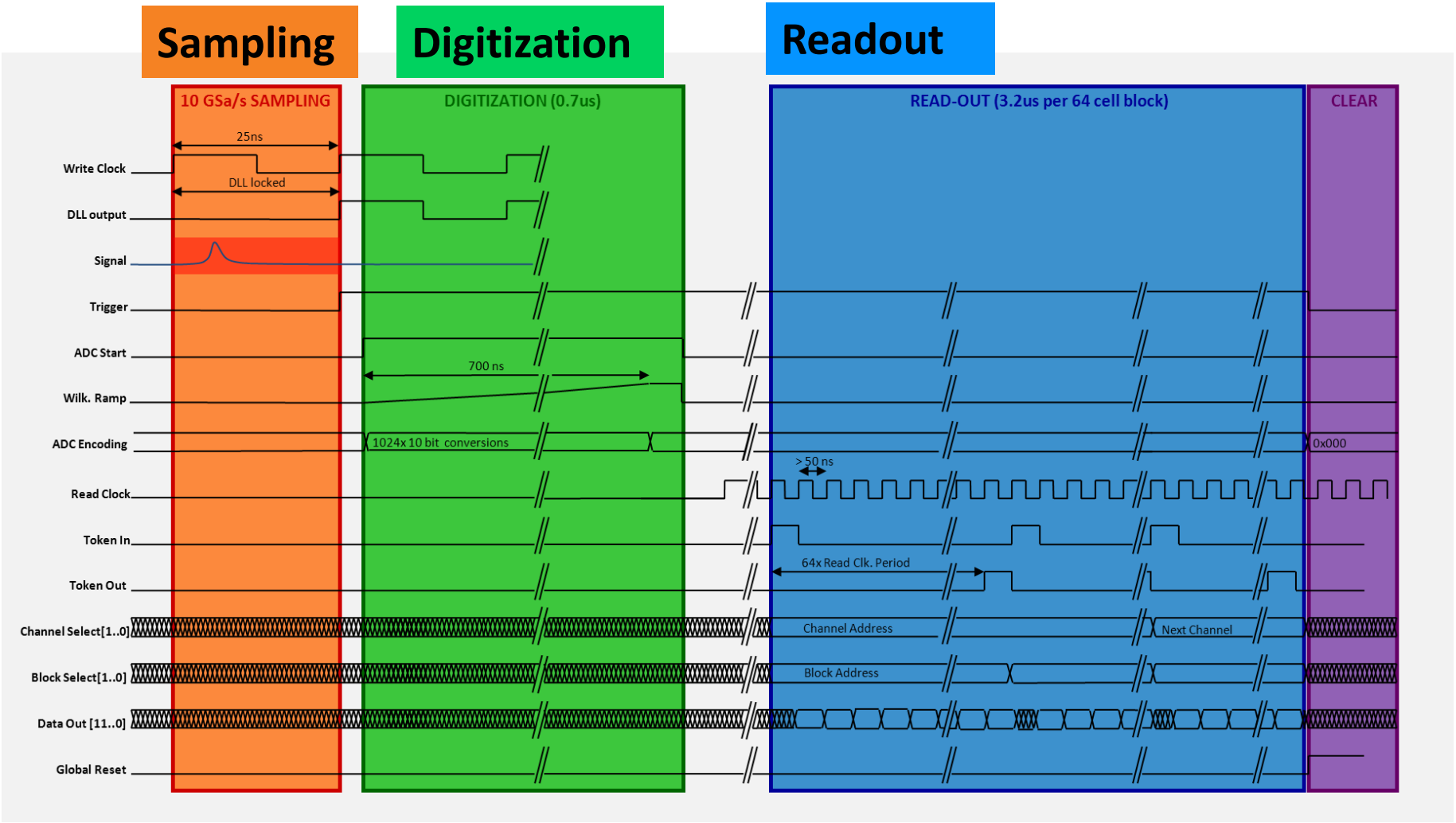
[GHz sampling→ 10-100 MHz readout: useful in most 'triggered event' applications]

Designed to sample & digitize fast pulses (MCPs):



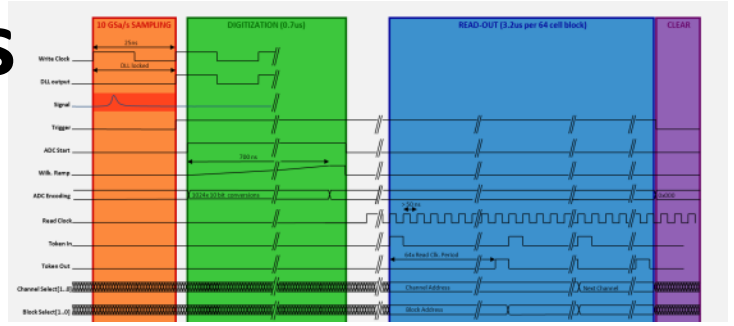


1) Design: How PSEC4 works

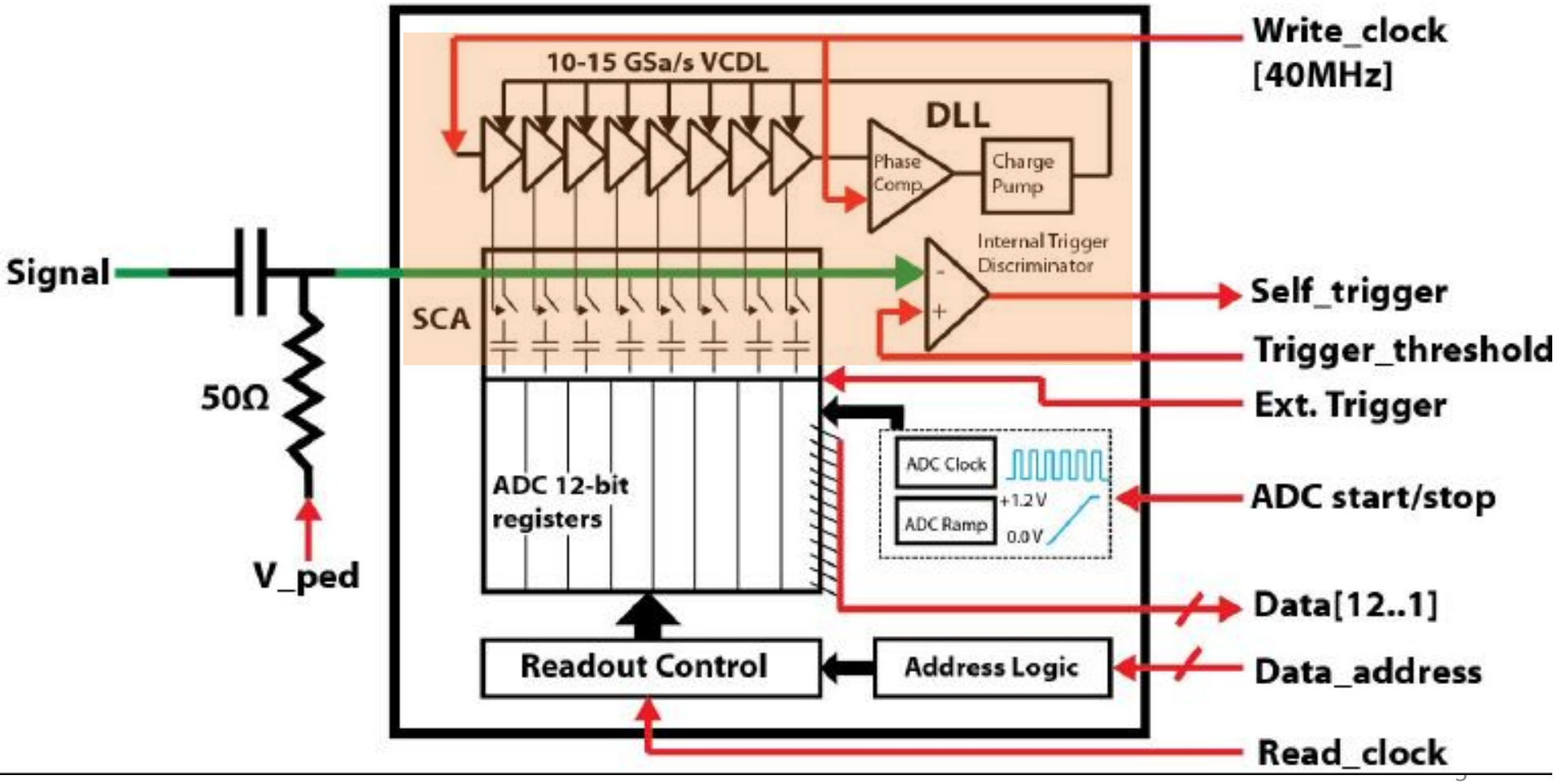


- *PSEC-3 timing shown (roughly the same), though PSEC-4 can run readout 2x faster – highly serial…

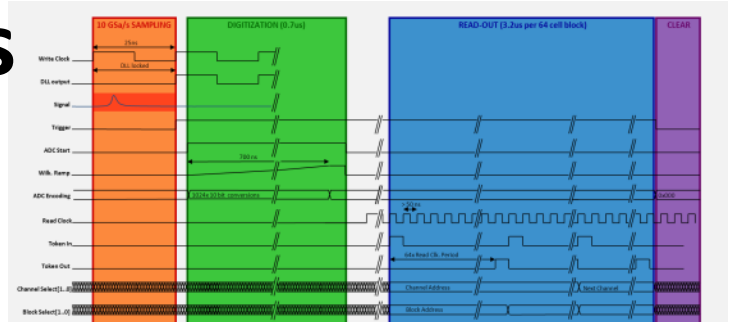
1) Design: How PSEC4 works



Sampling

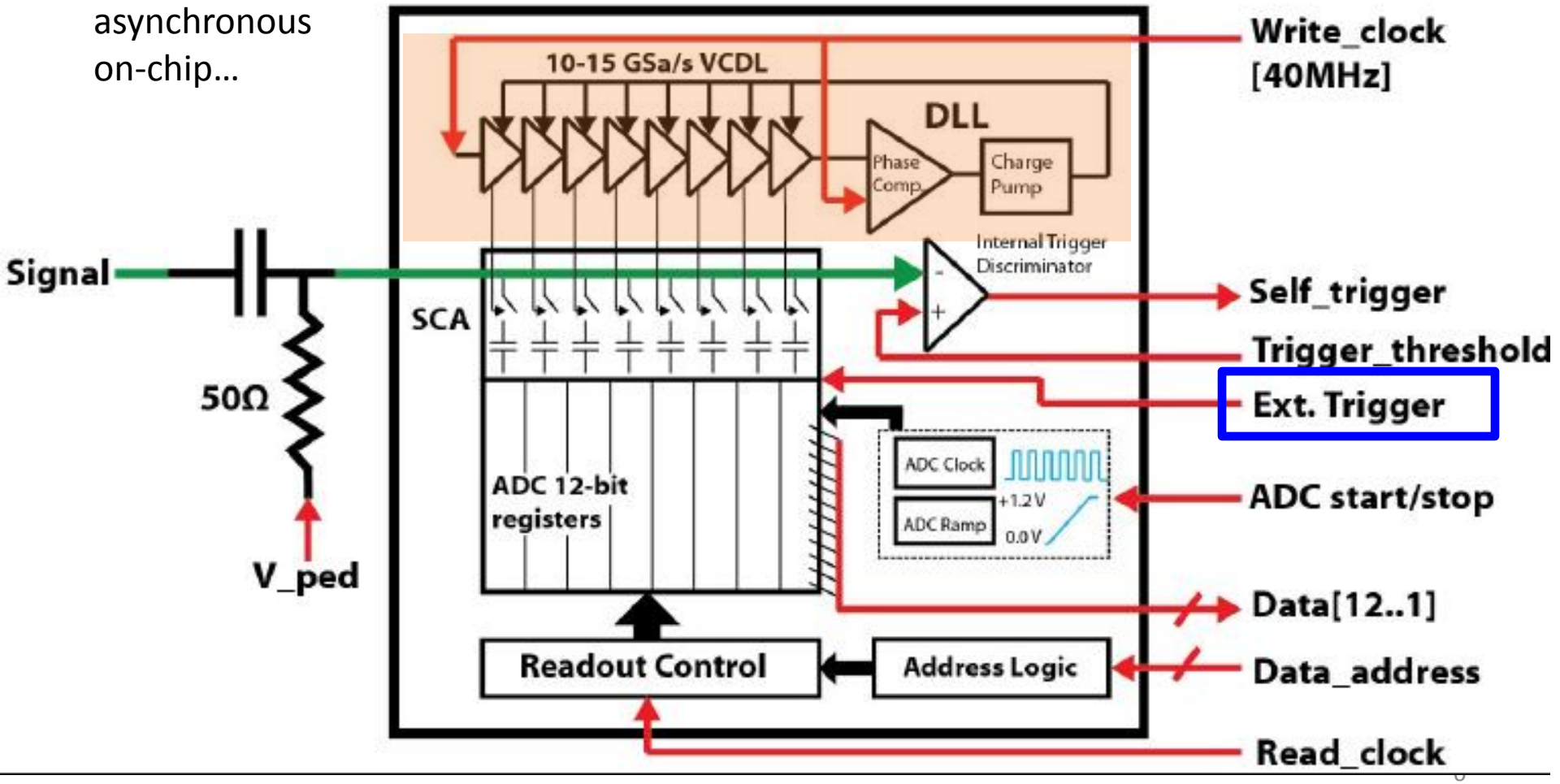


1) Design: How PSEC4 works

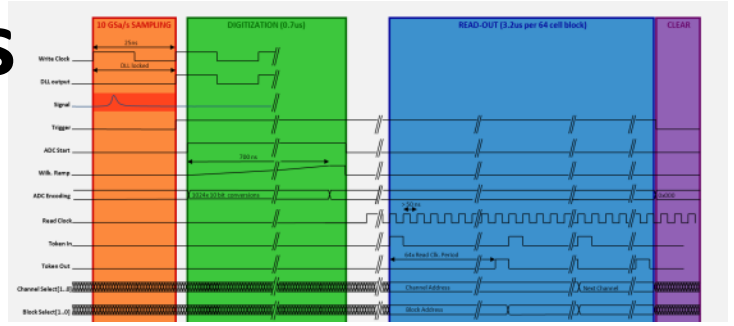


TRIGGER! Sampling

Trigger is asynchronous on-chip…

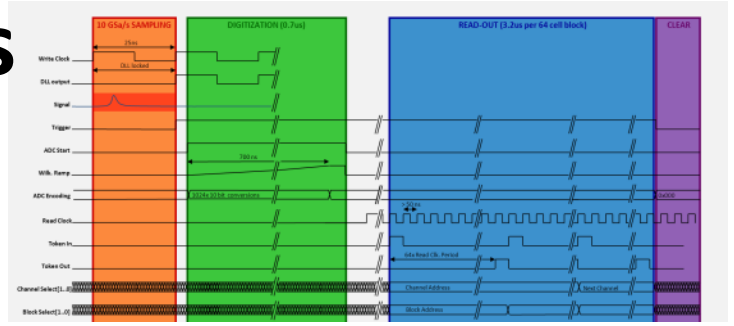


1) Design: How PSEC4 works



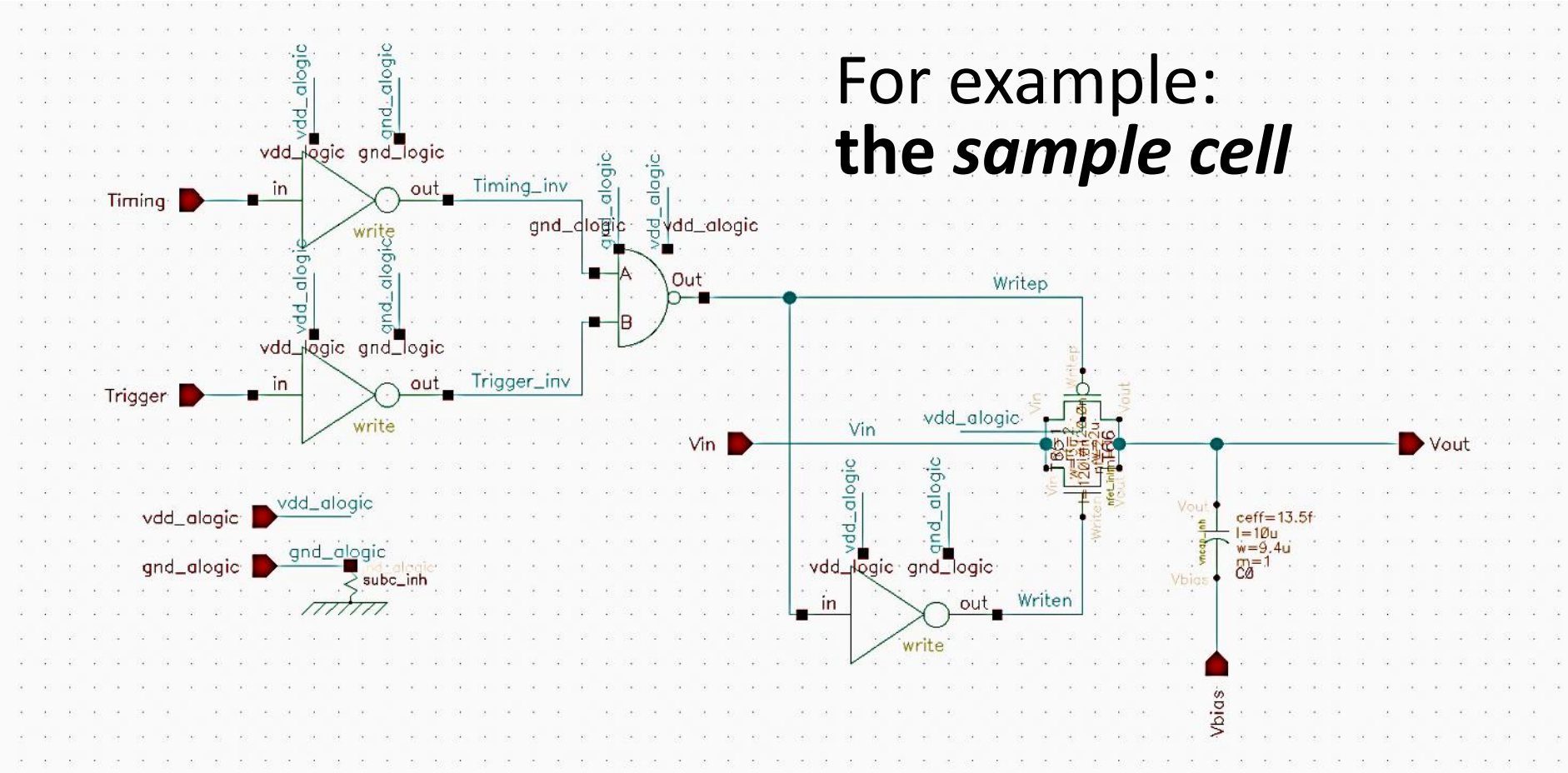
Digitization

1) Design: How PSEC4 works

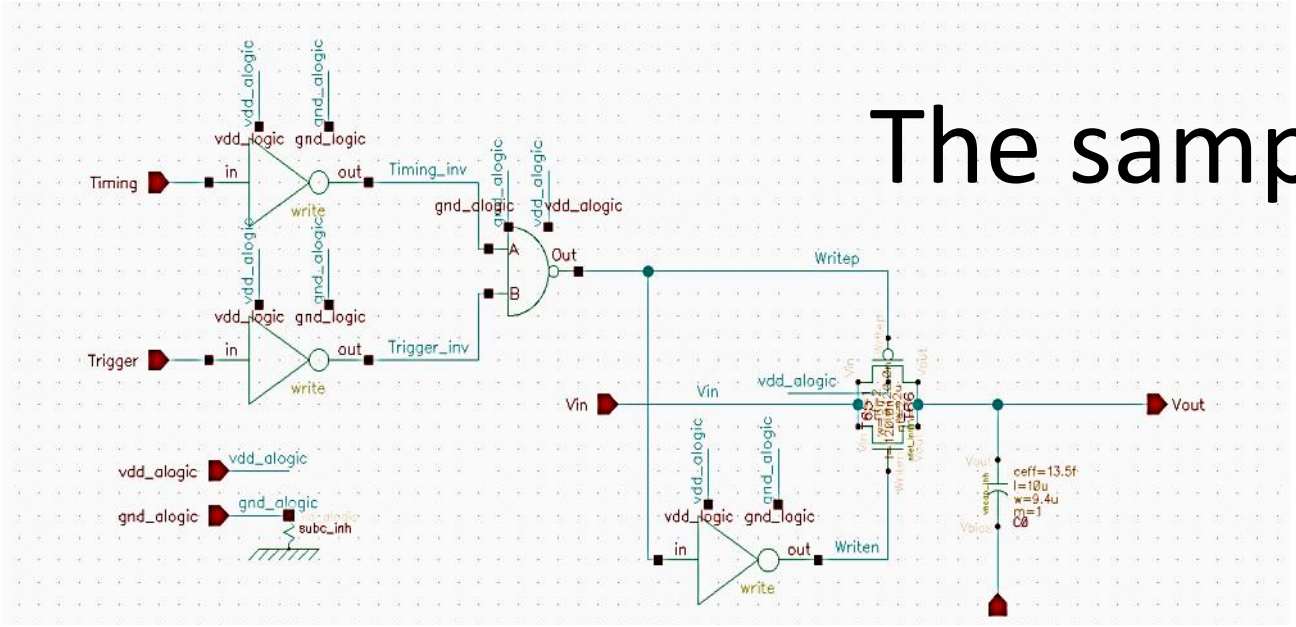


Readout

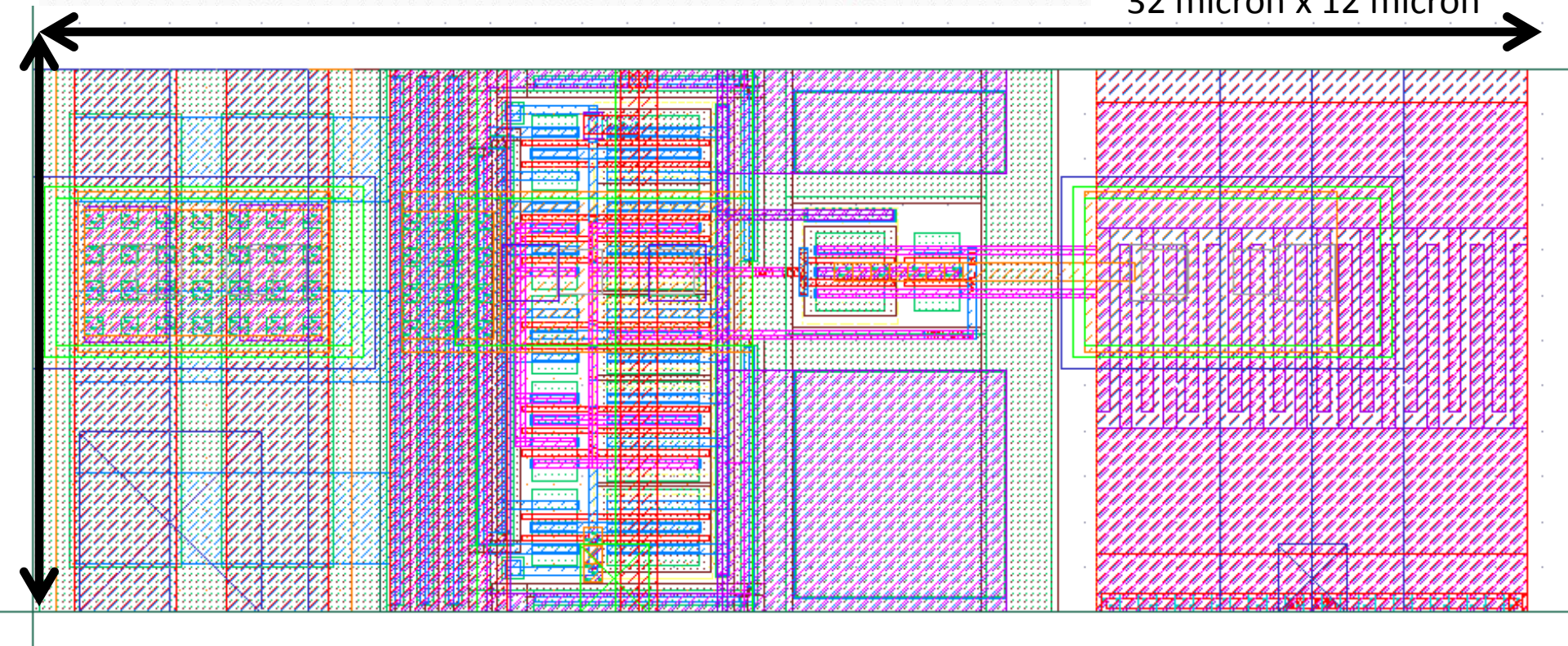
1) Design: circuit building blocks



The sample cell



32 micron x 12 micron

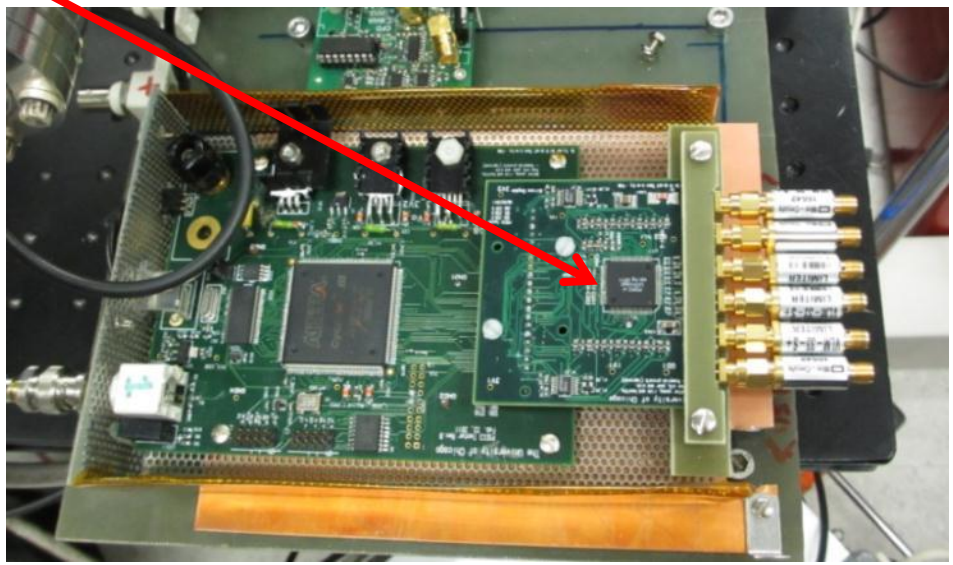


PSEC-4 ASIC (*University of Chicago*)

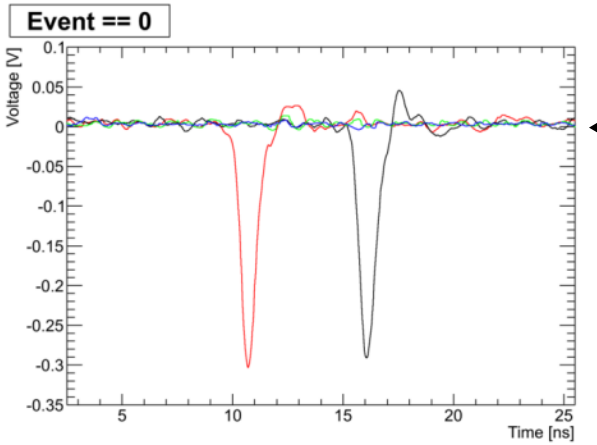
10-15 GSa/a Waveform Sampling ASIC

Designed as part of the Large-Area Picosecond Photo-Detector **(LAPPD)** project

	ACTUAL PERFORMANCE
Sampling Rate	2.5-15 GSa/s
# Channels	6
Sampling Depth	256 points (17-100 ns) per channel
Input Noise	<1 mV RMS
Analog Bandwidth	1.5 GHz (f_{3dB})
ADC conversion (ramp-compare)	Up to 12 bit (10 ENOB) clocked @ 1.6 GHz
Dynamic Range	0.1-1.1 V
Readout Latency	2 µs (min) – 16 µs (max)



6-channel PSEC-4 evaluation board in use at LAPPD micro-channel plate (MCP) test stand



Dual-end readout of LAPPD 20x20 cm² MCP w/ PSEC-4 @ 10 GSa/s

-- left anode strip
-- right anode strip

PSEC-4 ASIC (*University of Chicago*)

10-15 GSa/a Waveform Sampling ASIC

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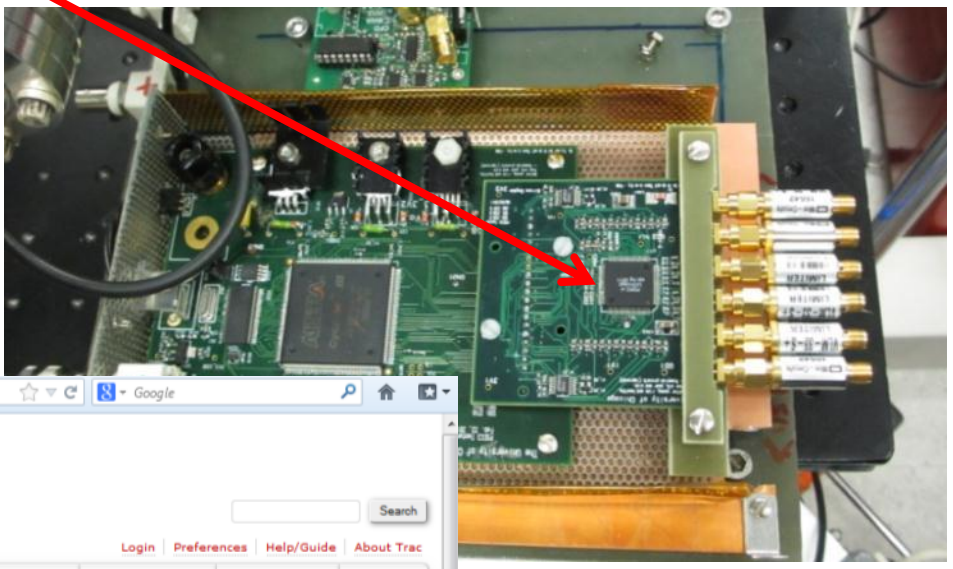
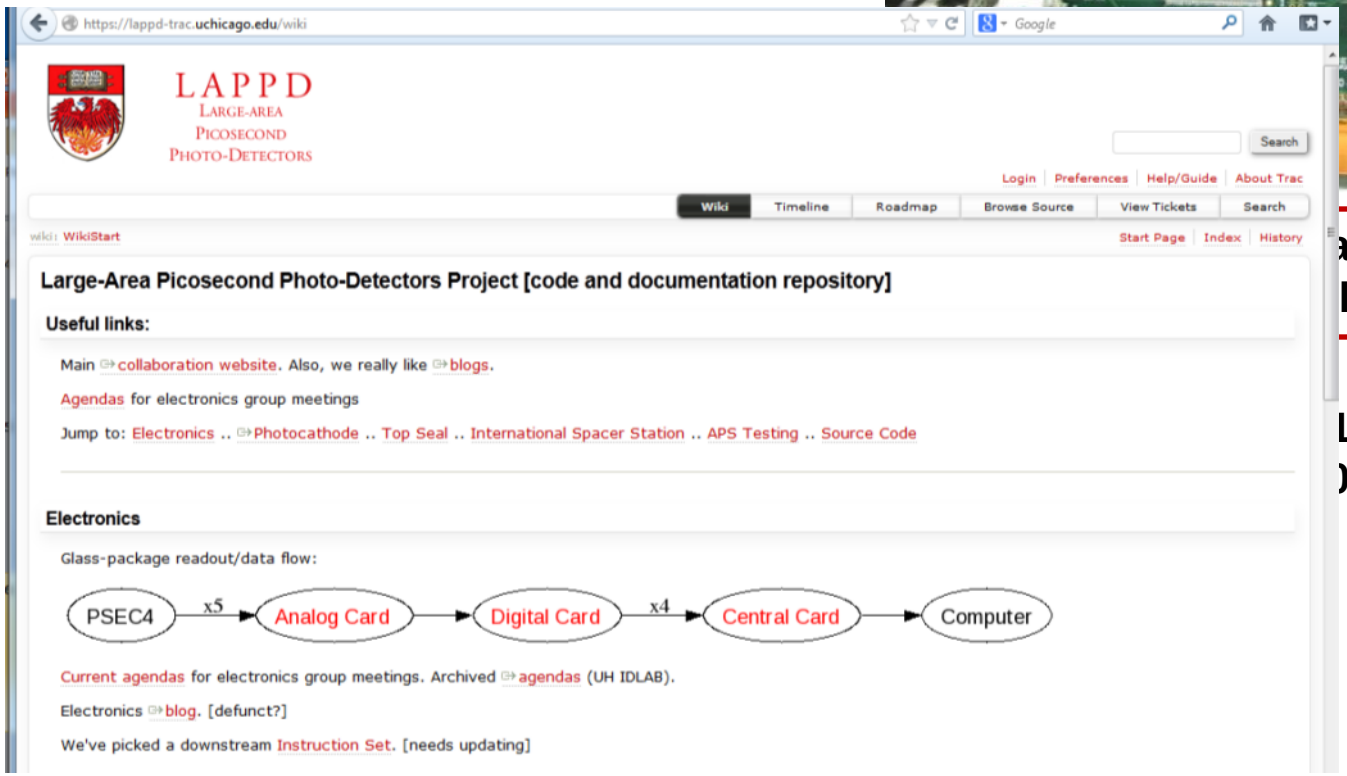
Evaluation board firmware, software, and generic analysis code up-to-date on LAPPD trac repository



aluation board in use at
l plate (MCP) test stand

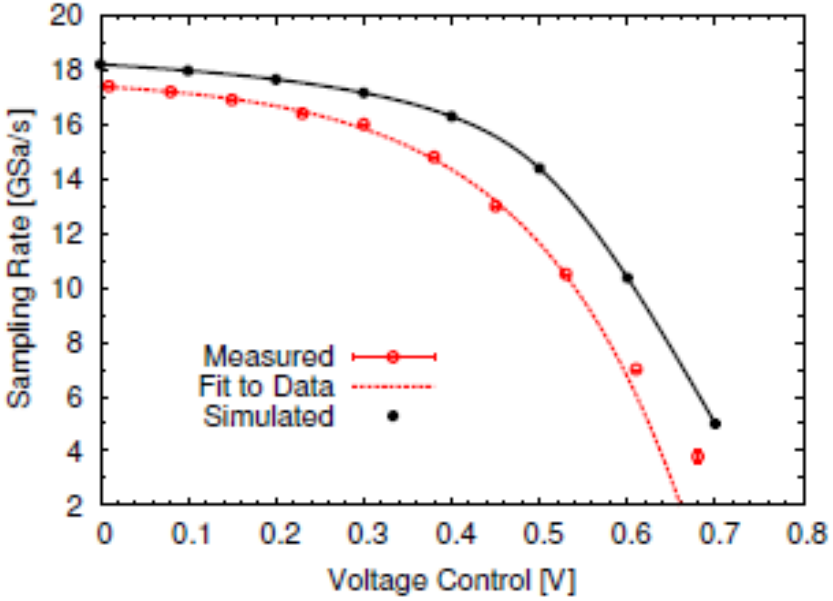
LAPPD 20x20 cm²
) GSa/s

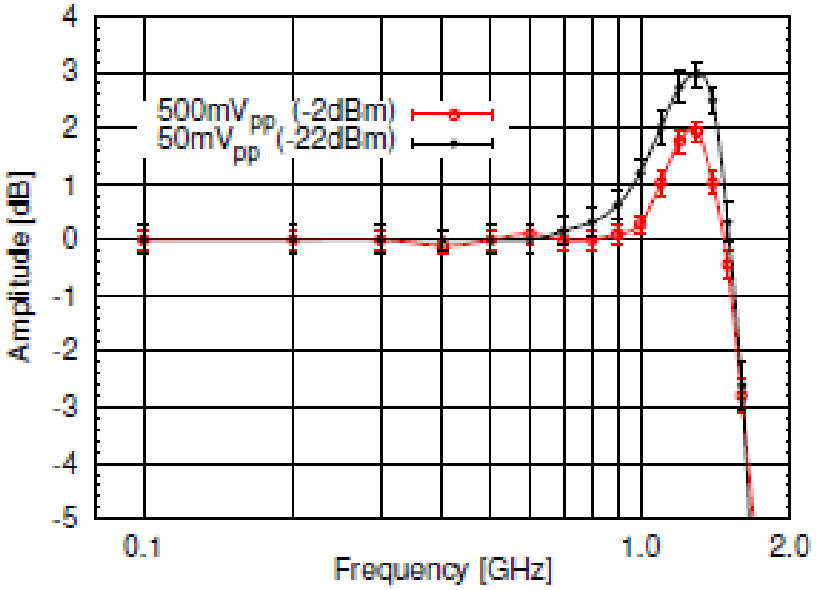


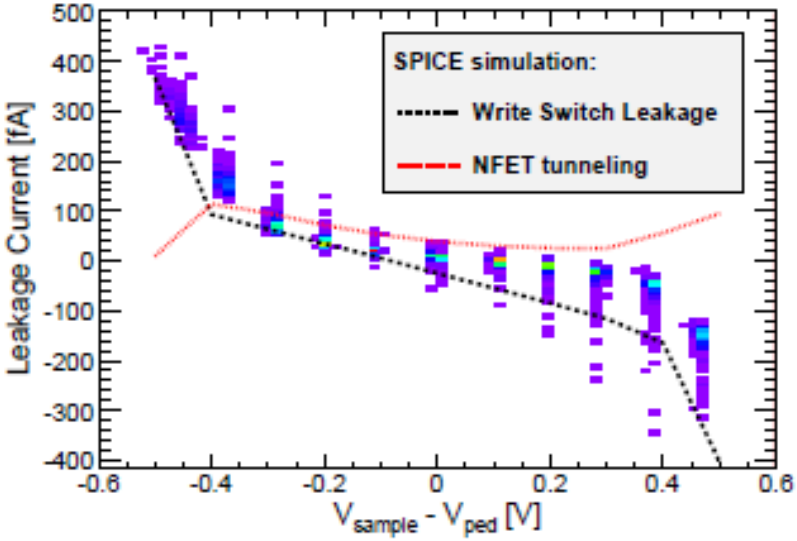
1) Design education

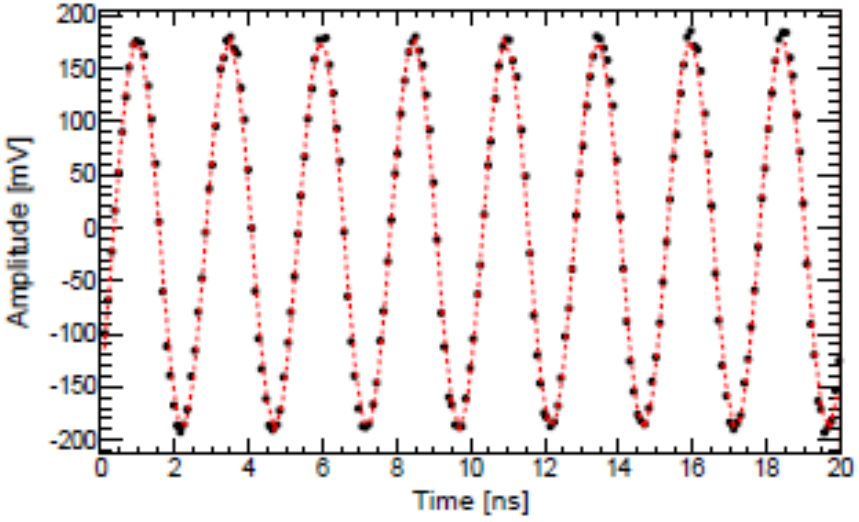
- **Simulation-driven** integrated circuit design
  - Confidence in layout extracted simulations and final chip design
  - Verification with several 0.13 µm chips:
    - **PSEC3, CHAMP, PSEC4…**
- 0.13 µm CMOS
  - Leakage not really a big issue
  - Maximize dynamic range over limited 1.2 V core voltage
  - Analog Bandwidth limited by input capacitance

2) Performance

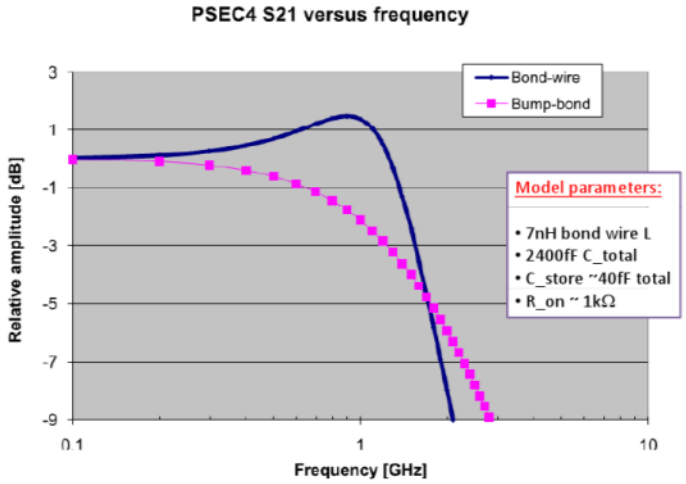


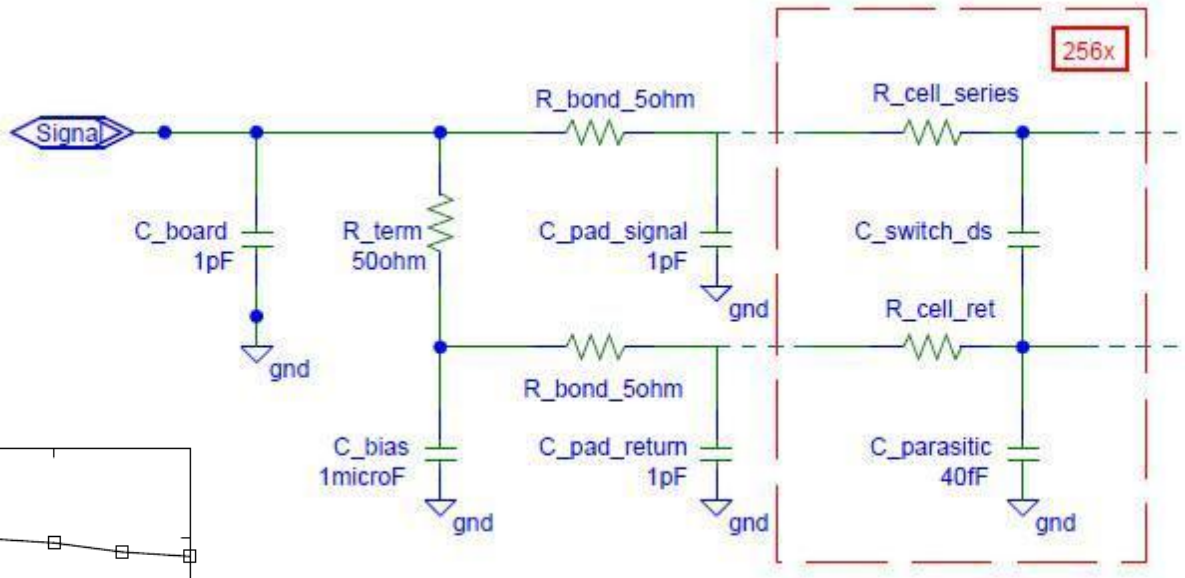


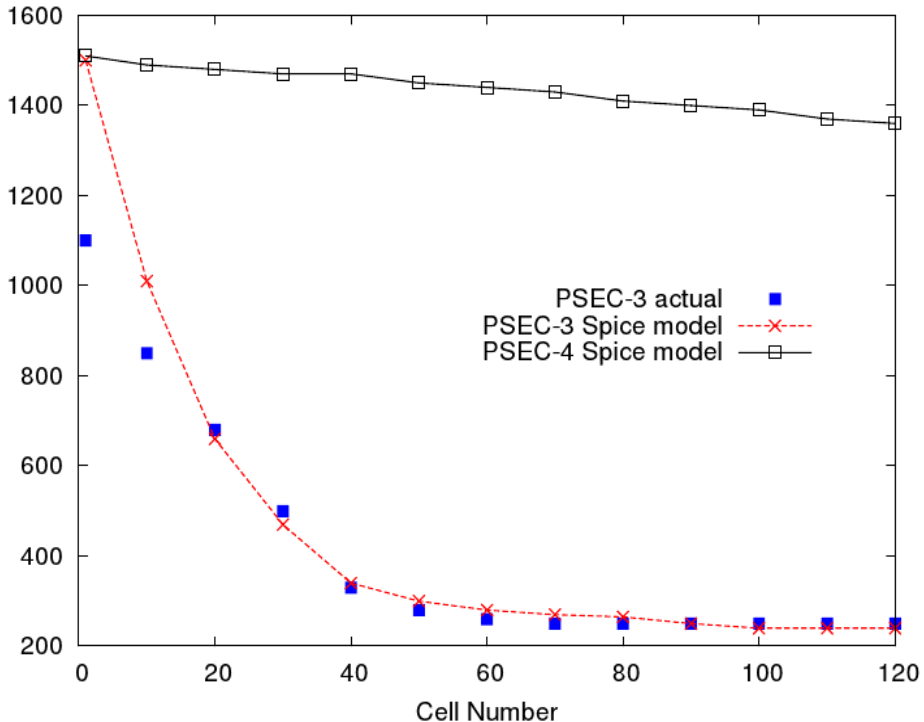




2) Performance: Analog BW Modeling







- Chip RC-only input line simulations match observed **PSEC-3/4** bandwidths

2) Performance: table of measured results

Table 1: PSEC4 architecture parameters and measured performance results.

Parameter	Value	Comment
Channels	6	die size constraint
Sampling Rate	4-15 GSa/s	servo-locked on-chip
Samples/channel	256	25 ns recording window at 10.24 GSa/s
Analog Bandwidth	1.6 GHz	~2.5 dB distortion at 1.3 GHz
Crosstalk	7%	max. over bandwidth
	<1%	typical for signals <800 MHz
Noise	700 μV	RMS (typical). RF-shielded enclosure.
Effective ADC Resolution	10.5 bits	12 bits logged
ADC time	4 μs	max. 12 bits logged at 1 GHz clock speed
	250 ns	min. 8-bits logged at 1 GHz
ADC clock speed	1.4 GHz	max.
Dynamic Range	1 V	after linearity correction
Readout time	$0.8n$ μs	n is number of 64-cell blocks to read ($n = 24$ for entire chip)
Sustained Trigger Rate	50 kHz	max. per chip. Limited by [ADC time + Readout time]$^{-1}$
Power Consumption	100 mW	max. average power
Core Voltage	1.2 V	0.13 μm CMOS standard

Submitted to NIM-A:

A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC

Eric Oberla[a,*], Hervé Grabas[a,1], Jean-Francois Genat[a,2], Henry Frisch[a], Kurtis Nishimura[b,3], Gary Varner[b]

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Crosstalk	7%	max. over bandwidth
	<1%	typical for signals <800 MHz
Noise	700 μV	RMS (typical). RF-shielded enclosure.
Effective ADC Resolution	10.5 bits	12 bits logged
ADC time	4 μs	max. 12 bits logged at 1 GHz clock speed
	250 ns	min. 8-bits logged at 1 GHz
ADC clock speed	1.4 GHz	max.
Dynamic Range	1 V	after linearity correction
Readout time	$0.8n$ μs	n is number of 64-cell blocks to read ($n = 24$ for entire chip)
Sustained Trigger Rate	50 kHz	max. per chip. Limited by [ADC time + Readout time]$^{-1}$
Power Consumption	100 mW	max. average power
Core Voltage	1.2 V	0.13 μm CMOS standard

Main limitation of PSEC4

Readout speed not optimized

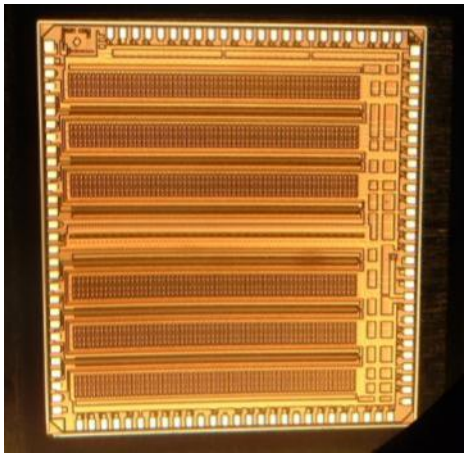
Submitted to NIM-A:

A 15 GSa/s, 1.5 GHz Bandwidth Waveform Digitizing ASIC

Eric Oberla[a,*], Hervé Grabas[a,1], Jean-Francois Genat[a,2], Henry Frisch[a], Kurtis Nishimura[b,3], Gary Varner[b]

2) Performance: calibrations

Oscilloscope on a chip? Not quite…a modified approximation:



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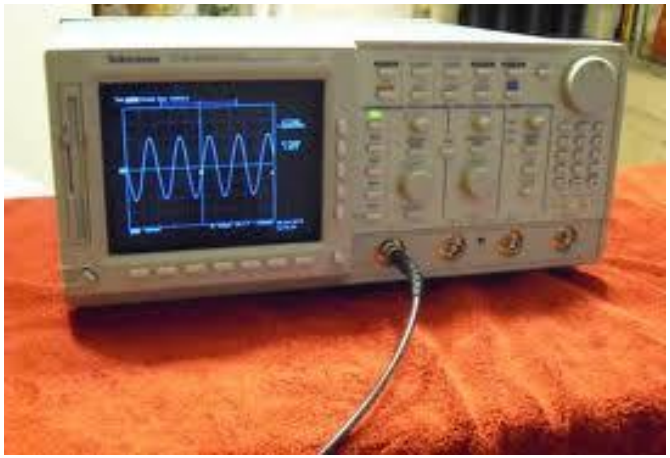
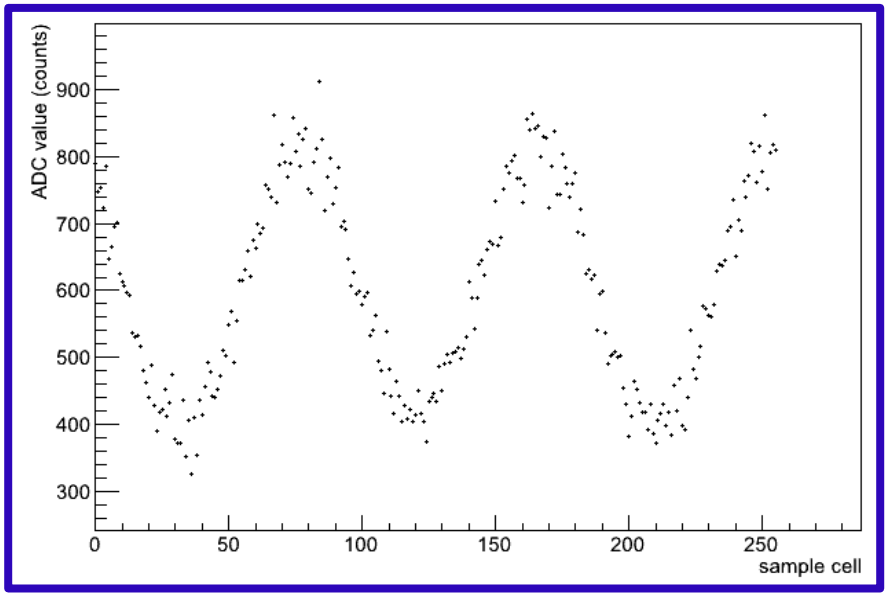


For example, a raw **PSEC-3** readout (10 GS/s) of 120 MHz, 150 mV_{rms} sine wave:



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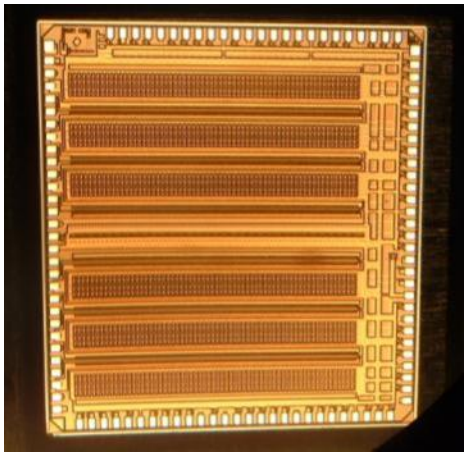

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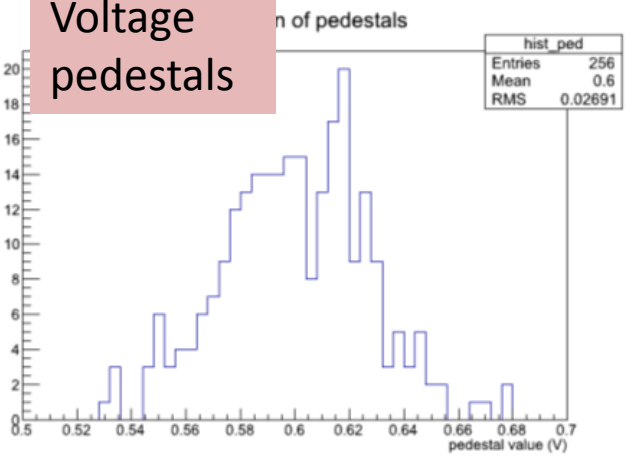
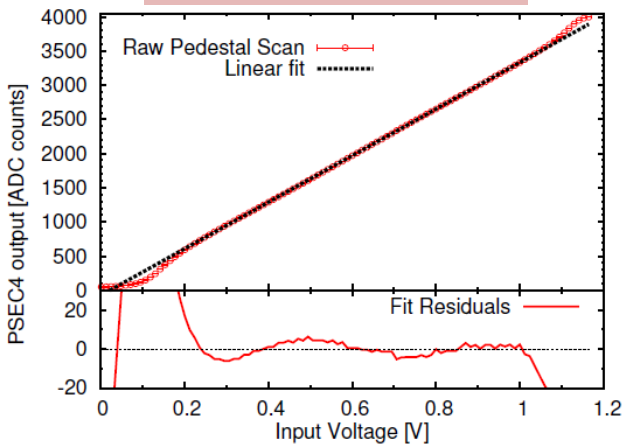
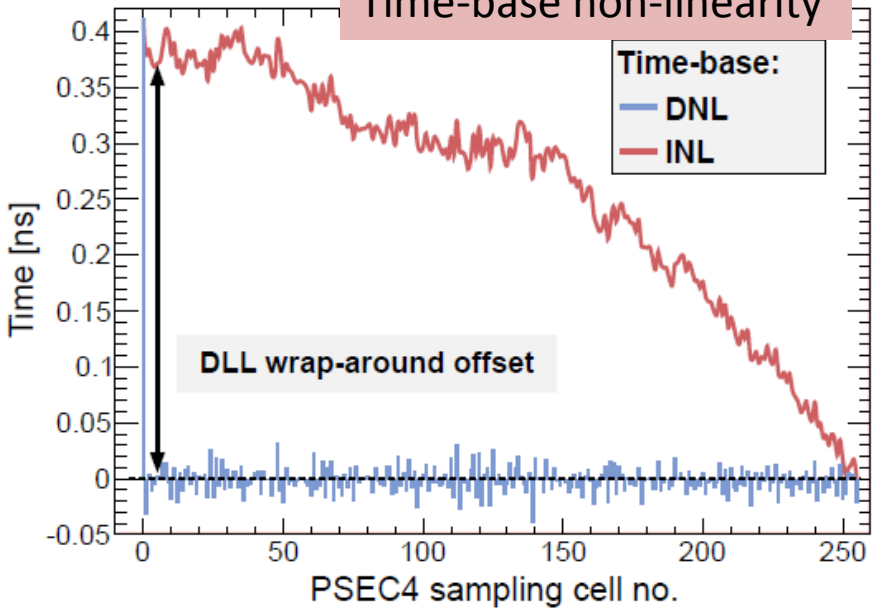
Voltage pedestals



ADC non-linearity



Time-base non-linearity



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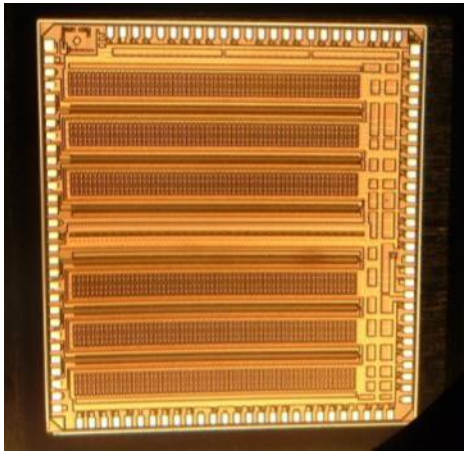

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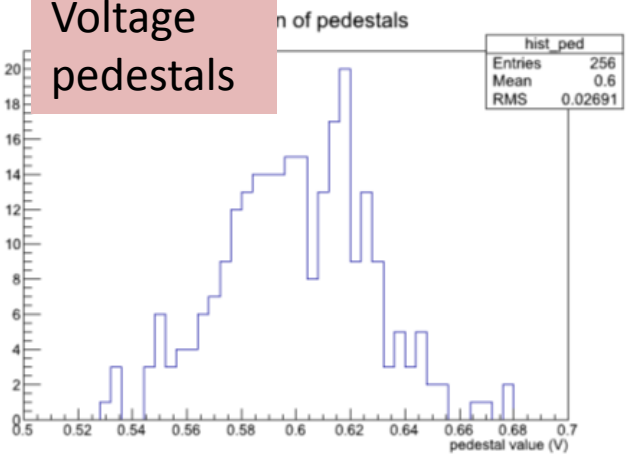
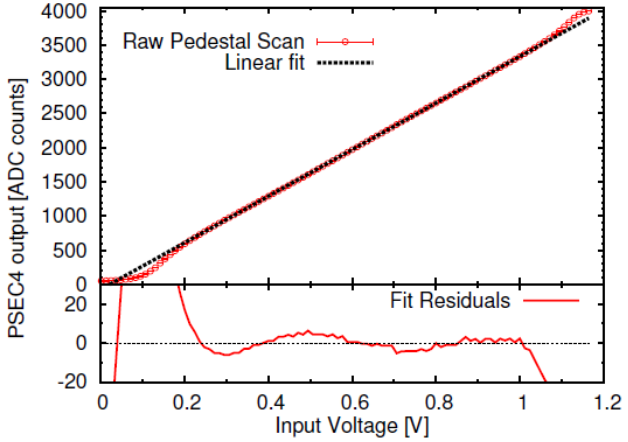
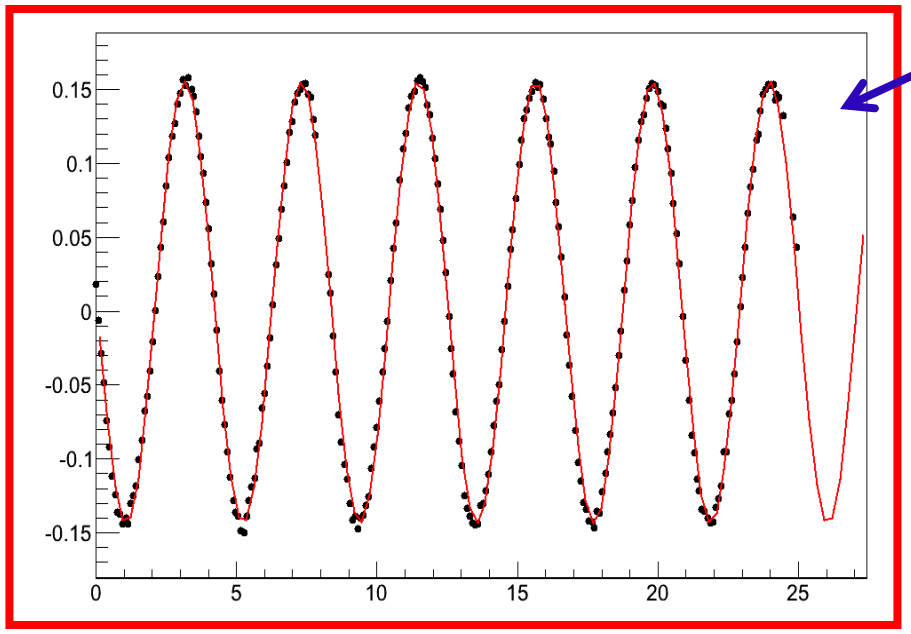


ADC non-linearity





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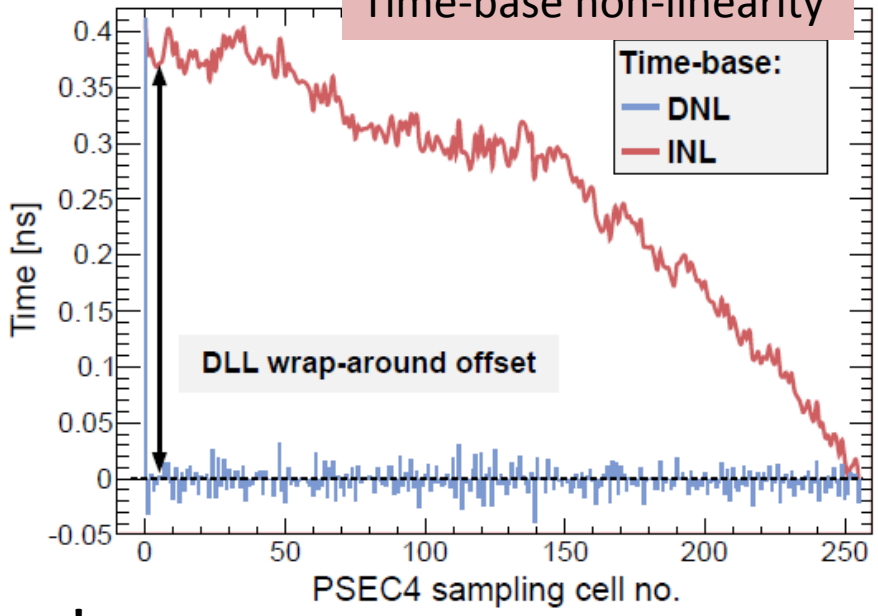


Want to minimize number of calibration steps!

What we learned: **3) 0.13 micron logistics**

2013 Fabrication Schedule

Technology		Customer Submission Date											
		Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
8HP	0.13 µm	28		25		28		29		30		25	
8RF [2]	0.13 µm		19			20			19			18	
8XP	0.13 µm							1				11	

IBM →

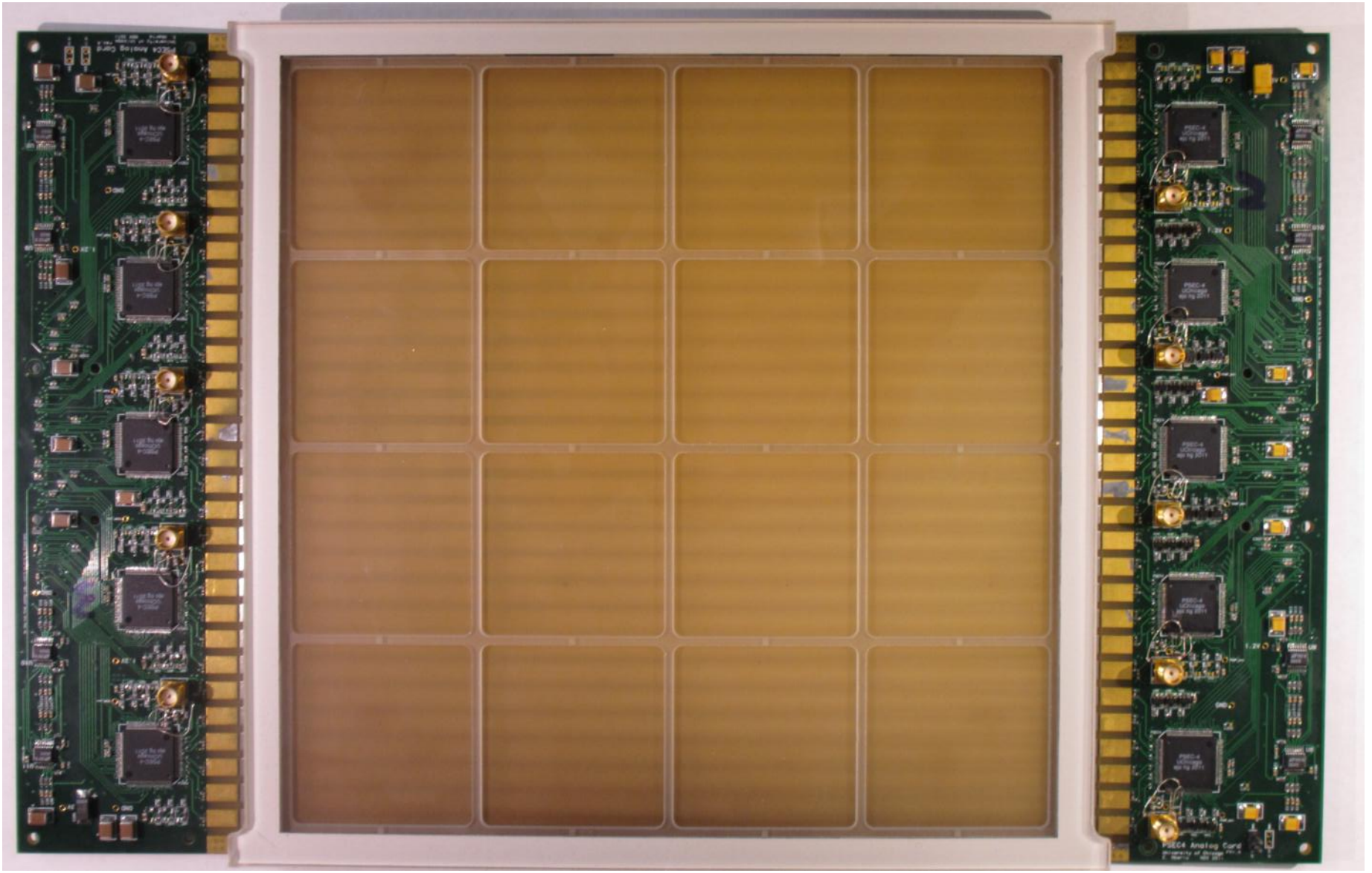
CL013/CM013	0.13 µm	7	11		8		10		5		7		9
CL013LP	0.13 µm	7	11		8		10		5		7		9
CL013LV	0.13 µm	7	11		8		10		5		7		9

TSMC

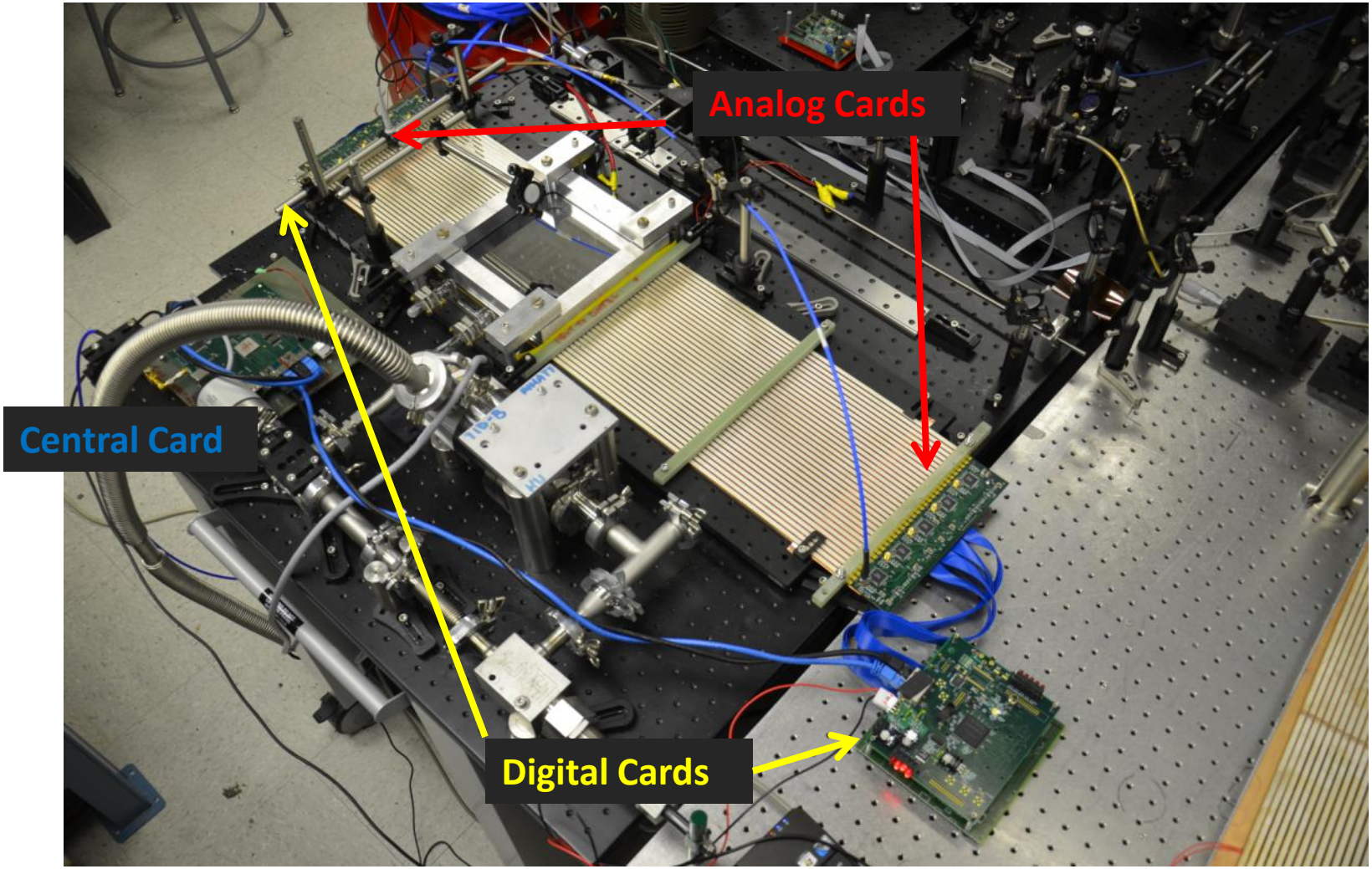
1. Frequency of fabrication runs
2. Cost

….defer these items to PSEC5 discussion

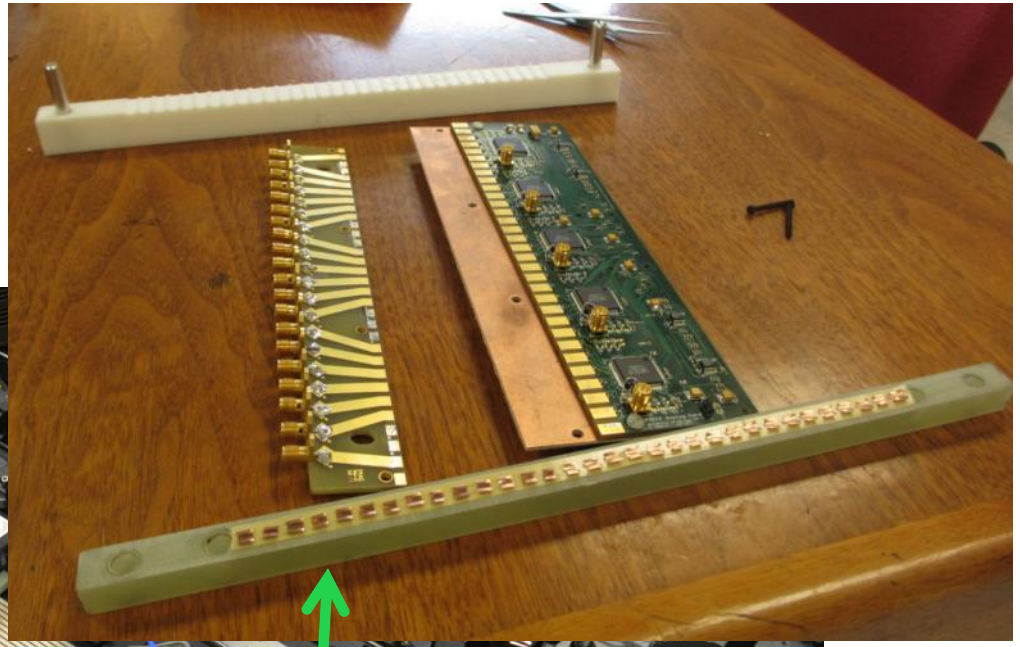
What we learned: **4) Detector Integration**

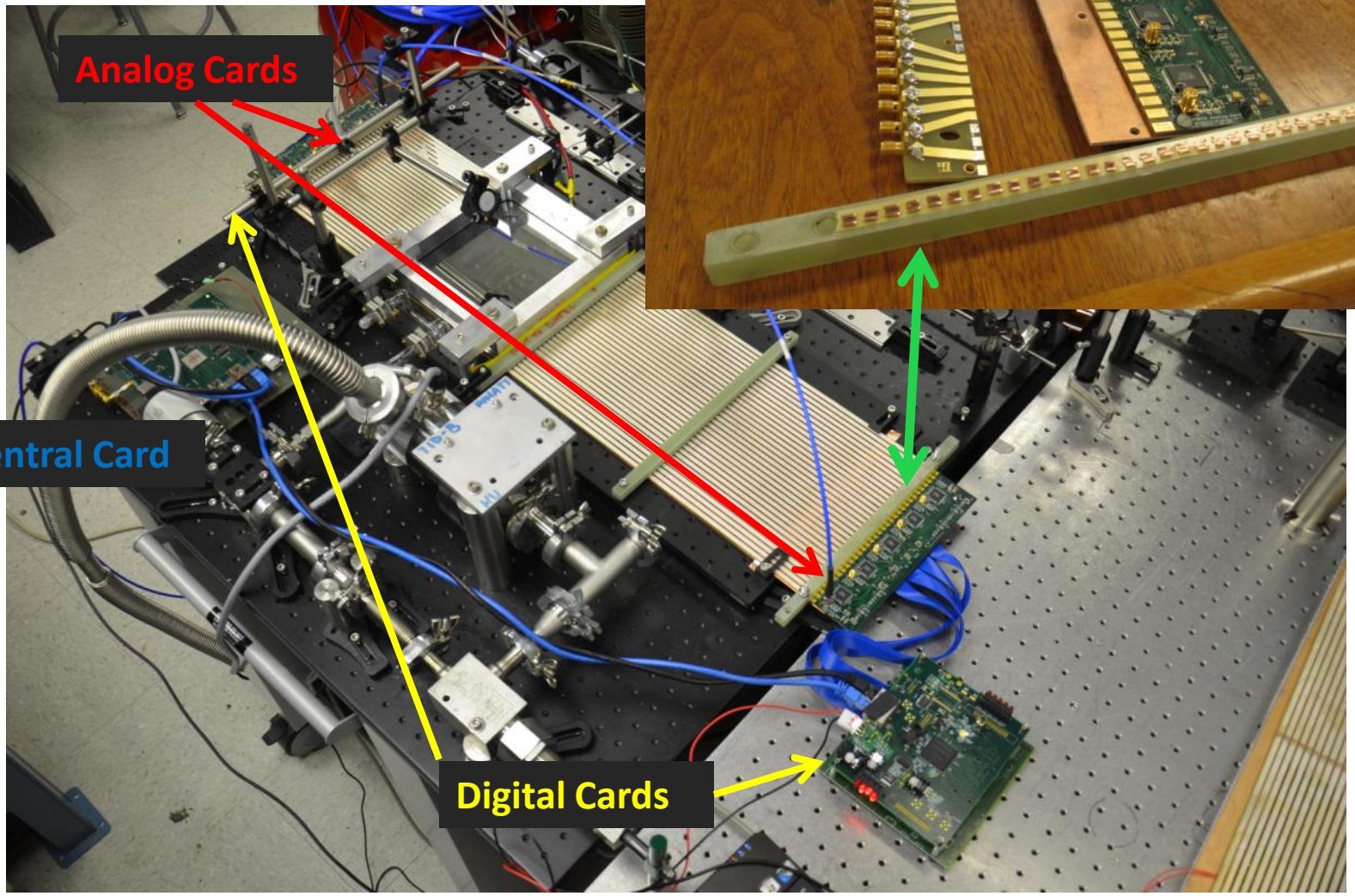


4) Integration: Demountable Setup Fitted w/ Full Electronics

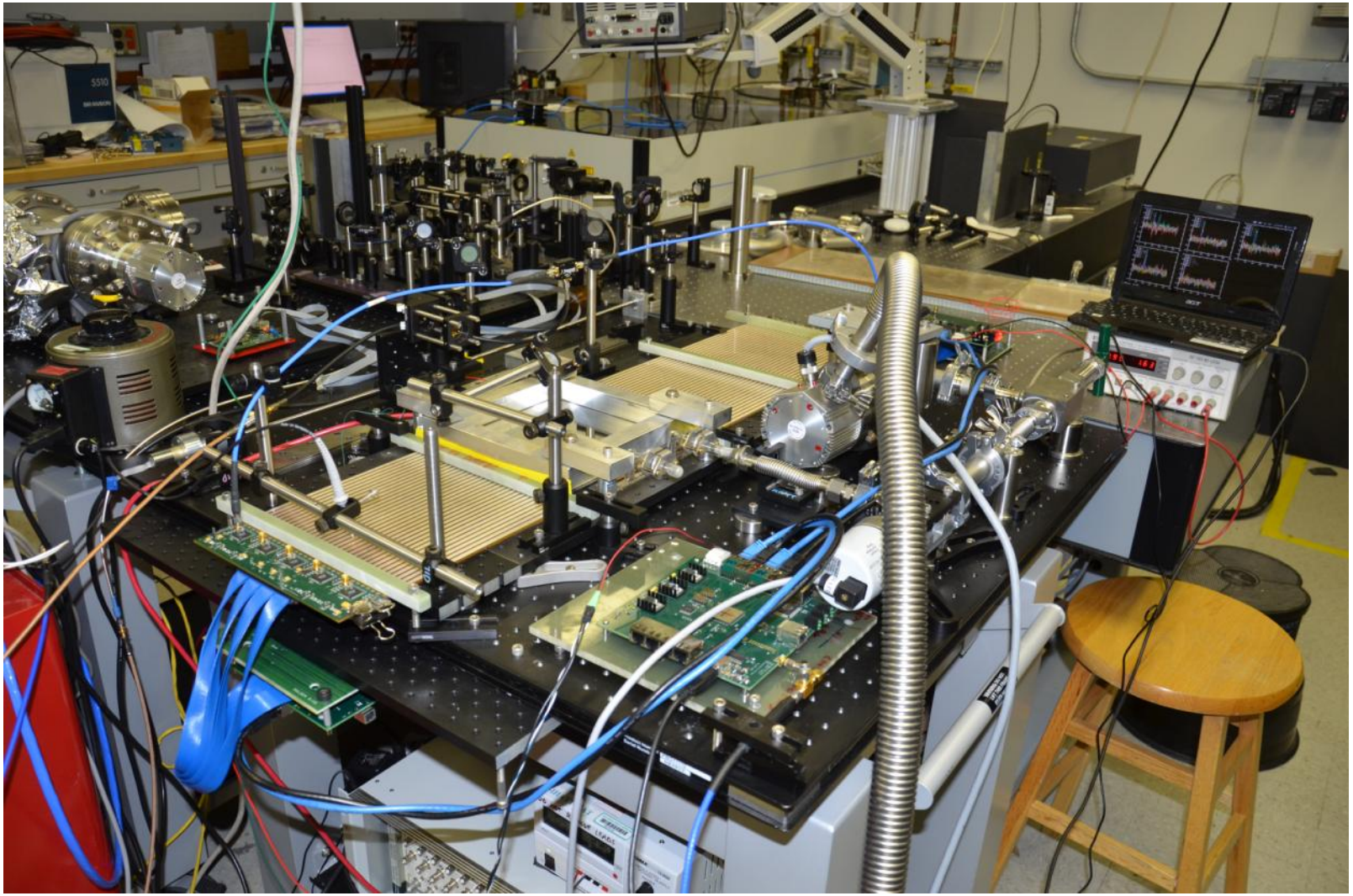


BeCu RF fingerstock used to make anode-anode/anode-electronics electrical connection



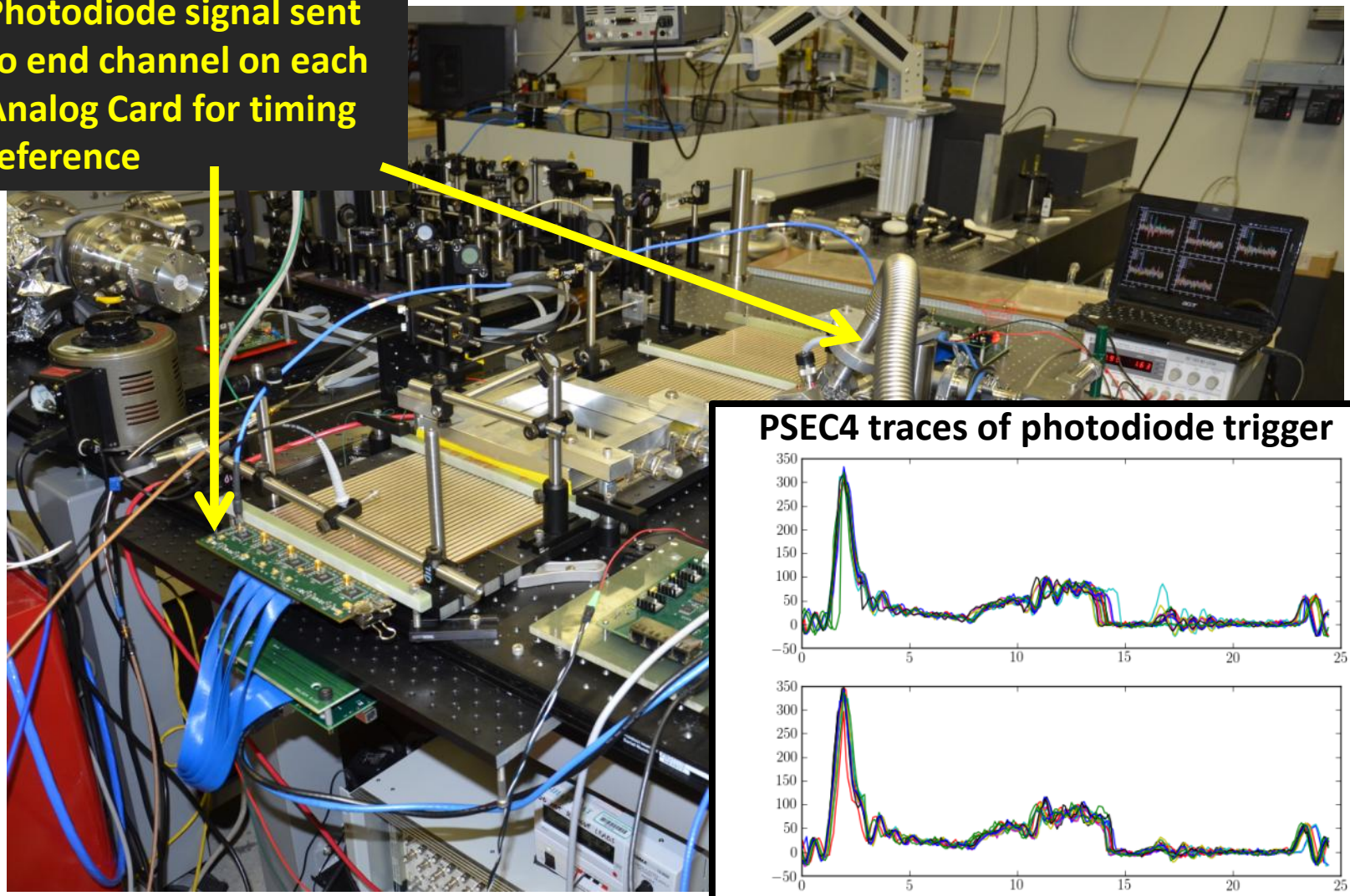


Super Module (SuMo) *Vertical Slice* System Testing



SuMo System Testing

Photodiode signal sent to end channel on each Analog Card for timing reference

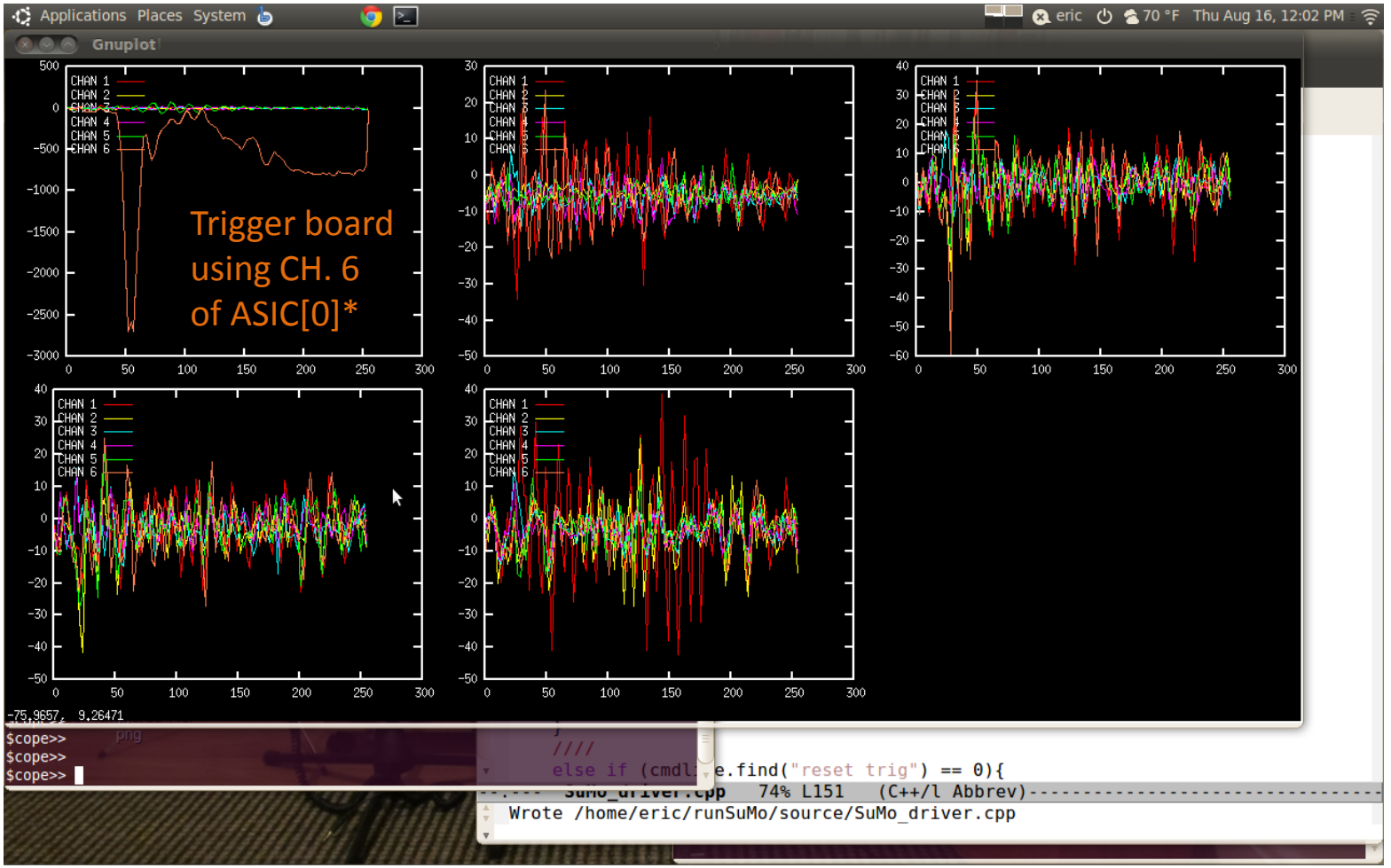


PSEC4 traces of photodiode trigger

Time [ns]

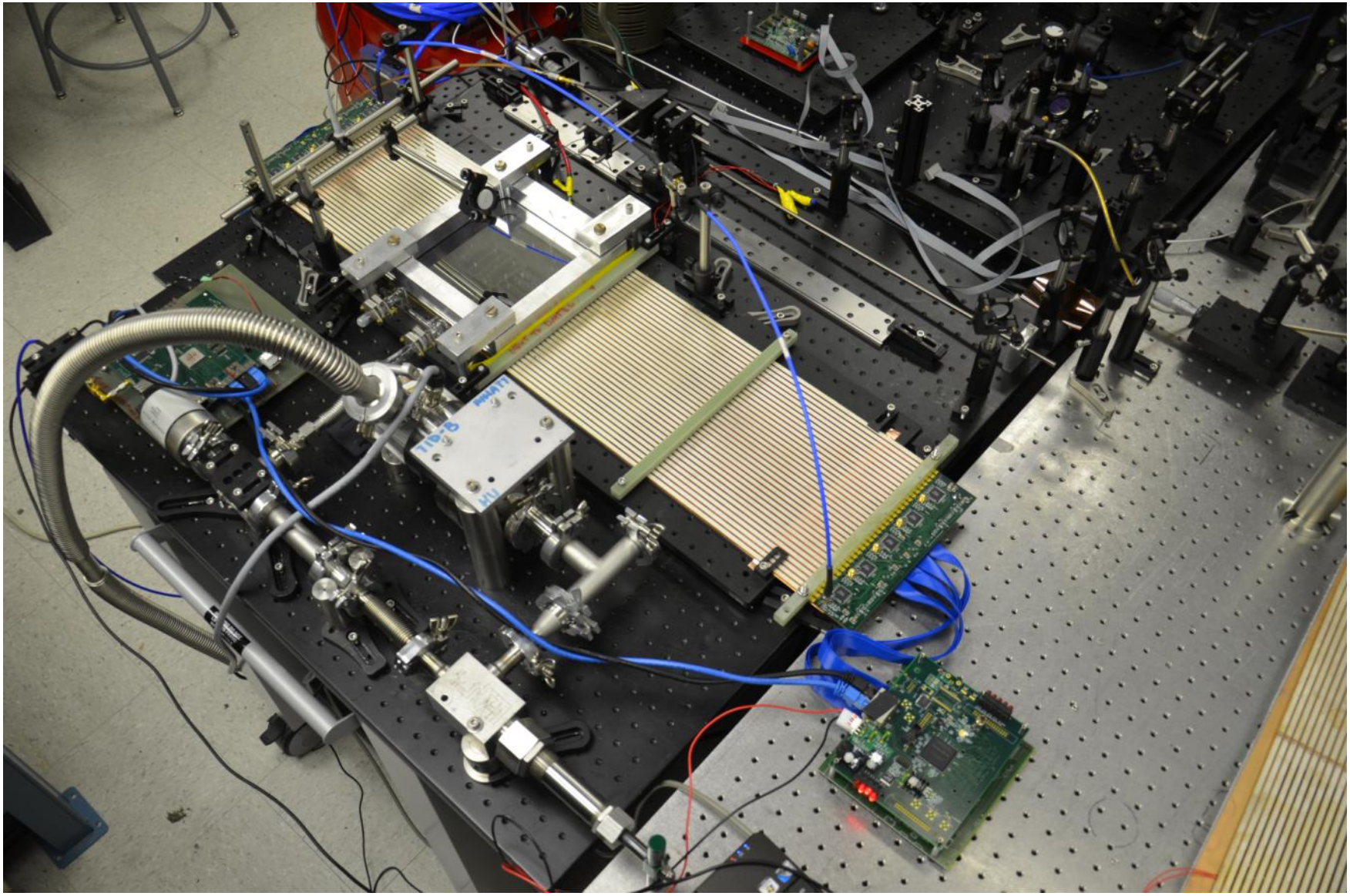
Analog Card can self-trigger

- Useful feature given PSEC-4's short buffer depth*
- **Successful testing at APS using trigger photodiode:**

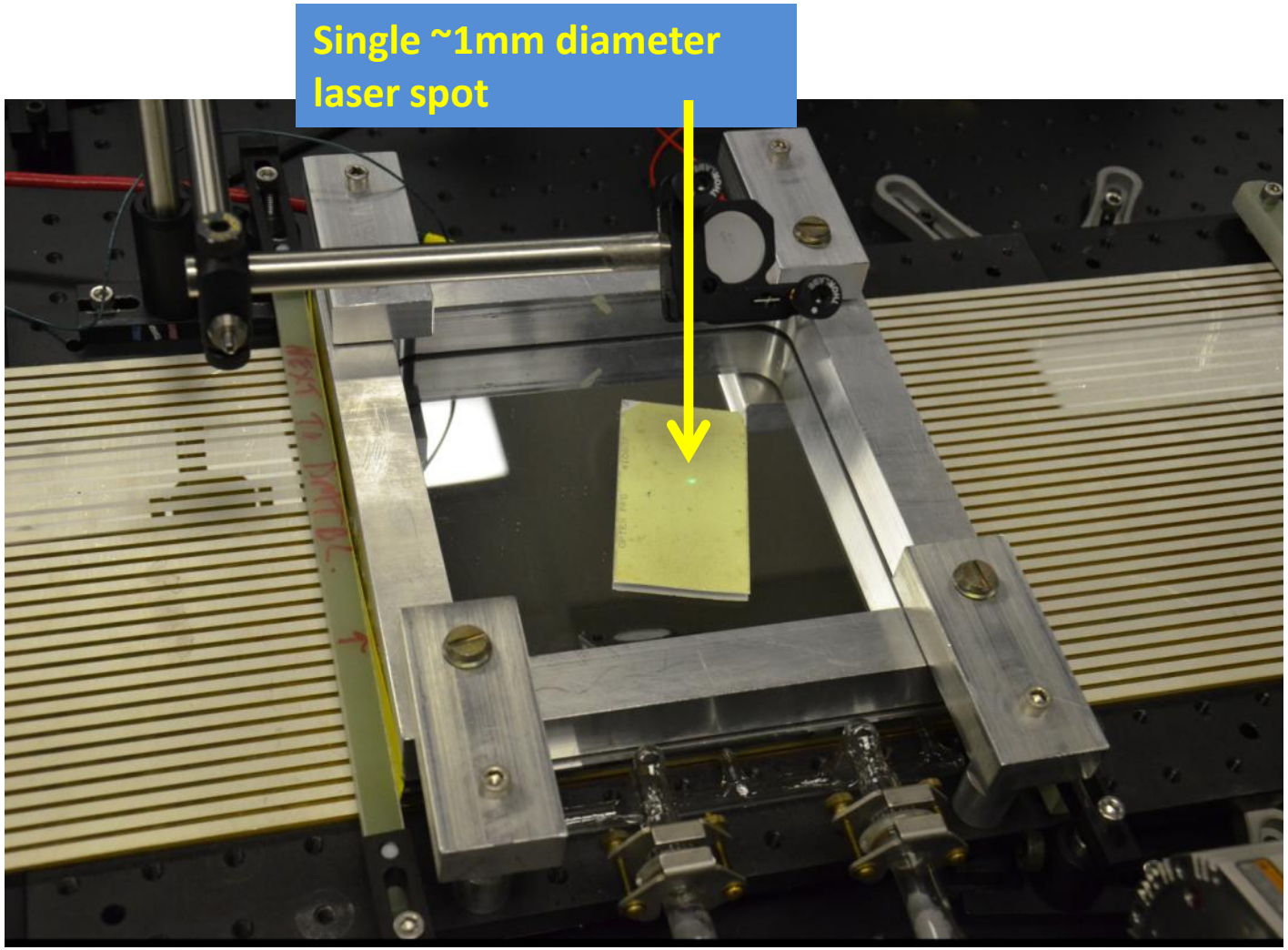


***However, for most tests we use TTL output from laser driver system for DAQ triggering** (much easier firmware…)

Dual-end PSEC4 pulse recording



Dual-end PSEC4 pulse recording:

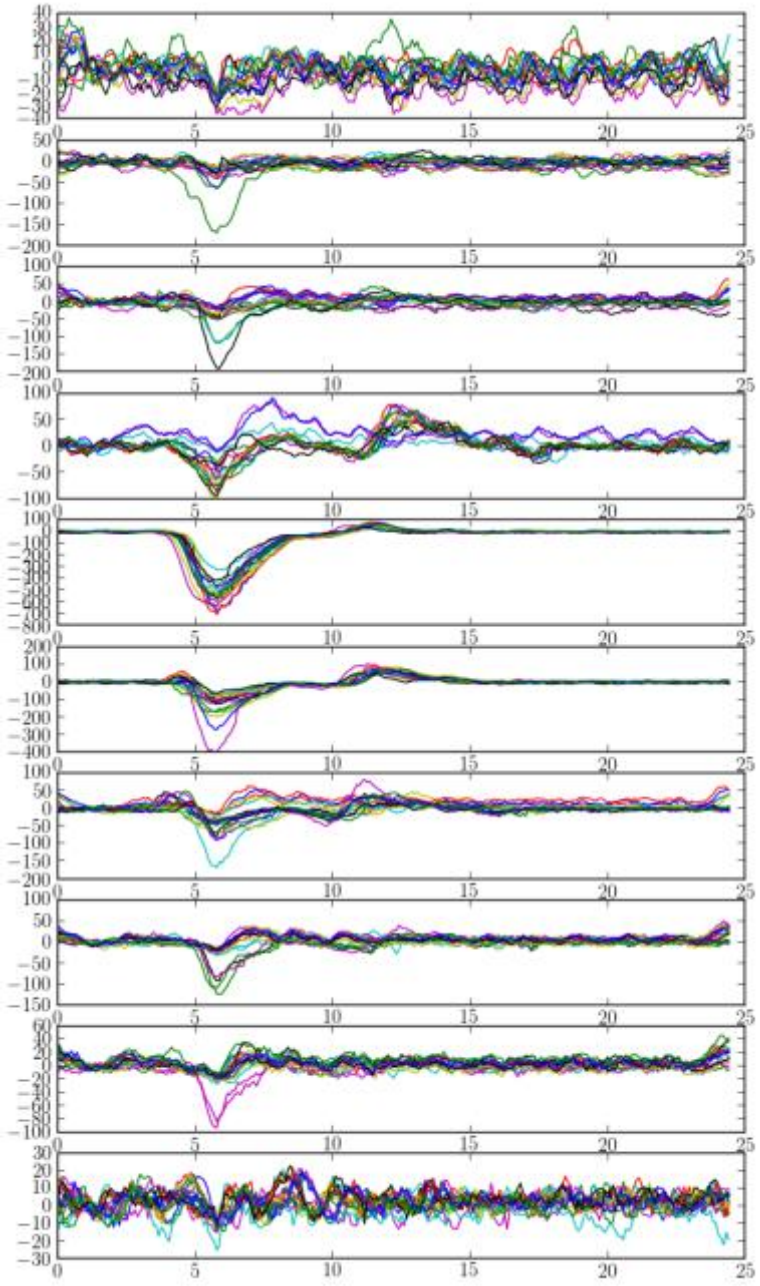


Dual-end PSEC4 pulse recording (10 strips):

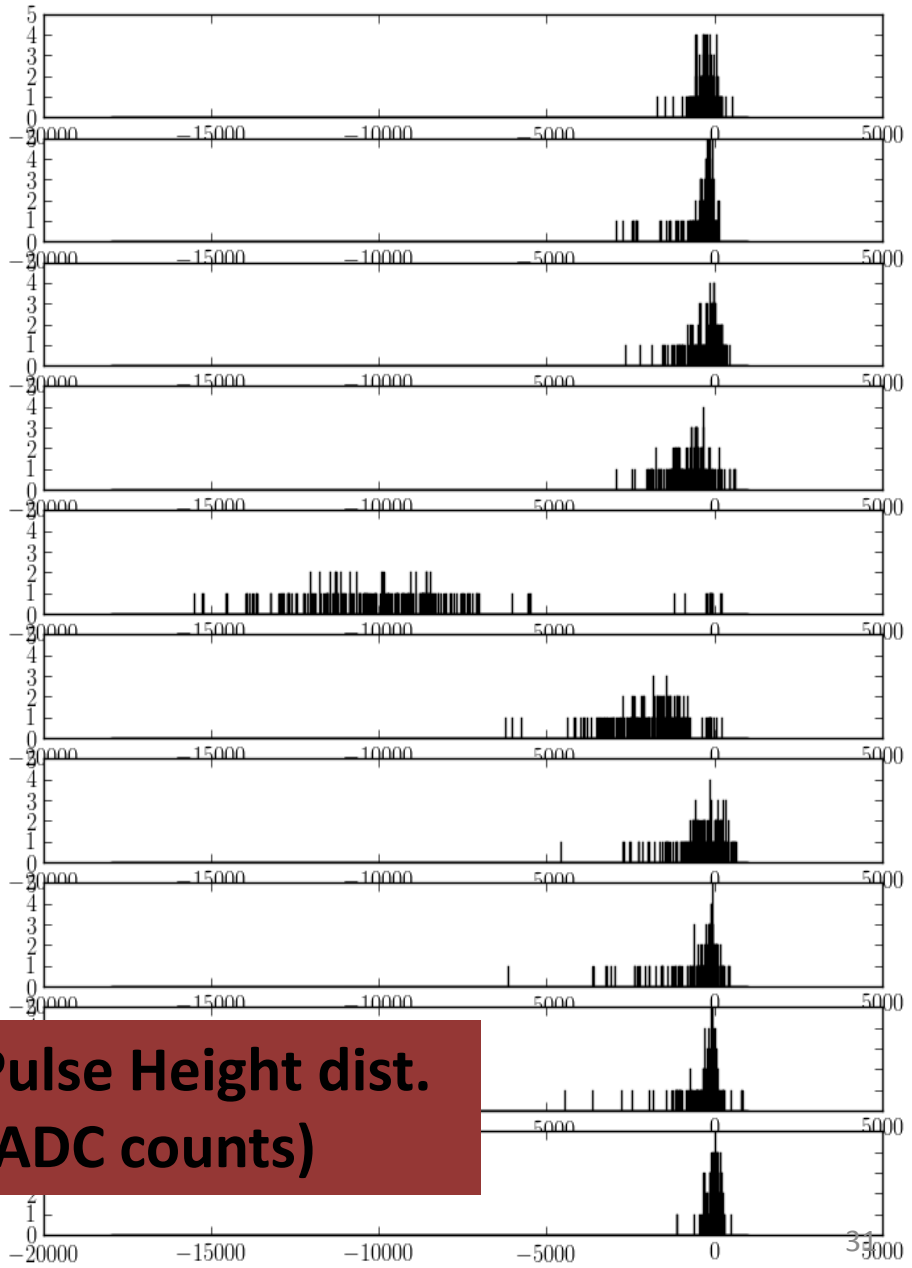
LEFT

RIGHT

Dual-end PSEC4 pulse recording (10 strips):

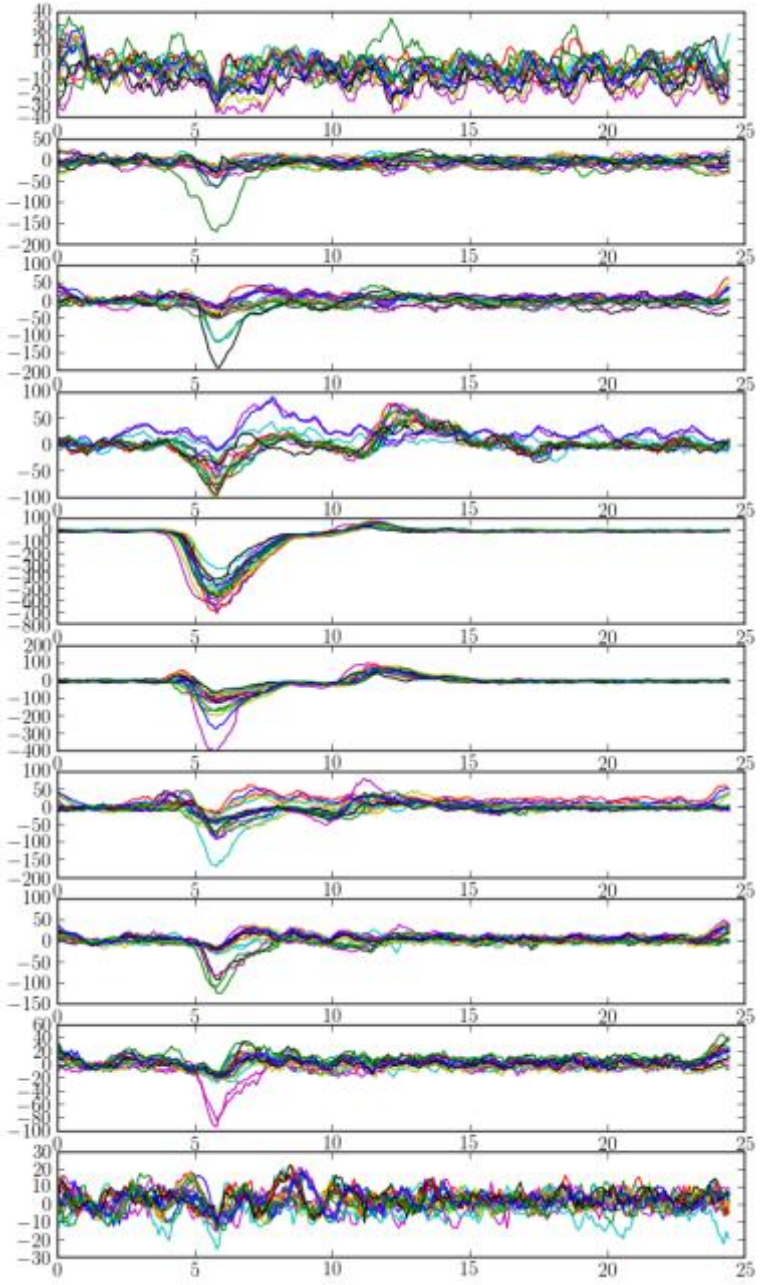


LEFT



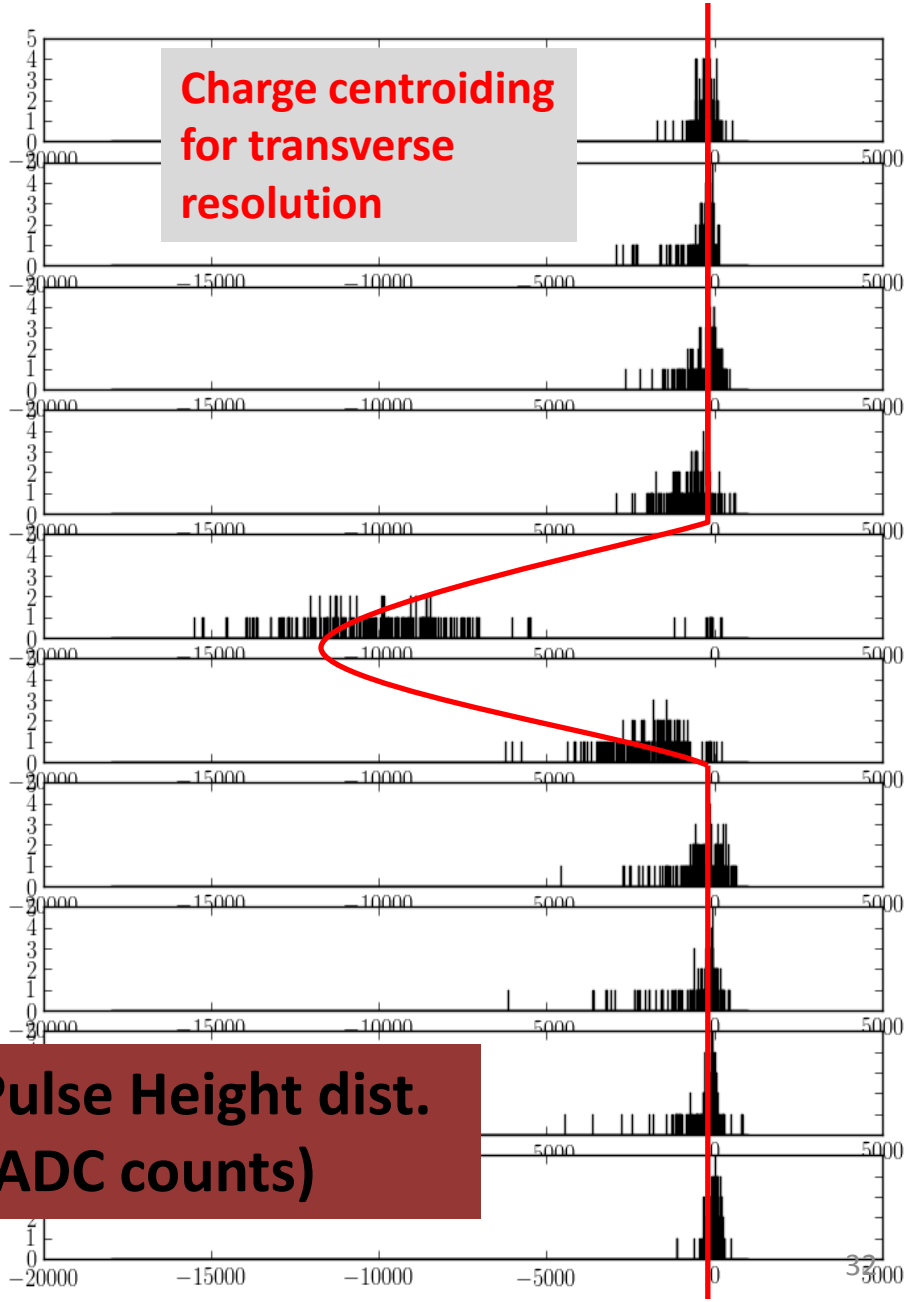
Pulse Height dist. (ADC counts)

Dual-end PSEC4 pulse recording (10 strips):



LEFT

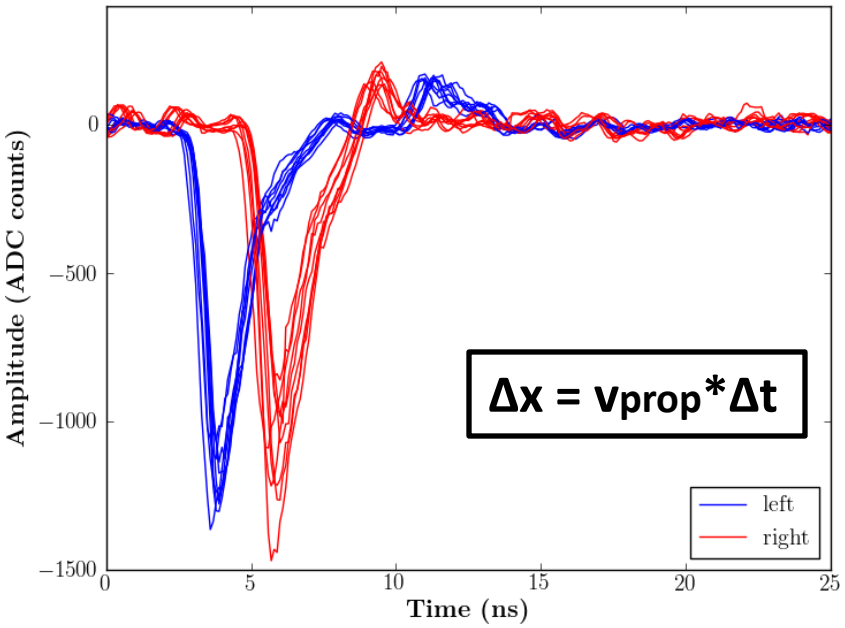
Charge centroiding for transverse resolution

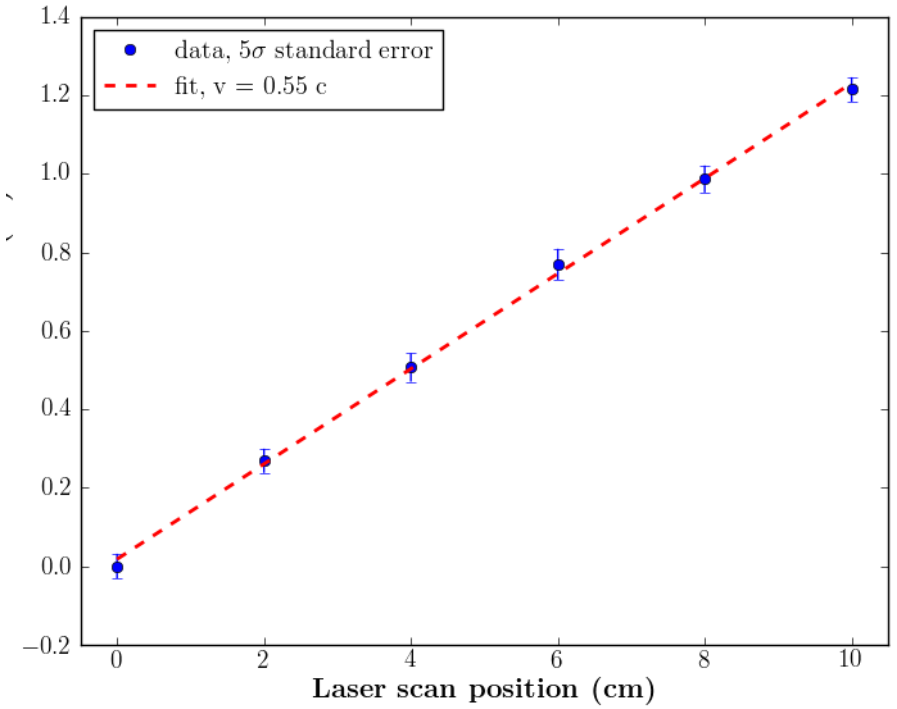


Pulse Height dist. (ADC counts)

Dual-end PSEC4 pulse recording

Time difference for parallel-strip resolution





- PSEC4 system (DAQ) timing resolution 50-100 ps 'out-of-the-box'
  - Timing over a ~100 channel PSEC4 readout system relies on good clock distribution, trigger syncing, and good noise rejection in hardware..all things that could be improved
- Single chip (2-channel) resolution ~2-10 ps, depending on signal processing algorithms

Conclusions

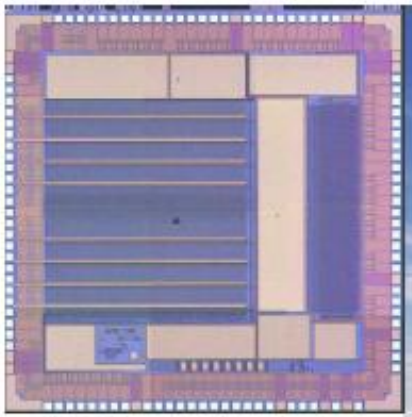
What we learned from PSEC4:

1. Design:
   - Full layout-extracted simulations required
2. Performance
   - Met all design specifications. Wish list: Better self-trigger, faster readout, **longer buffer**, better trigger timing/referencing on-chip…=PSEC5
3. Logistics
   - Slow turn-around time with IBM 0.13 CMOS
4. Integration
   - Have a working PSEC4 DAQ. See performance wish list

Backup

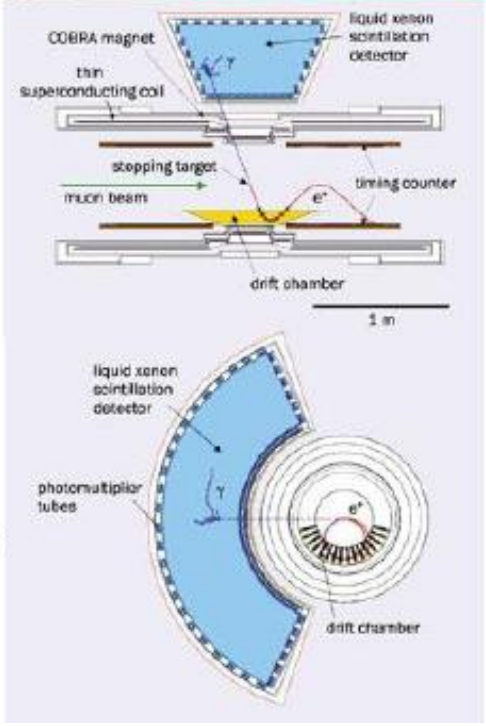
Waveform Sampling ASICs

- Already in use in many experiments…

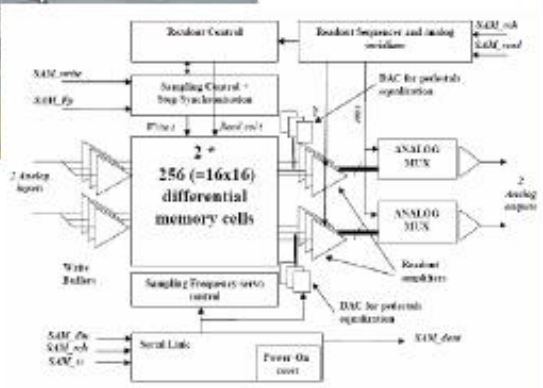


LABRADOR3,
ANITA Experiment

DRS4,
MEG Experiment



SAM,
H.E.S.S.-II



Waveform samplers ‘on the market’:

ASIC	Amplification?	# chan	Depth/chan	Sampling [GSa/s]	Vendor	Size [nm]	Ext ADC?
DRS4	no.	8	1024	1-5	IBM	250	yes.
SAM	no.	2	1024	1-3	AMS	350	yes.
IRS2	no.	8	32536	1-4	TSMC	250	no.
BLAB3A	yes.	8	32536	1-4	TSMC	250	no.
TARGET	no.	16	4192	1-2.5	TSMC	250	no.
TARGET2	yes.	16	16384	1-2.5	TSMC	250	no.
TARGET3	no.	16	16384	1-2.5	TSMC	250	no.
PSEC3	no.	4	256	1-16	IBM	130	no.
PSEC4	no.	6	256	1-16	IBM	130	no.