PSEC5

Eric Oberla

LAPPD2 Electronics Review

6-April-2013

Why PSEC5?

- **Most experimental applications require >25 ns of buffer depth**
- A more robust internal trigger
- Synchronize chip triggering with sampling
- Serialize slow controls, put DACs on-chip, etc.
  - Reduce peripheral cost
- Speed up readout (LVDS!)
- Build on proven technologies of PSEC4
- Aim to commercialize?

PSEC5 kick-off meeting

- Held on 27-Oct 2012 at UChicago.
- Discuss desired specifications and possible architectures of a PSEC5 chip.

- Andrey Elagin, University of Chicago
- Henry Frisch, University of Chicago
- Craig Harabedian, University of Chicago
- Mary Heintz, University of Chicago
- Kurtis Nishimura, University of Hawaii
- Eric Oberla, University of Chicago
- Larry Sadwick, InnoSys Inc.
- Gary Varner, University of Hawaii
- Alexander Vostrikov, University of Chicago
- Bob Wagner, Argonne National Lab
- Bill Worstell, Photo Diagnostic Systems

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An 8-page review compiled by Kurtis is posted on the LAPPD trac website

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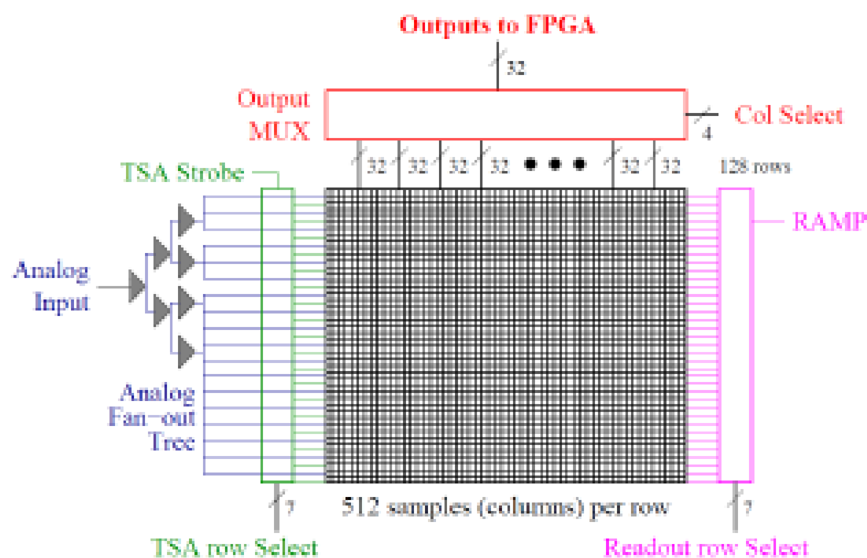
How to increase sample/buffer depth?

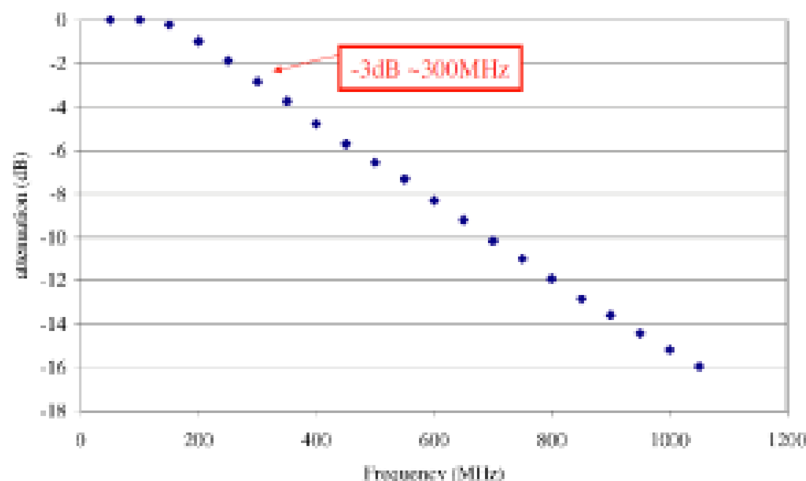
- Several options considered, based on deeper samplers designed at UHawai'i and elsewhere…

1

Fan-out to Multiple Arrays

- Examples (TARGET, BLAB, BLAB2):





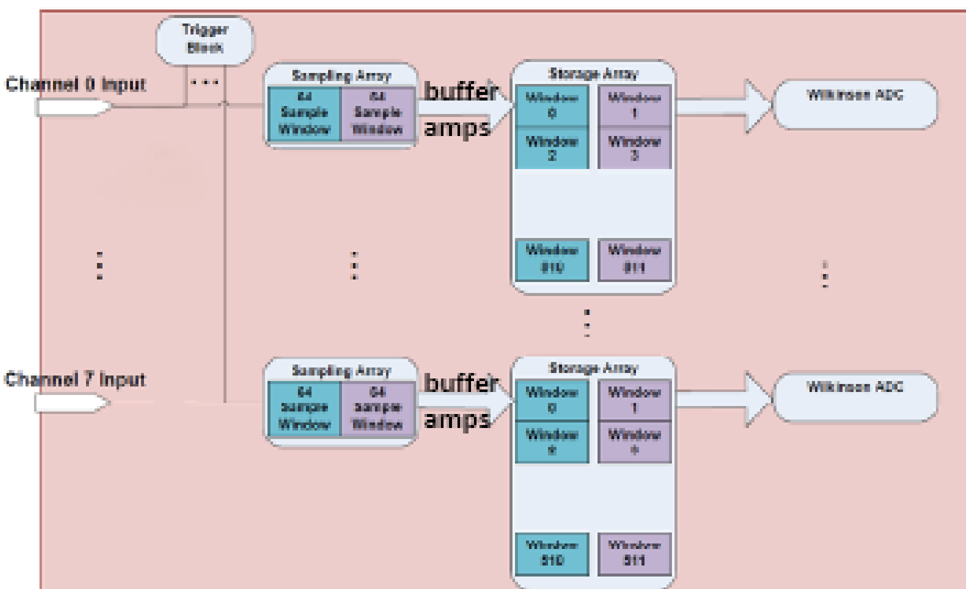
- Analog buffer tree fans input to all “rows”.
- Sampling strobe is independent for each row.
  - Addressing schemes can vary.

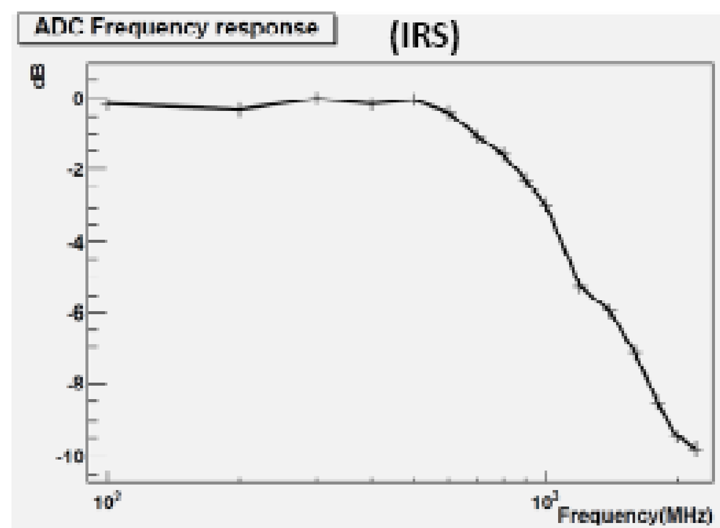
- Advantages:
  - Supports large analog storage buffers.
  - Relatively straightforward interface (e.g., control firmware).
- Disadvantages:
  - Amplifier tree limits bandwidth.
  - Each “row” has different timing calibration constants.
  - Large number of pedestal constants.

2

Multi-Stage Transfer

- Examples (IRS, IRS2/3B, TARGET4/5/6):



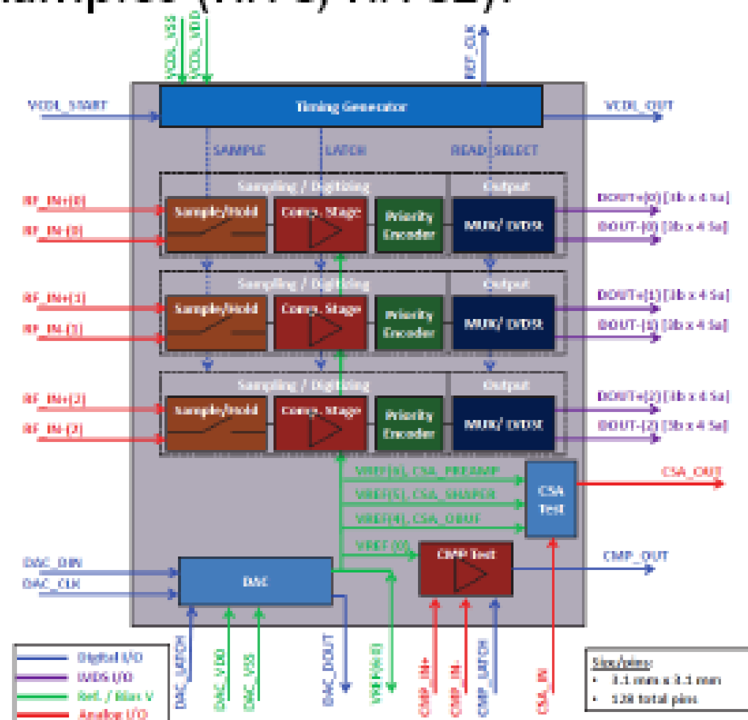


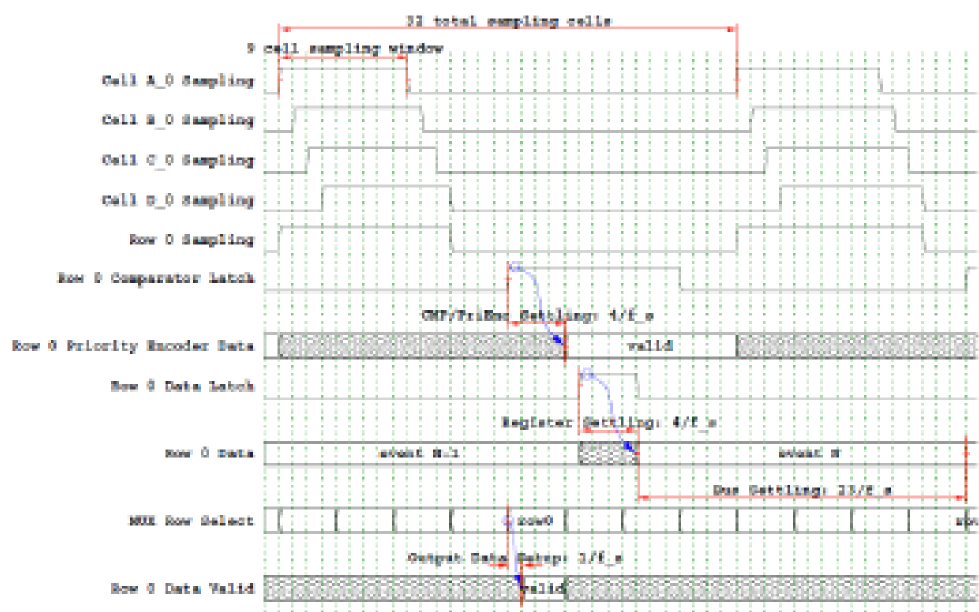
- Input signal is coupled to a small sampling array.
  - Logically divided into sub-arrays.
- Each sub-array connects to a set of analog storage cells via buffer amplifiers.
- "Ping-pong" sampling: while one sub-array is sampling, select and activate appropriate buffer amplifier to "transfer" the voltage from sampling sub-array to storage.

- Advantages:
  - Supports large analog storage buffers.
  - Improved bandwidth relative to buffer tree.
  - Timing calibration comes from sampling array only ➔ relatively few constants.
- Disadvantages:
  - More complicated control structure required (built into ASIC or firmware).
  - Mis-timed control ➔ data corruption.
  - Many buffer amps ➔ increased power.
  - Large number of pedestal constants.

Digitize-at-Speed

- 3 Examples (RITC, RITC2):





- Input signal is coupled to a small sampling array.
- Sampling array is divided into rows.
- As a row finishes sampling, begin digitizing.
- As a row finishes digitizing, begin readout.

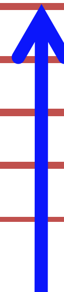
- Advantages:
  - Few sampling cells → few calibration constants.
  - Potentially high bandwidth, since input capacitance can be quite small.
  - Buffer depth is limited only by FPGA or external storage.
- Disadvantages:
  - Requires fast digitizer (e.g., flash), potentially high power.
  - Throughput must be proportional to number of bits and sampling rate to keep up.

PSEC5 target specs

PSEC-5 Baseline Specifications

The baseline PSEC-5 specifications are given in the following table.

Specification	Baseline Value
Fabrication process & feature size	IBM 130 nm
Channels per ASIC	4
Nominal sampling rate	10 GSa/s
Timebase stabilization method	On-chip DLL
Analog bandwidth	> 1.0 GHz
Length of sampling array	128 or 256 samples
Trigger latency accommodated[1]	8 µs
Absolute minimum buffer depth	100 ns [1000 samples @ 10 GSa/s]
Buffering style	Multi-stage transfer to analog storage; ≥ 1 stage digital buffering
Digitization style	Wilkinson ADC
Number of bits	12
Readout interface	Serial LVDS
Channel-level trigger capability	1 bit / channel



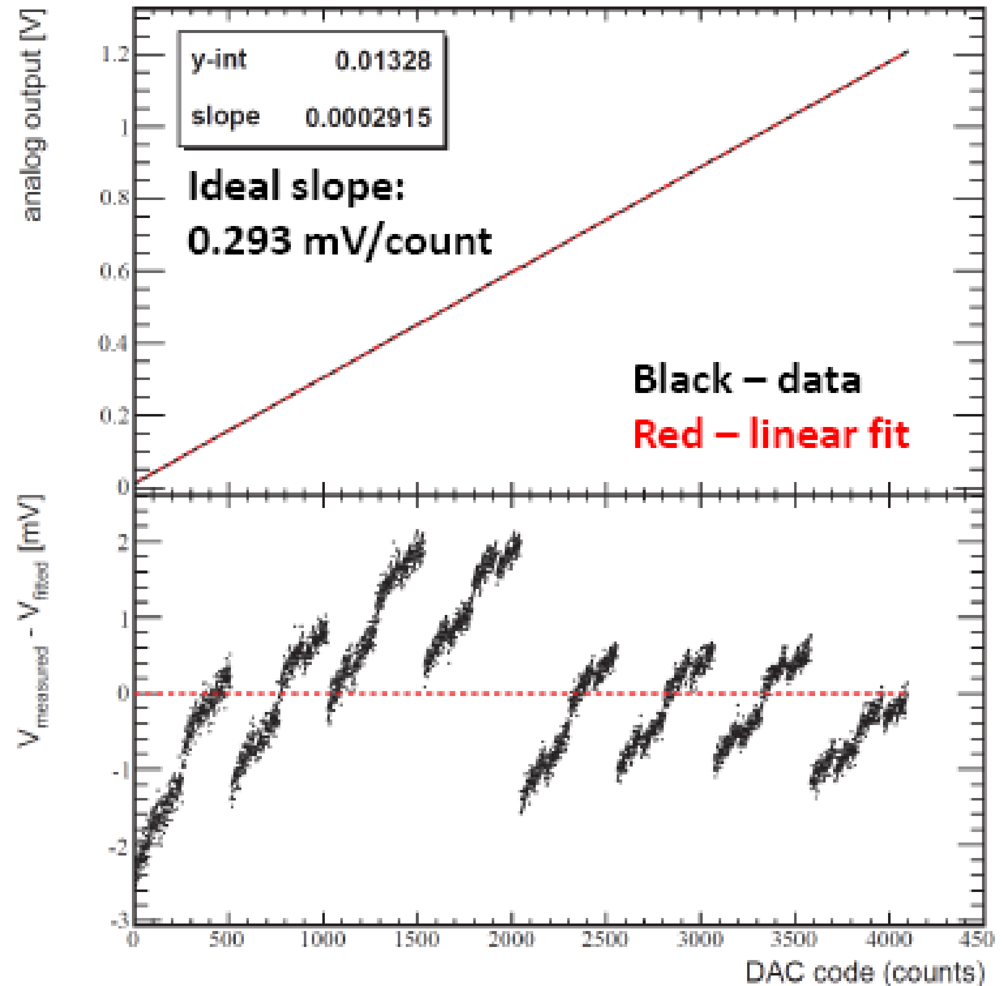
Decided on the multi-stage transfer architecture to maximize analog bandwidth

Collaborative efforts: leverage successful, existing 0.13 designs:

DAC Performance

- Serial interface verified:
  - – Runs at 600 kHz: ~0.7 ms to program 32x 12-bit DACs.
    - Probably can run significantly faster but not yet tested.
  - ✓ Expected interval between adjustments in flight is ~1 s.
- DAC features:
  - ✓ No gaps in coverage.
  - – Nonuniform steps due to intentional R-2R mismatch and process variations.
  - – Typical maximum nonlinearity of ~2-4 mV.
  - ✓ Adequate to reach full voltage range for comparators and sampling rate.

Typical DAC response & nonlinearity



What we learned: **0.13 micron logistics**

2013 Fabrication Schedule

IBM →

Technology		Customer Submission Date											
		Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
8HP	0.13 µm	28		25		28		29		30		25	
8RF [2]	0.13 µm		19			20			19			18	
8XP	0.13 µm							1				11	

TSMC

CL013/CM013	0.13 µm	7	11		8		10		5		7		9
CL013LP	0.13 µm	7	11		8		10		5		7		9
CL013LV	0.13 µm	7	11		8		10		5		7		9

1. Frequency of fabrication runs
2. Cost

MOSIS 130 micron pricing via Gary

Got very prompt/detailed response from MOSIS today. Sam Reynolds breaks down the numbers in detail below.

In summary, for 1k channels, the number isn't much different from the numbers provided by Eric that Bob used (previous and below). So ~ $50/channel

And the 100k channel number is basically the number accomodated on the dedicated mask set + processing (~ 500k$), or about $10/channel.

The 10k channel number is somewhere in between (10's of $/channel).

In the course of communication Wes Hansford (MOSIS CEO) promised to review the numbers that Eric had for the IBM process, to ensure the correct mask amorti

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For TSMC CM013, TSMC offers an 8 inch wafer line defaulting to 40 parts per wafer and a 12 in wafer line defaulting to 100 parts.
Given your quantity requirements, we would want to make sure to get on the 12 inch line.

The cost for up to a 25 sq mm area is $47,500. Lets assume we could get two copies of your layout on the mask using 33 sqmm of area. That would generate 200 parts per wafer. The cost for the first 200 parts would be 33/25*47500= $62,700 plus 1,000 for extra dicing charges = $63,700.

Additional parts can be obtained by ordering additional wafers at a cost of $4,820 each plus 1,000 for extra dicing charges = 5,820 for each additional lot of 200 parts.

You can use these numbers to generate a budgetary quote for any quantity which is a multiple of 200.

TSMC questions MWP orders of more than 2000 parts as they wish to direct larger quantites to dedicated mask sets and dedicated wafer lots of 6 wafers minimum costing ~ 480K for masks and 35K for wafers. As a rough estimate you should expect > 2500 16 sq mm parts per 12 inch dedicated wafer. TSMC inventories MPW masks for up to 6 months past wafer delivery which can be used to order more wafers. TSMC inventories dedicated mask set for up to 2 years past their last use and longer for a storage fee.

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65nm shift?

Access to 65nm technology

Inbox x

Kostas Kloukinas

Mar 28 (7 days ago)

to Abderrezak, Angel, Kock, Alex, Angelo, antonio, bweber, Claude, idzik, dabrowsk, Datao, Edo

Dear Colleagues,

Recently we had numerous requests from the chip design community in HEP from groups interested in starting soon activities in the new 65nm technology and therefore we would like to inform you on the status of the project.

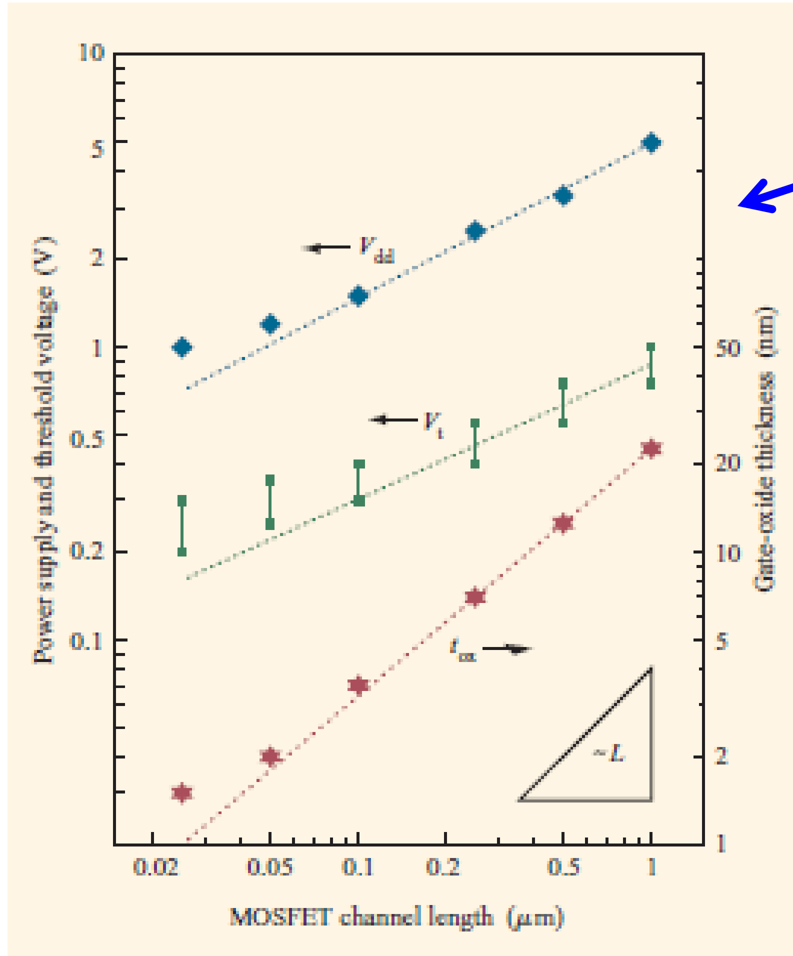
The CERN Finance Committee has approved in the session of March 20 the proposal for negotiating a detailed contract with IMEC for accessing a 65nm from TSMC, with a model essentially very similar to the one we had for accessing the old 130nm technology.

At this point there are essentially three issues pending and we would like to provide you with some more details about them:

- Status of the detailed commercial contract with IMEC.
- Status of the legal negotiations with TSMC to allow a collaborative effort among HEP Institutes all using their technology.
- Status of the design kit and tools necessary to support the utilization of this technology.

65nm CMOS shift?

Not totally crazy:



- Keep most of dynamic range relative to 0.13 CMOS (Vdd-Vt)
- Definitely more leakage
- But may be able to may a long-term storage sampler with digital storage? (so leakage would not be a problem, probably)
- **Will this effect 0.13 pricing?**

Conclusion

- Basic PSEC5 requirements specified and general architecture decided
- Assuming switch to TSMC 0.13 process
- Details of implementation will require in depth simulation studies. To begin shortly…

https://lappd-trac.uchicago.edu/wiki/Electronics/Agendas/PSEC-5_kickoff_meeting

Taur's

Leakage current density

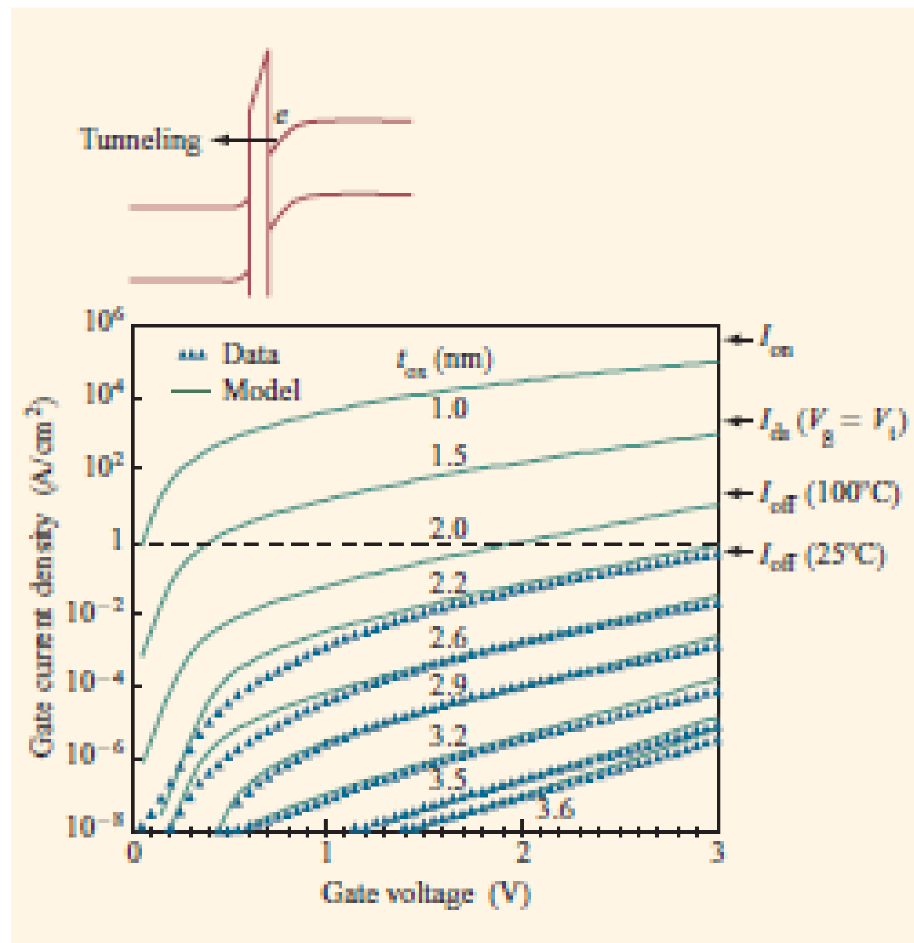


Figure 3

Measured and calculated oxide tunneling currents vs. gate voltage for different oxide thicknesses. Labels on the right, from the bottom up, mark the order of magnitude of off-currents at room and worst-case temperatures, source-to-drain current at $V_g = V_t$ ($V_{ds} = V_{dd}$), and on-current at $V_g = V_{ds} = V_{dd}$. The inset shows the band diagram for tunneling in a turned-on n-MOSFET.