

Alternative Readout System Architectures II

Mircea Bogdan, Henry Frisch, Mary Heintz, Rich Northrop, Eric Oberla,
The University of Chicago

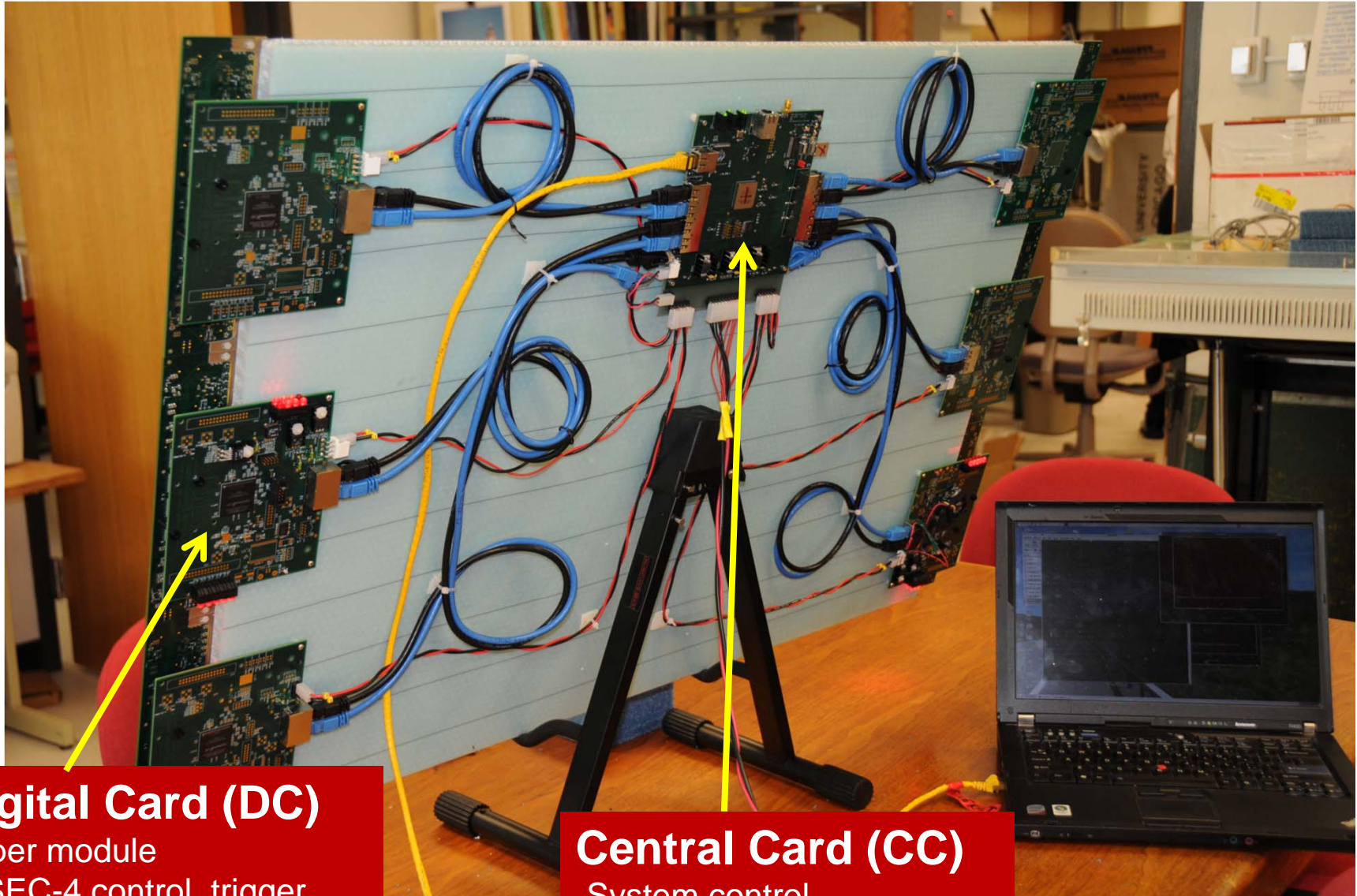
Gary Varner,
University of Hawaii at Manoa

Jean-Francois Genat
Universite Pierre et Marie Curie – Paris VI, France

Edward May
Argonne National Laboratory

LAPPD2 Electronics Godparent Review
April 6, 2013

Baseline - Super Module



Digital Card (DC)

- 6 per module
- PSEC-4 control, trigger handling, local data reduction & calibration

Central Card (CC)

- System control
- Feature extraction
- Interface (Triple Speed Ethernet & USB 2.0)

Baseline - Super Module

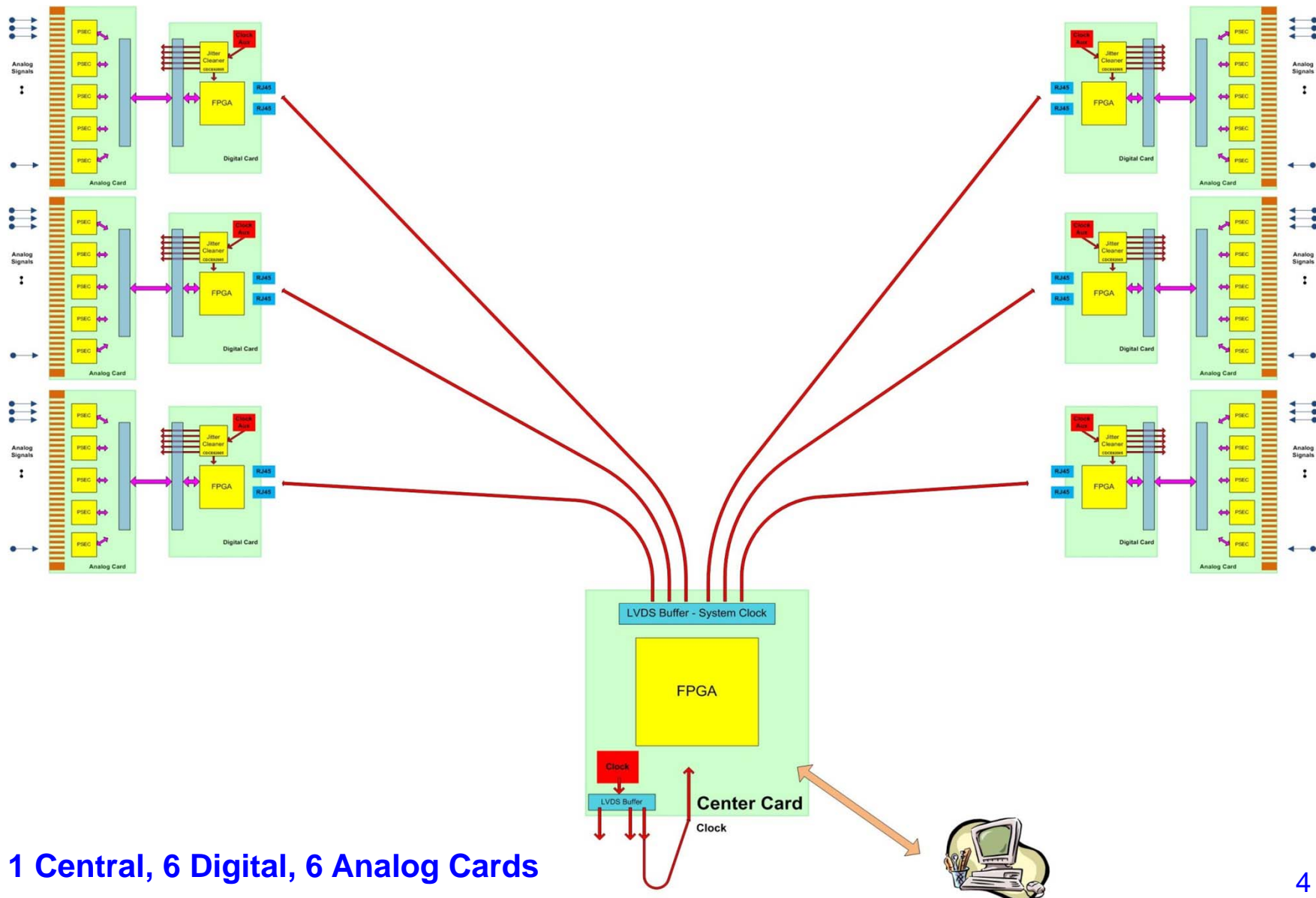
Baseline Readout System:

- Generic and flexible;
- Got us started;
- Addressed many issues.

Next DAQs will be more application specific, and optimized for performance and cost.

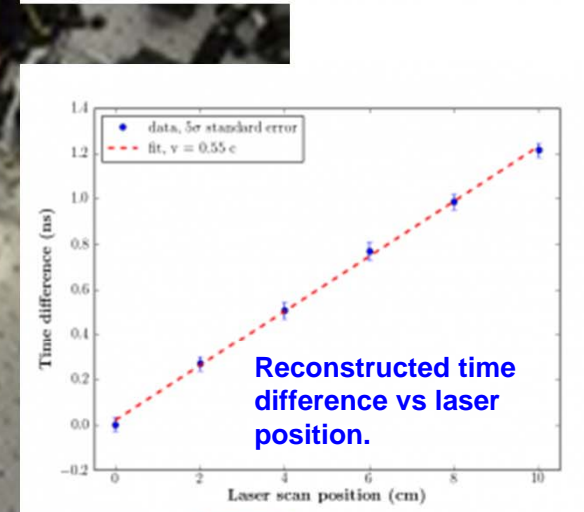
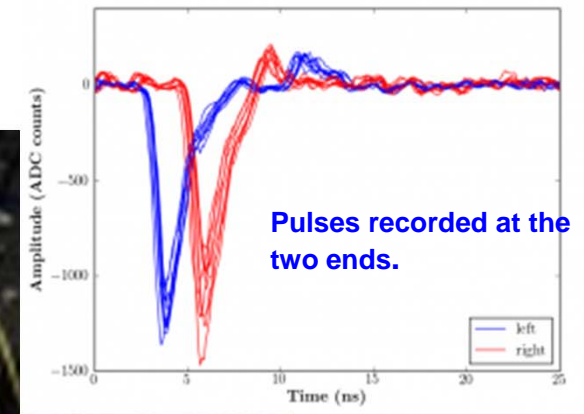
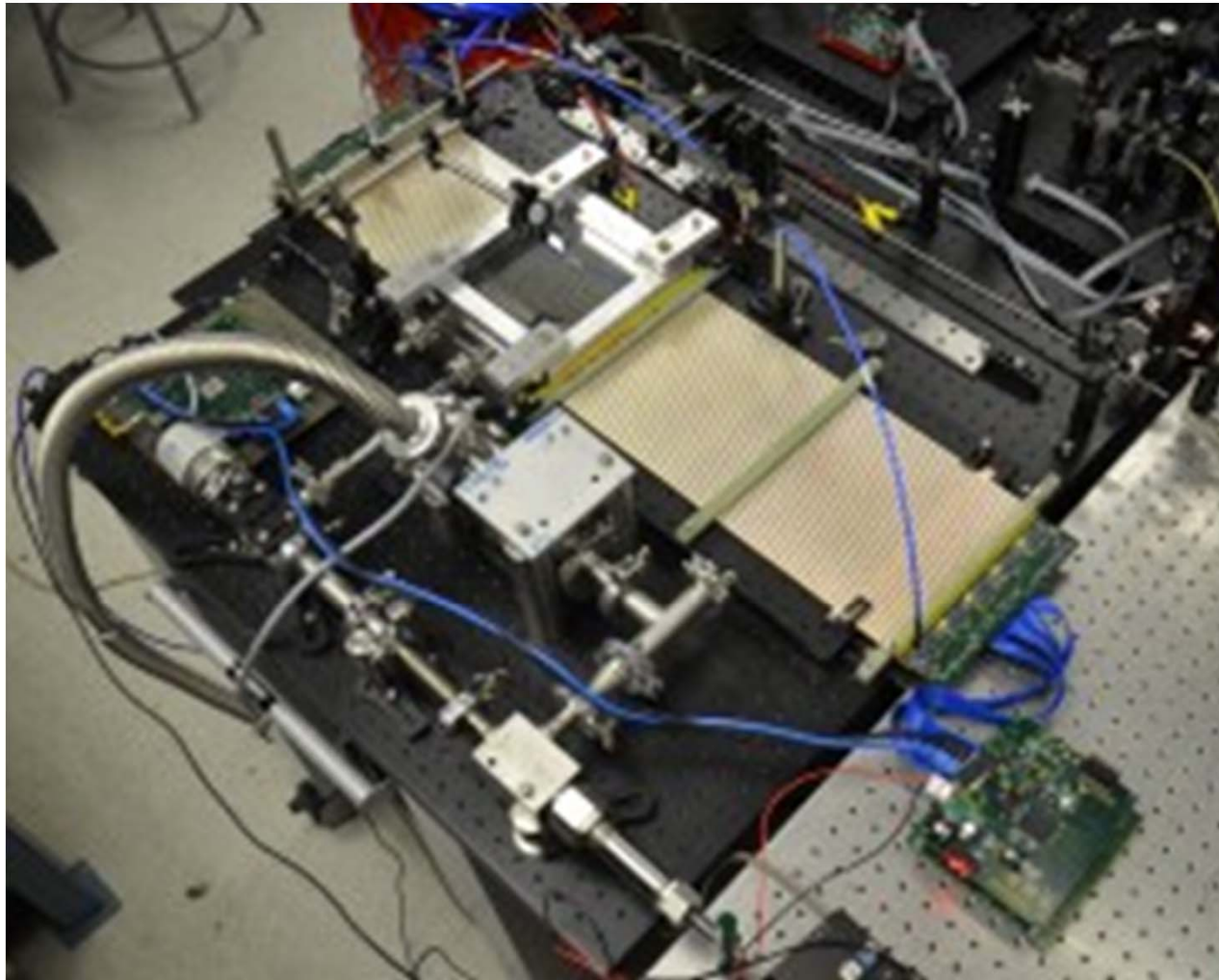
The next step will actually be easier. We've learned a lot already. Our resources should be adequate, subject to funding.

Baseline: Block Diagram



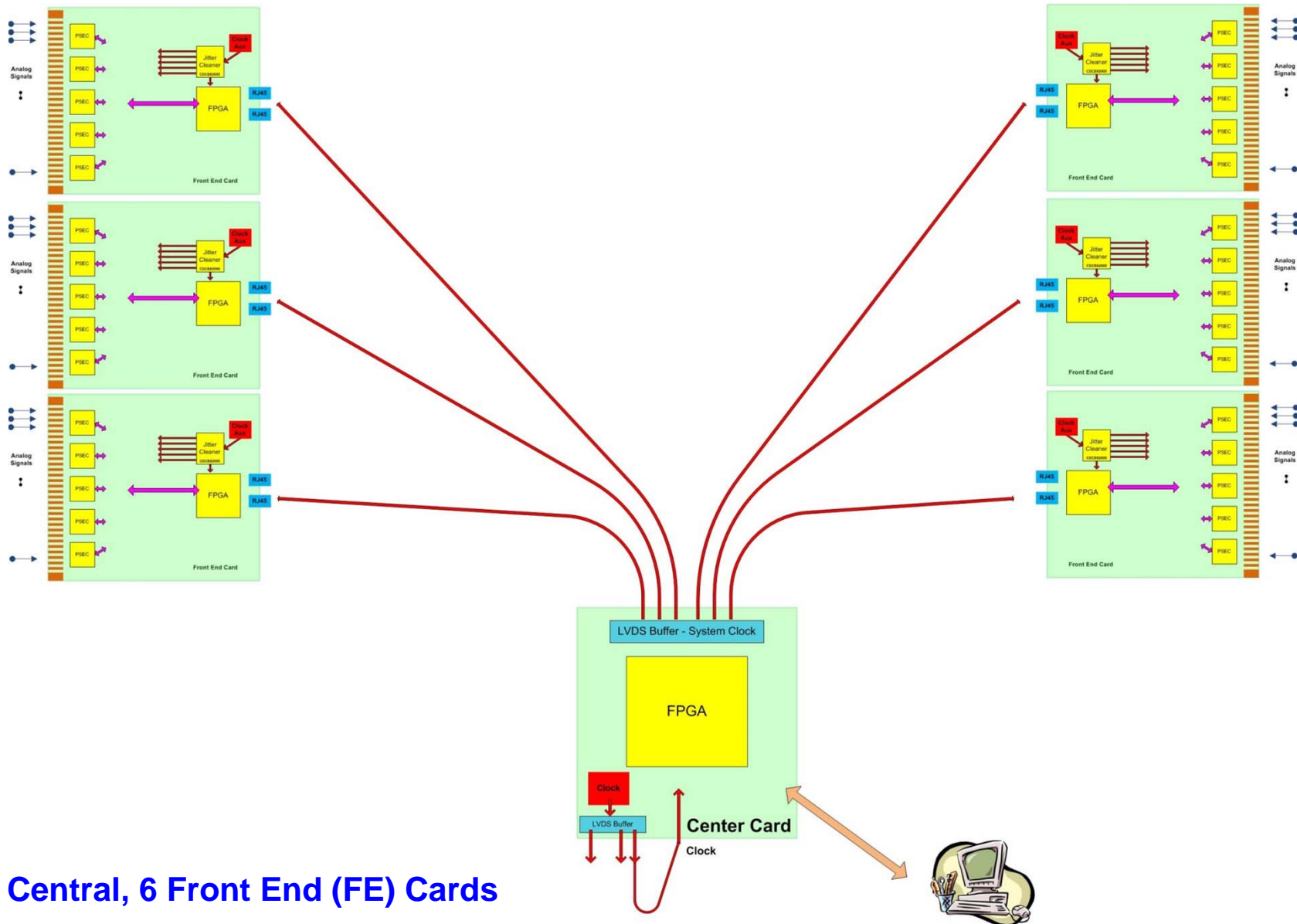
1 Central, 6 Digital, 6 Analog Cards

Baseline: Results

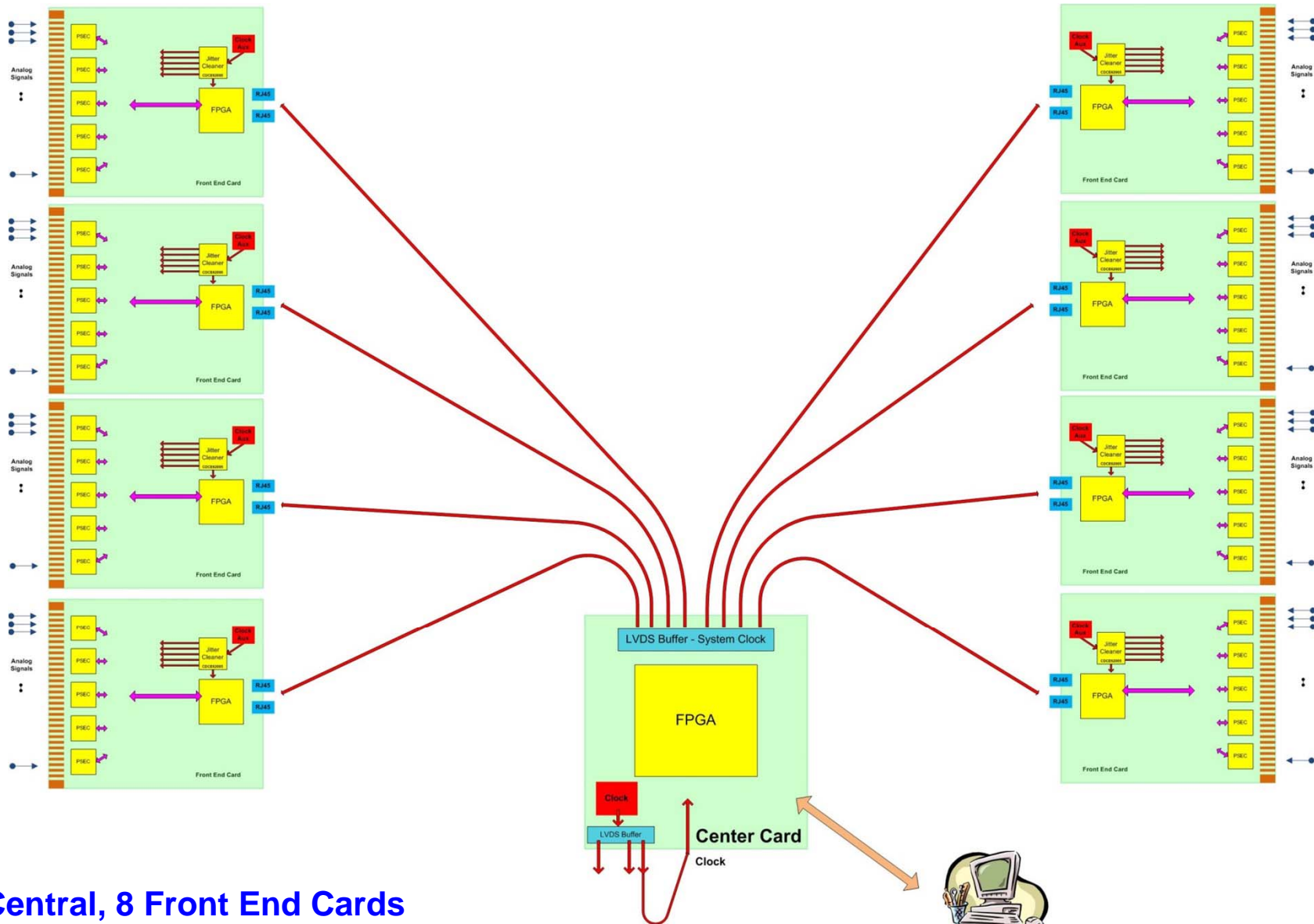


Demountable w/ full electronics – parallel scan

Alternative Architecture 1: Block Diagram

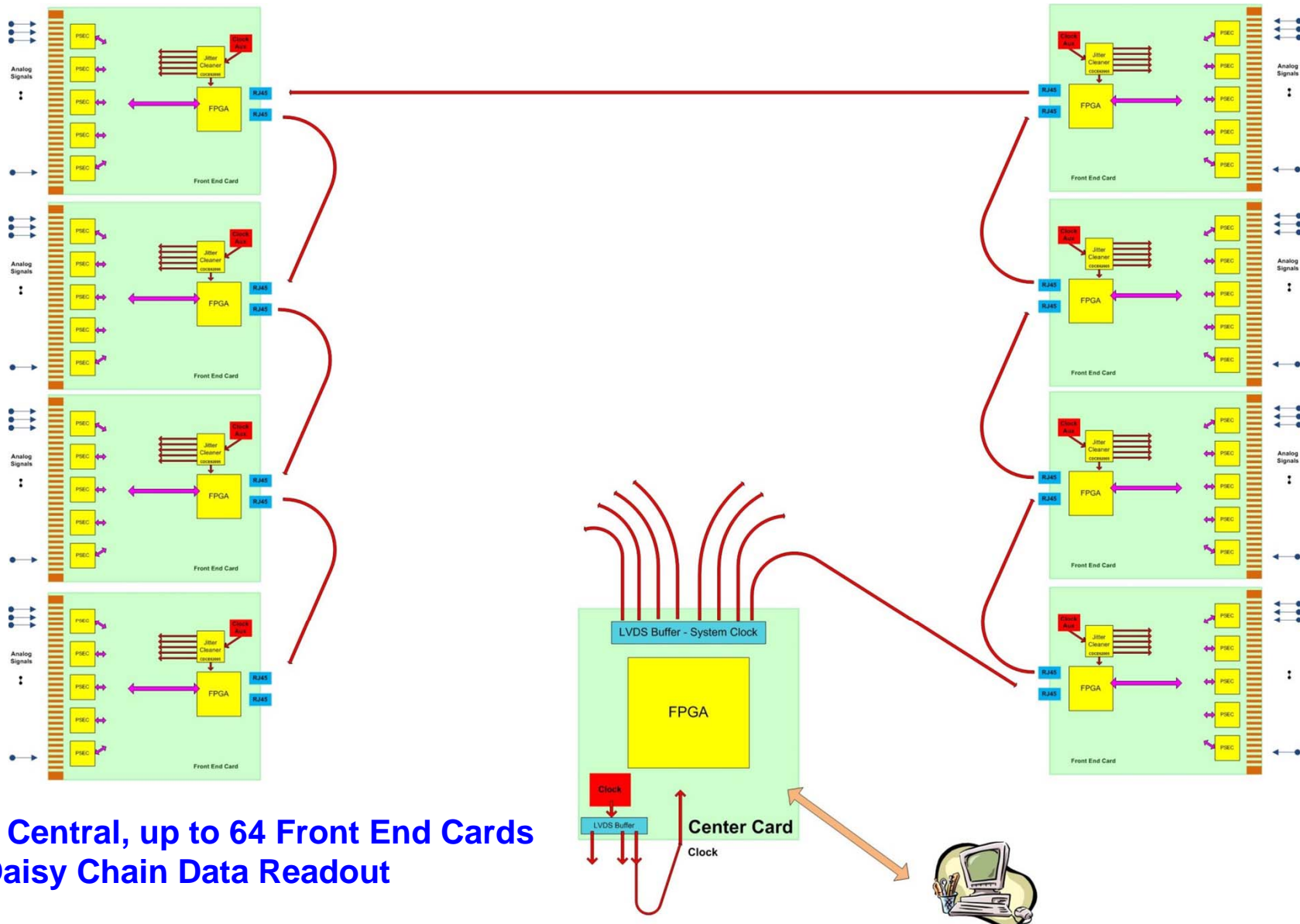


Alternative Architecture 1: Block Diagram



1 Central, 8 Front End Cards
Parallel Data readout – LVDS, max 800Mbps/line

Alternative Architecture 2: Block Diagram



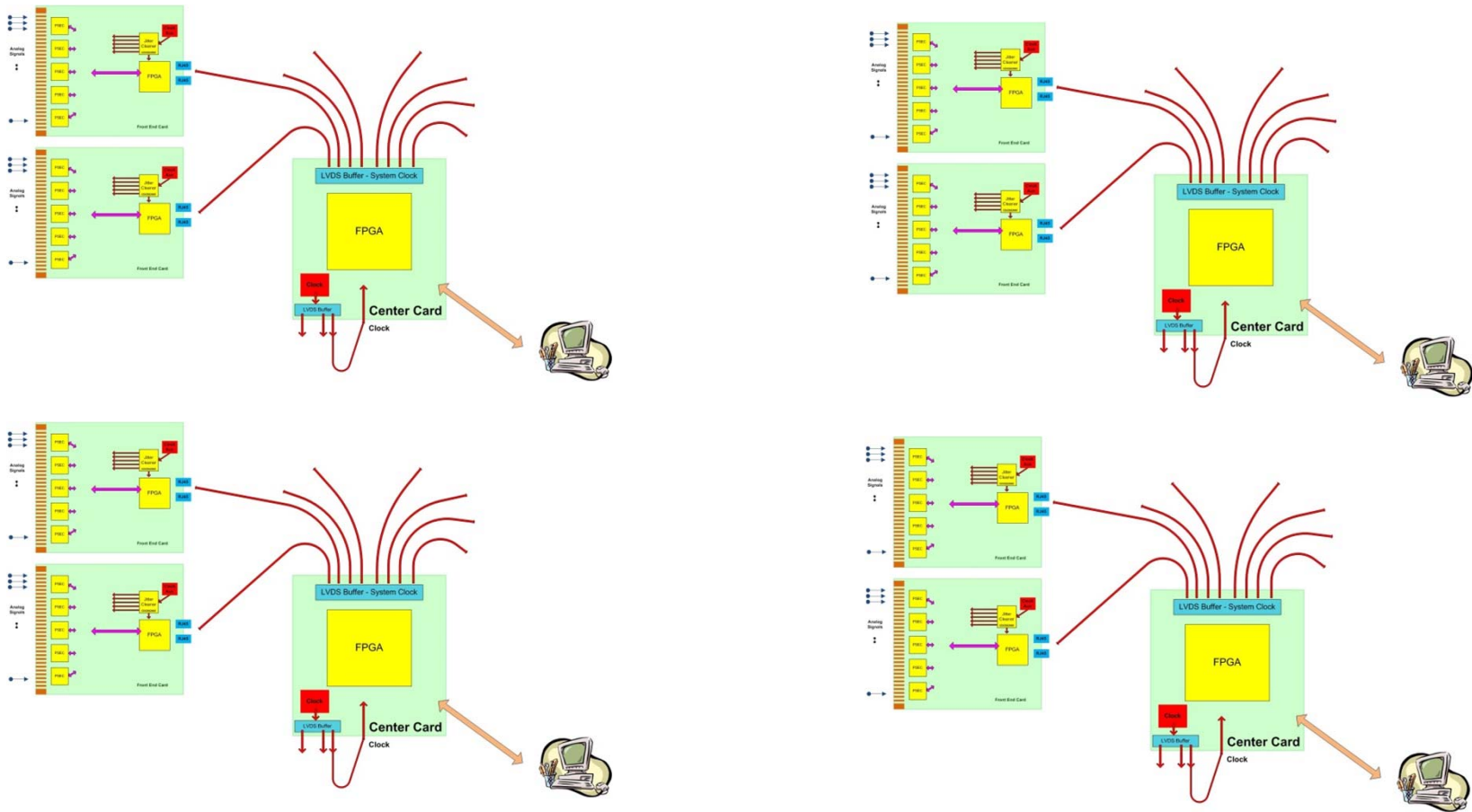
Responses To Review Panel

Question 1: What limited number of applications would you target as priorities in the next stage of development and why?

Answer: Three HEP and two directed toward market expansion:

- 1. TOF in the LArIAT Beam**
 - a) Why: Simplest set-up that has a large impact on HEP programs**
 - b) Straight-forward interface to experiment**
 - c) Local, have collaborators in place;**
 - d) Drop in for scintillators and PMTs at higher cost and better performance**
 - e) Spec: 4 stand-alone single tile stations, 10 psec time resolution, 50KHz (needs checking)**

4 Stand-Alone, Single-Tile Readout Stations



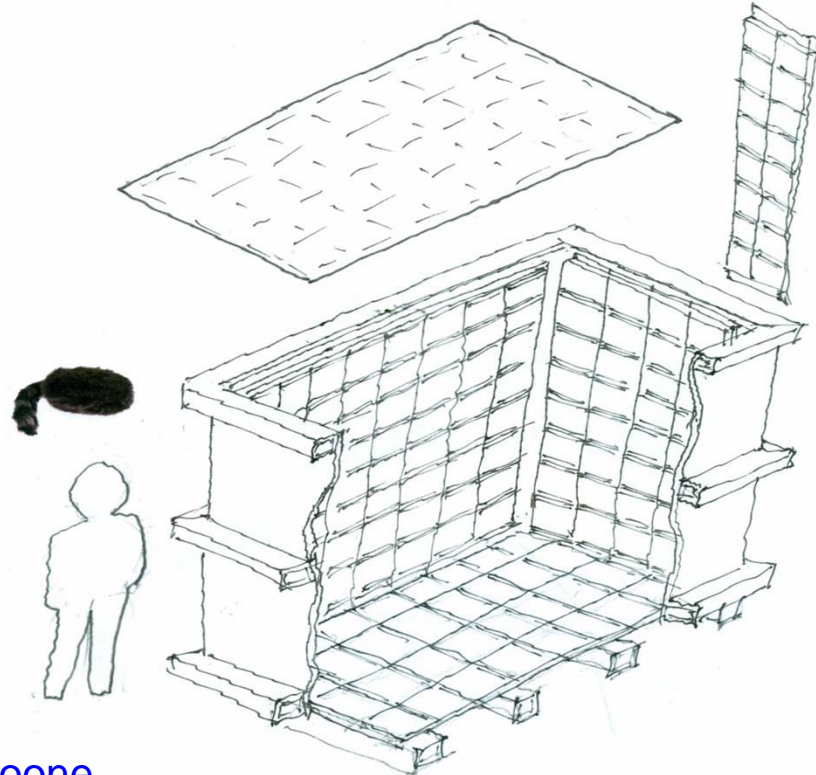
Use Alternative Architecture 1.

Max trigger rate:

$30 \text{ Channel} \times 10 \text{ bits} \times 24 \text{ samples} \times F_{\text{max}} = 400 \text{ Mbps}$

$F_{\text{max}} = 55 \text{ KHz.}$

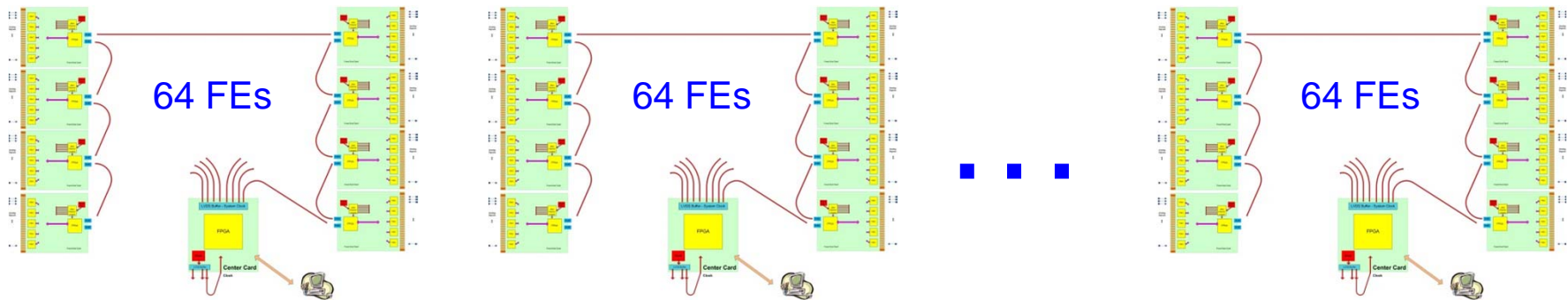
2. Small (1-4 m³) water neutrino detector prototype
- a) Why: Comparison to simulation; test of the optical TPC concept with track reconstruction
 - b) If successful, no competition
 - c) From 1 to 6 SuperModules;
 - d) Spec: Single pe resolution ~ 100psec, low rate



Daniel Boone

Water Neutrino Detector Readout

Requirements: 256 Front End Cards, slow Readout.

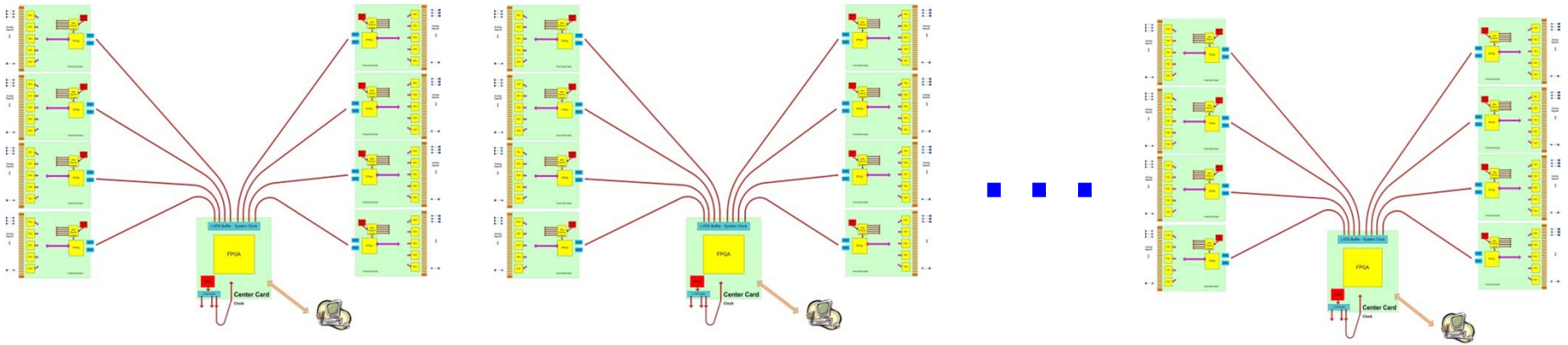


Each Central Card will read 64 Front End Cards in a daisy chain.
One of the Central Cards becomes Master and distributes the clock to all.

3. Pre-converter in KOTO

- a) **Why: Archetype for 3D localization and precise timing of high energy photons**
- b) **Good access to management and technical expertise in the experiment**
- c) **If successful, no competition**
- d) **1-4 SuperModules**
- e) **Spec: Timing = 1 psec; Rate = 200 kHz; Position = several mm; Trigger latency = 5 μ sec**
- f) **HEP benefit: Increased physics reach**

KOTO Pre-Converter Readout



Each Central Card will read 8 Front End Cards in parallel.
Readout for 200KHz trigger rate with 2 LVDS SERDES lines at 720MHz for each FE Card.

One of the Central Cards becomes Master and distributes the clock to all.
Front End needs to allow for 5 us external trigger latency.

4. PET

- a) **Why: Potential to decrease patient dose rate by >10 or increase patient throughput**
- b) **Current state of the art = 300 psec**
- c) **Spec: 50 psec (FWHM) TOF-PET resolution**
- d) **HEP benefit: Potentially large market drives the cost down**

Needs work.

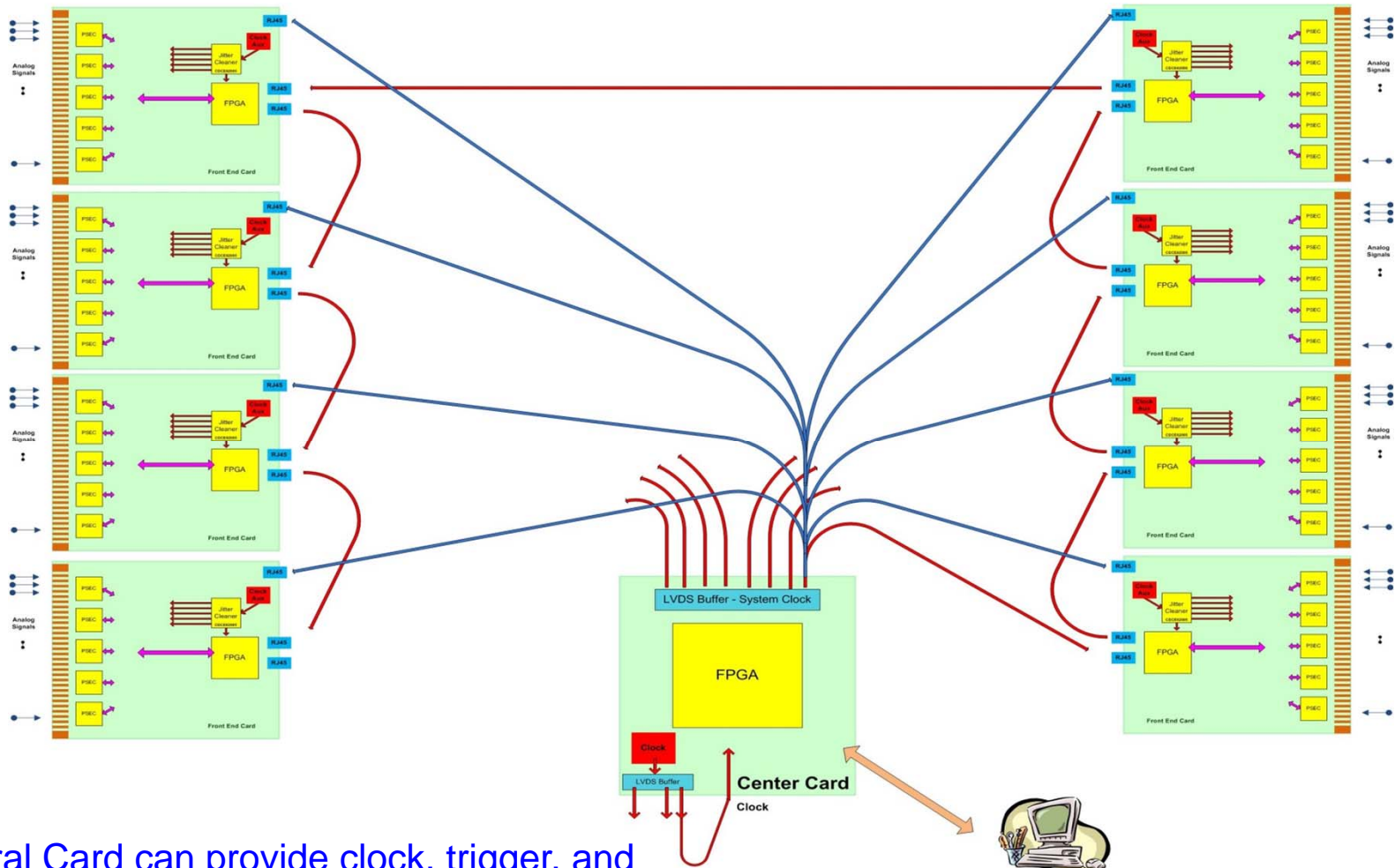
E.g. PDS Consulting in Massachusetts, Eric's Timing Setup at UC, etc.

5. **High spatial resolution X-ray diffraction**
 - a) **Why: Large area detector with high spatial resolution**
 - b) **Large area, high spatial resolution, multi-channel solid state detectors are very expensive and slow**
 - c) **Spec: 100 μm spatial**
 - d) **HEP benefit: Increase cross-disciplinary ties**

Needs work.

Clock Distribution

Synchronous clock fan-out to 64 FE Cards.



One Central Card can provide clock, trigger, and receive hits to/from all FE Cards in parallel.