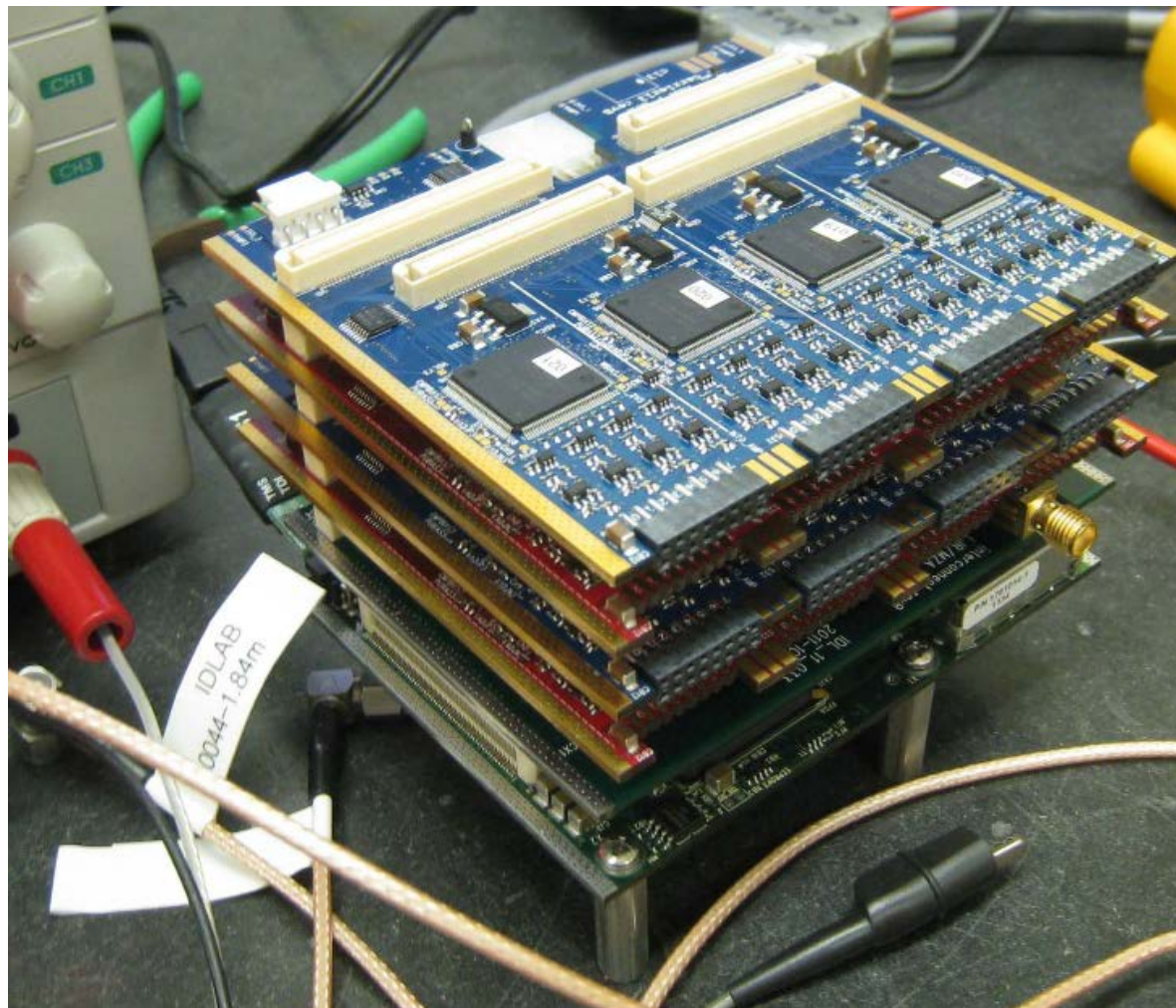


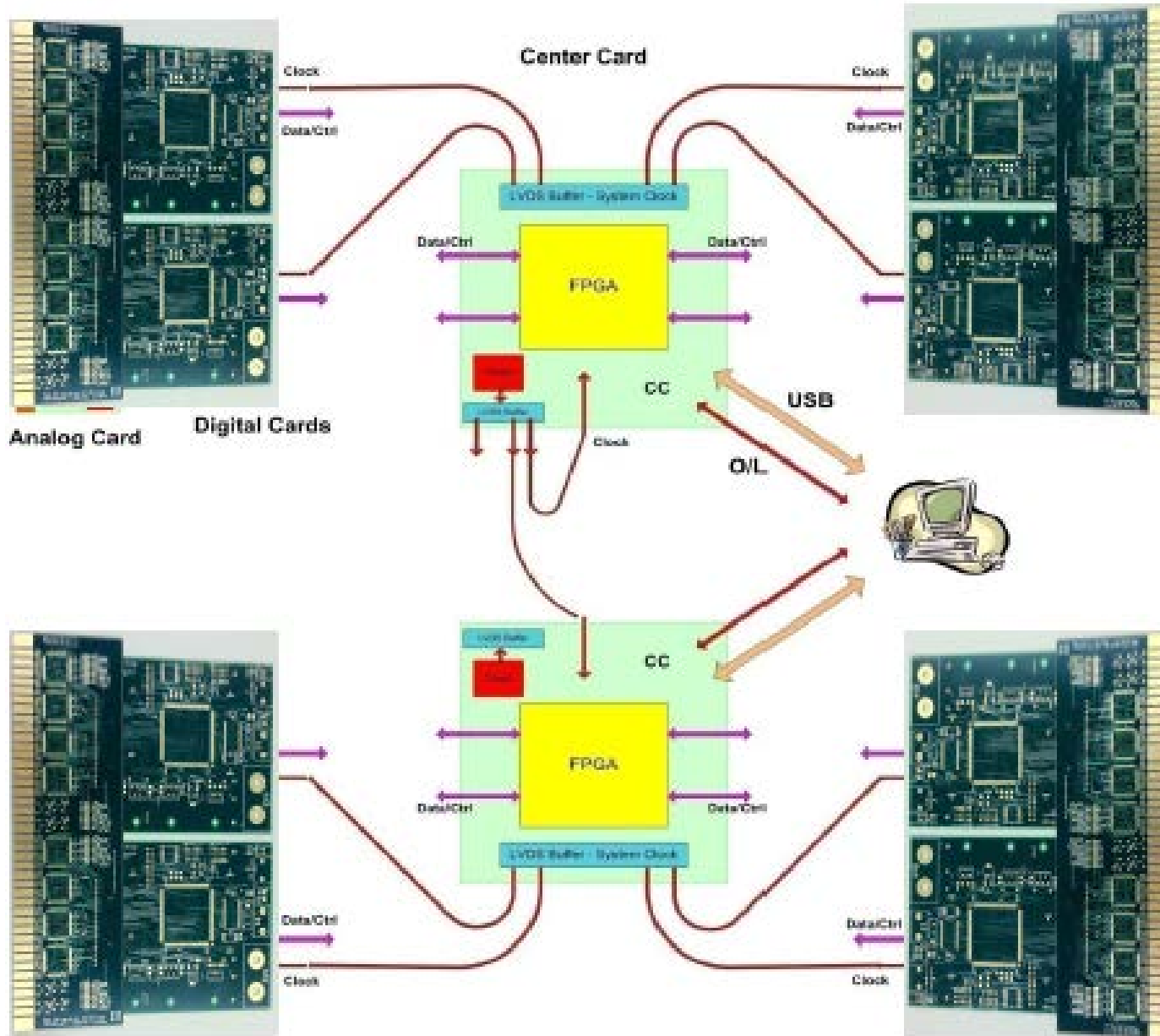
Alternative Architectures I



G. Varner

6-APR-2013 == godparent Review at ANL

Modular Readout System architecture

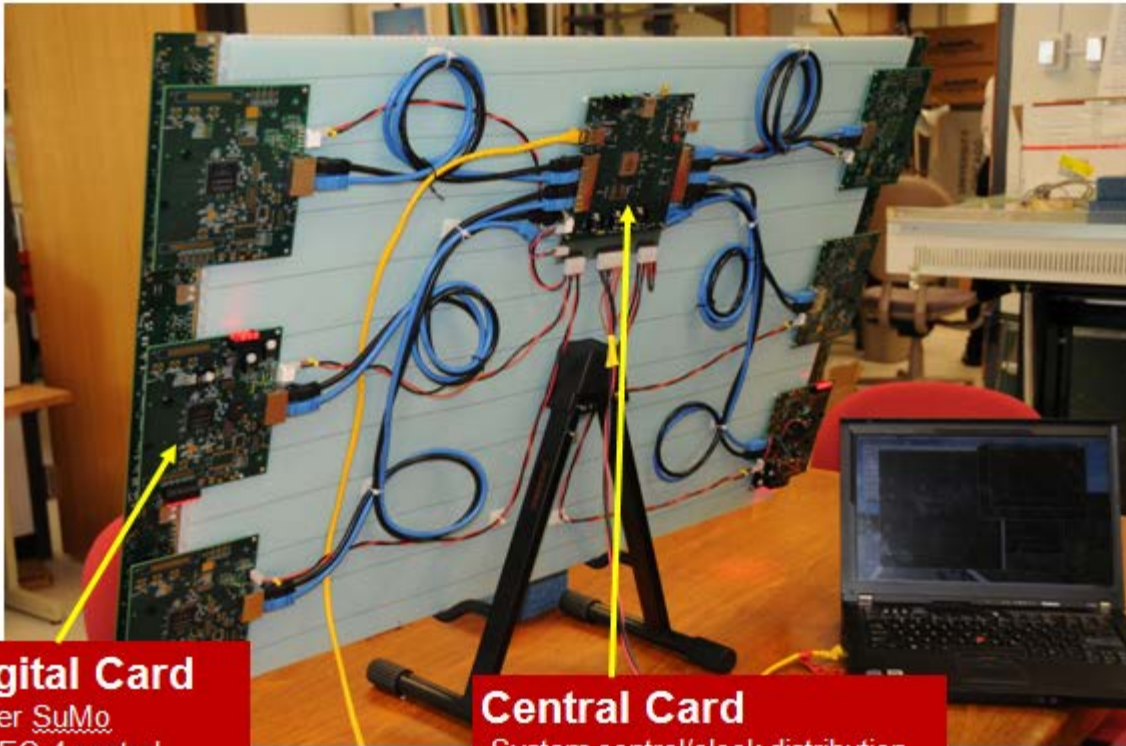


Respin Analog card only for different ASIC

A variety of data collection configurations possible

Demonstrate timing distribution @ ps level between modules

System Engineering Issues



Digital Card

- 6 per SuMo
- PSEC-4 control, trigger handling, local data reduction & calibration

Central Card

- System control/clock distribution
- Feature extraction & event pairing
- CPU/GPU interface

(10 Gbit Ethernet & USB 2.0)

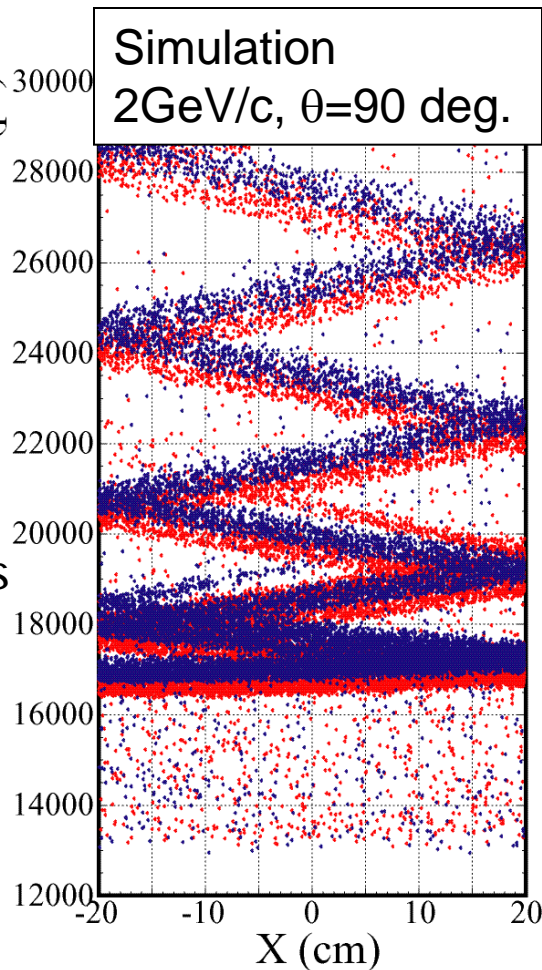
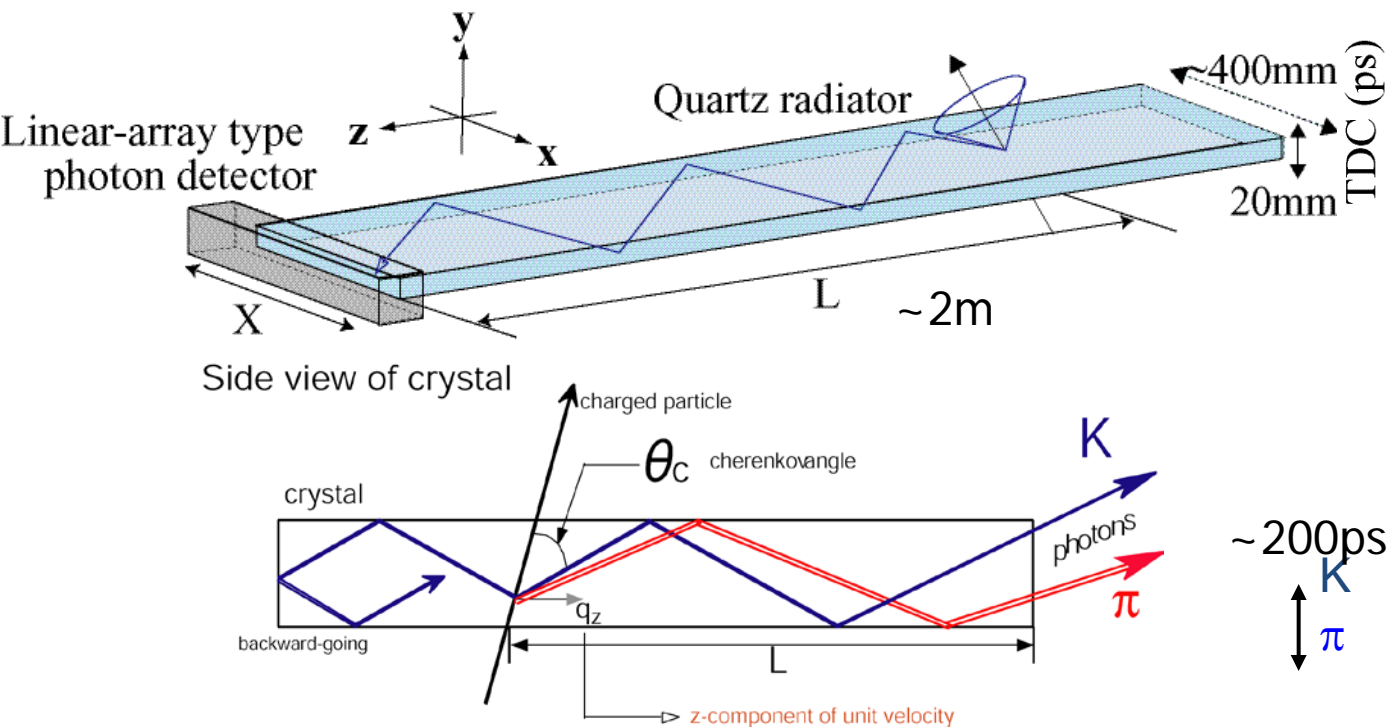


- **Current experience with Belle II iTOP development**
→ much firmware/infrastructure development required still

Example: TOP counter (concept)

Linear array PMT (~5mm)
Time resolution $\sigma \sim 40\text{ps}$

- Measure Position+Time



Different opening angle for the same momentum
→ Different propagation length(= **propagation time**)

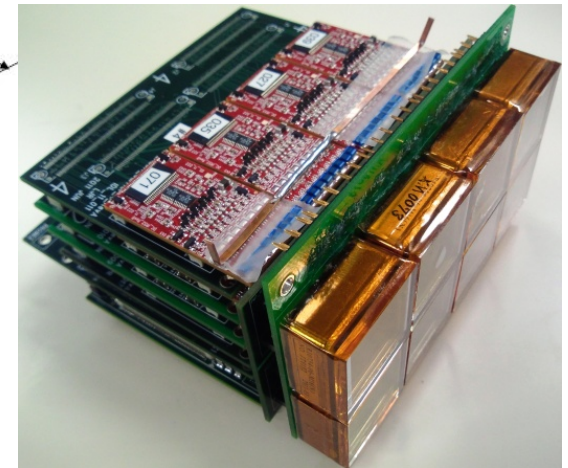
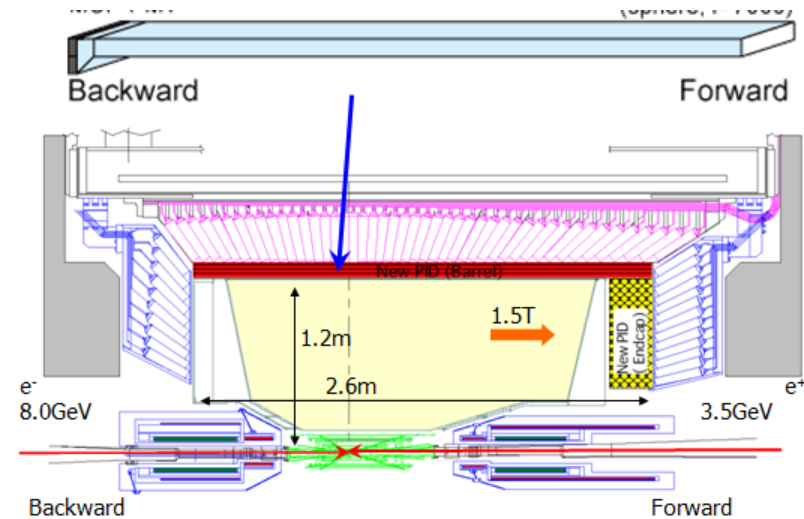
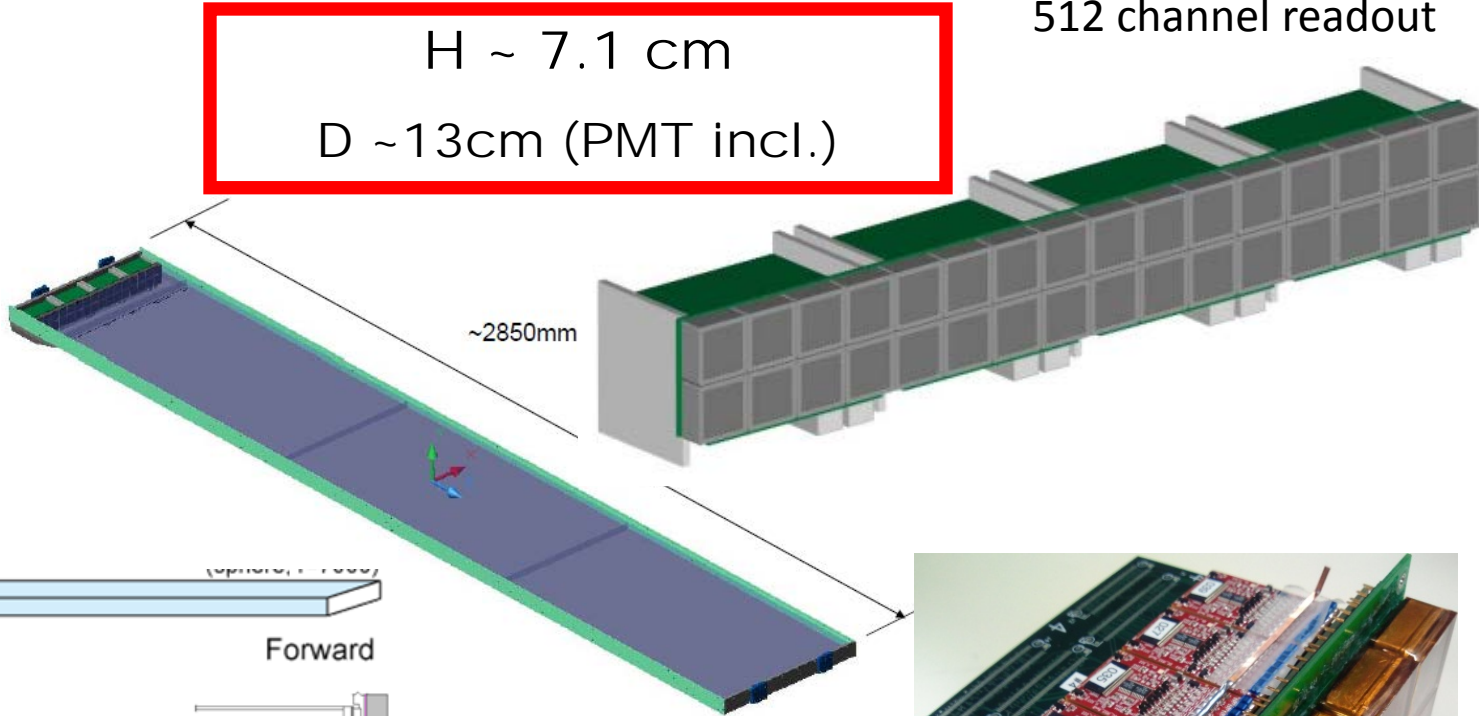
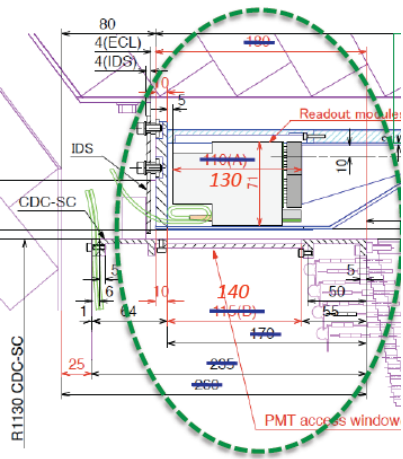
+ **TOF from IP** works additively.

Slightly Enhanced “image plane”

- Must fit in a very crowded envelope

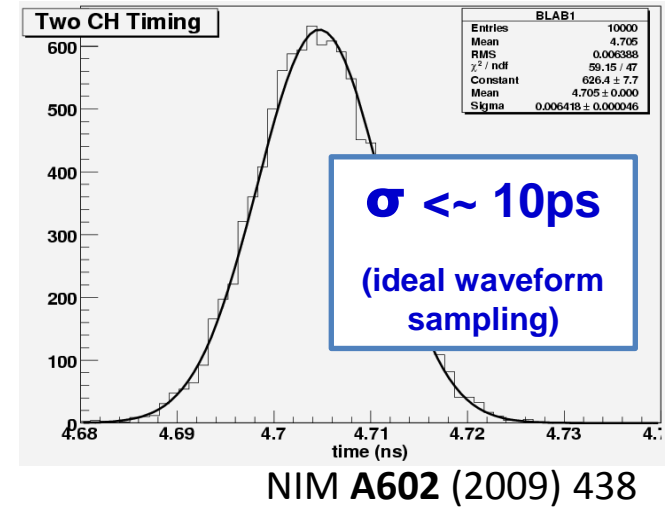
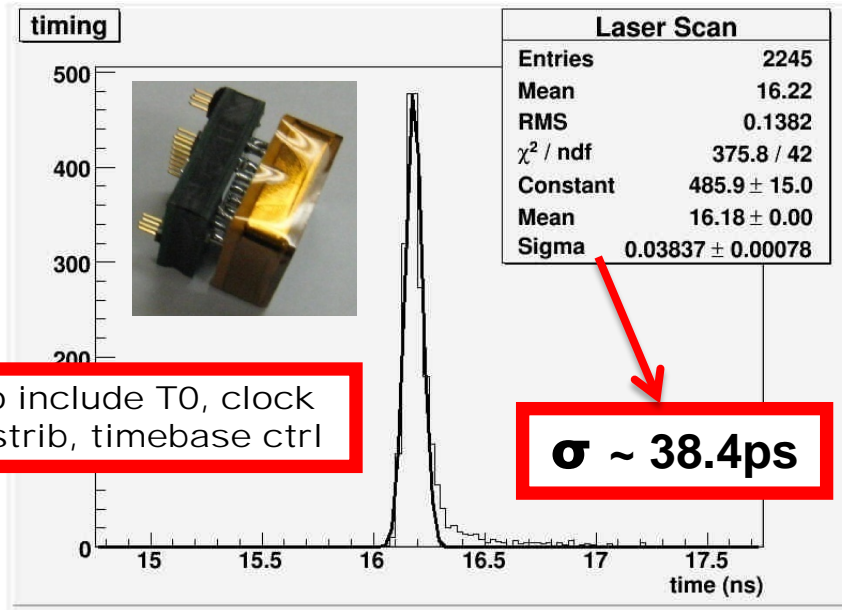
H ~ 7.1 cm
D ~ 13cm (PMT incl.)

512 channel readout



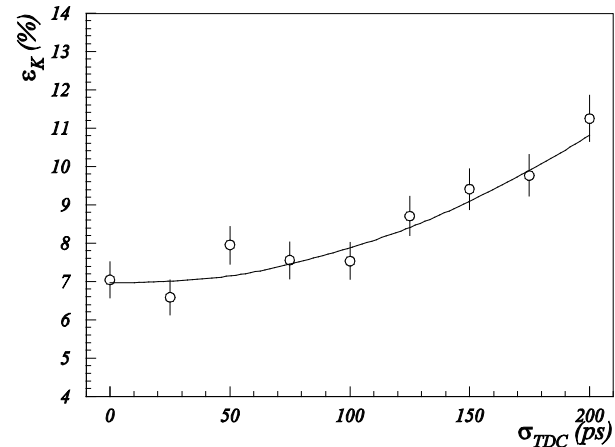
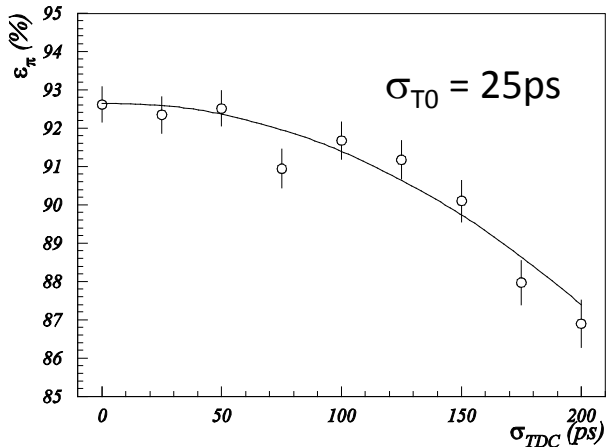
Performance Requirements (TOP)

- Single photon timing for MCP-PMTs



$\sigma \leq 100\text{ps} \rightarrow 1\% \text{ impact}$

$\sigma < \sim 50\text{ps}$ target

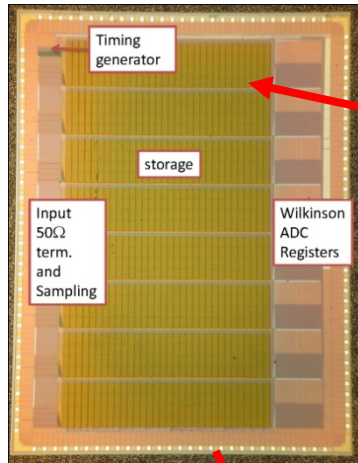


NOTE: this is single-photon timing, not event start-time "T0"

iTOP Readout Architecture

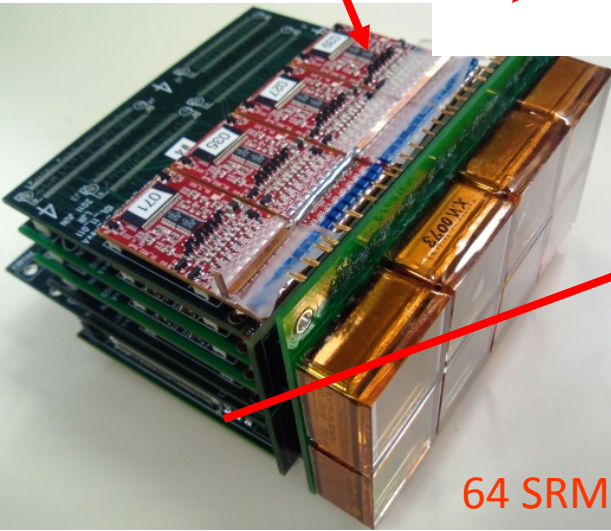
16 COPPER

Waveform sampling ASIC

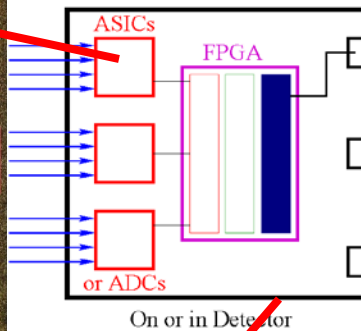


8k channels

1k 8-ch. ASICs



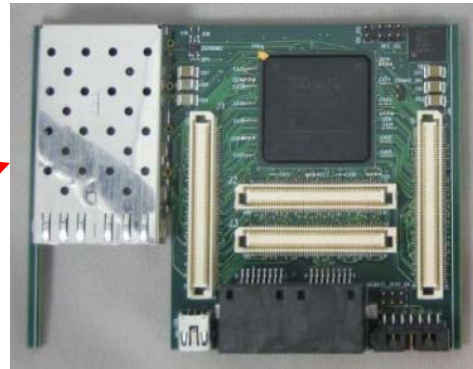
Subdetector Readout Module



FPGA firmware consists of 3 parts:

- 1) ASIC/ADC driver (common)
- 2) Trigger feature extract (subdet. specific)
- 3) Unified DAQ transport protocol

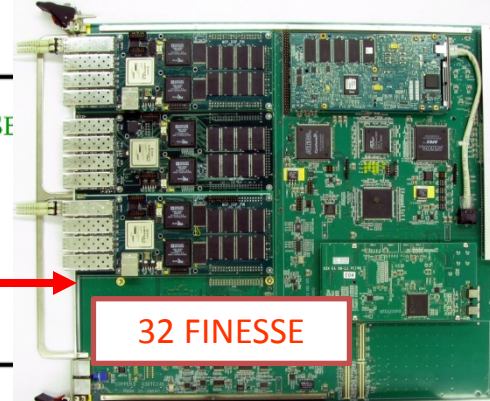
Clock jitter cleaners



Giga-bit Fiber Transceiver Links

COPPER

FINESSE



Global Decision Logic

9 TRGmod

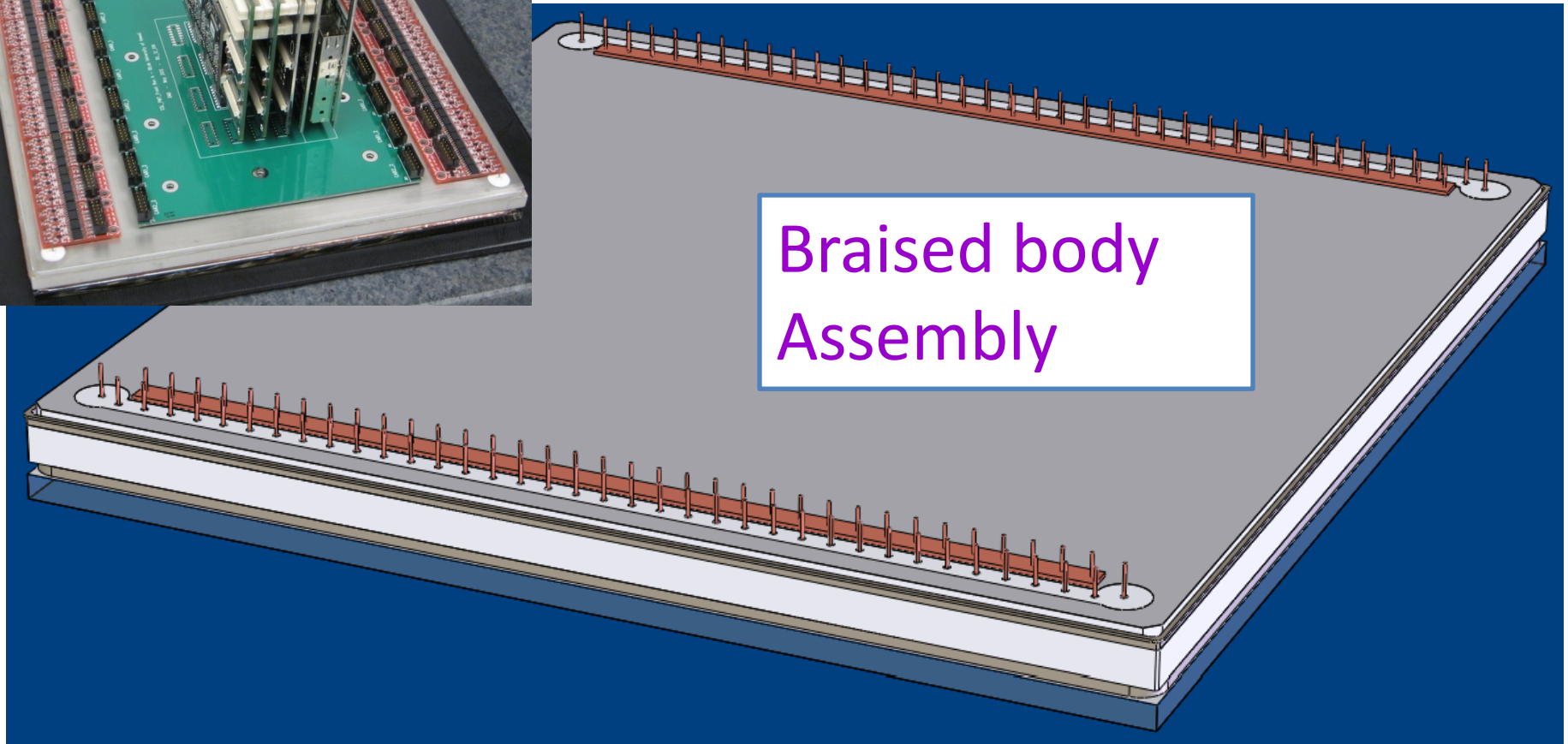
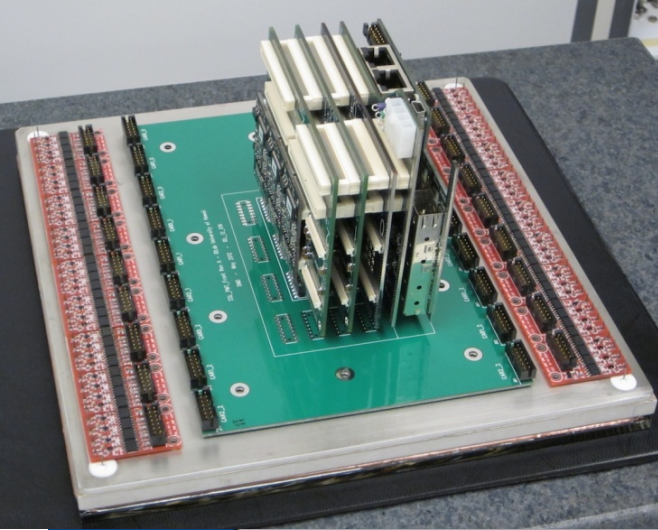


Clock/Event Timing Distribution

FTSW clock, trigger, programming



Ceramic design



- Mechanically different configuration
- Leverage Belle II iTOP HW/FW development effort
- Single p.e. TTS limitation

Alternative Architectures

- Part II will illustrate how 5 “first adopters” could be accommodated with variants of the primary LAPPD tile/anode readout
- **Acknowledge upfront application “users” will want to tailor: point is to provide a proof-of-concept/reference design**
- **Support of systems for first adopters is an issue – and not unrelated to architecture choice**