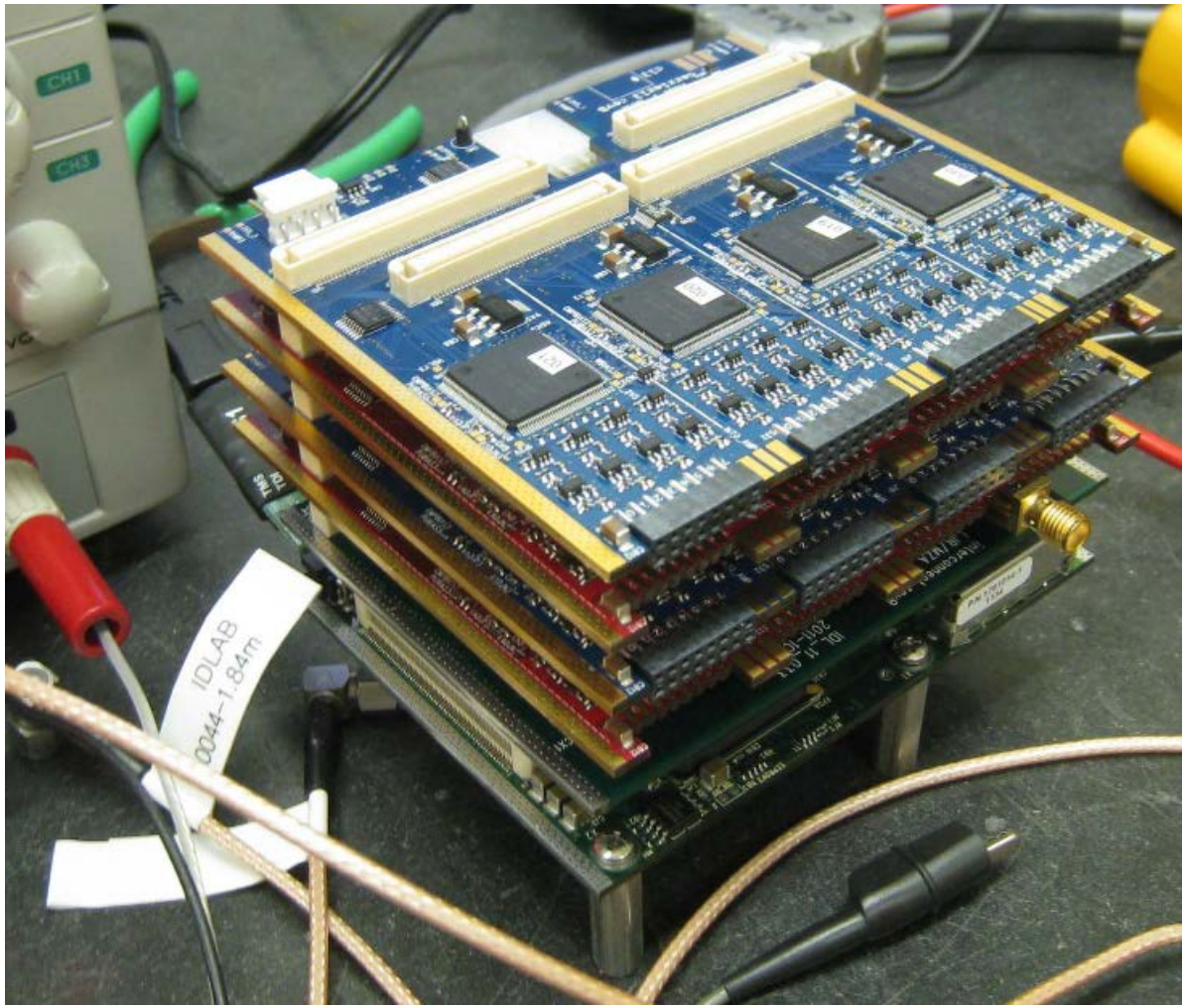
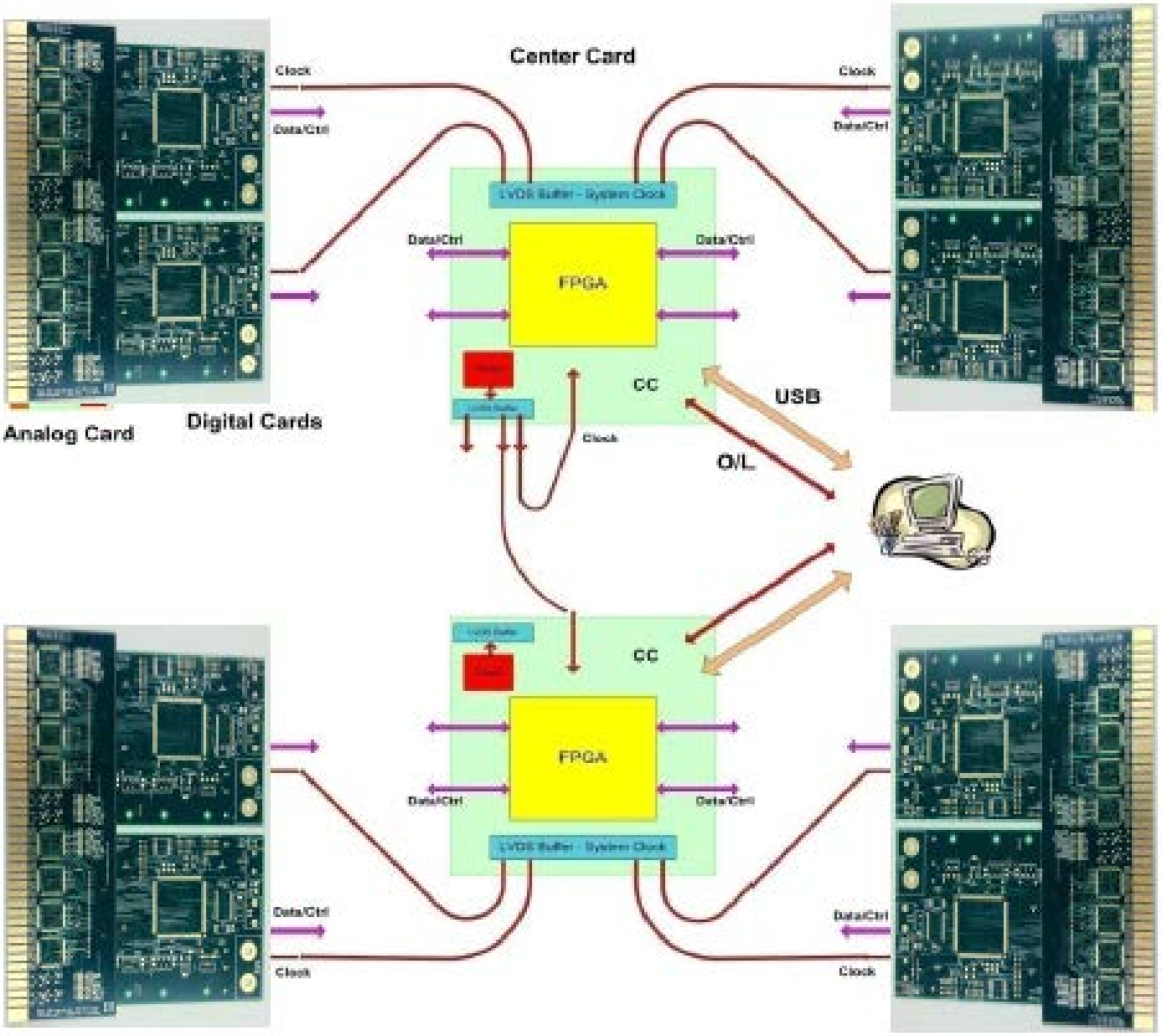
Alternative Architectures I



G. Varner

6-APR-2013 == godparent Review at ANL

Modular Readout System architecture

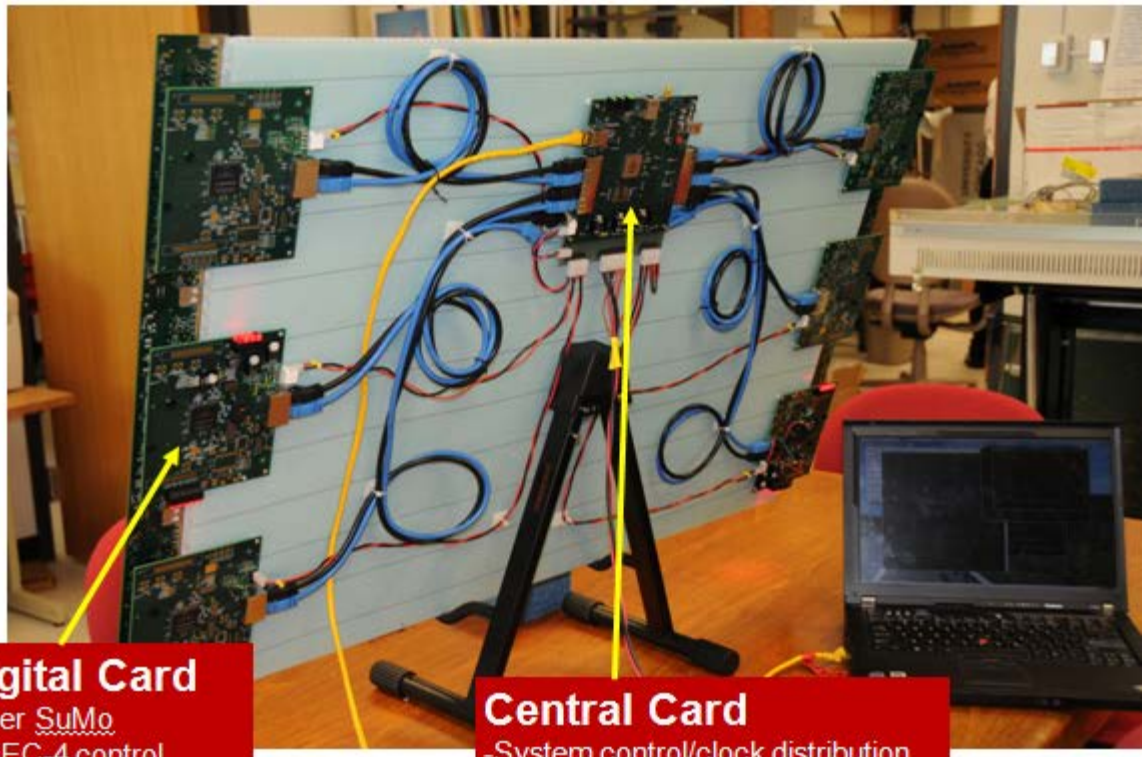


Respin Analog card only for different ASIC

A variety of data collection configurations possible

Demonstrate timing distribution @ ps level between modules

System Engineering Issues

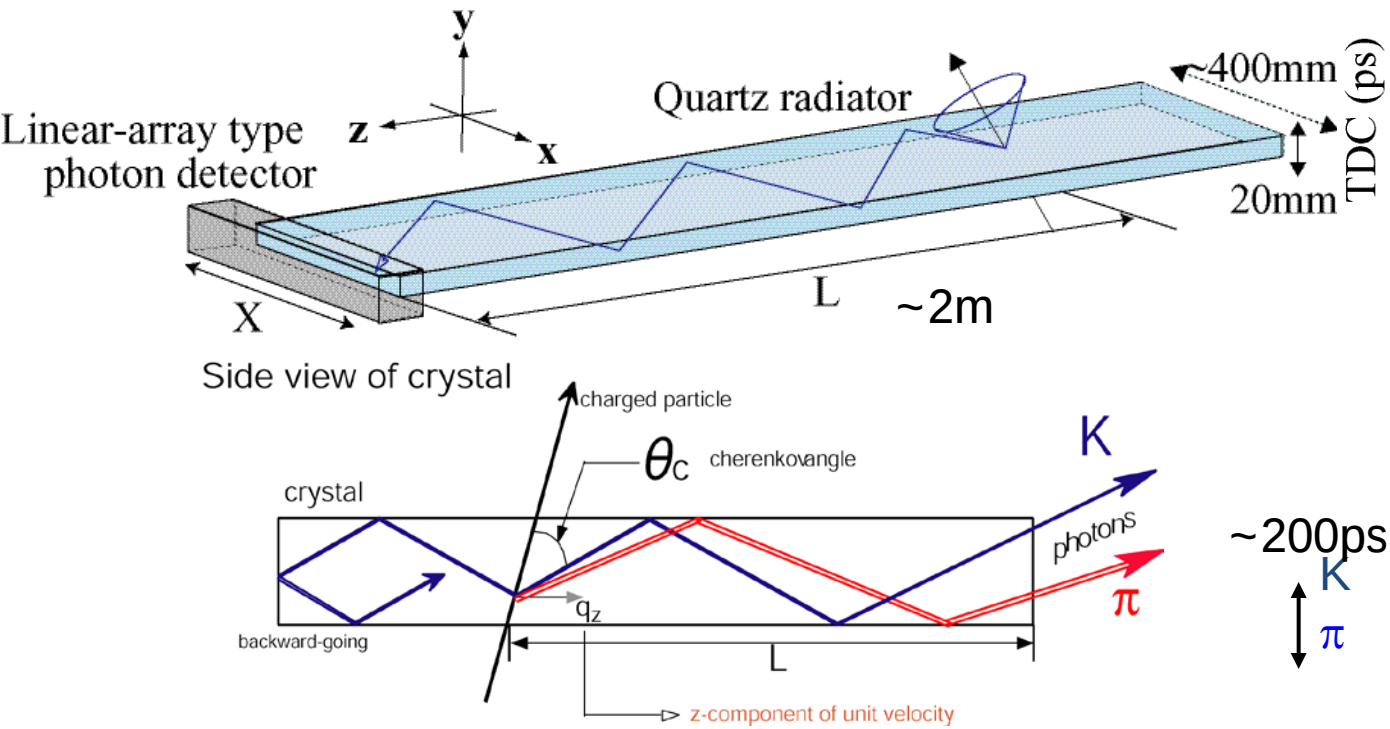


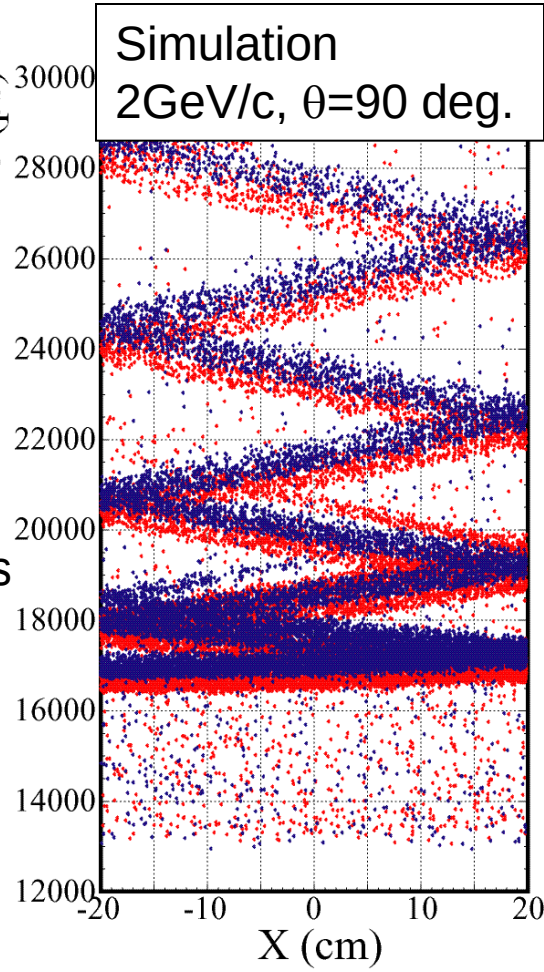
- **Current experience with Belle II iTOP development → much firmware/infrastructure development required still**

Example: TOP counter (concept)

Linear array PMT (~5mm)
Time resolution σ~40ps

- Measure Position+Time





Different opening angle for the same momentum
→ Different propagation length(= propagation time)

+ TOF from IP works additively.

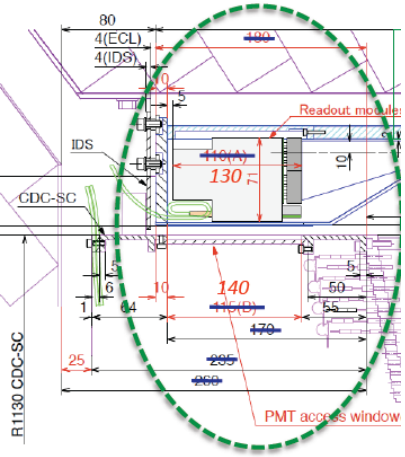
Slightly Enhanged “image plane”

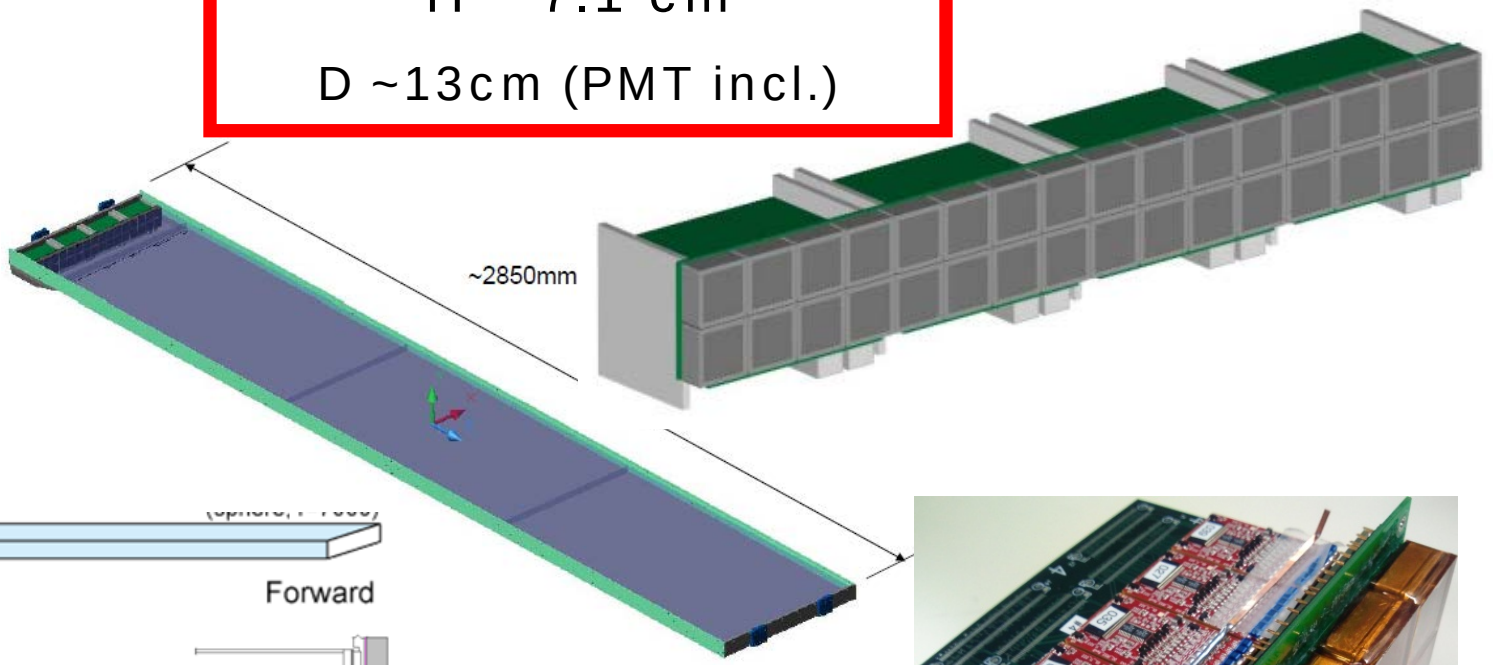
- Must fit in a very crowded envelope

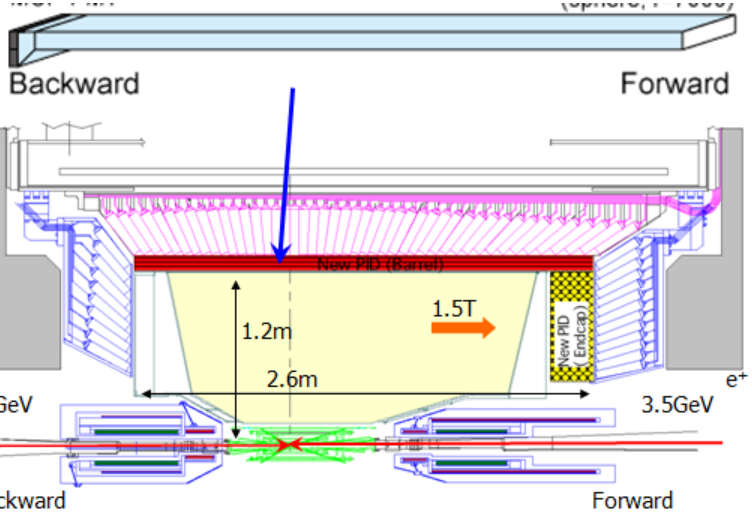
H ~ 7.1 cm

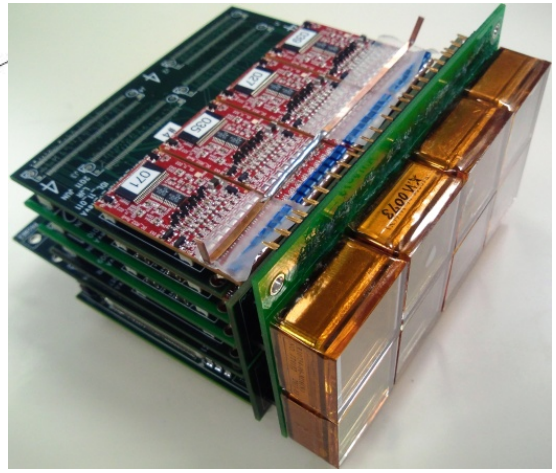
D ~13cm (PMT incl.)

512 channel readout



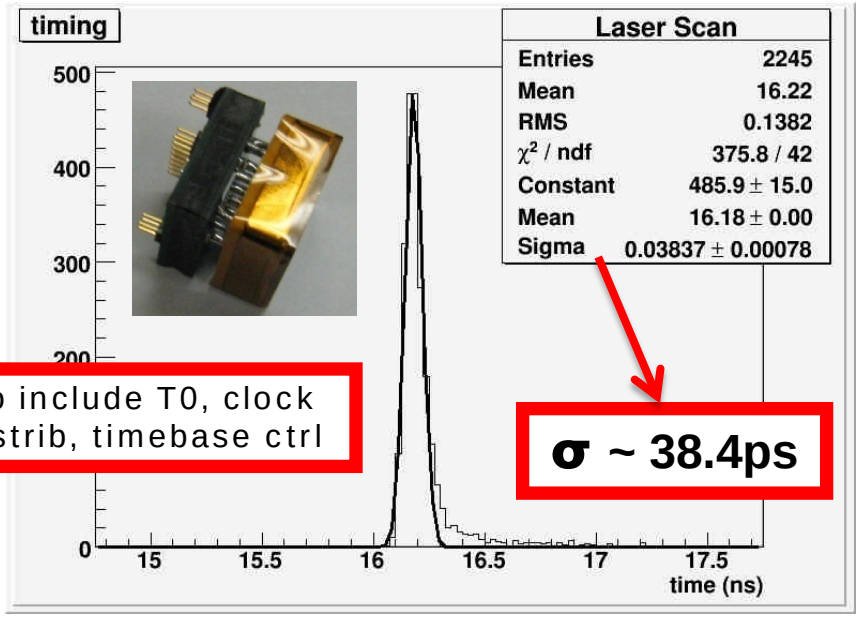


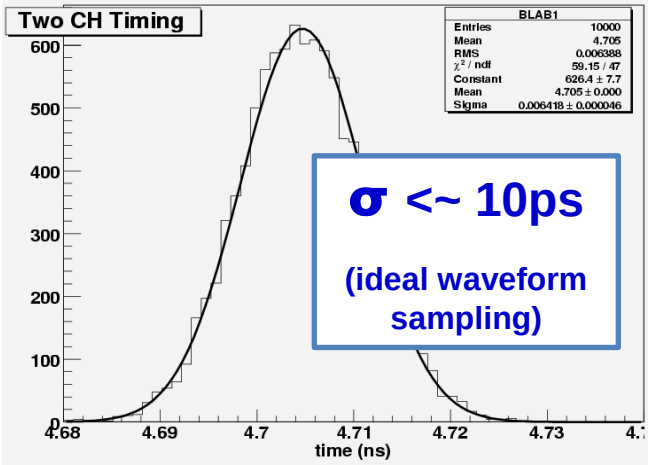




Performance Requirements (TOP)

- Single photon timing for MCP-PMTs

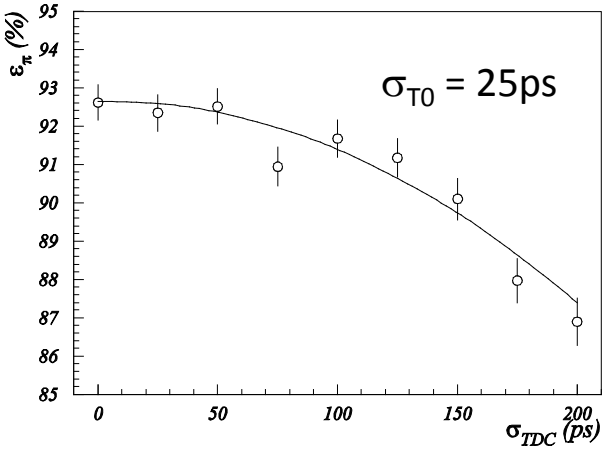


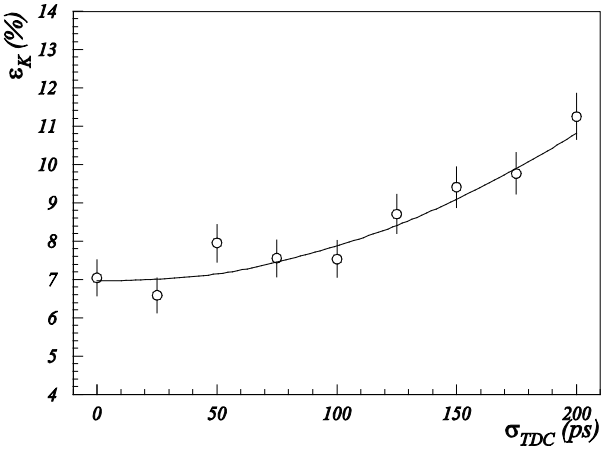


NIM **A602** (2009) 438

σ <= 100ps ➔ 1% impact

σ <~ 50ps target

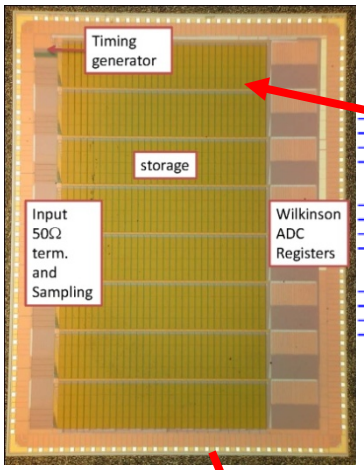




NOTE: this is single-photon timing, **not** event start-time "T_0"

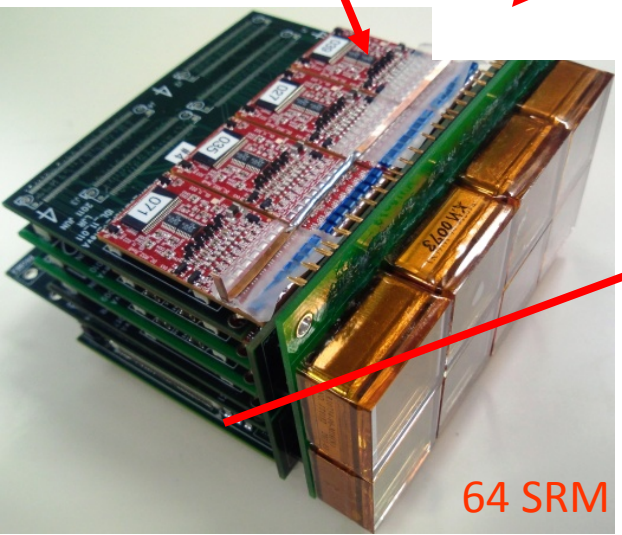
iTOP Readout Architecture

Waveform sampling ASIC

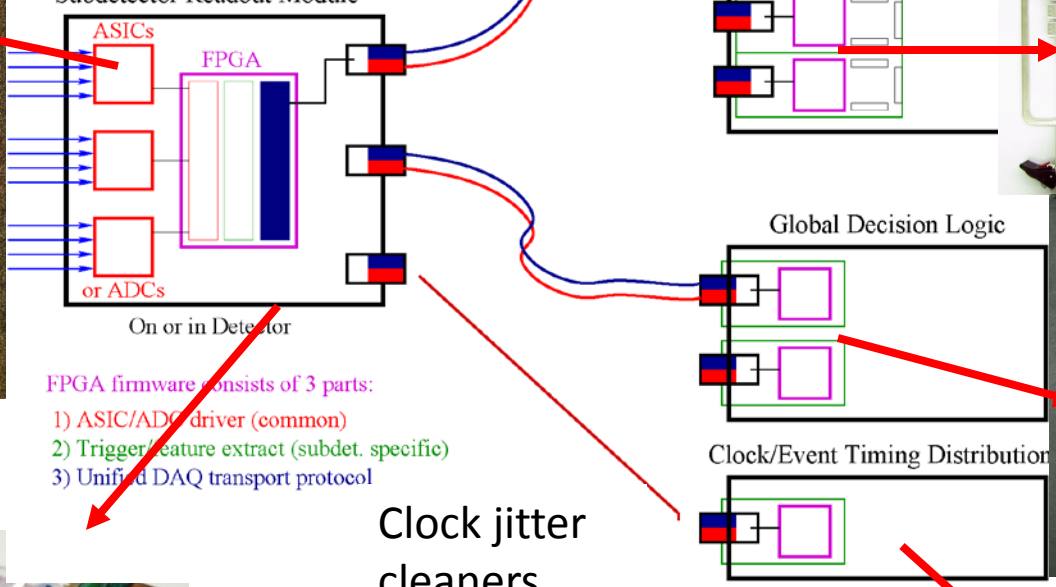


8k channels

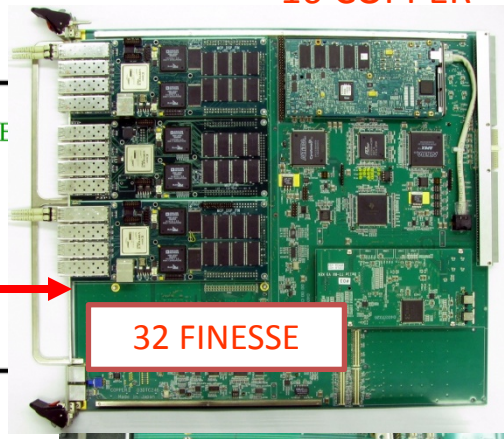
1k 8-ch. ASICs

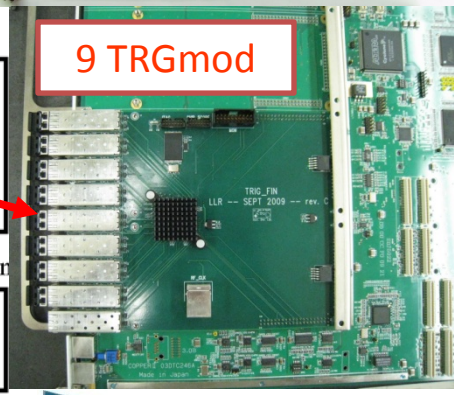


64 SRM

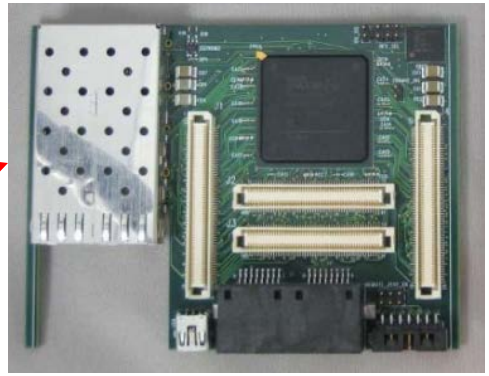


16 COPPER





Clock jitter cleaners

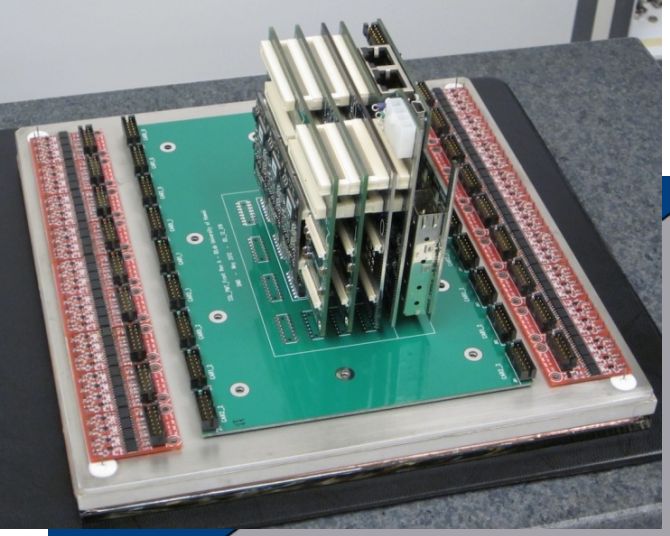


SRM Control "SCROD"

FTSW clock, trigger, programming

16 FTSW

Ceramic design



- Mechanically different configuration
- Leverage Belle II iTOP HW/FW development effort
- Single p.e. TTS limitation

Alternative Architectures

- Part II will illustrate how 5 “first adopters” could be accommodated with variants of the primary LAPPD tile/anode readout
- Acknowledge upfront application “users” will want to tailor: point is to provide a proof-of-concept/reference design
- Support of systems for first adopters is an issue – and not unrelated to architecture choice