Monday September 26th 2016

Silicon Detectors:
HV CMOS, LGAD, Thin Film, …

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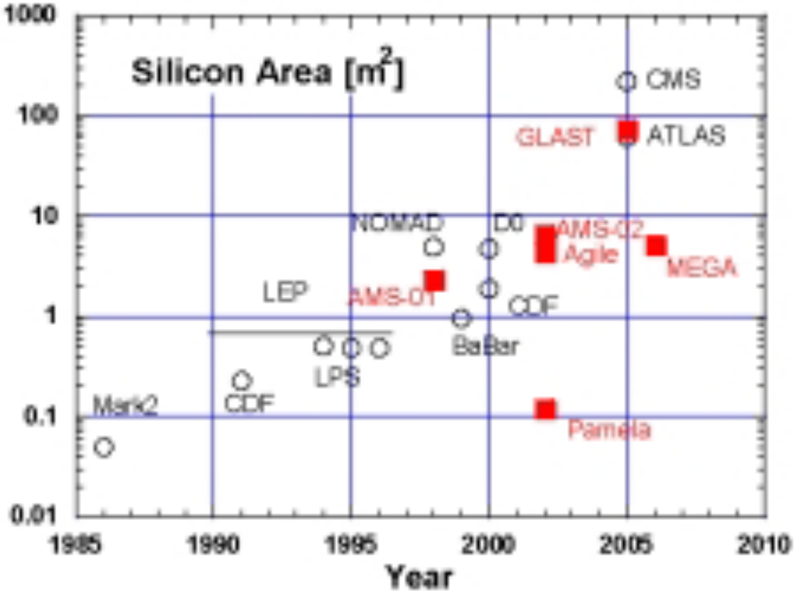
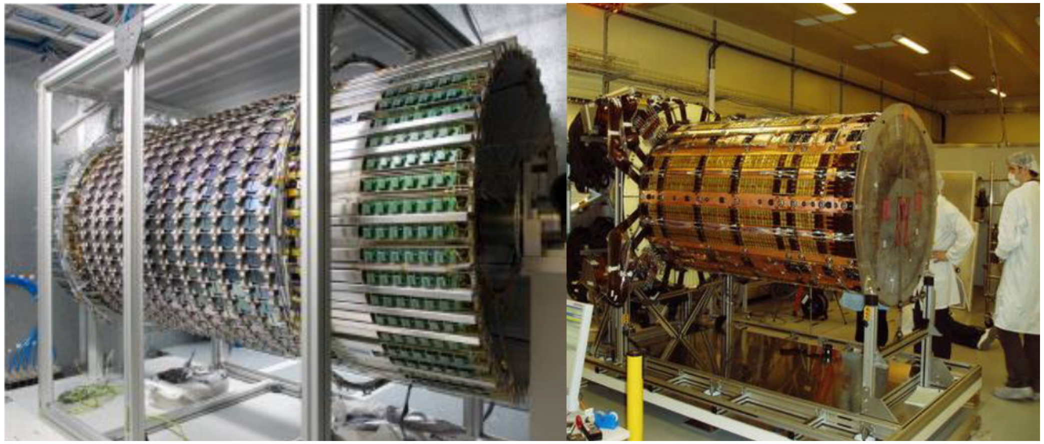
Silicon Detectors in HEP

Silicon detectors are a cornerstone of High Energy Physics

Larger fractions of detectors are made with silicon

- Limiting factor is often the cost
- More layers for precise tracking
- shift toward high precision silicon calorimeters
- no reason not to make the entire detector out of silicon other than cost



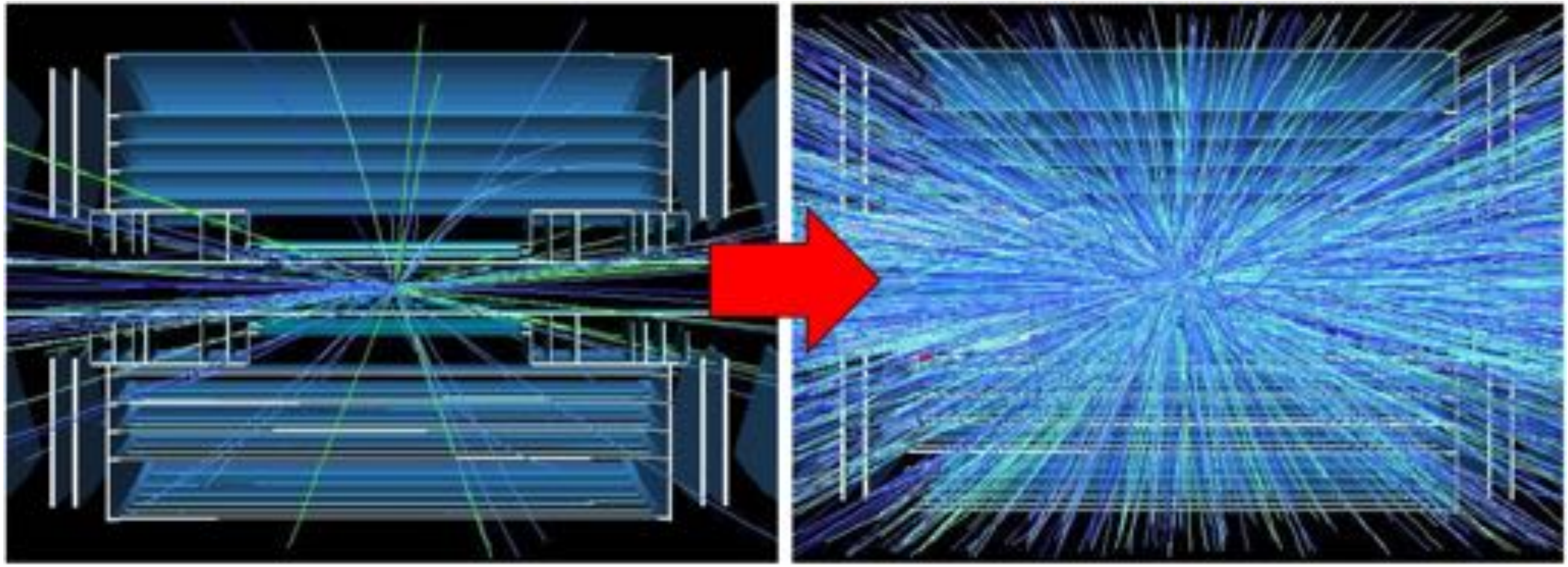


Design Challenges

High Luminosity

- enable more data, more science
- more interactions per event
- HL-LHC: average 200 interactions per event
- creates more challenges for the detector
  - radiation tolerance

Other Challenges/ Optimizations for other applications



$\langle\mu\rangle = 20$

$\langle\mu\rangle = 200$

Technology Requirements

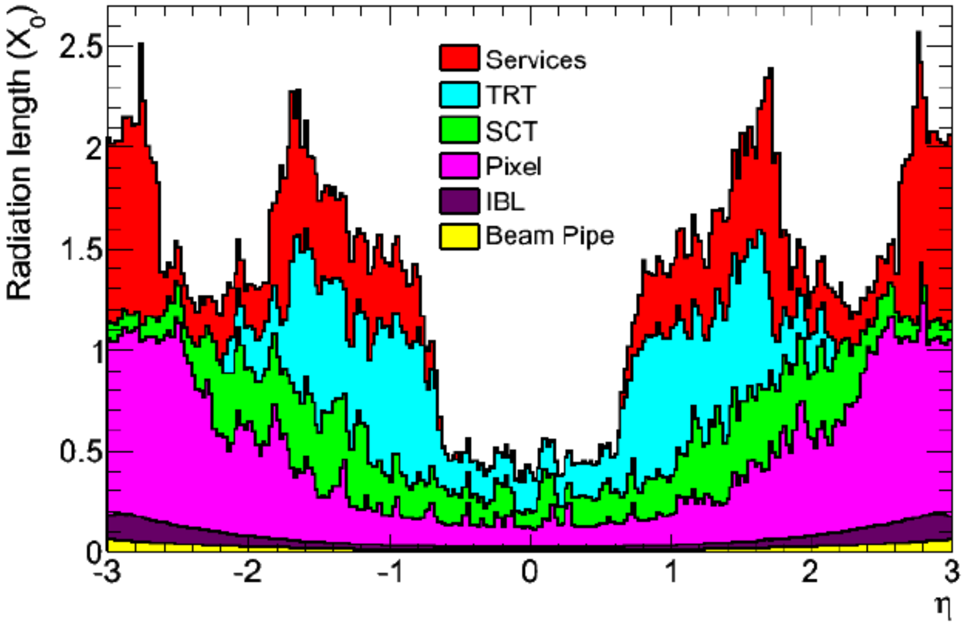
Requirements for future silicon detectors:

- high granularity for precision tracking
- shorter radiation length
- faster timing
    - 10 ps timing
        - interaction vertex identification
        - particle ID discrimination in calorimeters
- radiation tolerance
- reduce cost

⇒ Monolithic devices

⇒ Vertical Integration

⇒ Fast 'amplification' devices



Goals at Argonne

Goals:
Build a platform for a silicon R&D program honed toward achieving better performance at reduced cost for the next generation of HEP experiments.

Technologies:

- HVCMOS
  - fast timing
  - reduce costs

- 3D Vertical Integration
  - Reduce mass
  - Reduce complexity of assembly

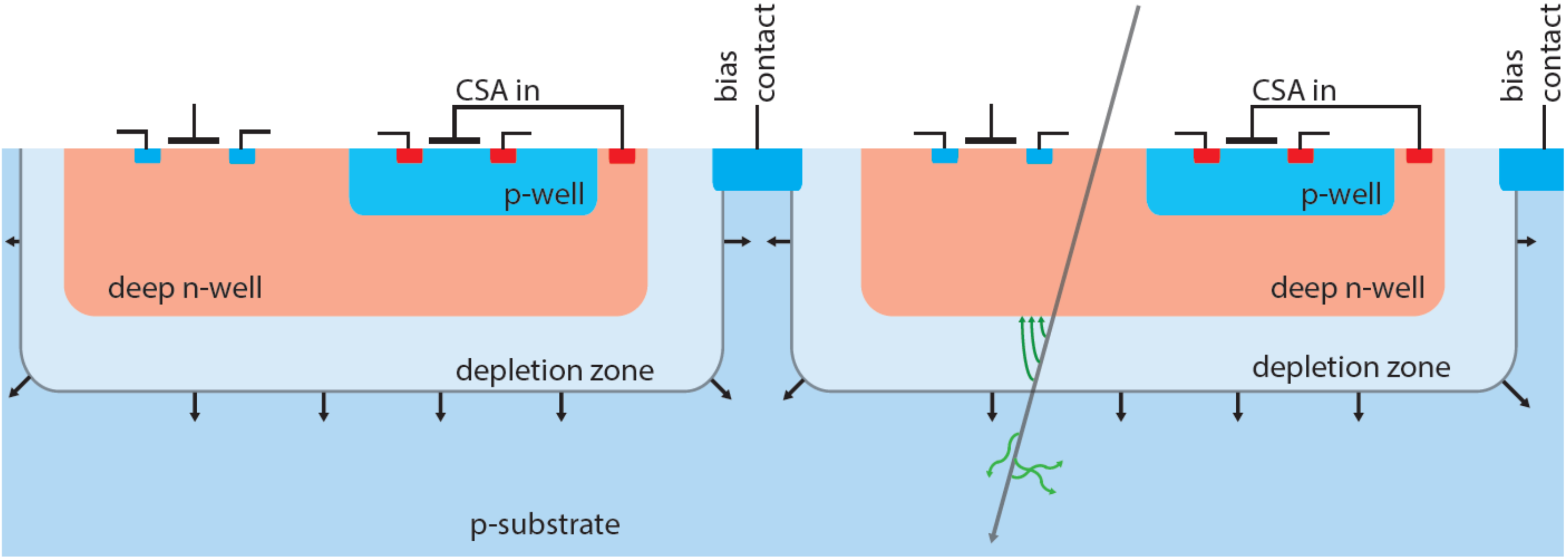
HVCMOS MAPS + Fast Timing + 3D Vertical Integration =

The Future…

HVCMOS MAPS

HVCMOS MAPS
(high voltage complimentary metal oxide semiconductor monolithic active pixel sensor)

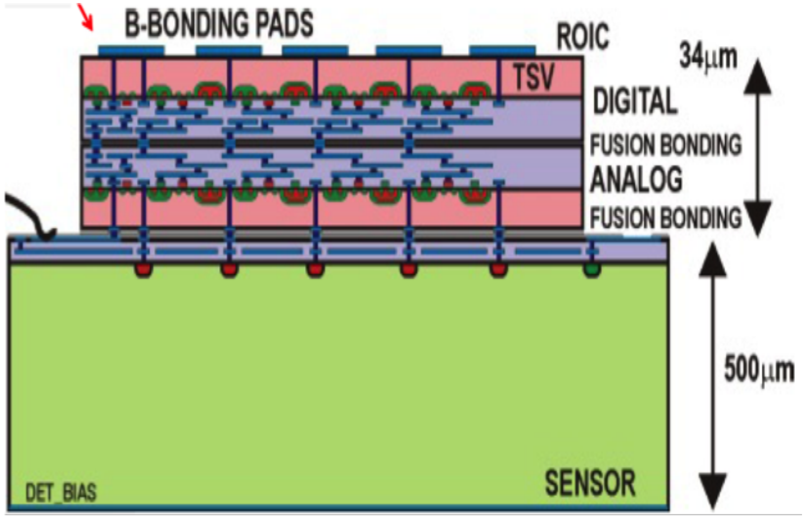
- Less expensive by x2 than traditional silicon sensors
  - Integrated sensor + signal amplification
  - Use commercially available CMOS processing with a few modifications
    - Deep n-well to isolate on-pixel electronics
    - high resistivity substrates for high voltage without breakdown
- Timing is currently ~1-100 ns



3D Silicon: Vertical Integration

3D Silicon: Vertical Integration

- stack multiple wafers and use vertical interconnects
- pixelated readout
- reduce mass
- reduce capacitance for lower noise
- eventually may eliminate bump bonding
  - reduce cost



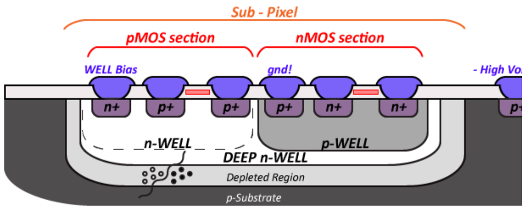
Three-tier Stack

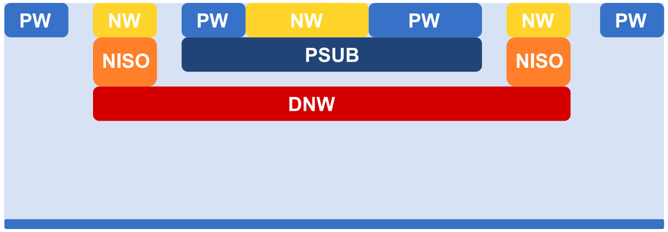
VIP chip

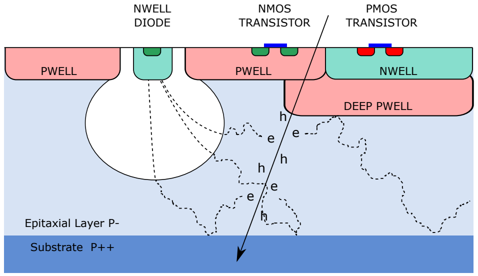
- demonstrator for ILC vertex read-out
- Argonne/Fermilab effort under US-Japan agreement
- successful readout of all 36,864 pixels

Silicon R&D

ATLAS Pixel HVCMOS/MAPS devices under investigation:





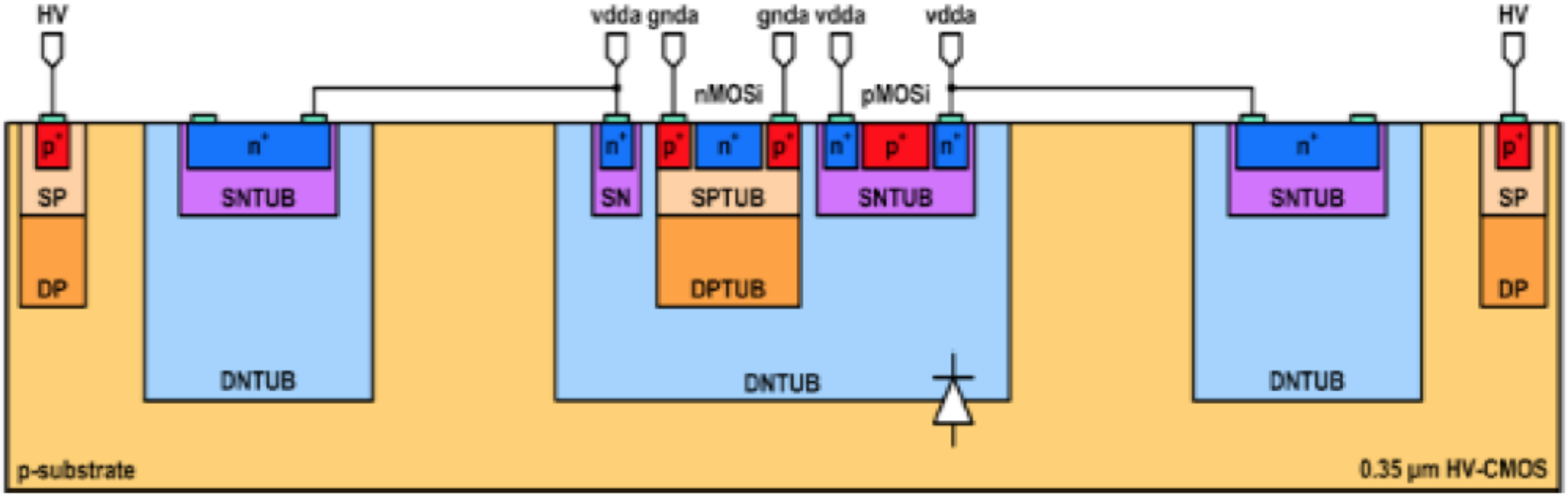


	AMS 0.18 HV	LF 150nm	TowerJazz 180nm
HV	<100V	<120V	<5V
HR substrate	1kohm/cm	2kohm/cm	1kohm/cm epi
Full CMOS	No (triple well)	Yes	Yes
Metal Layers	6	7	6
Max Depletion width	~95um@100V (70um@50V)	~140um@120V (70um@25V)	~25um@5V (~epi layer)
Collection Time	Fast (thinned to 95um)	Fast (thinned to 140um)	Fast (thinned to 25um)
Capacitance 50x50um (educated guess)	~100fF	~150fF	~2fF
MIP conversion	~7500e^-	~11000e^-	~2000e^-
Noise required for (S/N=50)	150e^-	220e^-	40e^-
Backside Processing	No	Yes	Yes
Stitching	No	Yes	Yes

Silicon R&D

Still an opportunity to join ATLAS HVCMOS/MAPS pixel effort

- Invited to join ‘AMS’ design
  - This design still requires bump-bonding to RD53 front-end readout ASIC
  - Contribute to gamma irradiations (only ones)
  - Use Felix compatible Caribou readout system
  - Provide assembly of new samples
  - ‘Demonstrator’ samples currently available
  - AMS18 samples will be available this fall
    - Can contribute to cost of run ~next month at ~$10-20k for ownership



Silicon R&D

LFoundry run:

- RD50 group at CERN is proposing a common run on HVCMOS at Lfoundry
- Can request basic components and circuits to compliment irradiation studies
  - Transistors, resistors, capacitors
  - Simple circuits

HV CMOS

Opportunity

- Join high profile collaboration
- Provide unique measurement feedback
- Potential to get funds through SBIR

Strengths

- High priority for DOE HEP
- Large number of experiments it can impact
- Monolithic design
- Lower cost than traditional silicon

Weaknesses

- Competitive collaboration to 'make our mark'

Threats

- Competitive collaboration to 'make our mark'

HV CMOS

Need

- High volume tracking detectors
- High granularity
- Low cost

Approach

- Join current ATLAS effort
- Focus on gamma irradiation damage
- Start TCAD simulation studies
- Expand effort over time to develop an ANL design

Benefit

- Gain valuable expertise
- Collaborate with BNL, European effort
- Understand charge build-up in oxides
- Position ANL to take leading role in next detector
- Bolster pixel assembly efforts

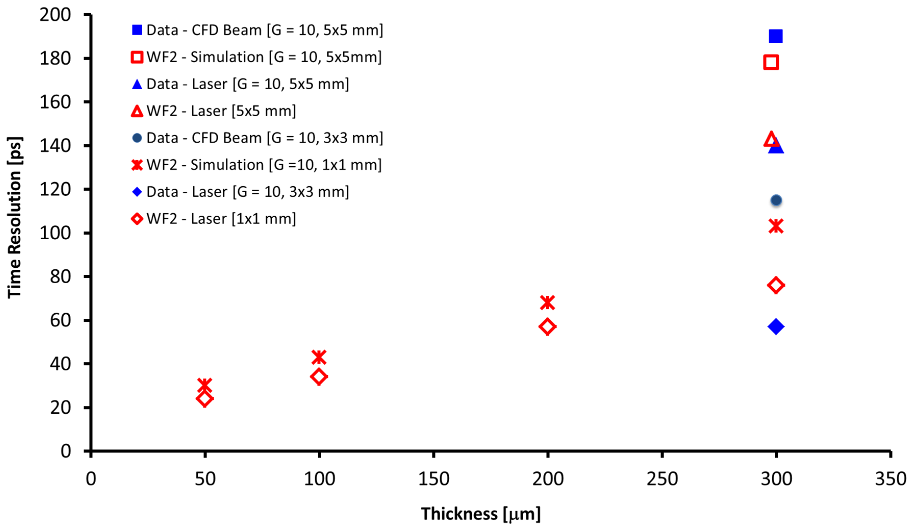
Competition

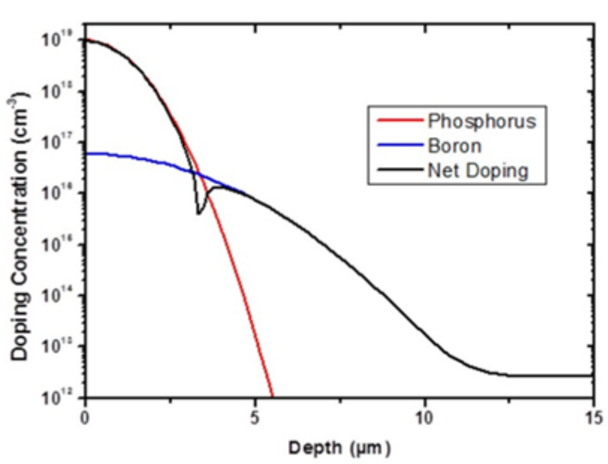
- Part of a large collaboration
- Unsure if adopted in ATLAS

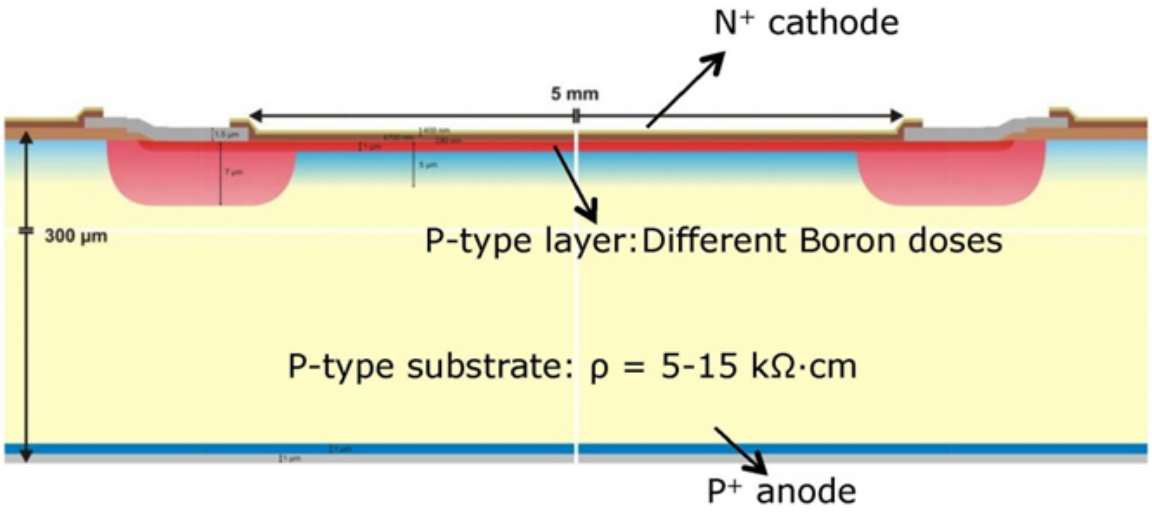
LGAD

Low Gain Amplifying Detectors (LGADs)

- rely on an amplifying region to boost collection speeds
  - thin layer of Boron or Gallium
  - modifies the electric field profile as indicated by the effective doping concentration profile
- Timing measured ~15 ps in test beam
- Not radiation tolerant due to the high reactivity of the accelerant layer





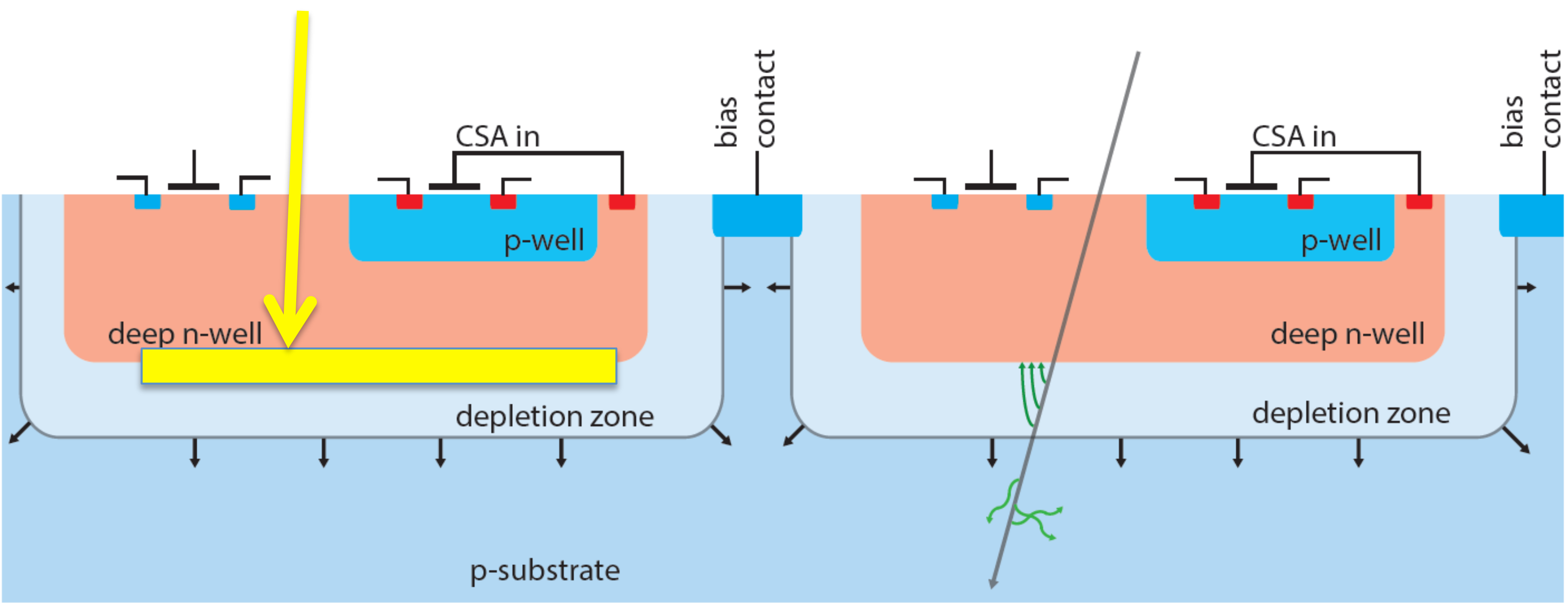


Sadrozinski, CPAD Meeting, Arlington 2015

Fast HVCMOS/MAPS

Modify HVCMOS/MAPS design to increase timing resolution

- incorporate amplification region characteristic of the LGAD sensors
- Manipulate geometries: thinner sensors, collection wells, applied bias, etc.



Add a boron layer similar to LGAD

LGAD

Opportunity

- New, emerging technology
- Unprecedented timing resolution for silicon trackers
- Contribute to understanding radiation damage mechanism
- Opportunity to move toward smaller pixels, monolithic design

Strengths

- 15 ps timing resolution achieved in test beams

Weaknesses

- Only in pad detector so far
- Not as radiation tolerant

Threats

- Groups are quickly gaining interest

LGAD

Need

- High volume tracking detectors
- High density tracking environments benefit from pileup rejection, impact parameter, b-tagging, etc.

Approach

- Join current UCSC effort
- Focus on irradiation damage?
- Start TCAD simulation studies
- Expand effort over time to develop an ANL design

Benefit

- Add time dimension to experimental tracking data
- Gain expertise in fast timing
- Potential to combine with HVCMOS effort for truly unique contribution in silicon

Competition

- Already emerging technology
- Part of a medium collaboration

TCAD Simulation

1. Simulate an HVCMOS sensor
    - Use APS experience to accelerate initiating TCAD simulations
    - Use APS Sylvaco TCAD license
2. get precise agreement between simulation and micro/macro characterization measurements
    - Use MSD and nanoscience experience for more accurate and complete characterization of materials for input to simulation
        - Identify crystalline properties: defects, trapping centers, doping concentrations, mobilities, etc.
3. Gain enough understanding to modify design for faster signal collection
    - Boost charge collection
    - Thinner sensors
    - Amplification regions
    - Optimize electric field profile
        - Reduce breakdown voltage
4. 3D: test bench and test beam measurements to evaluate performance

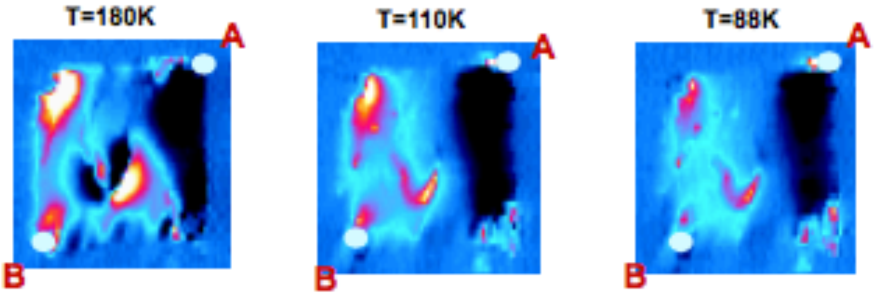
Experience at Argonne

Multidisciplinary approach to silicon detector research:

Material Science Division (MSD):

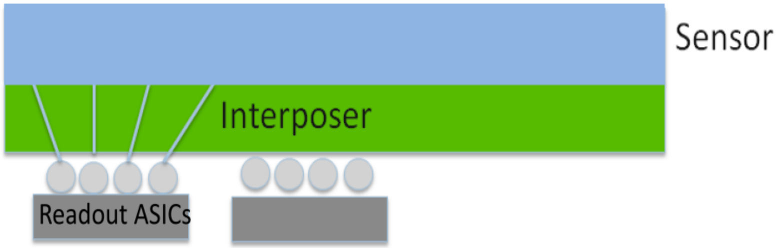
- Scanning Laser Microscopy
  - defect characterization
    - inclusions, strain, damage, twin bound., bandgap and doping variations, dislocation clusters, precipitates , stacking faults
- Scanning electron microscope
  - topography, composition, etc.

=> Input into simulations for better design



Advanced Photon Source (APS):

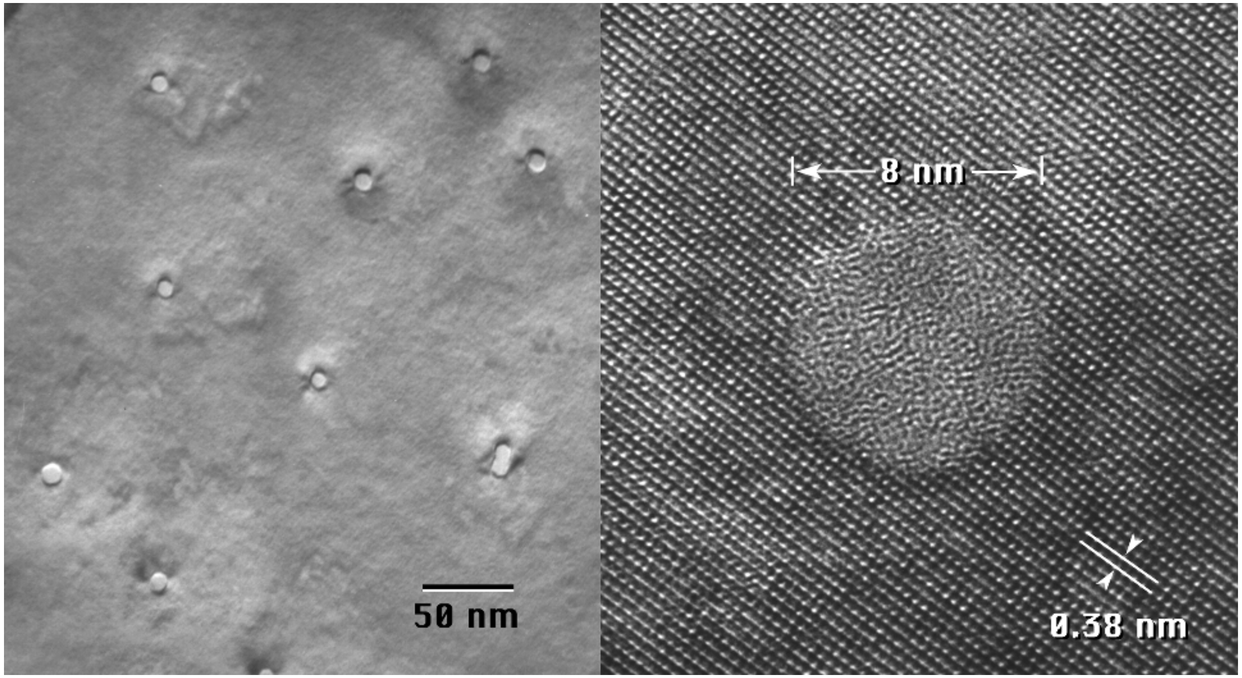
- TCAD silicon sensor device simulation (FASPAX)
- Vertically integrated sensors
  - VIPIC with interposer layer



Device Characterization

Understanding material properties better to provide input for simulations and smart design

- requires new tools; or new application of tools in other fields
- Use electron microscopy techniques in ANL MSD
- Image of radiation damage where lattice was struck
    - Changes effective doping concentration on a macroscopic scale
    - Better understand charge trapping, surface effects, etc.
- Could lead to super computer simulations of device structure and radiation response



Device Characterization Techniques

Opportunity

- Leverage expertise in MSD to better characterize irradiation damage
- Develop new tools for evaluation

Strengths

- Compliments potential HV CMOS and/or LGAD efforts
- Enable smarter future sensor designs
- Allow ANL to become world leaders in this area

Weaknesses

- Not a new technology on its own

Threats

Device Characterization Techniques

Need

- Need to understand radiation damage mechanisms for LGAD and HVCMOS/monolithic designs

Approach

- Collaborate with MSD to use electron microscopy and other techniques to look at irradiated samples
- Develop in-situ techniques during irradiation

Benefit

- Provide critical feedback for TCAD simulations of radiation damage in sensors
- Enhance understanding of basic science of irradiated materials

Competition

- Some spectroscopic techniques to identify trapping defects are already used by RD50 collaboration

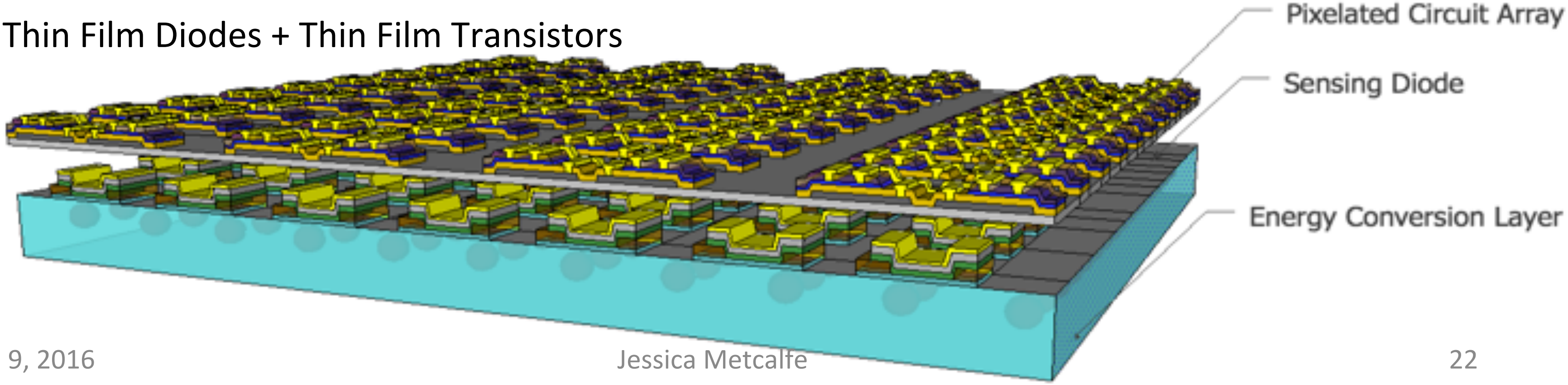
Thin Film Detectors

What's Next?

- Gain a greater understanding of sensor design with respect to material composition
- Make adjustments to that design
- Next Step: move toward Thin Film Detectors
- Challenge due to constraints from fabrication, but different constraints than traditional silicon
- Open the door for large area pixel sensors, material tailored for type of particle detection and energy range of particles, can be very inexpensive, low radiation length….

Thin Films: thin layers of materials ranging from nm to µm

- Current popular applications
  - solar cells
  - LCD screens
- Thin Films for Particle Detectors:
  - Thin Film Diodes + Thin Film Transistors



Thin Film Detectors

Thin Film (TF) Fabrication

Can do at CNM

- Thin Films can be fabricated using
  - chemical bath deposition
  - close-space sublimation
  - Crystals are grown in thin layers on a substrate with high precision
  - Compare to traditional silicon that relies on growing a large crystal and then drilling, etching, etc.
- TF's can be grown at least 200 μm thick
- TF fabrication is much less expensive
  - < \$10 per m^2 for a 2.5 μm thick CdTe film
- TF can be deposited on flexible substrates such as organic polymers and plastics

- Explore the possibility of 3D printing sensors
- ANL also has expertise in the design of the smallest thin film transistors

Thin Film Detectors

Thin Film techniques can be done with a wide variety of substrates. Only a few are standard material for HEP experiments, with silicon being the most widely used.

Material	Z	Density [g/cm^3]	Radiation length [mm]	Bandgap [eV]	Energy per e–h pair [eV]	Intrinsic resistivity [Ωcm]	Electron mobility [cm^2/(Vs)]	Hole mobility [cm^2/(Vs)]	Electron lifetime [s]	Hole lifetime [s]
Si	14	2.33	93.6	1.12	3.62	320′000	1450	450	10^{-4}	10^{-4}
Ge	32	5.32	23	0.66 at 77 K	2.9 at 77 K	50	36000 at 77 K	42000 at 77 K	10^{-4}	10^{-4}
InP	49/15	4.97		1.35	4.2	$\approx 10^7$	4600	150		
GaAs (bulk)	31/33	5.32	23.5	1.424	4.2	$3.3\ 10^8$	>8000	400	10^{-8}	10^{-9}
CdTe	48/52	6.2	14.7	1.4	4.4	$\approx 10^9$	1000	80	10^{-6}	10^{-6}
$Cd_{0.8}Zn_{0.2}Te$	48/30/52	6		1.6	4.7	$\approx 10^{11}$	1350	120	10^{-6}	$2\ 10^{-7}$
HgI	80/53	6.4	11.8	2.13	4.3	$\approx 10^{13}$	100	4	$7\ 10^{-6}$	$3\ 10^{-6}$
Diamond	6	3.5	122	5.5	13	$>10^{11}$	1800	1200		
a-selenium	34	4.27	29		6–8					

What other materials might work??

Thin Film Detectors

Material	Z	ρ (g/cm^3)	$\frac{-dE}{dx}$ [MeV/(g/cm^2)]	MIP in 10μm (keV)	E_i (eV)	$< N_{e-h\ pairs} >$ in 10 μm
B	5	2.370	1.623	3.85		
Diamond	6	3.51	1.78	6.25	13	0.5k
Si	14	2.329	1.664	3.9	3.62	1.1k
S	16	2.00	1.652	3.30	6.64*	0.5k
Zn	30	7.133	1.411	10.06	8.1*	1.2k
Ga	31	5.904	1.379	8.14		
Ge	32	5.323	1.370	7.29	2.96	2.5k
As	33	5.730	1.370	7.85		
Cd	48	8.650	1.277	11.05		
I	53	4.930	1.263	6.23		
Pb	82	11.350	1.122	12.73		
CdTe	50	6.2	1.26	7.81	4.43	1.8k
CdS	32	4.8	4.0*	19.08	6.49*	2.9k
PbS	49	7.6	6.2*	46.8	1.98*	23.6k
ZnO	19	5.6	4.4*	24.8	8.25*	3.0k
GaAs	32	5.32	1.4	7.45	4.2	1.8k
InP	32	4.97	4.0*	20.5	4.2	4.8k
HgI	66.5	6.4	5.6*	35.8	4.3	8.3k
InSb	50	5.78	4.9*	28.1	1.57*	17.9k
InAs	41	5.67	4.7*	26.8	1.94*	13.8k
HgTe	66	8.1	6.7*	54.7		
CdZnTe	43.3	6	5.0*	29.8	4.7	6.3k
IGZO	29.5	6			7.58*	

Material	$\mu_e \left(\frac{cm^2}{V \cdot s}\right)$	$\mu_h \left(\frac{cm^2}{V \cdot s}\right)$
Diamond	1800	1200
Si	1350	480
CdTe	1050	100
CdS	340	50
PbS	600	700
ZnO	130	
IGZO	15	0.1
GaAs	8000	400
InP	4600	150
HgI	100	4
InSb	78000	750
InAs	33000	460
HgTe	22000	100
CdZnTe	1350	120

Thin Film Detectors

Opportunity

- Opportunity for ANL to pioneer a new detector technology with potentially a very broad range of applications
- Advance basic science

Strengths

- Leverage CNM, MSD
- Nanoscience division already works on world's smallest thin film transistor

Weaknesses

- No guarantee of success
- Collection times may be slower
- Radiation damage properties are unknown

Threats

- Another group takes the lead before ANL

Thin Film Detectors

Need

- Large area tracking detector
- Very low cost
- Photon detector
- Neutron detector for national security

Approach

- Leverage expertise in Nanoscience division and MSD
- Produce TCAD simulations
- Make initial samples at CNM
- Device characterization

Benefit

- Completely new detector technology with broad range of potential applications

Competition

- UT Dallas has program for neutron detectors
- UK-Mexico grant was awarded
- (these are current collaborators, but we can't afford to wait forever)

3D Printing

Jimmy’s idea:
Use ANL’s Additive Manufacturing initiative to integrate services such as high/low voltage and data transmission in a printed carbon fiber structure to serve as the support structure in HEP experiments.

Backup

Silicon Detector Proposal for ANL

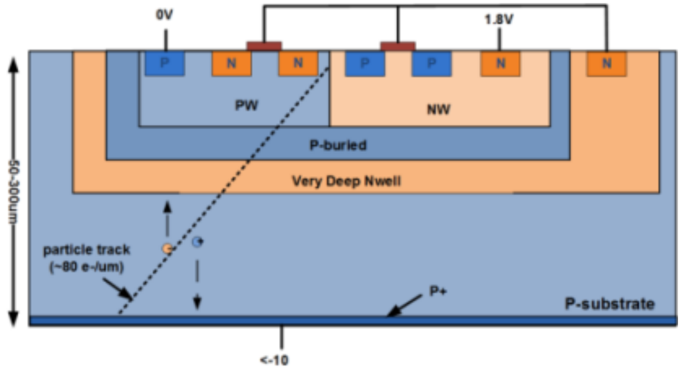
R&D approach:

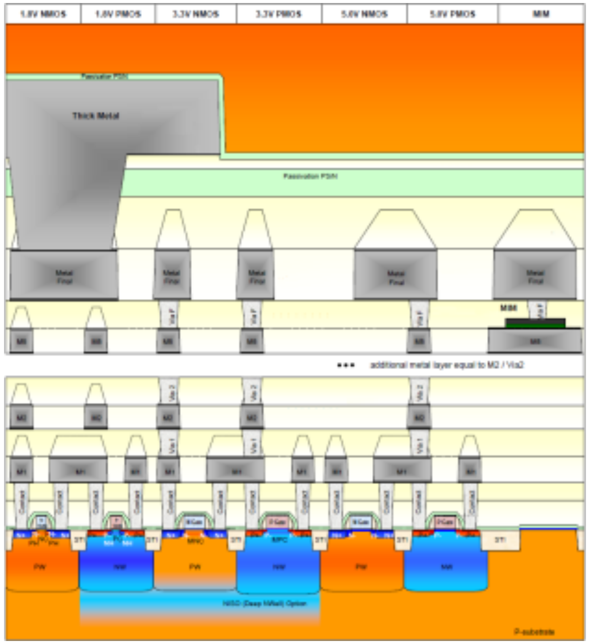
- strive for more intelligent silicon detector design
- enabled by recently available accurate simulations of semiconductor devices and radiation effects
- reduce R&D fabrication costs by needing fewer design iterations (wafer runs)

- aim for faster, cheaper silicon sensors while maintaining performance efficiency
  - propose to test 3D vertically integrated sensors
    - reduce radiation length
    - reduce costly assembly steps (bump bonding)
  - propose to research HVCMOS MAPS
      - inherently less expensive due to more commercialized fabrication
      - built-in pixel amplifications
    - propose to leverage experience in MSD to create more accurate simulations
      - more thorough material characterization
    - propose to capitalize on experience at the APS in TCAD simulations
    - propose to coordinate our efforts with Brookhaven for a more effective US program
  - ultimate goal: combine HVCMOS MAPS with vertical read-out integration for next generation of experiments

LFoundry LF150

UPDATE: CMOS MAPS design with full digital architecture (MonoPix) underway at Bonn





LFA150:

- L-Foundry 150 nm process (deep N-well/P-well)
- Up to 7 metal layers
- Resistivity of wafer: >2000 Ω·cm
- Small implant customization
- Backside processing

CCPD_LF prototype:

- Pixel size: 33um x 125 um (6 pix =2 pix of FEI4)
- Chip size: 5 mm x 5 mm (24 x 114 pix)
- Bondable to FEI4
- 300um and 100um version
- Bonn + CCPM +KIT

Room for improvement, but not great innovation…

Silicon R&D

Silicon Innovation Opportunities at ANL:

- Bump-bonding alternatives (low priority now)
- **Microscopic device characterizations for understanding radiation response (signal and damage)**
  - **In-situ measurements during irradiation**
  - **Input into TCAD simulations**
  - **Develop Innovative Tools and Techniques**
- Vertical Integration—already started by other institutions, need to look further into actual status to see if there is still room
- **Fast timing in HVCMOS/MAPS**
  - **Apply lessons from LGAD research to HVCMOS (fast timing is the basis of EIC LDRD)**
  - **Challenging but (reasonably) clear path forward: Innovative**
- **Thin Film Detectors (and 3D printed detectors) A leap forward, very innovative**