HEPiC 2017

Summary from the Workshop

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Scope of the HEPIC Workshops

- HEPIC Workshop 2017 is a workshop designed to bring together the US IC design community involved in developing integrated circuit electronics for particle physics.

- Participants from National Laboratories and Universities have an opportunity to:
  - communicate the latest activities and developments of the various groups,
  - analyze trends within the HEP design community in US and worldwide
  - evaluate design methodologies for HEP ASIC
  - review CAD/EDA tools, design kits, fabrication processes and their implications on the designs
  - speculate and make projections on new technologies.

- The workshop is meant to discuss any and all things that limit the US IC design community in HEP. To that end HEPIC focuses on the exchange of ideas on innovative circuit techniques, and serves as a forum to discuss new approaches to partnerships and the optimization of technical resources. Finally, HEPIC's unique structure stimulates investigation and promotion of feasible collaborations.

- This workshop is not meant to be redundant with existing topical conferences such as FEE, Pixel, TIPP, TWEPP, Vertex, IEEE NSS&MIC/RT or SPIE series, but instead provides a higher level overview of activities.

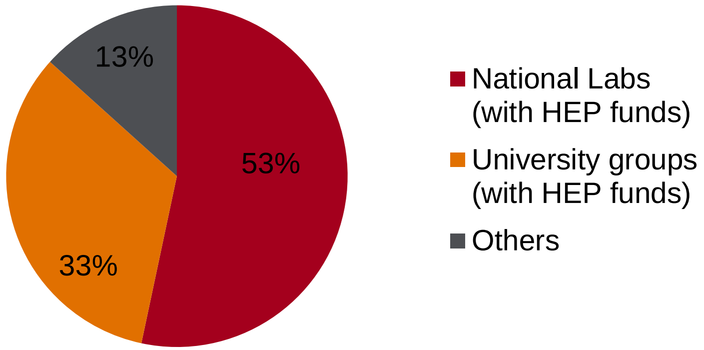
Participants

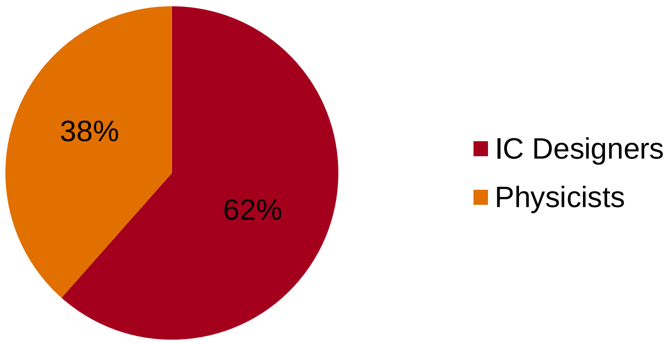
45 attendees from 15 institutions representing the majority of the HEP funded groups

National Labs:
- Argonne National Laboratory
- Brookhaven National Laboratory
- Fermi National Accelerator Laboratory
- Lawrence Berkeley National Laboratory
- SLAC National Accelerator Laboratory

US Universities:
- Columbia University
- University of Hawaii
- UC Irvine
- Michigan University
- University of Pennsylvania
- UC Santa Barbara
- UC Santa Cruz
- SMU EE Department
- SMU Physics Department
- UT Austin

Other:
- CERN, MOSIS, ClioSoft, Cadence






2017
SLAC
NATIONAL
ACCELERATOR
LABORATORY

Some background

- DOE OHEP initiated an "optimization" process for the HEP Labs
- In response HEP Labs decided to be proactive and take a closer look at the optimization of IC engineering
  - Good example of a key HEP capability where expertise is distributed among several labs and universities
- Lab POCs were identified to survey Lab IC capabilities and put together a summary
  - University capabilities need to be included as well; one of the purposes of this meeting
- Re-iterated recommendations of 2013 IC workshop

Lab IC Capability Summary

- Four HEP/multi-program DOE labs have IC groups, with a total of ~26 IC engineers
  - 9 FTE fully supported by HEP funds in 2017 (for comparison CERN has a flow of 40-45 ASIC designers working some fraction of time during a year)
  - Significant "work for others" activity (BES, NNSA, etc)
  - Highly leveraged capability; CAD tool costs distributed
  - HEP demand is on a rise from a local minimum starting from 2017

- In-house IC engineering has many advantages over outside contractors
  - Strong connection to physics and experiments
  - Re-use of building blocks by multiple projects
  - Economical relative to commercial ASIC design firms
  - Concentration of knowledge significant to HEP – e.g. extreme environments

Lab IC Capability Summary

- Overall, HEP IC designer resources are insufficient to the complexities and significance of the tasks currently projected, but distribution of skills and resources over labs appears appropriate
  - No apparent cost savings on concentrating/moving designers
    - CAD cost is per seat
  - HEP IC development is facilitated by a strong connections between physicist and engineers (moving all IC designers in one place breaks this connection)
  - FTEs funded are FTEs working on projects; FTEs are funding limited not resource limited (independent at what institution FTEs are provided by)

- Multi-program situation benefits HEP,
  - work for other fluctuates with the HEP demand,
  - skills developed in non-HEP projects are of benefit to HEP projects
  - Presence of groups that are funded exclusively by HEP does not seem to be optimal in the future
  - Now non-HEP programs provide critical mass in expertise across required areas
    - Used to be the other way around

And now the Agenda

Five sessions

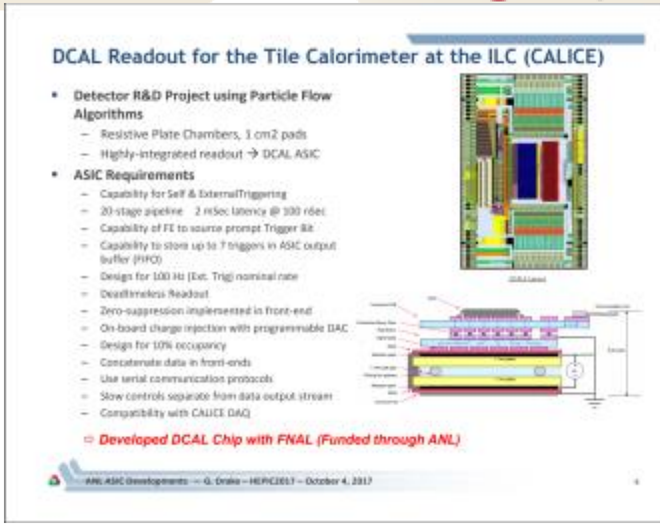
- Overview of group activities and operation models
- Collaborating between institutions (roundtable)
- New developments, trends and plans
- Collaborations and partnership with other research agencies and industry (roundtable)
- New collaborations and training initiatives (roundtable)
- HEP ASICs database (roundtable)

Detailed agenda and presentations can be found at https://conf.slac.stanford.edu/hepic2017/

Summary of groups activities (1/8)

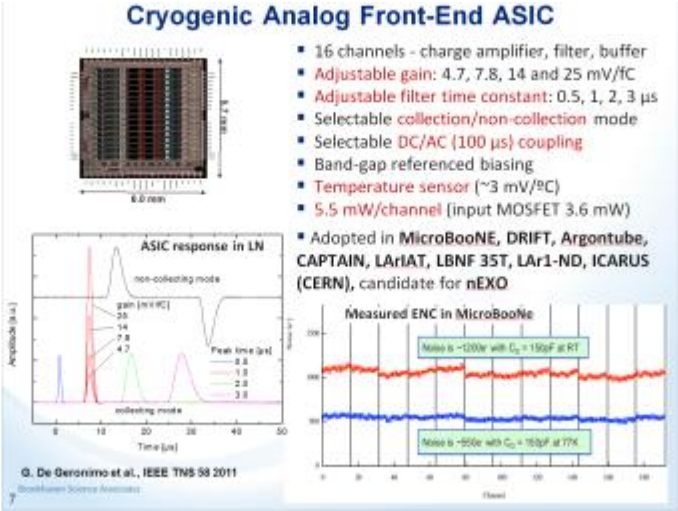
Argonne National Laboratory (Gary Drake)

- No ASIC designers
- Strong strategic partnership with FNAL ASIC group
- IC related activities in HEP and BES Photon Science
- HEP key projects: QIE for ATLAS TileCal, DCAL for tile calorimeter in ILC
- Core competences: System integration and characterization
- Used technologies: 130nm, 65nm



Brookhaven National Laboratory (Shaorui Li)

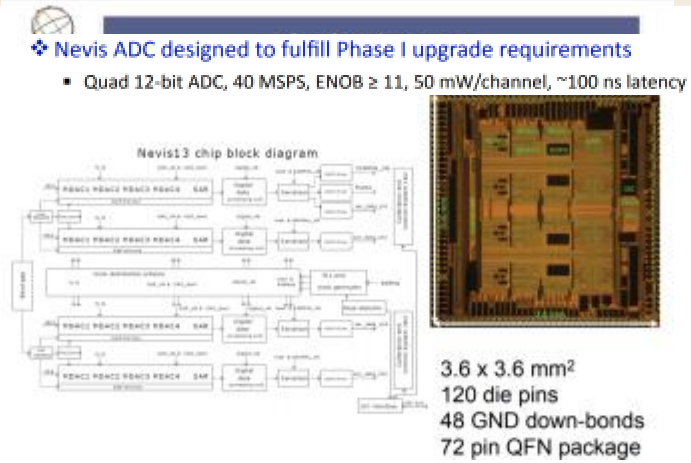
- 5 ASIC designers (2 HEP funded) + 2 PhD students (SBU)
- Collaborations with: FNAL, LBNL, UPenn, CERN, SLAC, Umich
- IC related activities in Particle and Nuclear Physics, BES Photon Science, Medical Imaging, Nonproliferation
- HEP key projects: Cold FE and Current-mode/SAR ADC ASICs for DUNE (89K), FE-SOC: ASIC for ATLAS Muon Spectrometer, HLC1 for ATLAS upgrade LAr Calorimeter
- Core competences: Low Noise Analog FE, Cold Electronics, High functionality front-end ASICs
- Used technologies: 250nm, 180nm, 130nm, 65nm



Summary of groups activities (2/8)

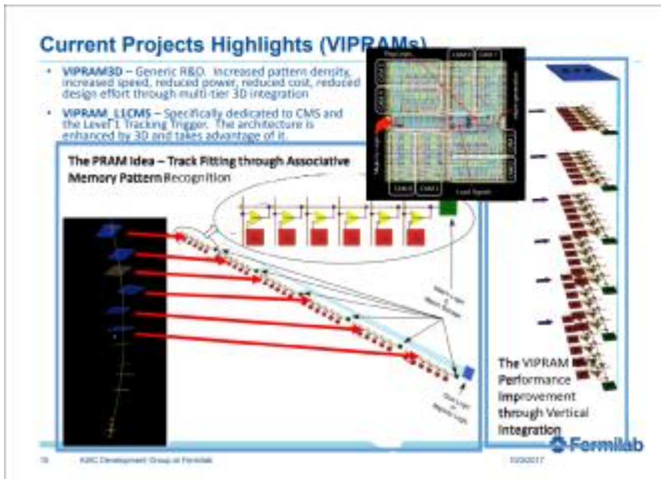
Columbia University (Gustaaf Brooijmans)

- HEP key projects: LHC, Phase-I upgrade, HL-LHC, Dune
- Core competences: ADCs, Multiplexer/serializers
- Benefit from reusing blocks developed within the CERN collaboration
- Used technologies: 130nm, 65nm



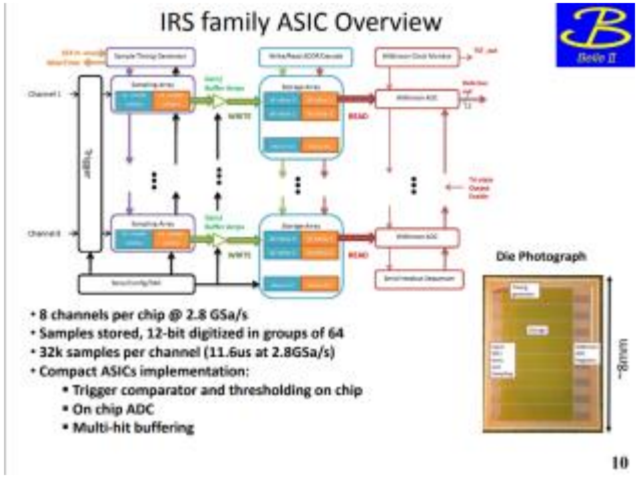
Fermilab National Laboratory (Grzegorz Deptuch)

- 7 ASIC designers (5 HEP funded)
- Collaborations with: ANL, BNL, SLAC, Southern Methodist University, UPenn, NWU, CERN, AGH-UST Krakow Poland, U. of Bergamo Italy
- IC related activities in HEP and BES Photon Science
- HEP key projects: COLDATA and ADC for Dune (89K), FanTastIC: Fast Timing Integrated Circuit for CMS forward Calorimeter, VIPRAM: VI Pattern Recognition Associate Memory, HGCal Concentrator: High Granularity Calorimeter Data Concentrator for CMS, FCP130/iFCP65 and RD53A: Fermilab CMS Pixels (RD53)
- Core competences: Large SoCs, FE ASICs, Digital-on-Top, 3D-IC, Cold Electronics, SystemVerilog and UVM verification.
- Used technologies: SiGe 350nm, 250nm, 130nm, SiGe 130nm, 65nm CIS 180/130nm, 55nm, 45/40nm



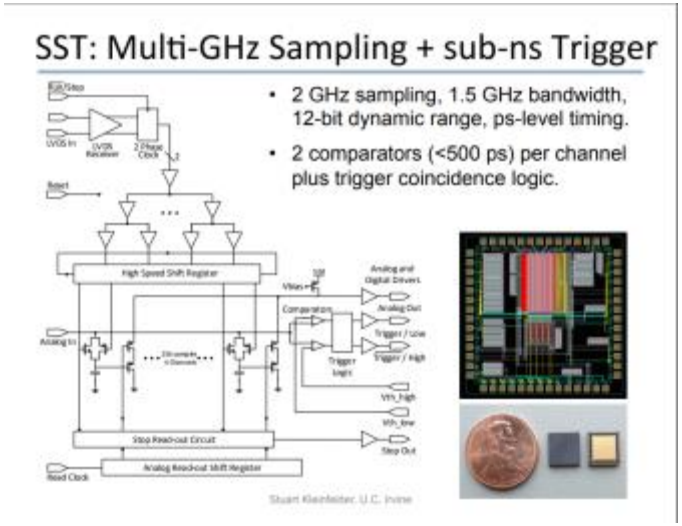
Summary of groups activities (3/8)

University of Hawaii (Gary Varner)



- Key projects: LABRADOR (UHE ν searches), IRS (ARA and Belle II iTOP), TARGET (Belle II KLM, CTA)
- Core competences: Picosecond Timing, SCA, WFS, Analog SoC
- Used technologies: 250nm, 130nm

UC Irvine (Stuart Kleinfelder)

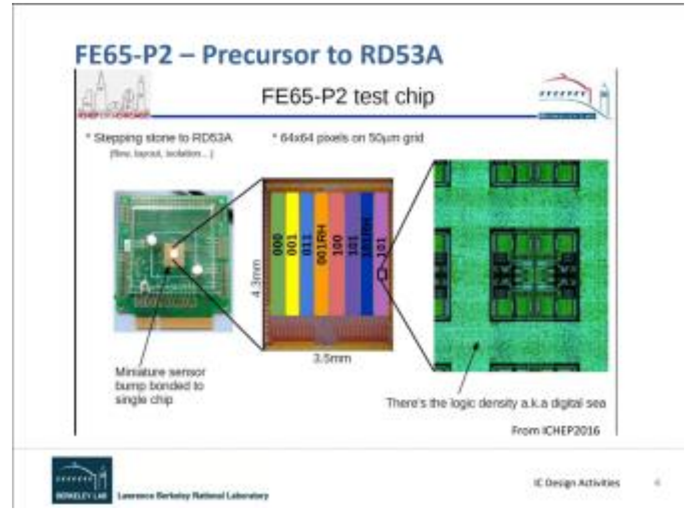


- Key projects: SST Multi-GHz Sampling +sub-ns Trigger
- Core competences: Waveform Sampling, Fast-Timing, Imaging

Summary of groups activities (4/8)

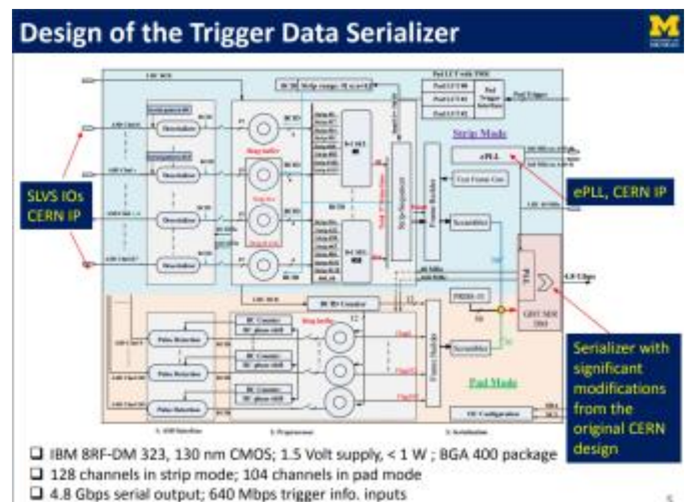
Lawrence Berkeley National Laboratory (Carl Grace)

- 5 ASIC designers (1 HEP funded)
- Collaborations with: FNAL, CERN, SLAC
- IC related activities in HEP and BES Photon Science, Neuroscience
- HEP key projects: FE65-P2 (Precursor to RD53A), RD53 (analog front ends, DRAD chip), LArPix (Cold Readout for ArgonCUBE demonstrator), cold Pipeline ADC ASIC for DUNE (89K)
- Core competences: SoCs, Image sensors, FE ASICs, Digital-on-Top, Cold Electronics
- Used technologies: 180nm, 130nm, 65nm



University of Michigan (Jinhong Wang)

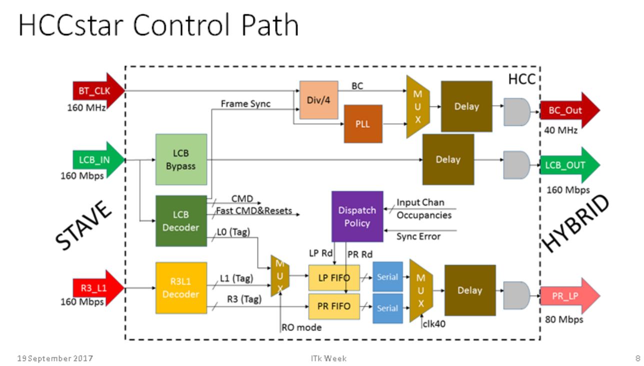
- HEP key projects: Trigger Data Serializer for the sTGC detector, Time to Digital Converter for the upgrade of the MDT electronics (Upgrade of the ATLAS Muon Spectrometer)
- Core competences: TDCs, Serializers
- Benefit from reusing blocks developed within the CERN collaboration
- Used technologies: 130nm



Summary of groups activities (5/8)

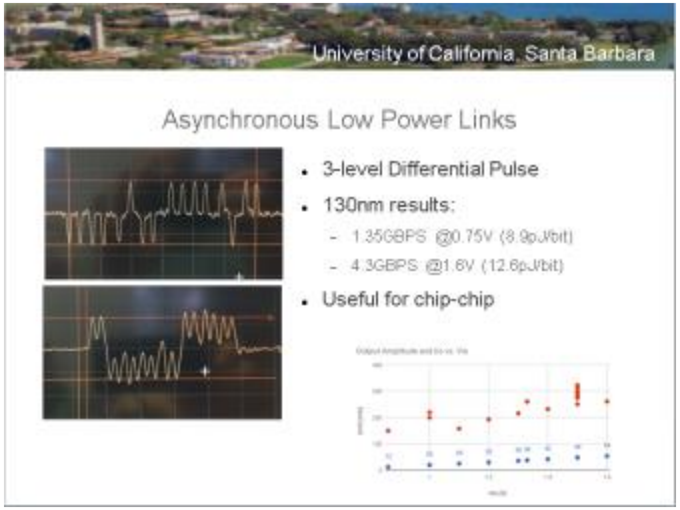
University of Pennsylvania (Mitch Newcomer)

- Collaborations with UCSC, CERN, DESY, RAL, UCL, Freiburg, Liverpool, FNAL
- HEP key projects: ATLAS Strips Upgrade (HCCstar ASIC (entire design), AMAC Autonomous Monitoring and Control ASIC (entire design), blocks to the 256 channel ABCstar front end chip.
- Previous ASICs: SNO, ASDQ(COT@CDF) , ASDBLR & DTMROC (ATLAS TRT), HCC130 (ATLAS upgrade)
- Core competences: Fast Analog FE, ADC, Drivers, Library modelling, Digital on top synthesis of A & D circuits and Place & Route capabilities
- Used technologies: 180nm SiGe, 130nm, 65nm



UC Santa Barbara (Forrest Brewer)

- IC related activities in in HEP and BES Photon Science
- HEP key projects: Rad hard Pulsed Gate Library, High Speed serial links and IOs, Asynchronous low power links, Oscillators and Clocks generators
- Core competences: Pulsed Gate High speed, low power blocks
- Used technologies: 130nm, 65nm



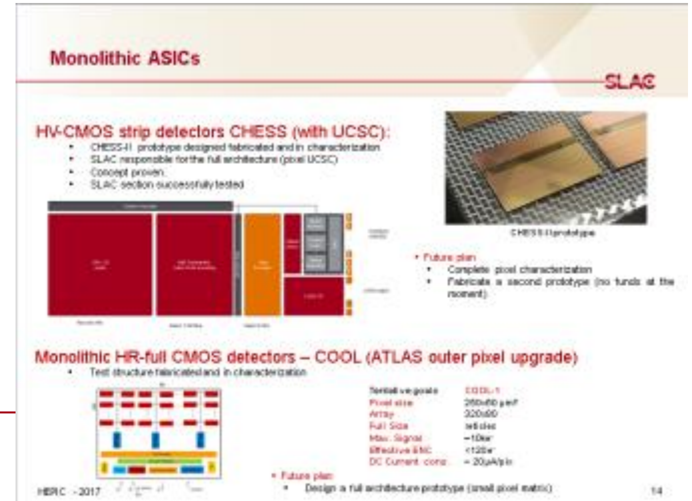
Summary of groups activities (6/8)

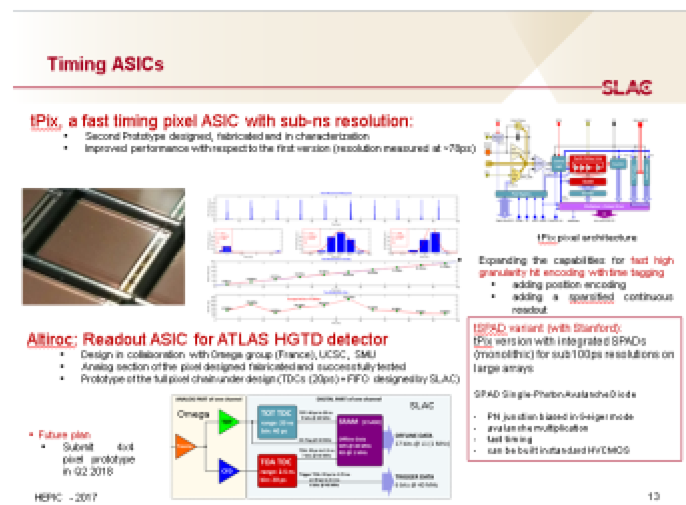
UC Santa Cruz (Herve Grabas)

- Collaborations with: SLAC, CERN,
- Benefit from reusing blocks developed within the CERN collaboration
- HEP key projects: CHESS Atlas strip, ADCstar, RD53
- Core competences: HV-CMOS FE, picosecond timing
- Used technologies: 350nm HV, 130nm, 65nm

SLAC National Accelerator Laboratory (Angelo Dragone)

- 10 ASIC designers (1 HEP funded)
- Collaborations with: Stanford EE, UCSC, UCD, University of Oregon, UTA, UNM, Bonn University, Stanford SoM, Sherbrooke, POLIBA, DESY, EuXFEL, Omega, SMU
- IC related activities in HEP and BES, Medical Imaging/Neuroscience, Industry Collaborations
- HEP key projects: HGTD: high granularity timing ASIC 20ps, CHESS and COOL: HR-MAPS R&D for ATLAS upgrade, CRYO: a waveform digitizer for cold experiments (nEXO 160K).
- Core competences: Reticle size Mixed Mode SoCs, Analog FE, Digital-on-Top, Cold Electronics, Monolithics, Integrated sensors, Precision Timing
- Used technologies: 250nm, 180nm, 180nm HV, 180nm CIS, 150nm, 130nm, 130nm HV, 130nm SiGe, 65nm, 40 nm

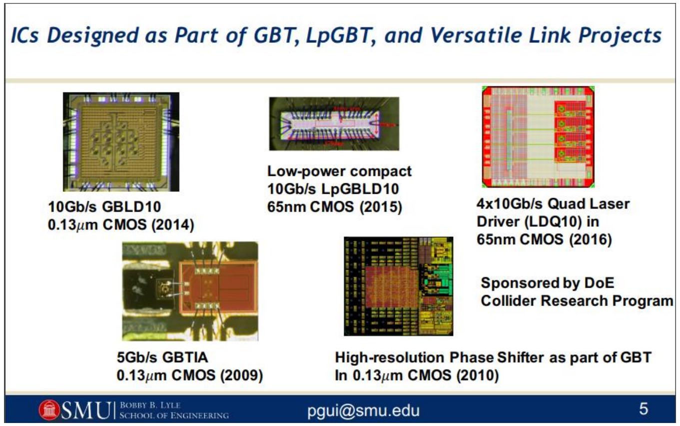




Summary of groups activities (7/8)

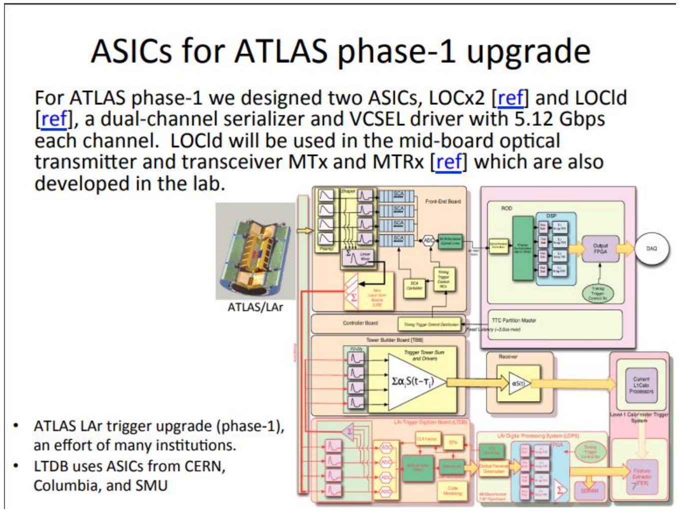
SMU – EE Department (Ping Gui)

- Collaborations with: CERN, FNAL, Industry
- IC related activities in in HEP, Biomedical, Consumer electronics
- HEP key projects: GBT, LpGBT, and Versatile Link, COLDDATA
- Key IC blocks including PLLs, VCSEL Drivers, Transimpedance Amplifiers (TIA)s, Phase Shifters, and ADCs.
- Core competences: Analog, Mixed-signal and RF blocks, Cold Electronics
- Used technologies: 130nm, 65nm, 28nm



SMU – Physics Department (Jingbo Ye)

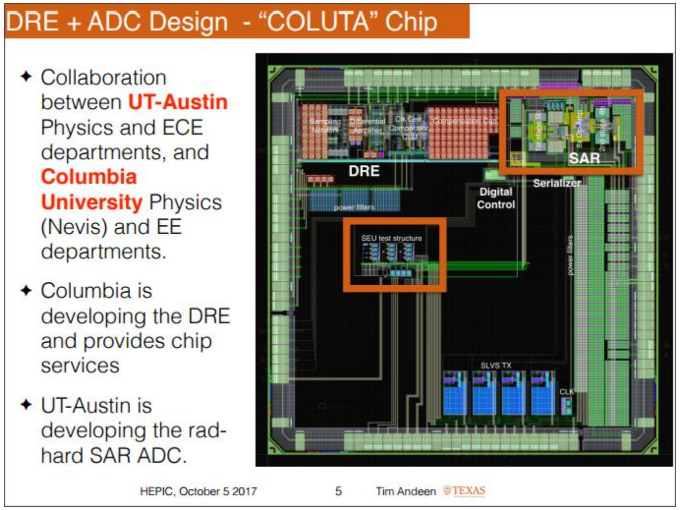
- Benefit from collaborations with: CERN, BNL, Columbia, UM, IN2P3, CCNU, Omega, SLAC
- IC related activities in in HEP
- HEP key projects: LOCx2 and LOCld, a dual-channel serializer and VCSEL driver with 5.12 Gbps, LpGBT blocks, HGTD, GCT (Gigabit CMOS Senor Transmitter) for ATLAS upgrades and future R&D
- Core competences: Ser/Des, VCSEL drivers, Phase Shifters, LVDS I/Os
- Used technologies: 250nm, 180nm CIS, 130nm, 65nm



Summary of groups activities (8/8)

UT Austin (Tim Andeen)

- Collaborations with: Columbia, UT Austin EE Dept
- HEP key projects: Electronics for LAr readout at the HL-LHC
- Core competences: ADCs,
- Used technologies: 65nm



New developments, trends and plans

HEPIC 2017

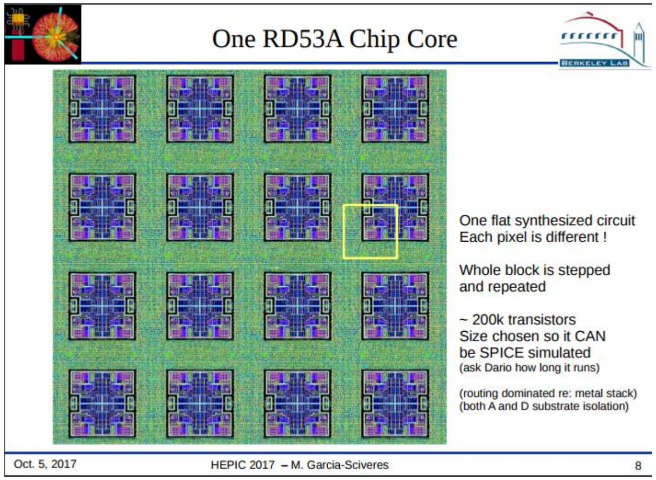
Thursday, Oct 5

8:00 AM	8:30 AM	**Registration** / *breakfast*	
8:30 AM		**New developments, trends and plans (P. O'Connor)**	
8:30 AM	8:40 AM	Introduction	P. O'Connor
8:40 AM	9:00 AM	Digital-on-top Mixed Signal Design	M. Horowitz
9:00 AM	9:20 AM	Trends in pixel readout chip designs for high rate and radiation	M. Garcia-Sciveres
9:20 AM	9:40 AM	Precision Timing in HEP experiments	G. Varner
9:40 AM	10:00 AM	Front-end in extreme conditions	S. Li
10:00 AM	10:20 AM	Rad-hard methodology and cad tools	S. Miryala
10:20 AM	10:40 AM	*Coffe Break*	
10:40 AM	11:00 AM	Advanced Interconnections between Sensors and Integrated Circuits	C. Kenney
11:00 AM	11:20 AM	3D-IC status and trends	R. Lipton
11:20 AM	11:40 AM	Content addressable memories for HEP	T. Liu
11:40 AM	12:00 PM	Information-centric analog interfaces	B. Murmann
12:00 PM	1:00 PM	*Lunch Break* / **Poster Session**	
1:00 PM	1:20 PM	Cadence: trends in CAD tools and services	M. Nizic
1:20 PM	1:40 PM	MOSIS technology Roadmap	R. Pina
1:40 PM	2:40 PM	Roundtable	
2:40 PM	3:00 PM	*Coffe Break*	
3:00 PM		**Collaborations and partnership with other research agencies and industry (A. Dragone)**	
3:00 PM	3:10 PM	Introduction (Advantages for HEP from synergies with industry)	A. Dragone
3:10 PM	3:30 PM	Working with National Labs	M. Willardson
3:30 PM	4:30 PM	Roundtable	
6:00 PM		**Social Dinner**	
		Left Bank - 635 Santa Cruz Av. Menlo Park	

Key Invited Speakers on Hot topics

Areas to invest in R&D:

- Digital-on-Top Methodologies
- System-on-Chip
- Verification
- Deeper nodes (28nm?)
- Rad-Hard for deeper nodes
- Precision Timing
- Monolithic Pixels
- Cold electronics
- 3D-ICs
- Advanced Interconnections



Findings

- Large portfolio of activities with high impact on key experiments
  - Essentially no effort duplication (unless required for risk mitigation on key projects on hard schedules)

- Efficient management of limited resources
  - Labs are more research and product-oriented than educational
  - Universities are more educational and fundamental research-oriented
  - Labs benefit from
    - Work in multiple fields (HEP, BES, Neuroscience, Collaboration with Industry)
      - IC block reuse, tools costs sharing, balance work load fluctuations
    - Large number of collaborations among complementary institutions
    - Fundamental research from universities
  - Universities benefit from
    - Collaboration with larger institutions (National Labs, CERN)
    - Access to the project hubs formed by major IC design works occurring at the Labs
    - IC blocks sharing (ex. CERN RD53 collaboration)

Findings

- Future HEP (and non HEP) experiments rely on the possibility to realize complex real-time processing at high speed, with high precision and with a large scale of parallelism. These characteristics can only be achieved using integrated circuits.

  Risks:

  - Complexity of designs is exponentially increasing with technology scaling and circuit complexity required by new functionalities. Digital-on-top methodologies are becoming a must.
  - The increase in ASIC demand is unprecedented.
  - Only large groups have sufficient critical mass and expertise to handle complex architectures.
  - Yet HEP funding is decreasing and key core competences built in several years are at risk.

Findings from the roundtables

Four roundtables focused on increasing the collaboration opportunities:

- Analyzing existing collaborating within HEP
- Analyzing collaborations and partnership with other research agencies and industry
- Exploring strategies for new collaborations and for necessary professional development
- Analyzing paths toward an HEP ICs database

- Clear recognition among groups on the benefits of increased collaboration.
  - University groups lack the mass and continuity to manage a complex large scale HEP IC product development, but can still participate significantly via collaboration with the Labs (Labs as Hubs)
  - Labs can utilize the agility and expertise present at the Universities to address needs that arrive from within the large projects and thereby share work.

- CERN RD53 Collaboration has been very successful. To export in US this model, where major laboratories works together with satellite institution toward a common goal, there are barriers that need to be lowered:
  - Foundries require common NDAs to allow access to technologies and related information
  - Library development companies require common NDAs to permit sharing of circuit designs
  - Clear and consistent guidelines on IP sharing content both internal to an external to the HEP community
  - Resources for Education and Professional Development

Recommendations from the HEPIC workshop

1. Continue to encourage the strong physicist-IC designer links in the US. This is a vital part of innovation and also important to the educational/training mission.
   - Labs are a great place where physicists and engineers work closely together
2. Provide ASIC R&D to establish knowledge in new technologies.
   - Long term benefit for future advanced developments (ex R&D on 28nm and 3D-IC)
3. Basic literacy on IC technology should be included in the education of physics students to facilitate the communication between physicists and engineers, which is especially true for analog circuits for detectors.
   - Co-develop material for courses
4. To facilitate communication among designers, hold a yearly workshop of US IC designers. Include technical training to keep up with industry developments.
   - Next year HEPIC 2018 will be at …. (soon to be announced)
   - Add training at FEE. One extra day with a deep dive on a case of study
   - Engineering class at NSS for designers
5. Investigate practical options for a designer at institute A to work a small fraction of time on a project at institute B on which institute A is not involved. This would be very helpful for load balancing.
   - Most of the labs have already available visiting position
   - More communication is required to broadcast opportunities (open positions, fellowship, internships)
6. Complete and maintain an up-to-date catalog of existing ASICs
   - A catalog of designs updated to 2013 is already available and will be updated
   - Legal barrier needs to be solved to turn the catalog into a sharable database
7. Explore the feasibility of a inter-institution organization HEPIC.ORG (need to figure out the format (LLC, etc))
   - see next slide

Key scopes

Remove Legal Barriers:

- Enable sharing of design blocks
  - Common ground for foundry NDAs (Eg. TSMC, ARM)
- Establish clear and consistent guidelines on design blocks sharing among partners
  - Acknowledgment of credits
  - Understanding of critical needs related to multi-purpose institutions

Create more opportunities for collaboration and increase communication:

- Organize yearly workshops
- Catalog of designs / Data management
- Promote Cross-institution MPWs
- Lists information on groups and projects
- Maintains a Twiki and FAQs repository
- Provide Education and Training (course material to share)
- Advertise Jobs / Fellowship opportunities
- Lists ideas for student projects

by increasing communication and lowering or removing barriers for collaboration any costs incurred by the organization will be offset by its clear benefits

Thanks to the Organizers

Local Organizing Committee

- Angelo Dragone, SLAC (Chair)
- Gunther Haller, SLAC
- Marty Breidenbach, SLAC
- Pietro Caragiulo, SLAC
- Bojan Markovic, SLAC
- Hussein Ali, SLAC
- Traci Kawakami, SLAC

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- Grzegorz Deptuch, FNAL
- Angelo Dragone, SLAC (Chair)
- Carl Grace, LBNL
- Mitch Newcomer, UPenn

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- Robert S Tschirhart, FNAL
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- Marty Breidenbach, SLAC
- Klaus Honscheid, OSU