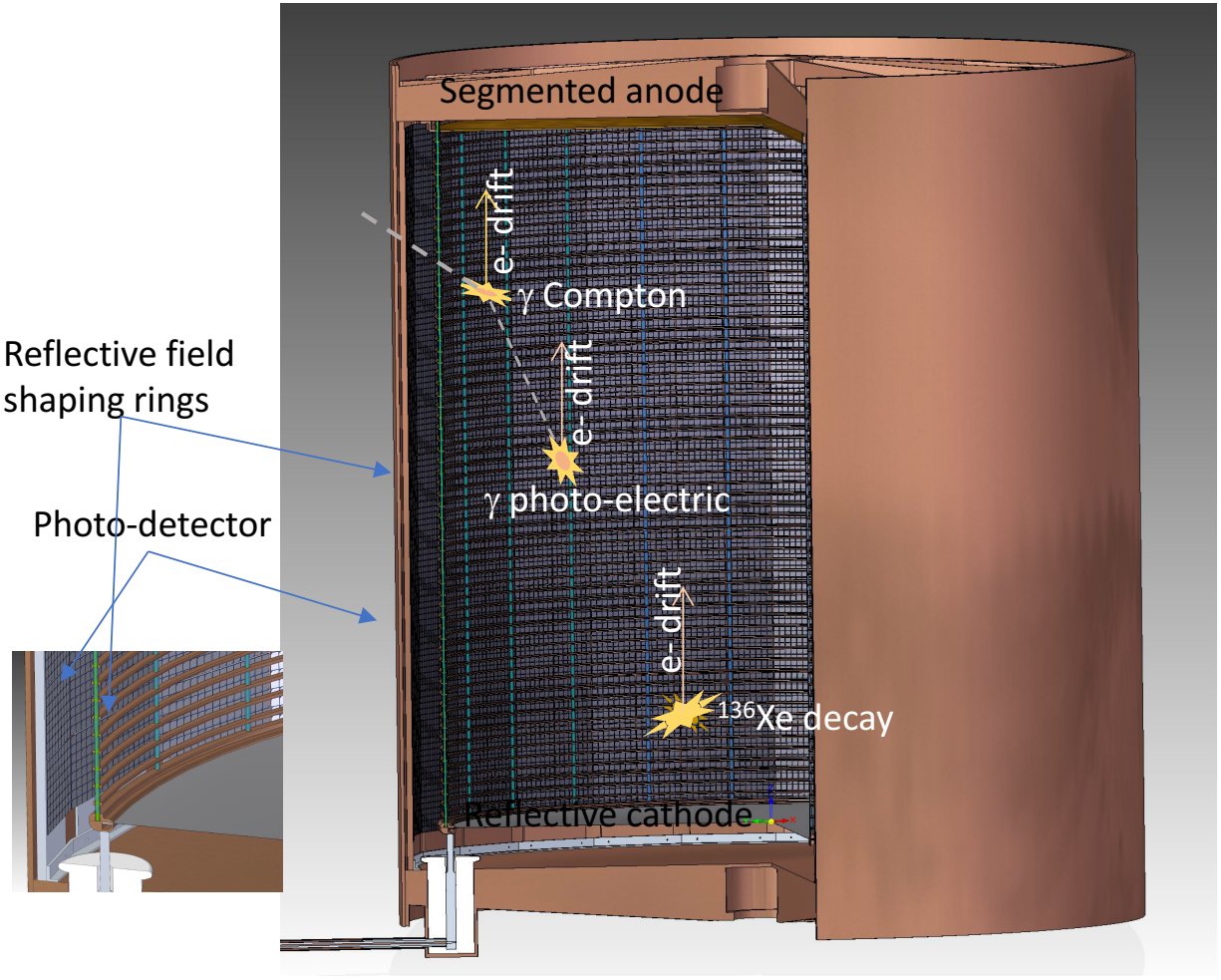
3D integrated digital SiPM

F. Retière (TRIUMF) & U. de Sherbrooke (Sherbrooke, QC) &

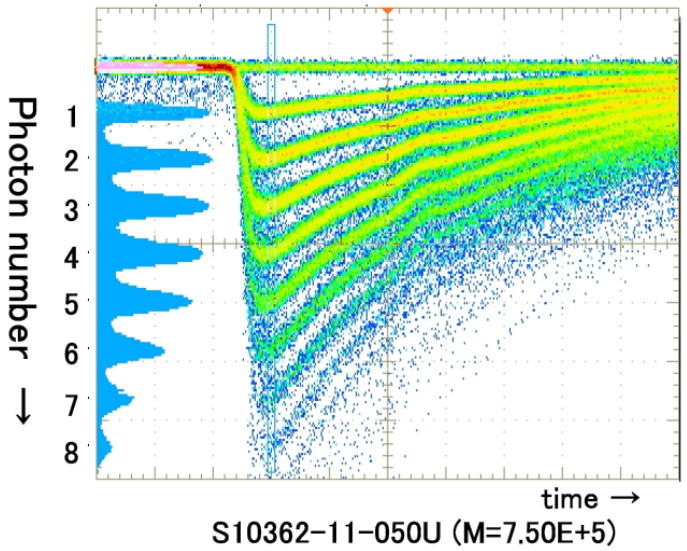
nEXO collaboration

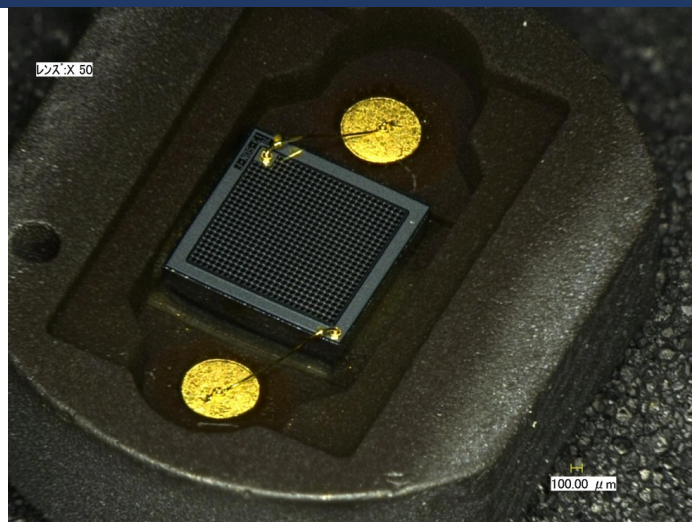
Motivation. nEXO

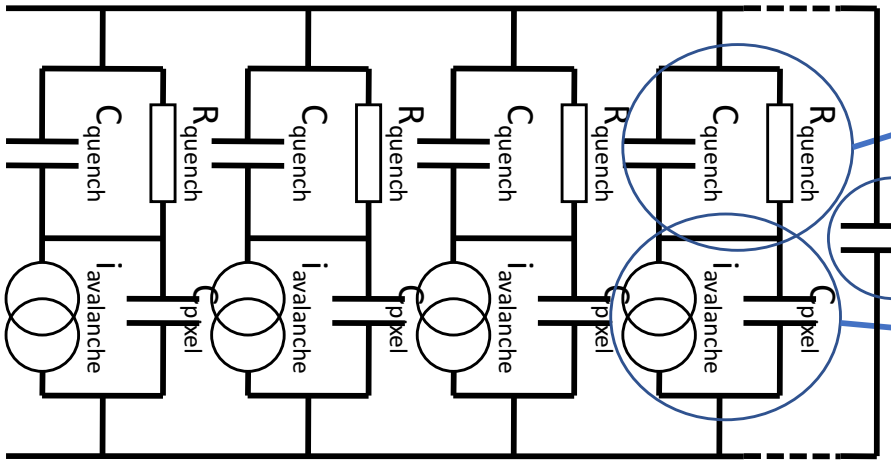
- 4-5 m^2 SiPM
  - Single VUV photon sensitive
    - >15% efficiency
  - Very low radioactivity
    - Silicon is generally very radiopure
- SiPM electronics in liquid Xenon
  - Power dissipation < 100W
  - Challenging to achieving noise < 0.1PE per channel of 1-10cm^2 because of large capacitance
    - With analog electronics need to limit bandwidth
    - **Digital SiPM promise better performance and lower power**

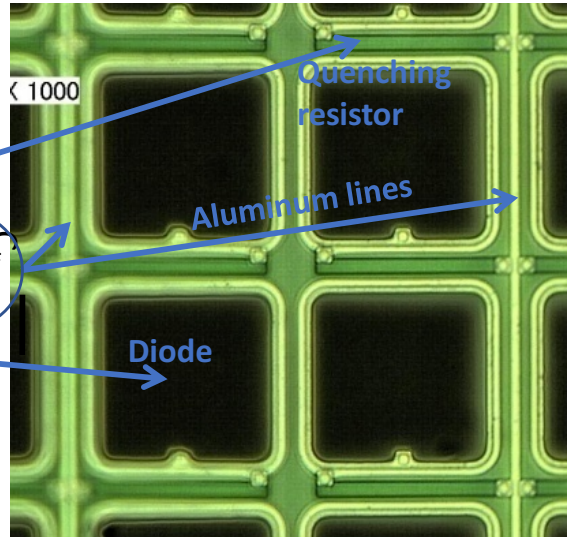


Analog Silicon Photo-multipliers







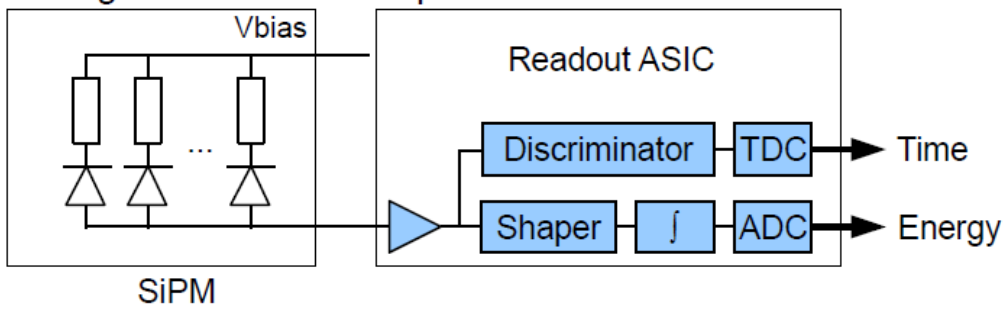


The digital SiPM concept

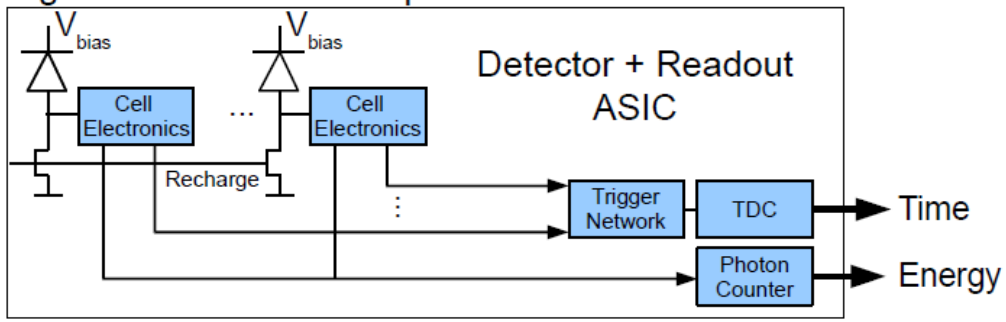
PHILIPS

Digital SiPM – The Concept

Analog Silicon Photomultiplier Detector



Digital Silicon Photomultiplier Detector



IEEE Nuclear Science Symposium / Medical Imaging Conference, Orlando, FL October 28, 2009

2009

Photon to bit conversion

- As opposed to photon to analog to bit conversion

Quenching scheme

- Current sense per diode
- Quench upon discharge
  - Control quench time
- Time tag and count the avalanche

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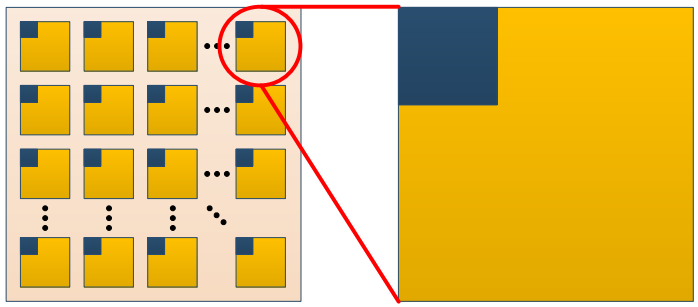
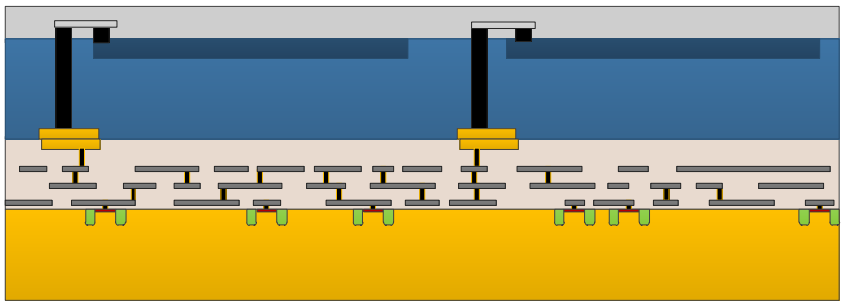
From monolithic digital SiPM to 3DdSiPM

- Monolithic issues
  - Electronics circuit limits the active area
    - Trade off between active area (1b) or performance (1c)
  - Compromise between photo-detector and electronics technology
- 3D solves most issues
- Main challenge
  - Connect each diode on photo-detector chip to quenching electronics chip



1a 1b

1c



1d

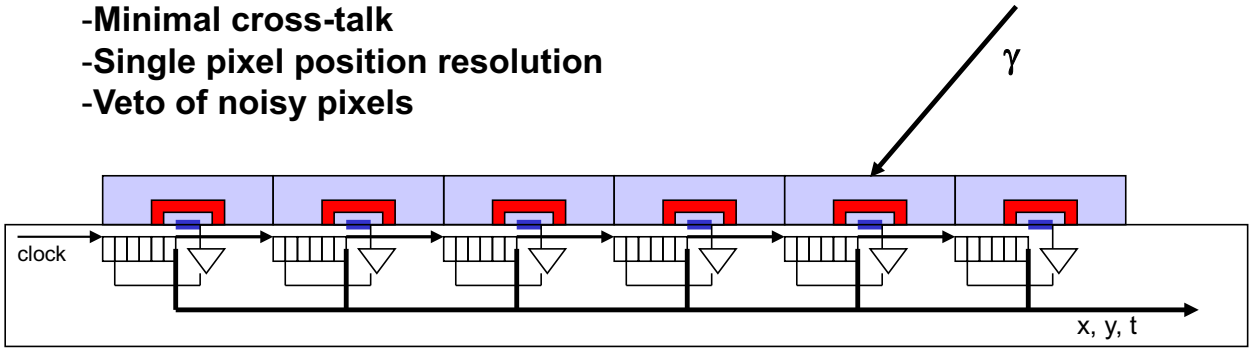
Not a new idea

H-G Moser
Max-Planck-Institute for Physics
Semiconductor Lab

Smart SiPMs

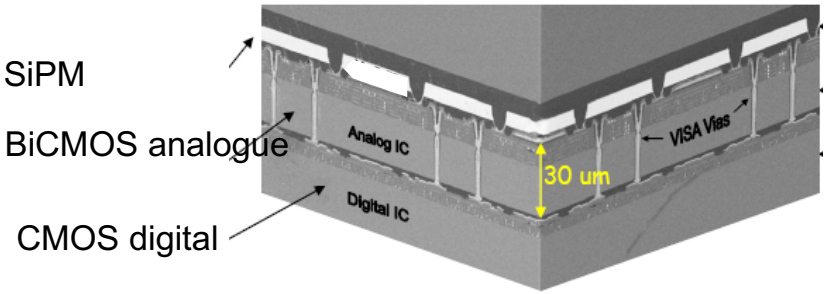
Connect ASIC chip to back-illuminated SIPM
For each pixel: signal detection & active quenching

-Fast timing (no stray capacitances)
-Low threshold -> low gain
-Active quenching -> low gain
-Minimal cross-talk
-Single pixel position resolution
-Veto of noisy pixels



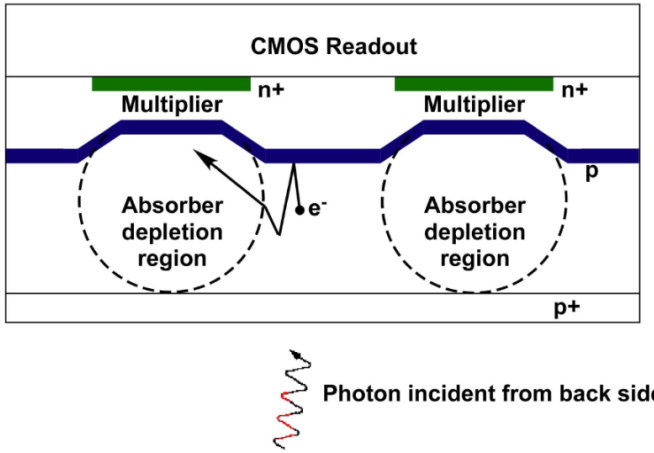
Could be made using

•Bump bonding
•3D integration techniques

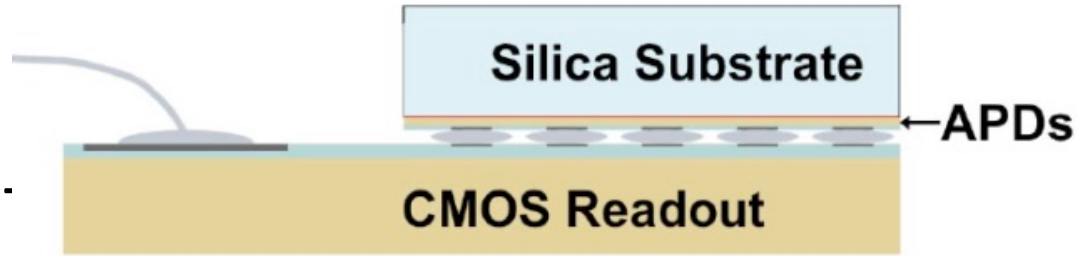


Pioneer work at MIT Lincoln Lab

- 25µm pitch
- 180nm CMOS + custom (APDs)
- 7-bit counter/pixel
- Backside illumination



- **10 - 20% detection efficiency** (limited by optical cross-talk)



B. Aull et al., IEEE Sensors J., 2015

Pioneer work at MIT Lincoln Lab

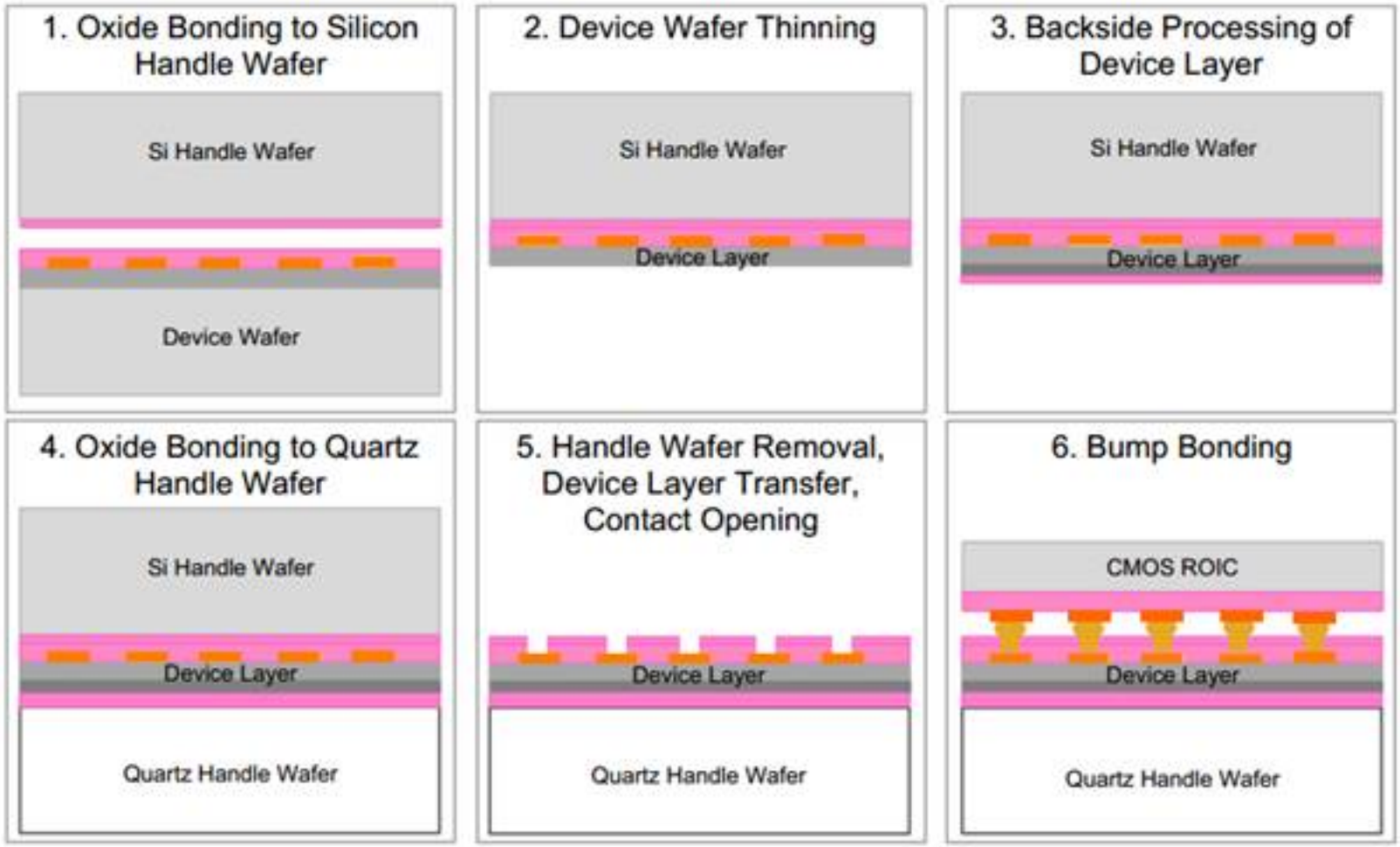


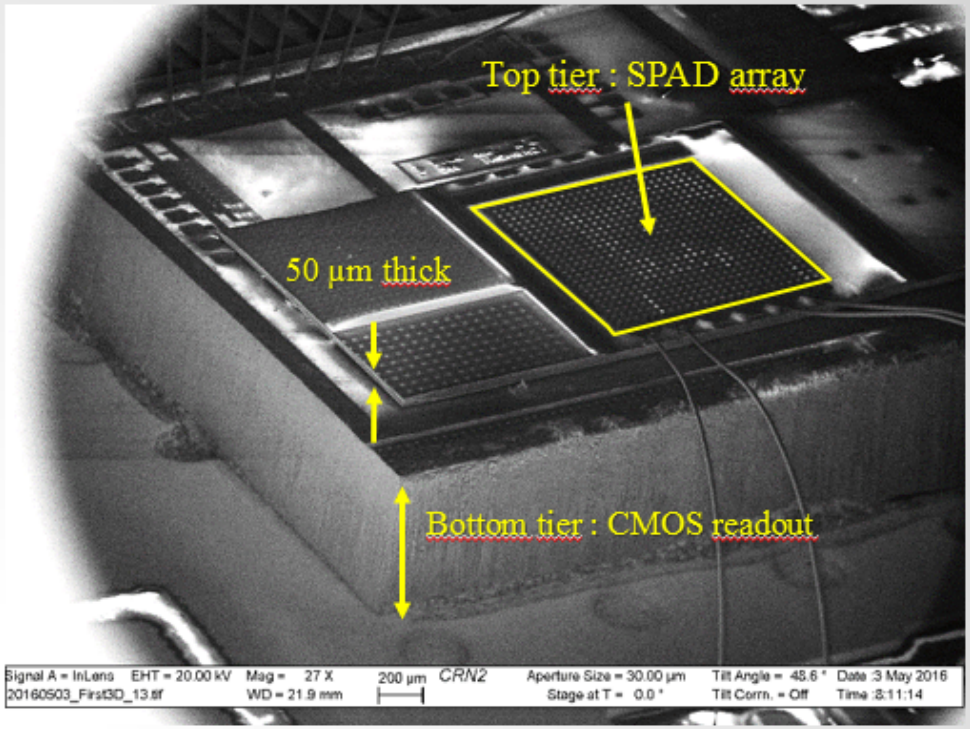
Figure 3: GM-APD back-illumination process flow illustrating the major steps to process a wafer of GM-APD devices that has completed front-side processing through to hybridization with a CMOS ROIC. To simplify the illustration, the relative positions of the components of the bonded wafer stack are maintained in all process description panels.

TRIUMF

And in Canada

- U.Sherbrooke (QC, Canada)
  - Photo-detector tier design
  - Electronics tier design
  - 3D assembly
- In collaboration with Teledyne-DALSA (Bromont, QC, Canada)
  - Photo-detector fabrication
  - 3D assembly
  - (CMOS chip made by TSMC)

Scanning Electron Microscope Image



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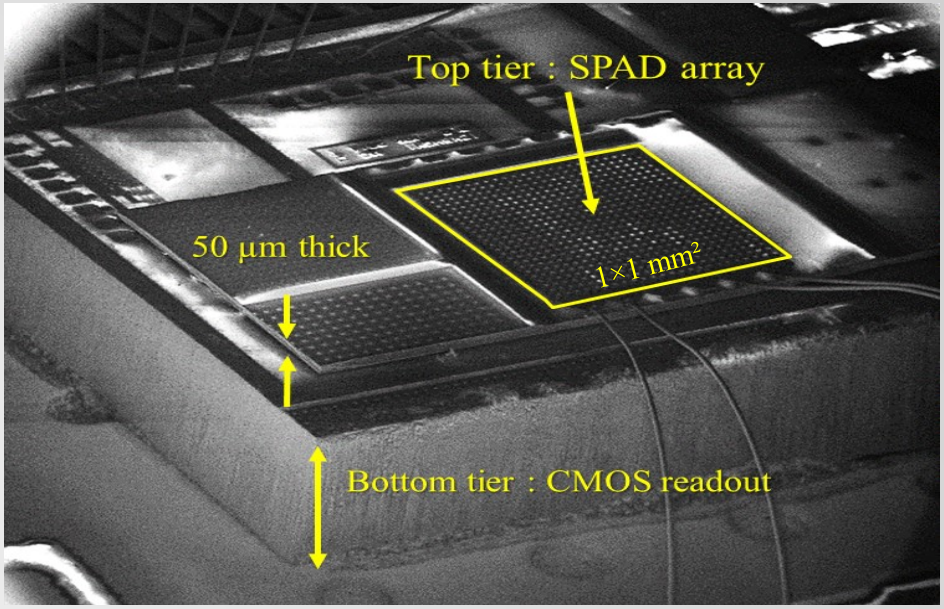
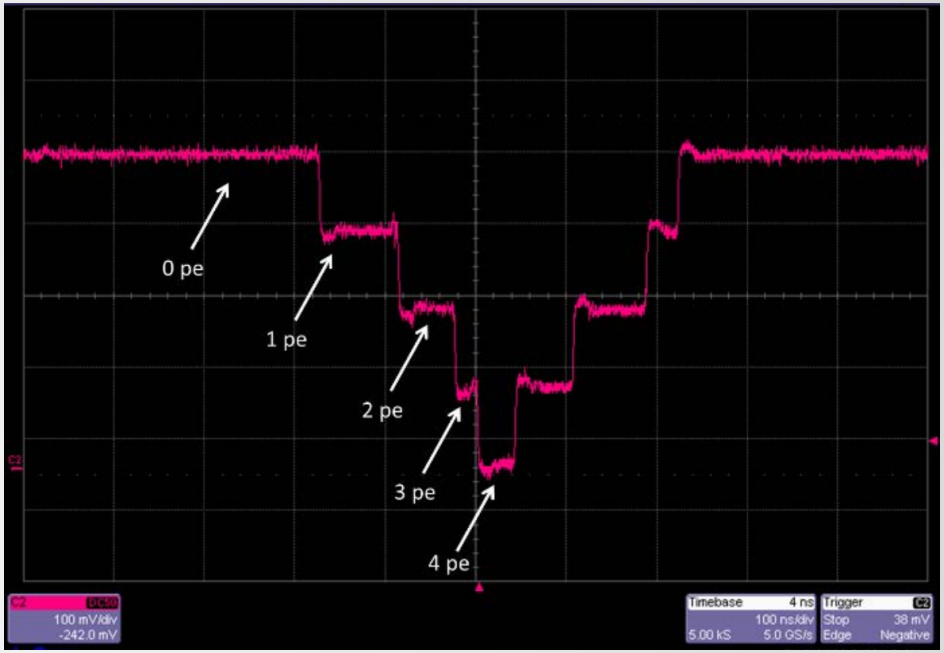
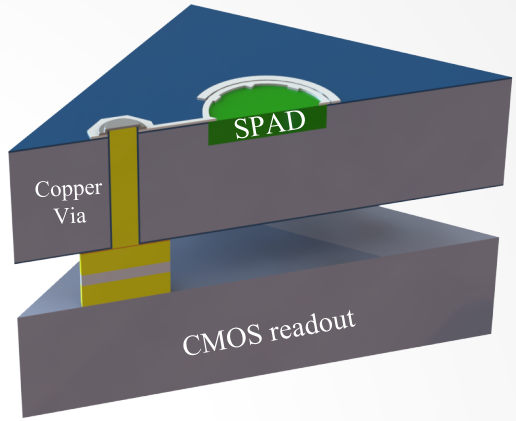
Sherbrooke's first 3D digital SiPM

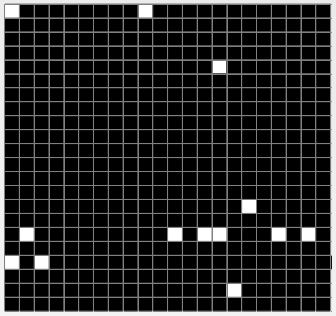
- Concept 1st proposed in 2010
- Proof of concept
  - SiPM : 22 x 22 SPAD cell
  - SPAD : Modified CMOS process
  - CMOS readout: Teledyne-Dalsa (HV 0.8 µm)
- Key Features
  - adjustable hold-off time
  - adjustable amplitude
  - single SPAD enable/disable



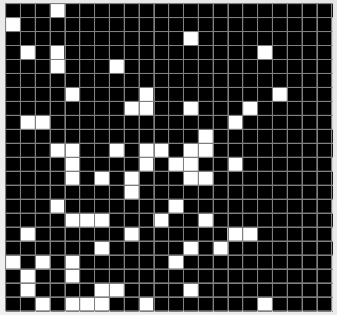




1st Prototype Results



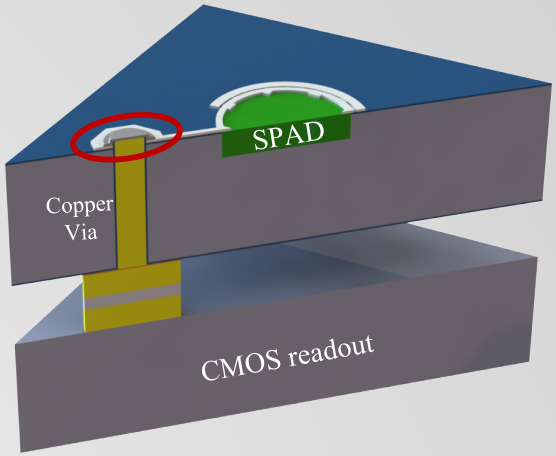
Proto1 : 13/484 pixels



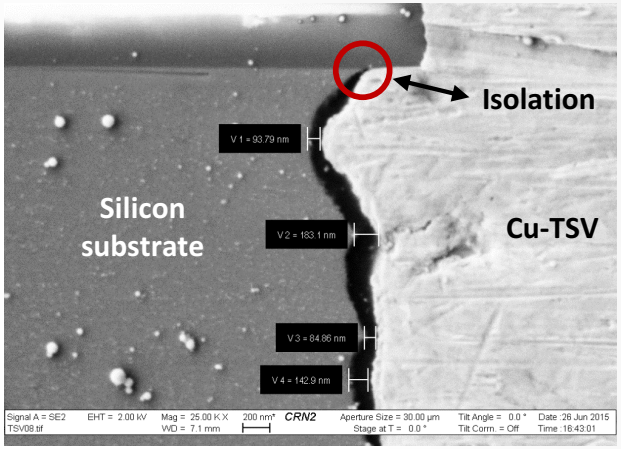
Proto2 : 67/484 pixels

Working

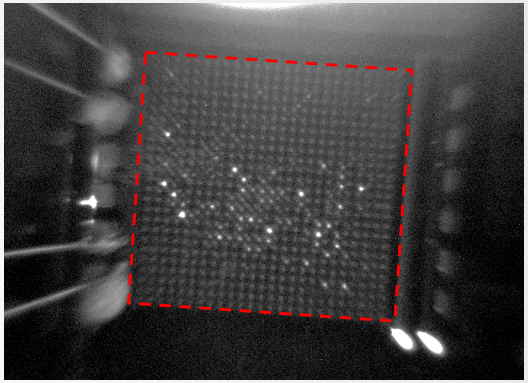
Open circuits



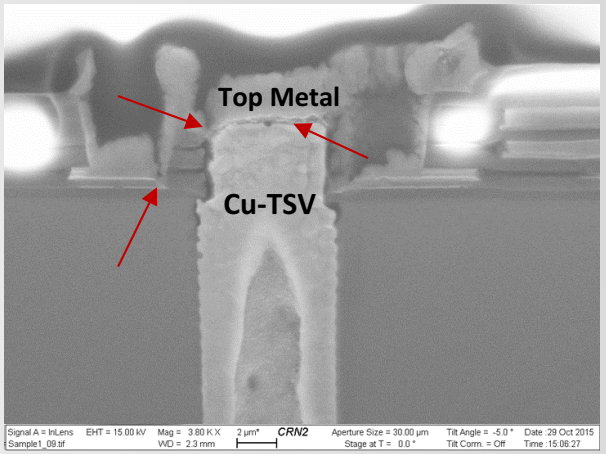
Low-R paths – anode to GND



Light emission from SPAD turned OFF



High-R paths – SPAD to TSV



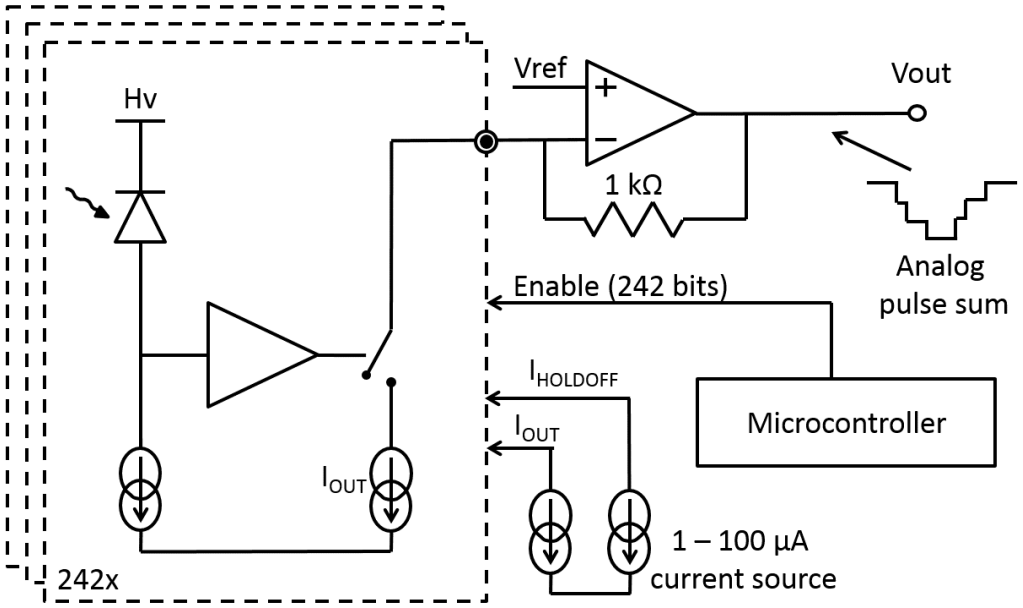
1st Prototype Results

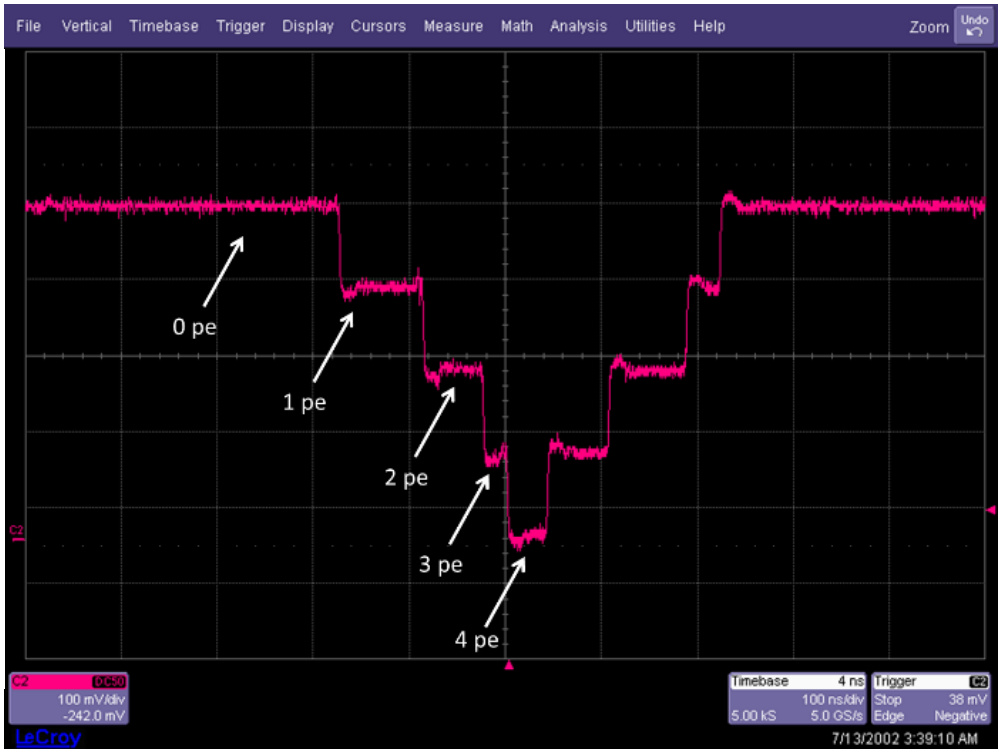
Device	2D digital SPAD	3D digital SPAD (in array[1])
Technology	800 nm CMOS	800 nm CMOS

Operation	
V_{BD} (V)	23
V_{ex} (V)	5
Diameter (µm)	20

Parameter		
Dark Count Rate (kHz)	100	~100-1000[1]
Photodetection Efficiency (>15 %) (nm)	435-740	435-740
PDE peak (550 nm) (%)	~30	~30
Single Photon Timing Resolution (ps FWHM) (410 nm)	39	100

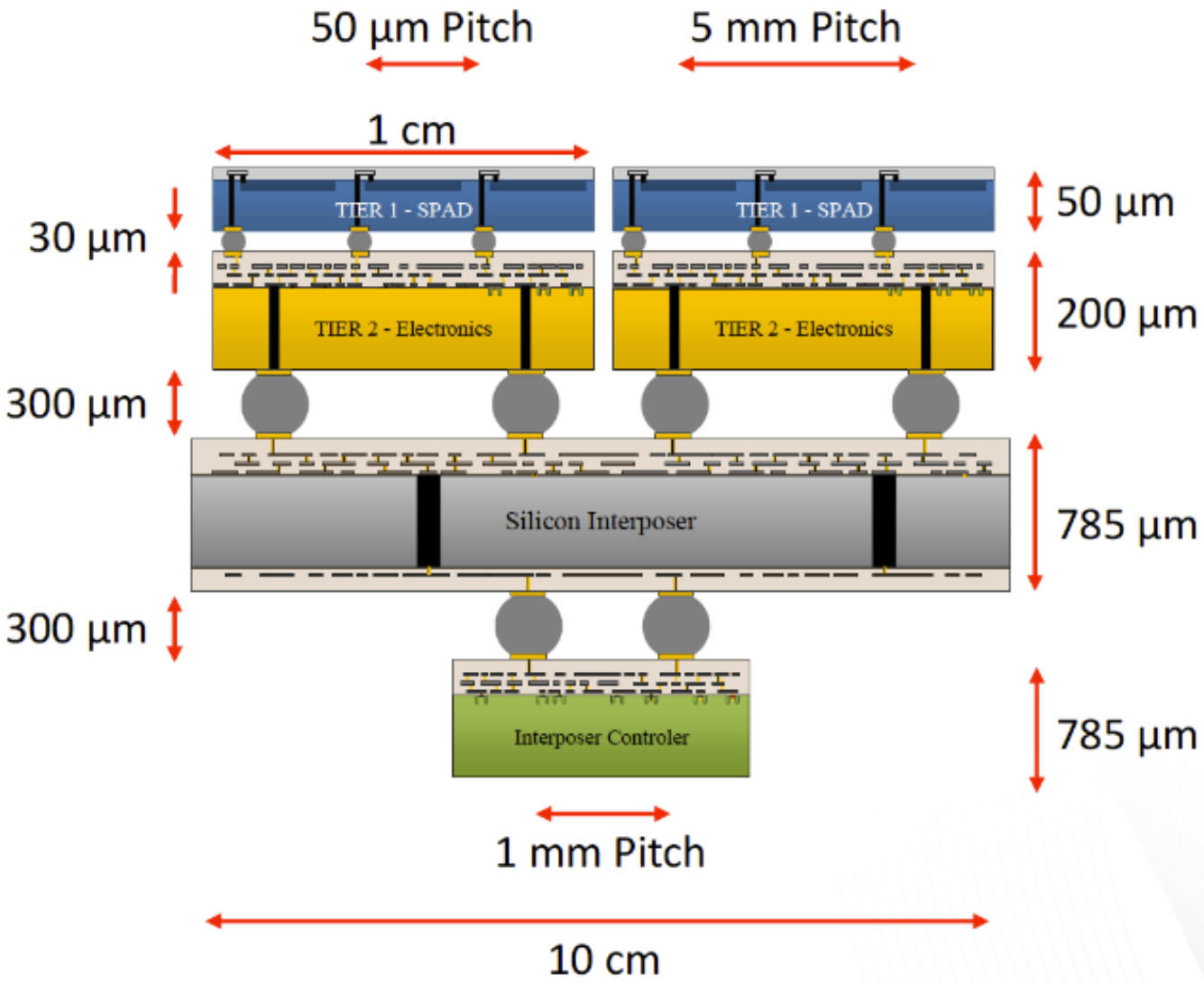
The pseudo-digital output





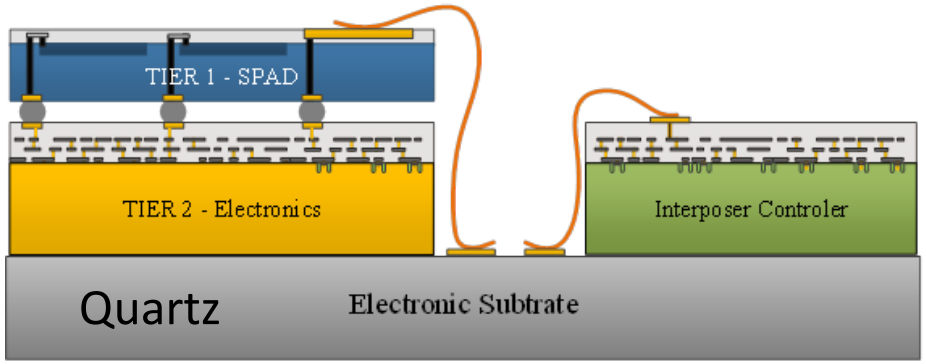
- An intermediate step very valuable for testing configurations

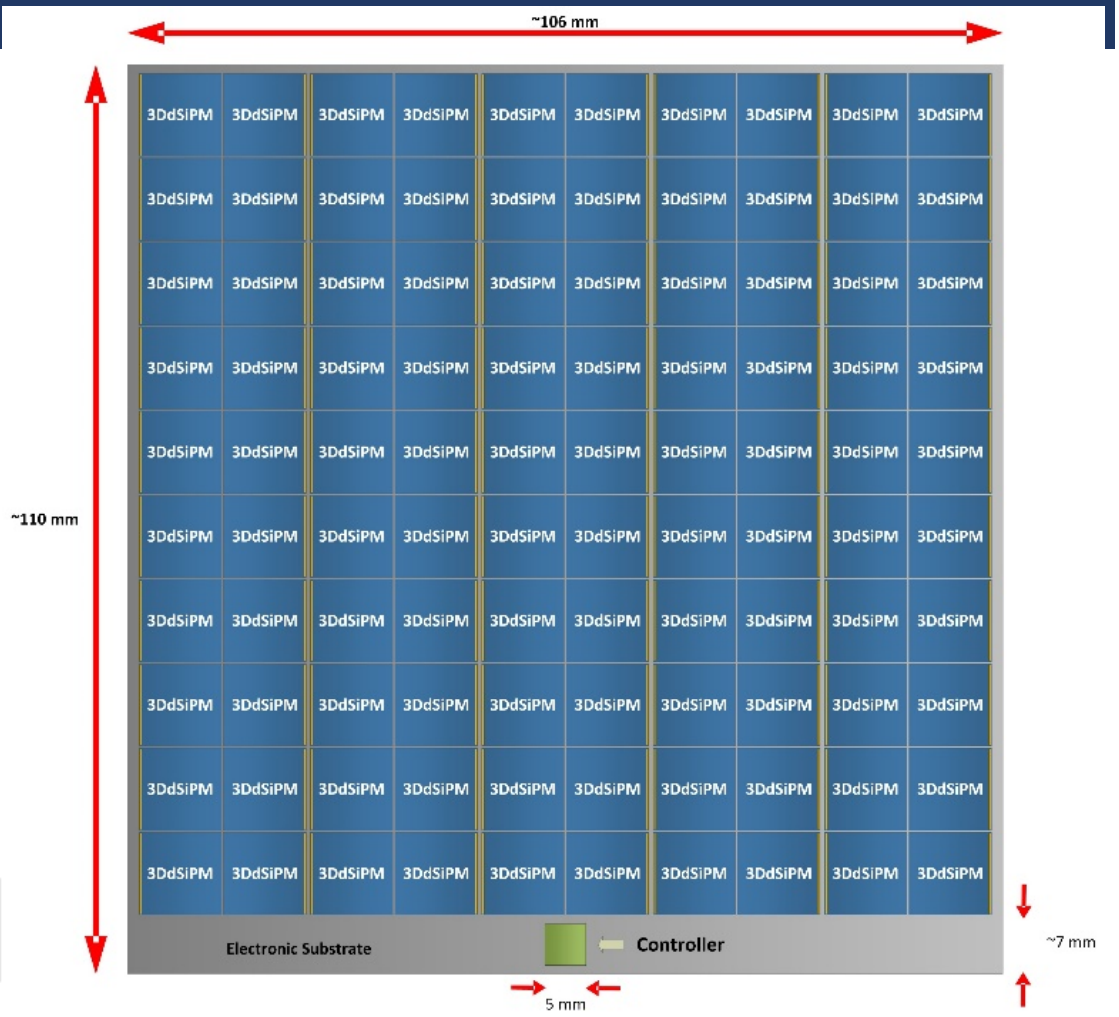
A fully 3D integrated concept



And the reality towards nEXO

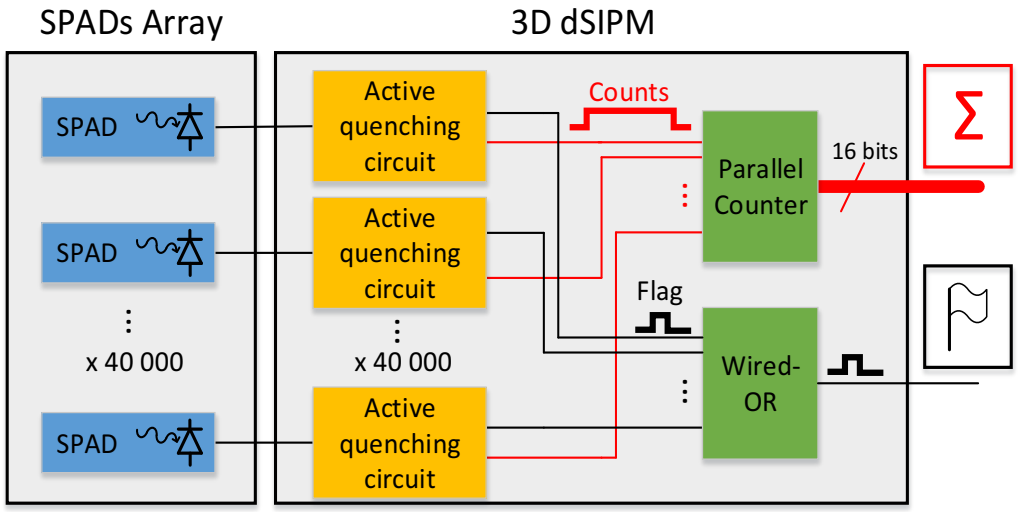
- Tailor photo-detector tier for VUV detection
- Demonstrate scalability
  - In particular power dissipation
- Demonstrate cost <2M$/m^2
- Funds requested for proof of concept





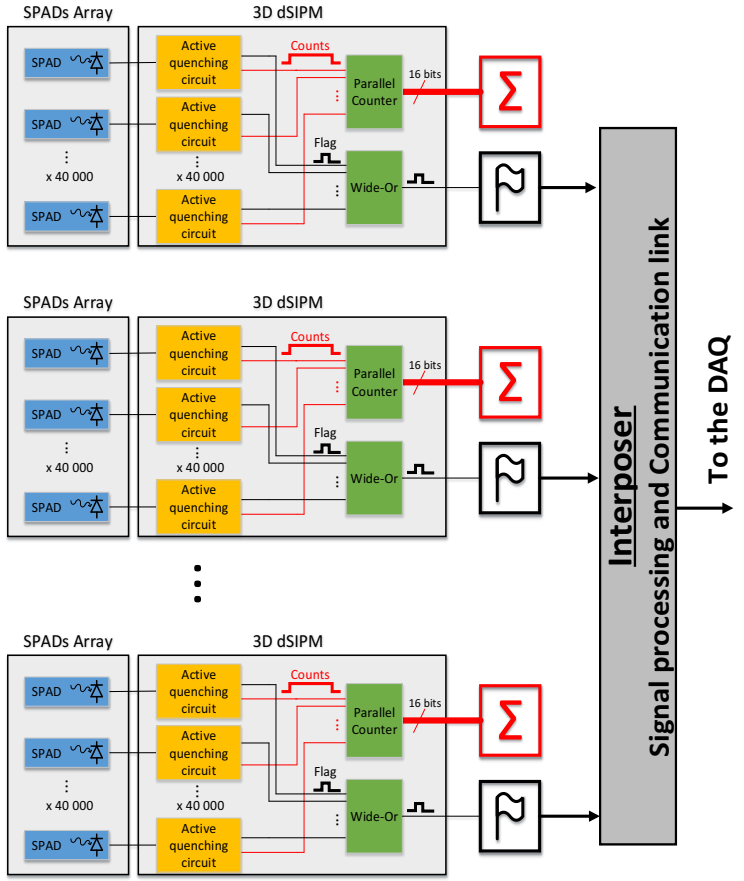
3DdSiPM "schematics"

- About 1x1cm^2
- Wired-OR
- Parallel adder provides the number of SPAD fired upon interposer request
- Low power digital asynchronous logic (no clock)



Tile for coincidence and triggering

- Adjustable coincidence window
- Adjustable threshold
- A trigger is generated when:
  - Flag count > threshold
  - Inside the coincidence window
- The parallel adder of each 3DdSiPM is activated for the duration of the scintillation
- Data transmission logic



Power consumption

- The proposed 3DdSiPM has a total area of 1 cm^2 and is composed of three modules.
  - 40 000 quenching circuits to individually quench the SPAD
  - A wired-or for the flag
  - A parallel adder for the sum
- Power consumption of the 3DdSiPM depends on the event rates
  - Power consumption evaluated for a DCR of 5k s^{-1} /cm^2
- **So… for 4 m^2, the digitization cost ~0.7 W! About x20 estmimated for analog SiPMs**

Consumption per 3DdSiPM (1 cm^2)			
	Static (µW)	Dynamic (µW)	Total (µW)
Quenching circuit (40k)	10	1	11
Wired-OR	0.3	1.3	1.6
Adder	5.2	1E-3	5.2
Total	15.5	2.3	**17.8**

Other advantages of 3DdSiPMs in LXe and LAr

- Timing resolution < 1ns (towards 10ps) overall large area
  - Without huge power dissipation
  - May allow separating Cerenkov and scintillation photons
    - Possible background rejection handle in $0\nu\beta\beta$ experiment
- Fine granularity (at no extra cost)
  - mm^2 scale possible
  - Combined with electro-luminescence allows exquisite charge cloud reconstruction in liquid Xenon. Another possible background rejection handle in $0\nu\beta\beta$ experiment
  - Allow tagging activity on the photo-detector surface
- Zero after-pulsing due to active quenching
  - Enhance energy resolution and pulse shape discrimination
  - Though does not eliminate cross-talk (including delayd cross-talk)
- Push cost down to allow >100m^2 coverage for ~10M$

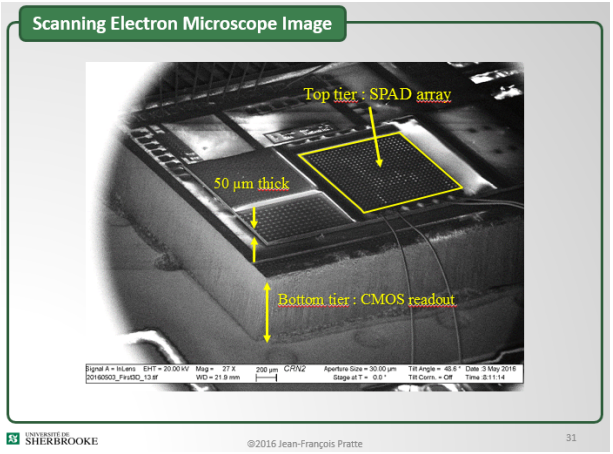
Program in Canada

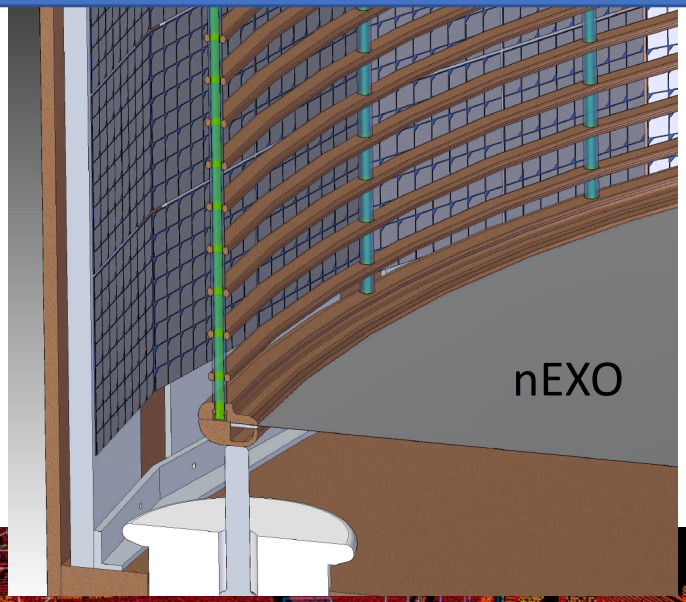
- ~1.5M$ from Canadian Foundation for Innovation
  - Carleton – McGill – TRIUMF
- 3DdSiPM to match specifications of nEXO and LAr

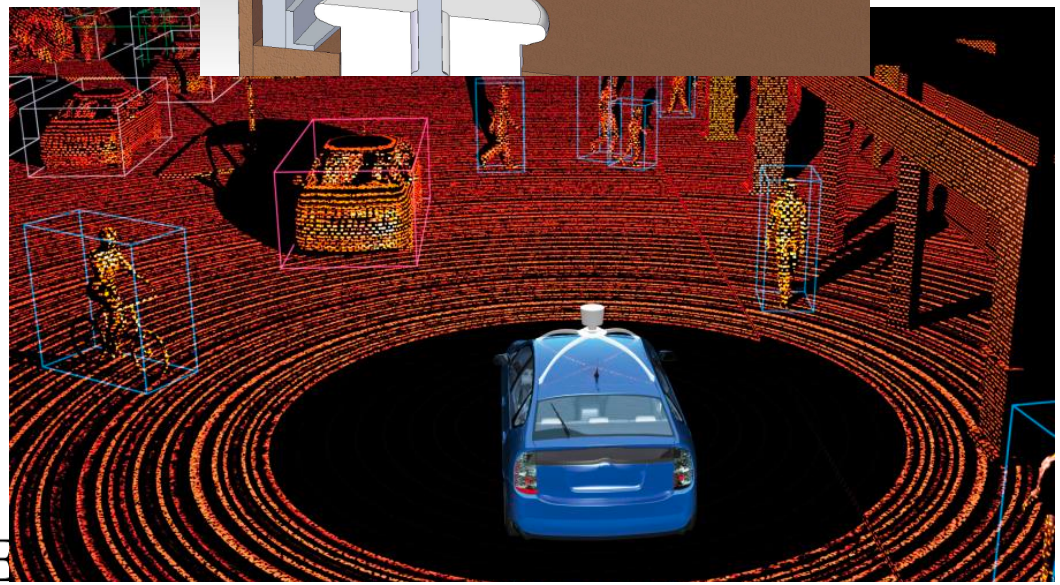
2018	2019	2020
SPAD array optimized for 3D	Complete performance validation	Large scale 5x5mm2 production
Dummy wafer to wafer assembly and test	Functional wafer to wafer assembly demonstration	Large scale production
Small scale CMOS With CMOS SPAD for testing	Full scale CMOS wafer production	
		16x16 of 5x5mm2 3DdSiPM tile

Long term outlook

2015 **2025** **2035**

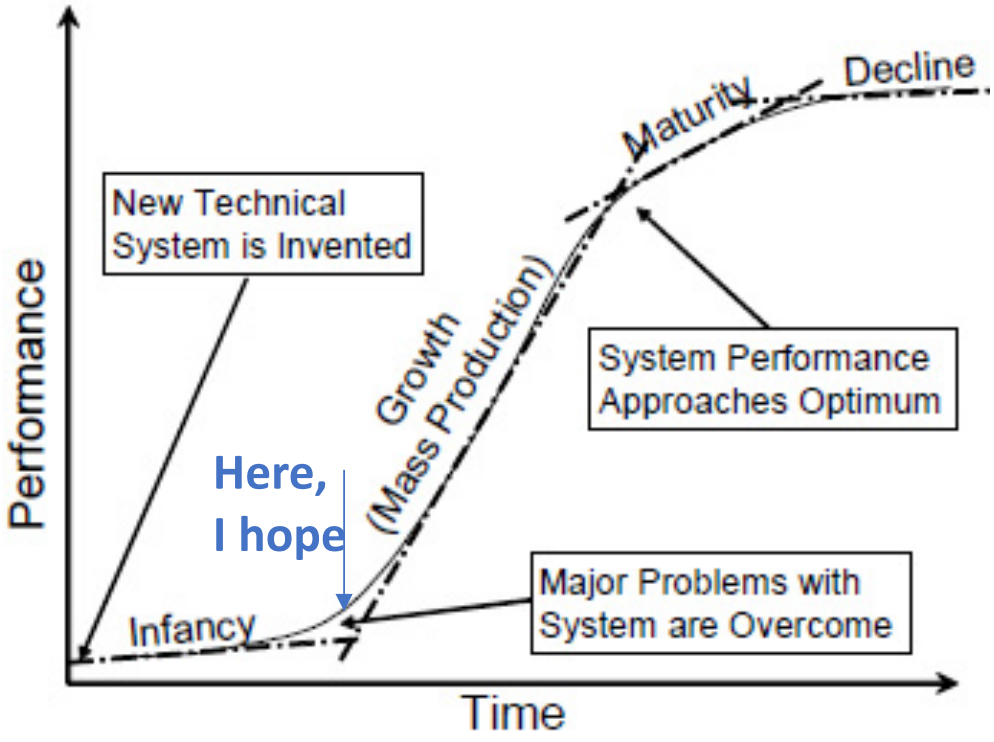






A more sobering outlook

- Where are we?

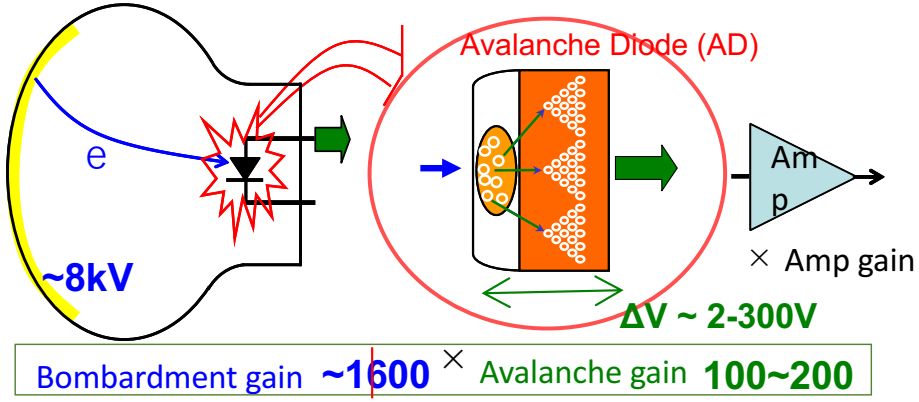


Technology life-cycle curve

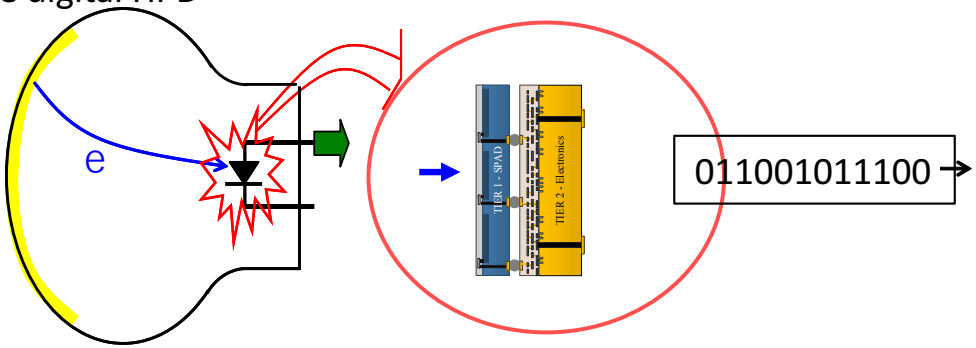
- Mitigating risks through an expanded collaborative effort?
- And challenges that I glanced over
  - Optimum SPAD array configuration for 3D?
  - VUV sensitivity
  - IR sensitivity
    - Silicon or something else?

Another application: Digital Hybrid Photo-Detector

Analog HPD from Hamamatsu, Tokyo & Kyoto University



The digital HPD



- Use 3D Geiger-mode avalanche diode array for gain stage
  - Size 0.1-1 cm^2 with photocathode 100-1000cm^2
- May be cheaper than very large 3DdSiPM plane
  - 1/1000 reduction of Si area
- Dark noise
  - Not an issue cold, e.g. in LAr
  - Need to play some tricks at room temperature. Same as detecting charge particles

Thank you