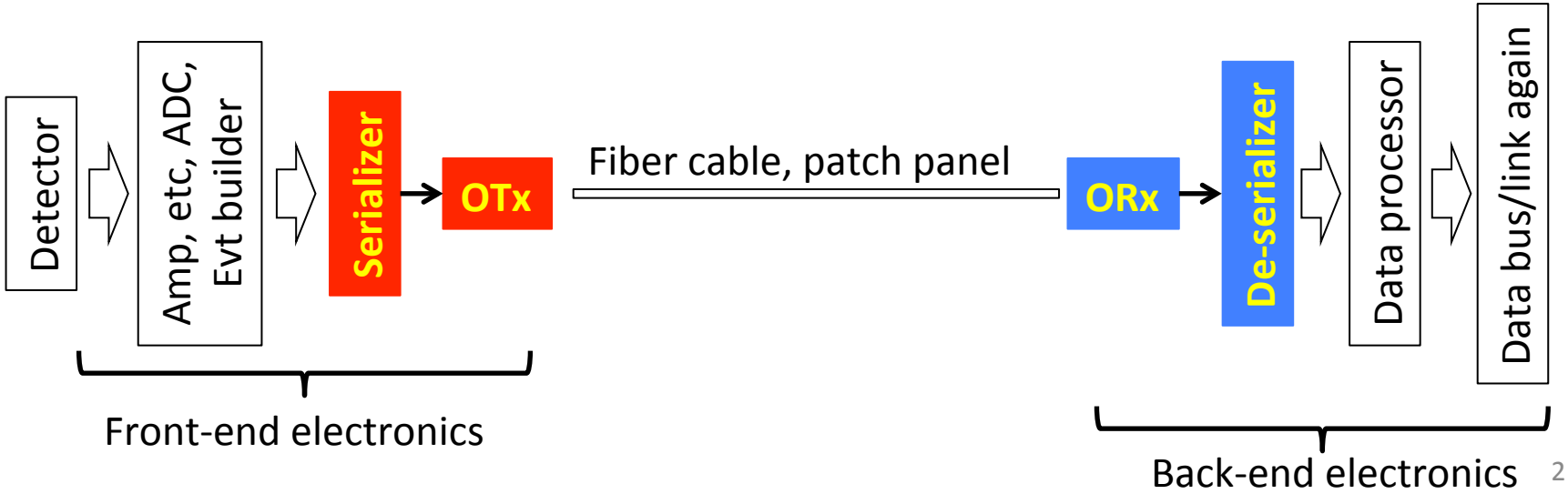
Developments in Optical Links for Detector Front-end Readout

Jingbo Ye
Physics, SMU

CPAD2017
Oct., 2017 @ UNM

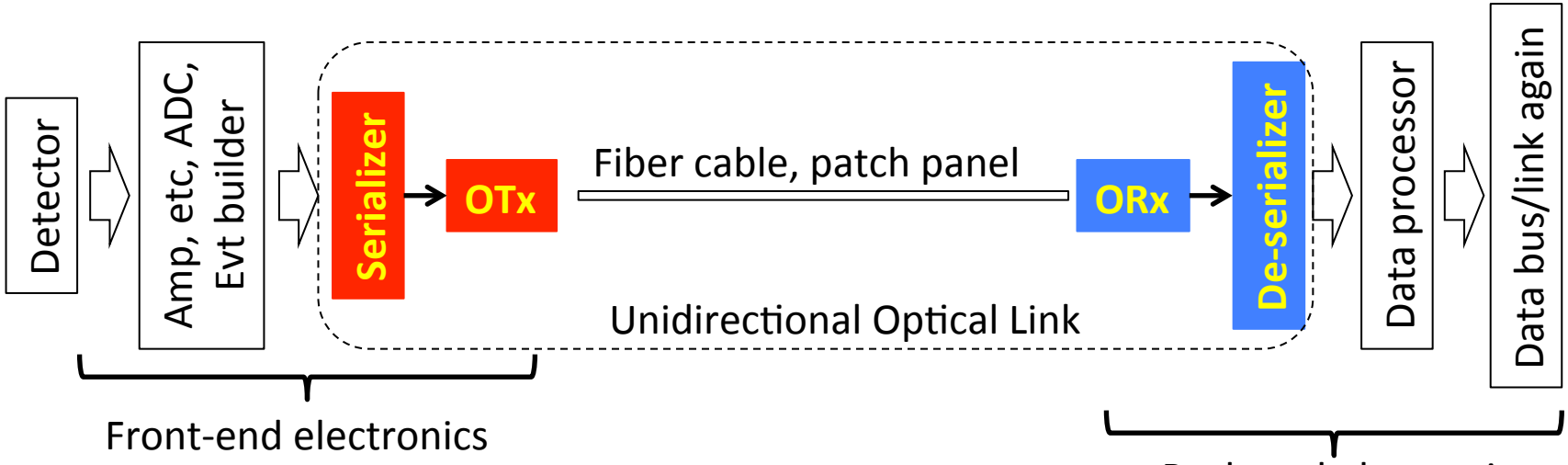
Serial Data Transmission over Optical Link

- To my knowledge optical links were used in CDF and D0.
- In LHC experiments, optical links are used extensively in detector front-end readout.
- At least in ATLAS and CMS, the calorimeter readout uses serial data transmission over fibers.



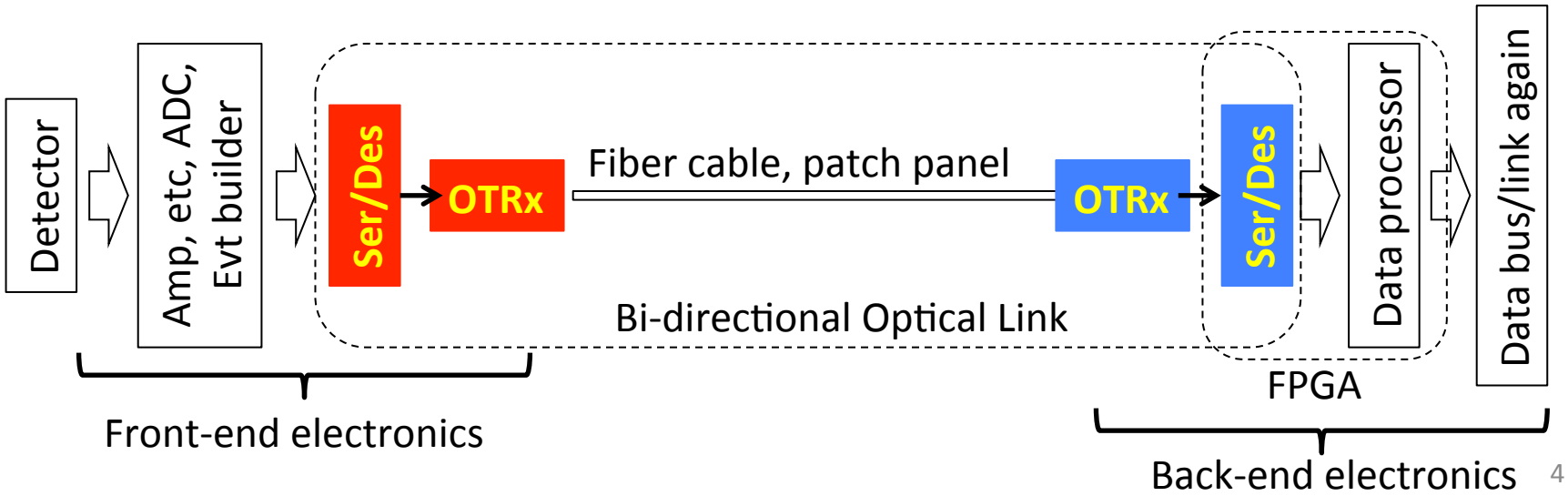
Serial Data Transmission over Optical Link

- To my knowledge optical links were used in CDF and D0.
- In LHC experiments, optical links are used extensively in detector front-end readout.
- At least in ATLAS and CMS, the calorimeter readout uses serial data transmission over fibers.



Serial Data Transmission over Optical Link

- To my knowledge optical links were used in CDF and D0.
- In LHC experiments, optical links are used extensively in detector front-end readout.
- At least in ATLAS and CMS, the calorimeter readout uses serial data transmission over fibers.



From Mbps to Gbps

- Tevetron experiments

10s of Mega-bit per second per fiber

- Current LHC experiments
  2000 - 2005

10s of Mbps to 0.8 and 1.6 Gbps

- After LHC LS2 (phase-1)
  Now - 2020

4.8 or 5.12 Gbps

- HL-LHC experiments

10.12 Gbps or higher

From Mbps to Gbps

- Tevetron experiments

10s of Mega-bit per second per fiber

- Current LHC experiments
  2000 - 2005

10s of Mbps to 0.8 and 1.6 Gbps

1.25 to 2.5 Gbps in industry

- After LHC LS2 (phase-1)
  Now - 2020

4.8 or 5.12 Gb 28 Gbps

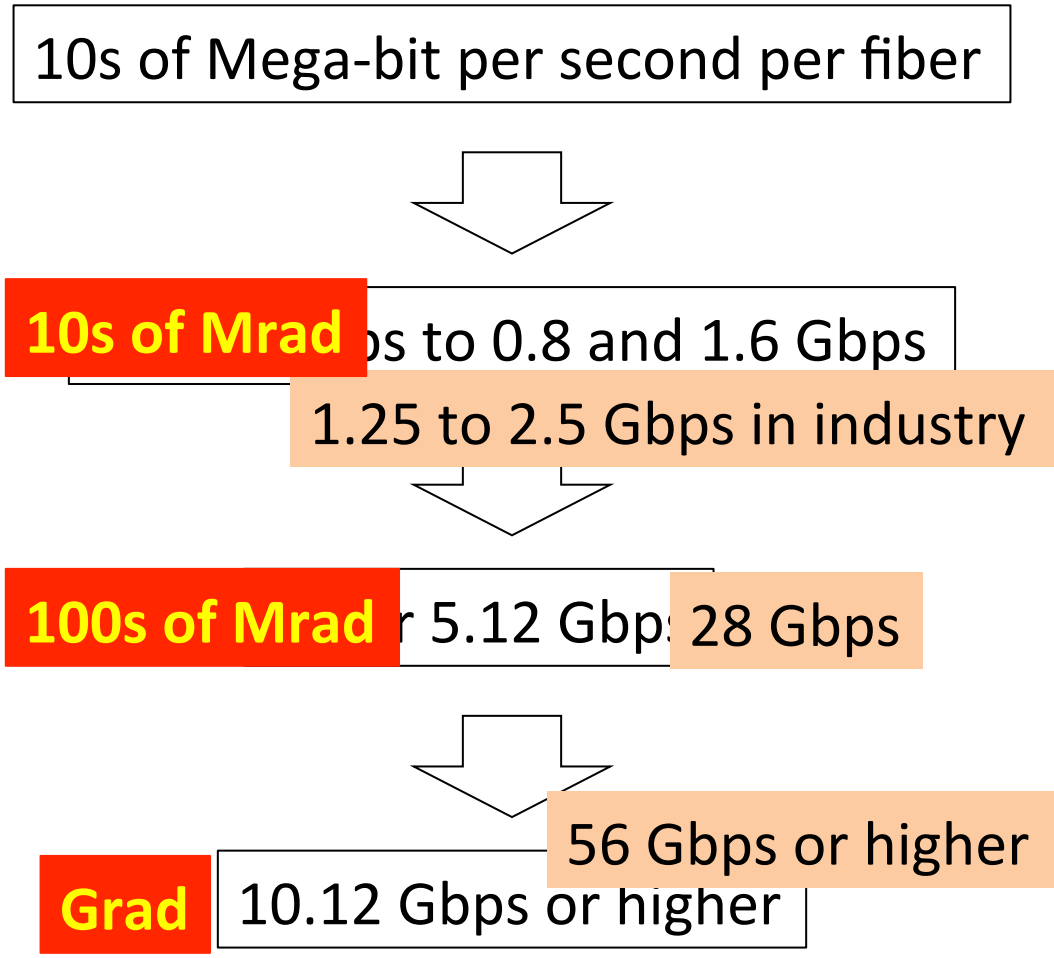
- HL-LHC experiments

56 Gbps or higher

10.12 Gbps or higher

But

- Tevetron experiments
- Current LHC experiments
  2000 - 2005
- After LHC LS2 (phase-1)
  Now - 2020
- HL-LHC experiments

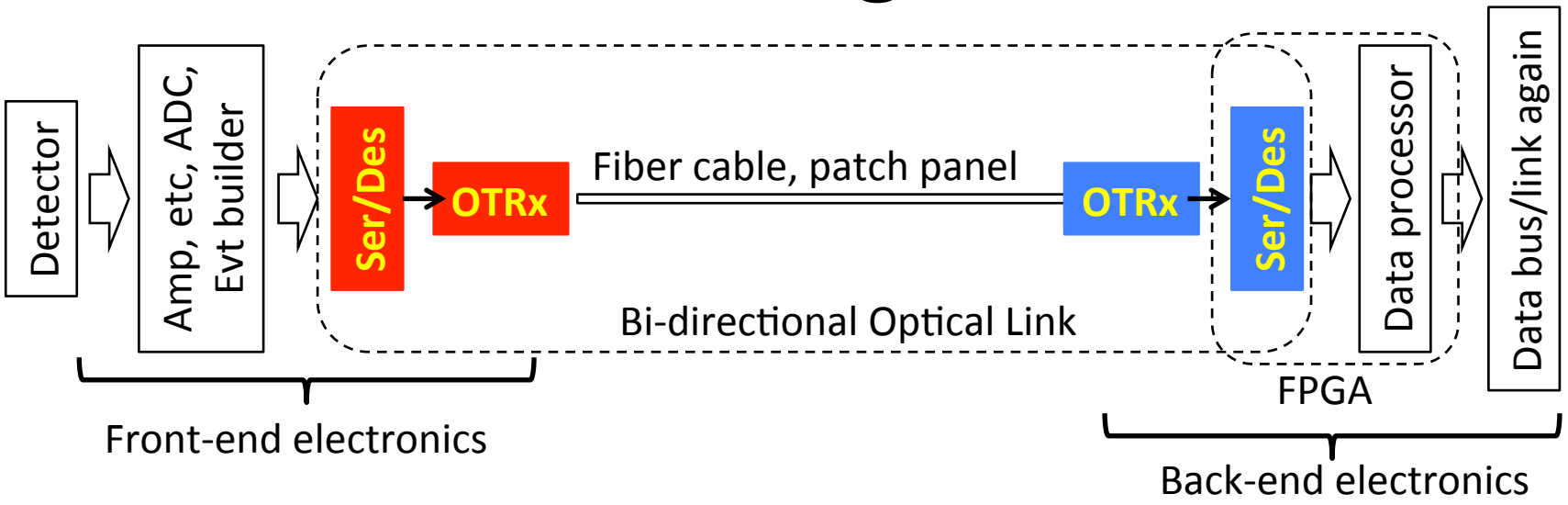


But

- Tevetron experiments
  - 10s of Mega-bit per second per fiber
- Current LHC experiments
  2000 - 2005
  - 10s of Mrad
  - ps to 0.8 and 1.6 Gbps
  - 1.25 to 2.5 Gbps in industry
- After LHC LS2 (phase-1)
  Now - 2020
  - 100s of Mrad
  - r 5.12 Gbps
  - 28 Gbps
- HL-LHC experiments
  - Grad
  - 10.12 Gbps or higher
  - 56 Gbps or higher

High channel density, low power dissipation, low-mass small formfactor, etc

The Building Blocks

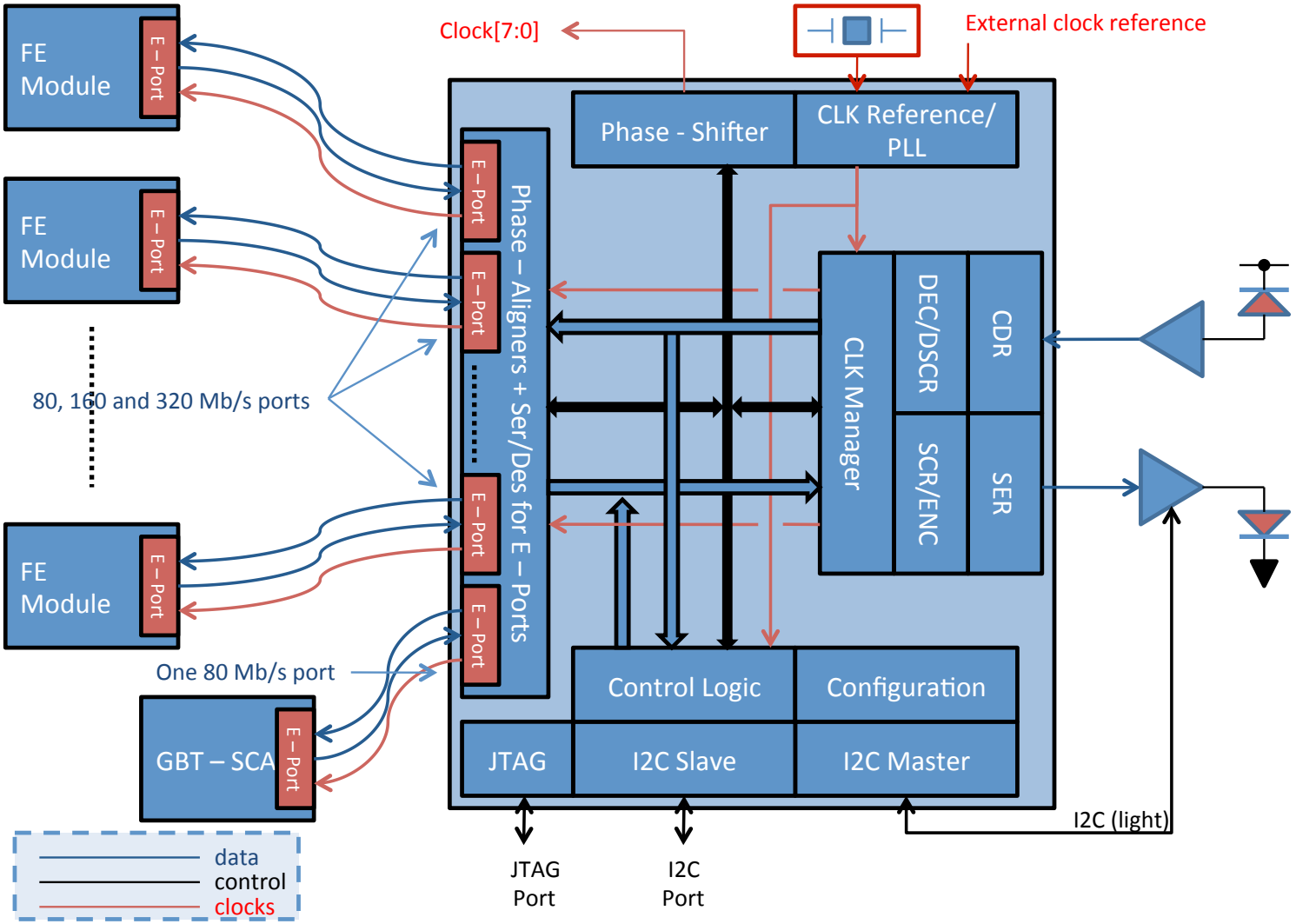


- FE: components-of-the-shelf (COTS) to custom developments (ASICs)
  - Serializer or Ser/Des: GLink, GOL, GBTx, LOCx2, lpGBT
  - OTx and OTRx (some also called VTTx, VTRx, MTx, MTRx, etc)
- BE: outside of radiation but sometimes special mechanical requirements: custom to COTS

Closer Look at Serializers and Ser/Des

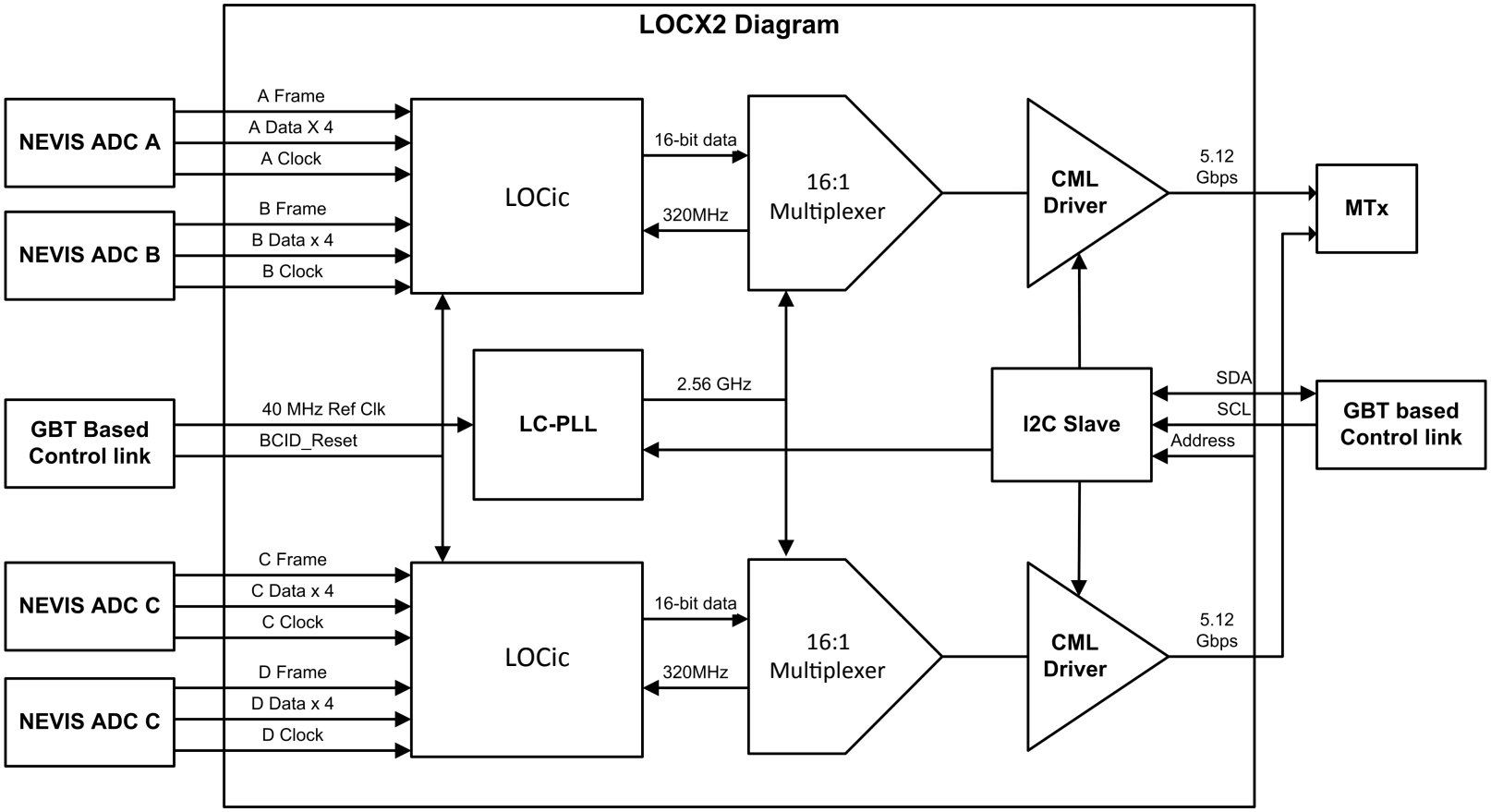
- GLink, serializer and deserializer chipset, COTS, CIMT (GLink transmission) protocol, 1.25 Gbps (runs at 1.6 Gbps in ATLAS/ LAr), bipolar based, 1.5+ W/chip, or 938 mW/1Gbps
- GOL, serializer, CERN ASIC, CIMT or 8B/10B protocol, 0.8 or 1.6 Gbps (I2C or JTAG configurable), 0.25 um CMOS based, 400 mW/chip, 250 mW/1Gbps
- GBTx, ser/des, CERN ASIC, 3 protocols (GBT w/ error correction, 8B/10B, WideBand), 4.8 Gbps bi-direction, I2C interface, 130 nm CMOS based, 980 mW/chip, ~100 mW/1Gbps
- LOCx2, dual-channel serializer, SMU ASIC, LOCic protocol and only interfaces to 3 types of ADCs, 2x5.12 Gbps, I2C interface, 250 nm SOS CMOS based, 950 mW/chip, 93 mW/1Gbps
- lpGBT, ser/des, CERN ASIC, protocols w/ error correction, 5.12 or 10.24 Gbps uplink, 2.56 Gbps downlink, I2C interface, 65 nm CMOS based, 500 mW (5.12 Gbps) or 750 mW (10.24 Gbps), ~37 mW/1Gbps.

GBTX Block Diagram



Many functional blocks, efforts of many designers

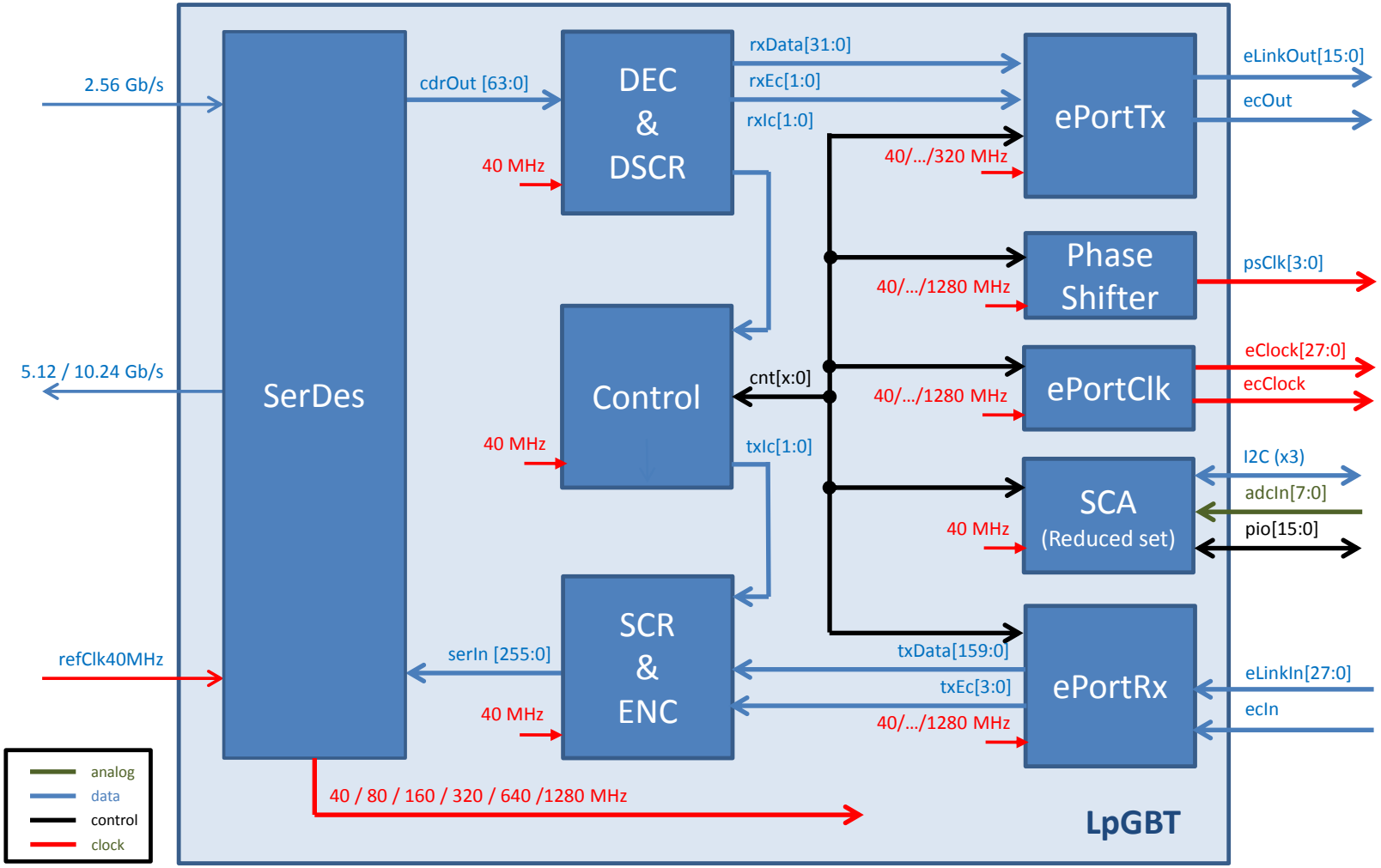
LOCx2 Function blocks



We use NevisADCs as an example. The input ADCs can also be ADS5272 and ADS5294. The drop-in backup, LOCx2-130, based on GBTx PLL and serializing units is a better design than LOCx2.

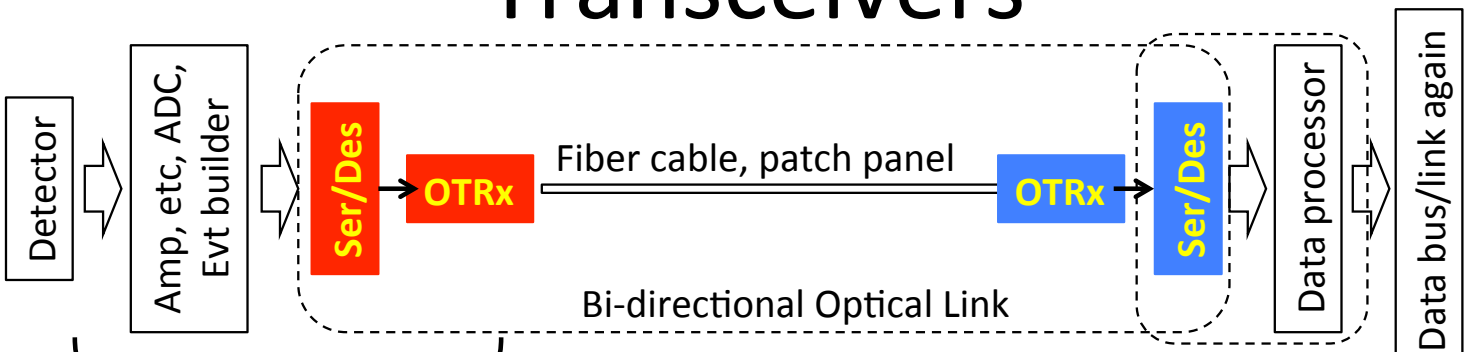
Simpler than GBTx, designed by a university group through years of R&D

LpGBT Block Diagram

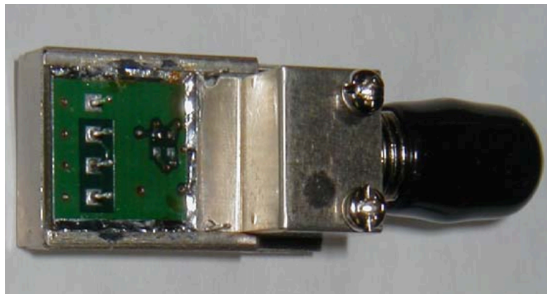


Built on GBTx experience, CERN led efforts of many designers

Closer Look at Optical Transmitters/ Transceivers



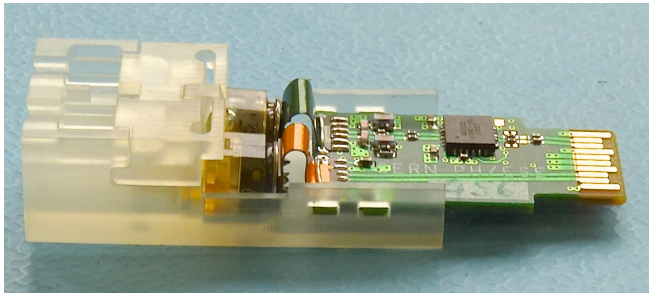
- There were quite a few custom developments to meet mostly mechanical requirements in the front-end boards of a particular detector.
- The optical coupling between the VCSEL to the fiber was also done in various ways, ranging from a full custom fashion to the industrial standard ST/SC TOSA (transmitter optical subassembly).



OTx, based on ST coupling, was developed for ATLAS/ LAr FEB readout.

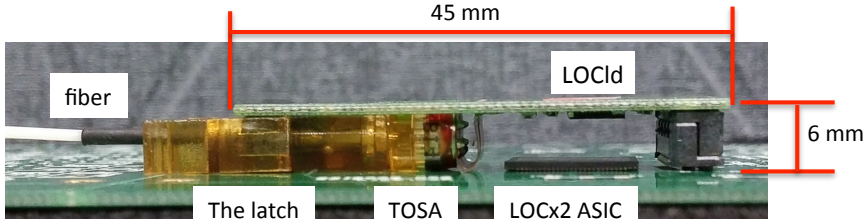
Closer Look at Optical Transmitters/ Transceivers

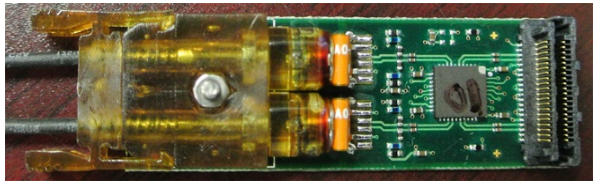
- The Versatile Link (VL) common project was established (10 years ago) to address this issue of many developments and the “products” from this project, which will be widely used in LHC phase-1 upgrades, are the VTRx and VTTx. Data rate: 4.8 Gbps. They are LC based.



VTRx by VL common project. Use LC and SFP+

- Still there are special requirements that need to be met: the MTx (2x5.12 Gbps) and MTRx for ATLAS/LAr trigger upgrade (phase-1).

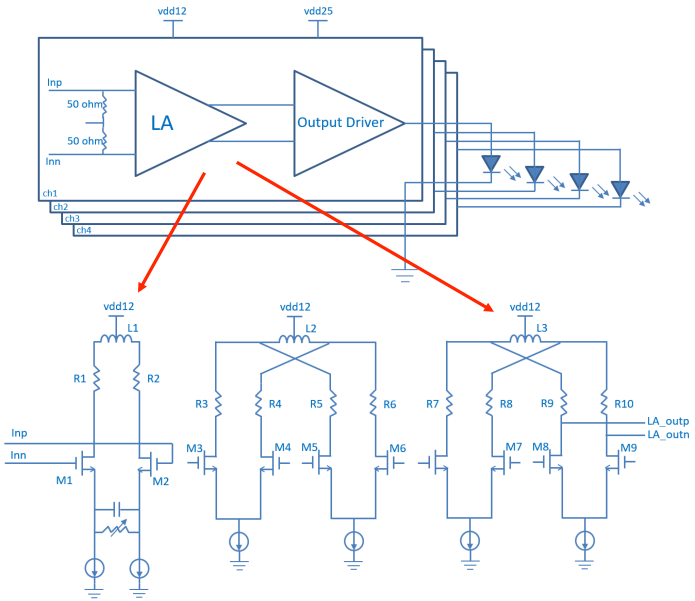


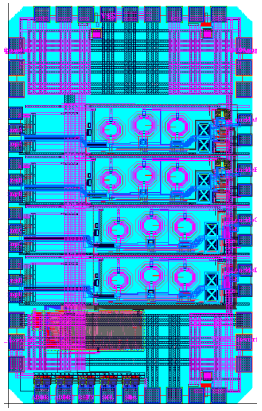


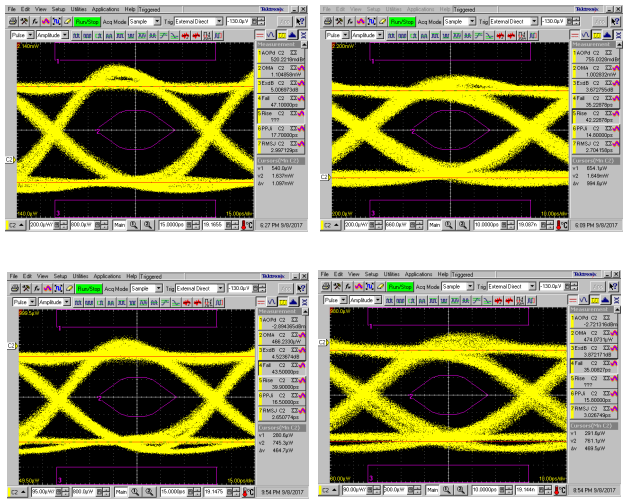
Closer Look at Optical Transmitters/ Transceivers

- The Versatile Link+ (VL+) common project is mainly for the LHC phase-2 upgrades. The promised deliverable is presented at TWEPP2017 (next slide)
- The same as in phase-1, not all requirements can be met by the VL+ modules. Developments in the community (e.g., ATLAS ITK pixel) are on-going to address these special issues.

Example, the VLAD VSCEL driver with an EQ at the input



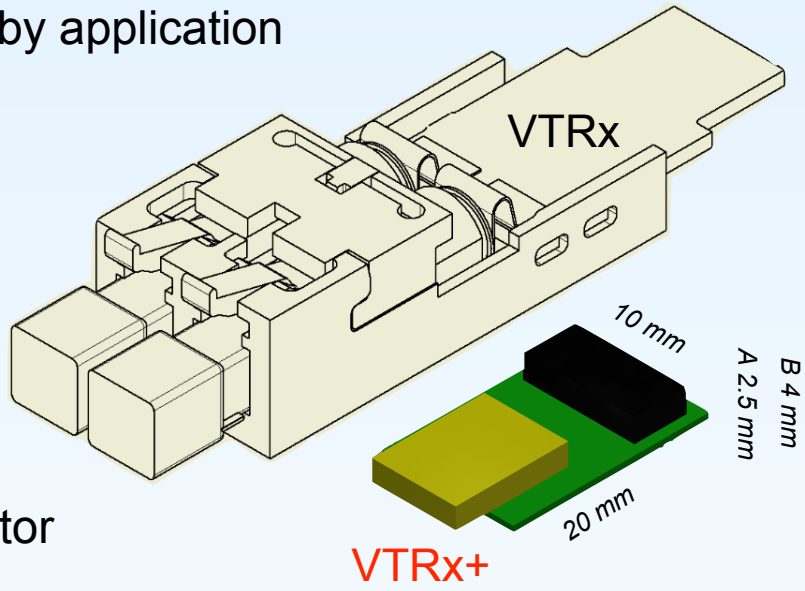




VLAD14 tested at 10 and 14 Gbps

VL+ module

- Versatile
  - multi-channel, Rx/Tx count usage defined by application
- MM only
  - 850 nm VCSEL
  - InGaAs PIN (TBC)
- Miniaturized
  - Target dimensions 20 x 10 x 2.5/4 mm
- Pluggable
  - Either optical or electrical (or both) connector
- Data-rate matching lpGBT:
  - Tx: 5 and 10 Gb/s
  - Rx: 2.5 Gb/s
- Environment
  - Temperature: -35 to + 60 °C
  - Total Dose: 1 MGy qualification
  - Total Fluence: $1x10^{15}$ n/cm^2 and $1x10^{15}$ hadrons/cm^2

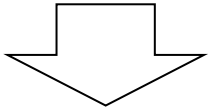


Total Quantity
20000-50000 modules

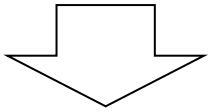
From ST/SC to LC to array optics

- Tevetron experiments
- Current LHC experiments
- After LHC LS2 (phase-1)
- HL-LHC experiments

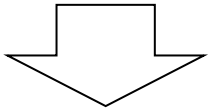
COTS or custom based on ST/SC



Custom, ST/SC and array (low speed)



Custom based on LC



Custom array with industry fab.

ST, SC and LC plus array (MT) are still mainstream in industry, with maybe LC and MT dominating.

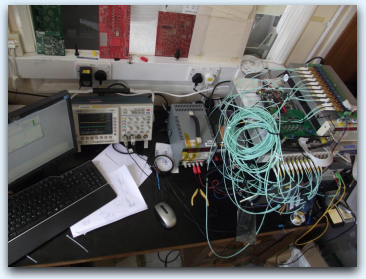
Not a Project (yet) but Discussions

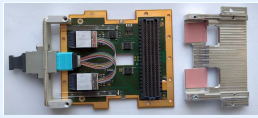
- In HEP experiments the primary job of the data link is to ship data off the detector. The so-called uplink (from detector to counting room) has much higher data rate and number of fibers than the downlink.
- With 10 Gbps, the number of fibers is still high (cost, maintenance, etc. e.g., ATLAS FEB2 will need about 30,000 fibers @ 10G/fiber).
- There are discussions among designers to group two channels of the lpGBT serializer (an ASIC from the design blocks of lpGBT Ser/Des) and increase the output data rate to 20 Gbps.
- There is already a prototype of 20 Gbps VCSEL driver (VLAD28, fabricated but not tested yet).
- There are even discussions to follow the trend in industry to develop a radiation tolerant PAM4 driver to go up to 40 Gbps.

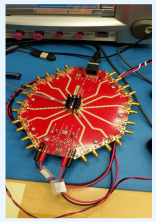
A Word about the Off-detector BE and the Passives

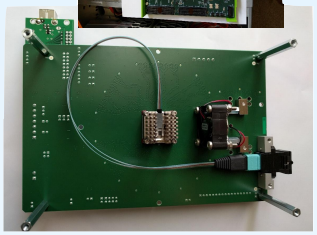
- BE and passives (fiber and patch panel adaptors) , including component and system level reliability, have been looked at in the VL+ common project. Instead of “products”, VL+ will make recommendations on these parts.

VL+ project collaboration



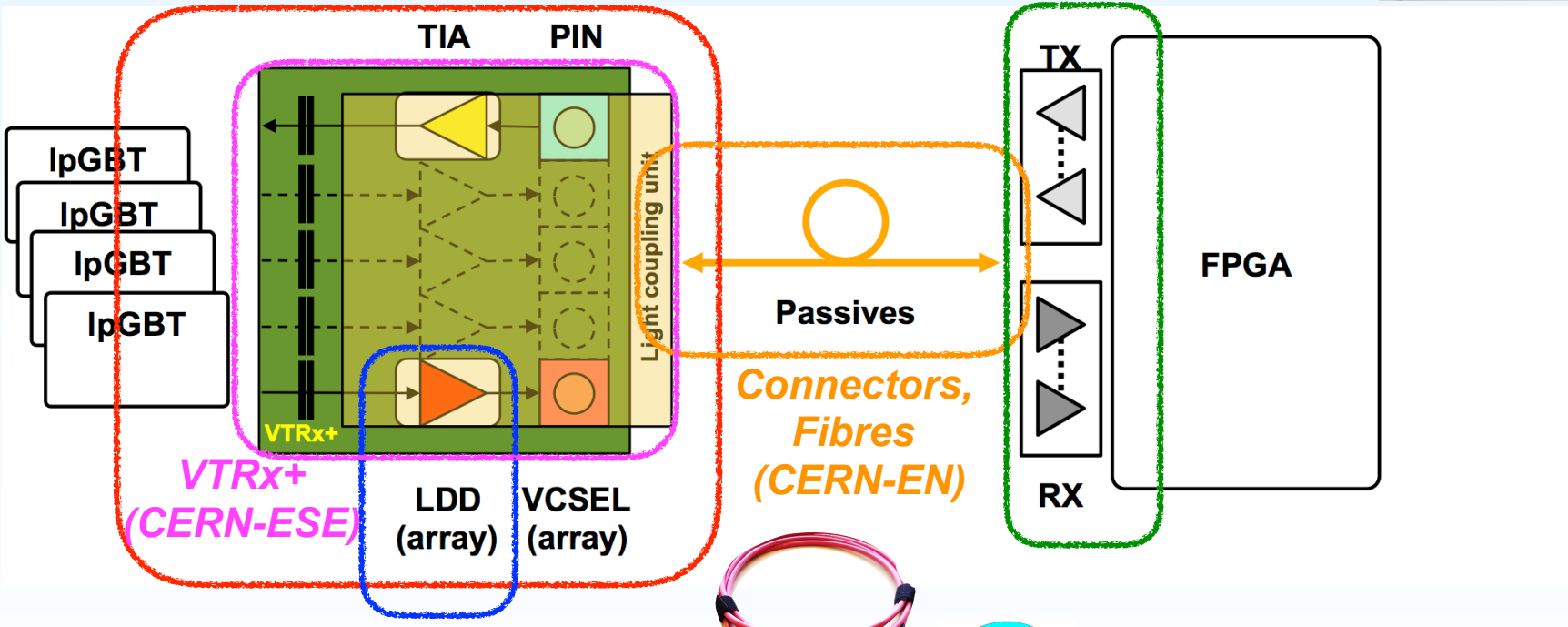






Reliability (Oxford, Academia Sinica)

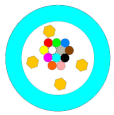
Commercial Array TRx (FNAL)



VTRx+ (CERN-ESE)

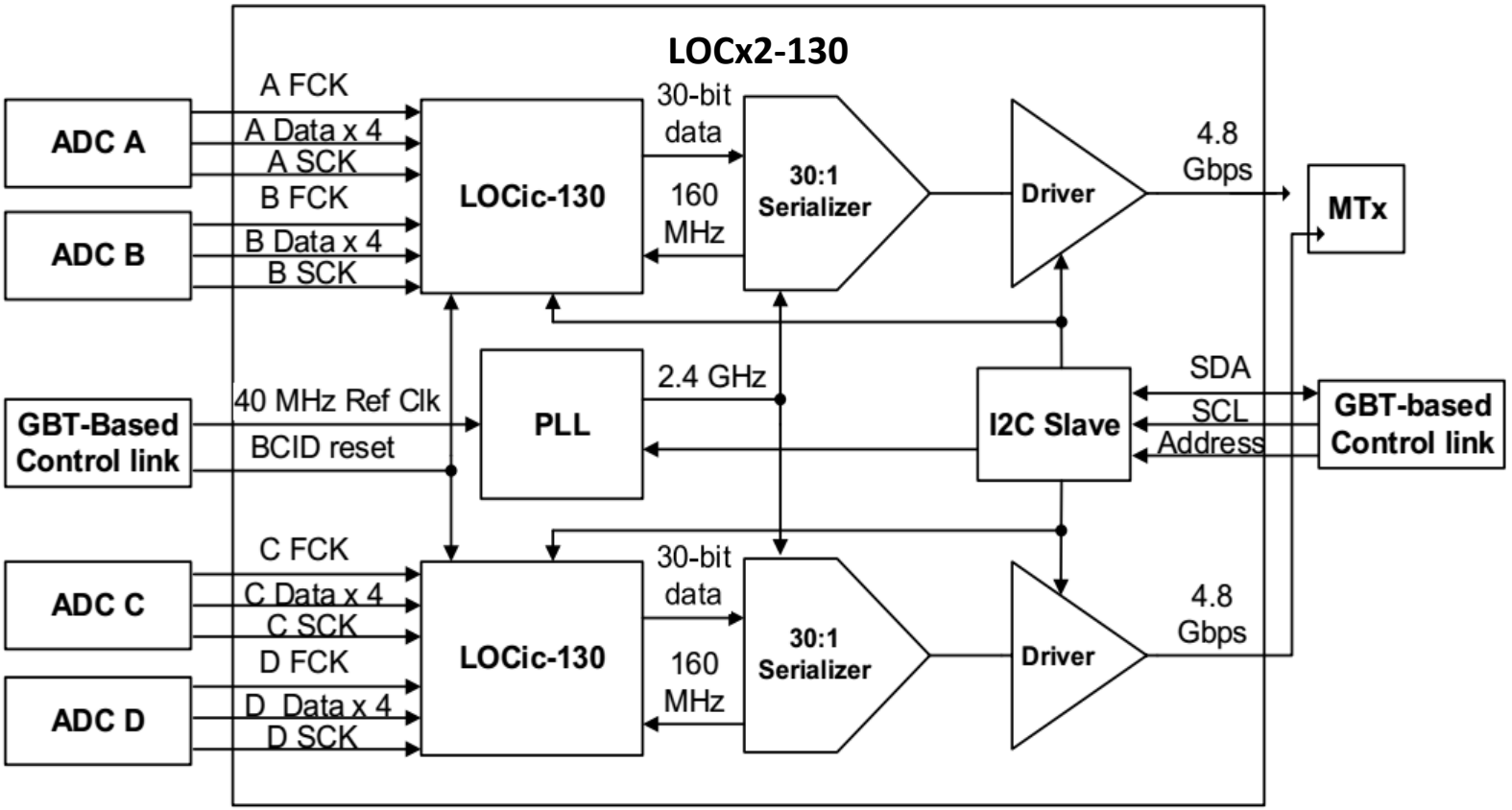
Connectors, Fibres (CERN-EN)

Laser Driver LDQ10 (SMU)



Collaboration in ASICs and Modules

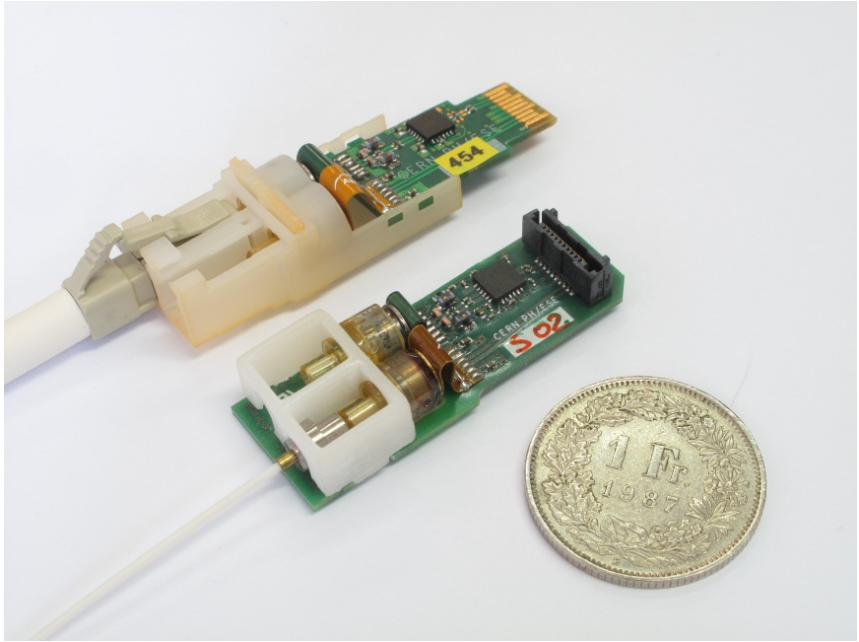
- One example on collaboration in ASIC development

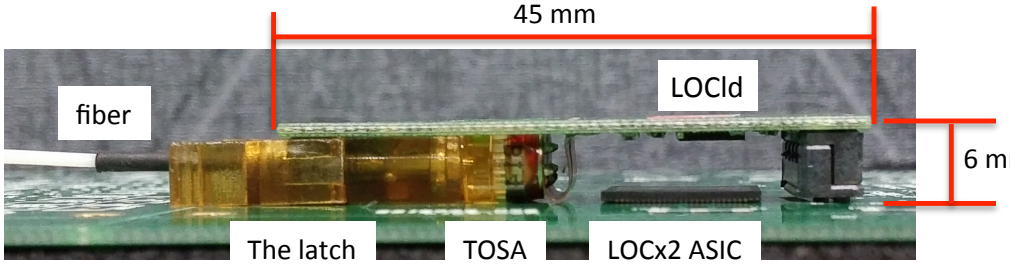


A drop-in backup to LOCx2 successfully developed in 6 months, reusing design blocks from GBTx, TDS (ATLAS muon).

Collaboration in ASICs and Modules

- One example on collaboration in optical module development
  - The idea of MTx comes from the VL common project but developed to meet the requirement in ATLAS/LAr.





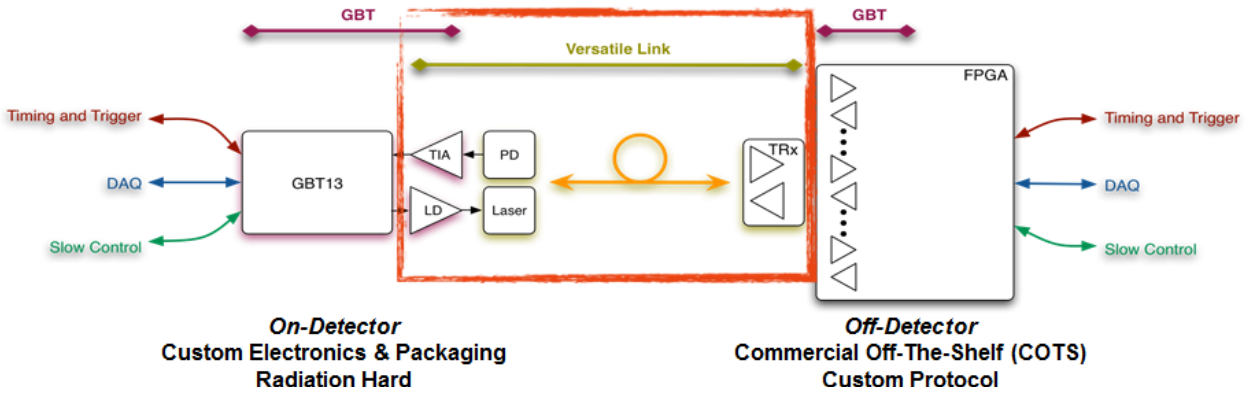
Summary

- The development on the optical link has become more and more challenging.
- The CERN centered common projects are set up to meet the requirements in the LHC upgrades.
- Not all requirements can be met by these common “products”. R&Ds are on-going to address those particular needs.
- The best model would be to collaborate in common projects to address, well, common needs, and to build on design blocks developed in the common projects and develop ASICs/modules to address particular needs.

Thanks!

Backup Slides

The Versatile Link Application Note



Abstract:

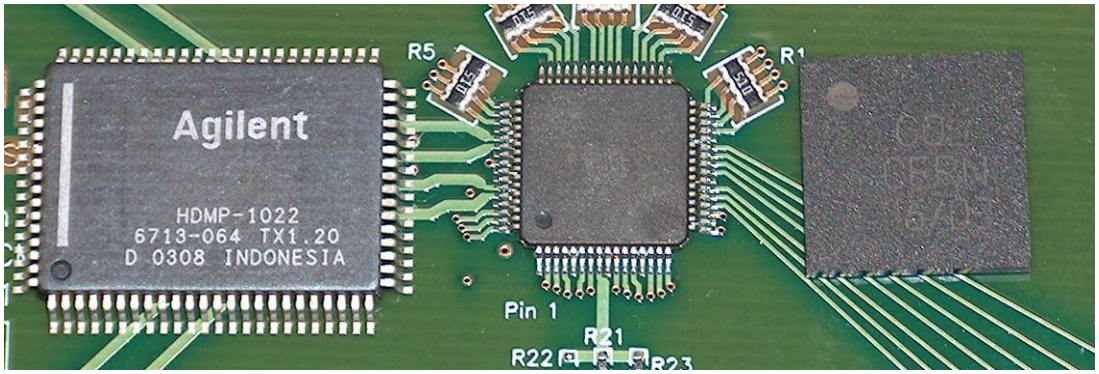
This application note describes how to implement a Versatile Link-based system in a typical High Energy Physics experiment. It summarizes the most relevant Versatile Link features and available options, and points to the relevant documentation. It guides the optical system designer in his/her engineering effort, highlighting in particular those system aspects that are not directly or fully covered by the Versatile Link specification.

1 to 2 Gbps serialisers, why GOL

G-Link
1.25 Gbps

TLK2501
2.5 Gbps

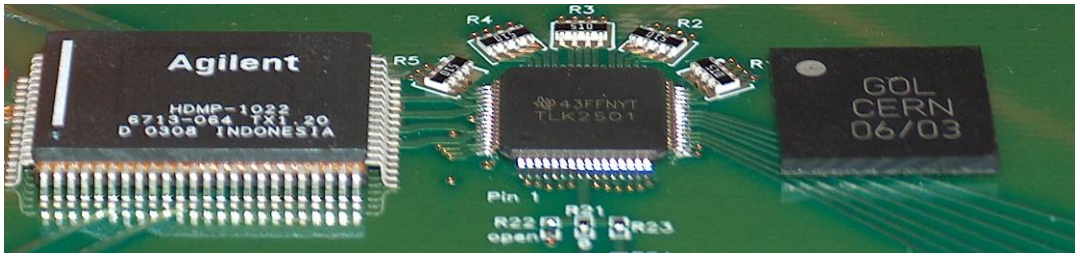
GOL
1.6 Gbps



Rad-hard
Bi-polar, 2.5 W

Rad-soft
360 mW

Rad-hard by design,
400 mW LD driver included



23.2×17.2mm^2×2.7mm
Price: $50/pcs

12.2×12.2mm^2×1mm

13×13mm^2×1.7mm
Price: $15/pcs