RD53 Model of ASIC Development

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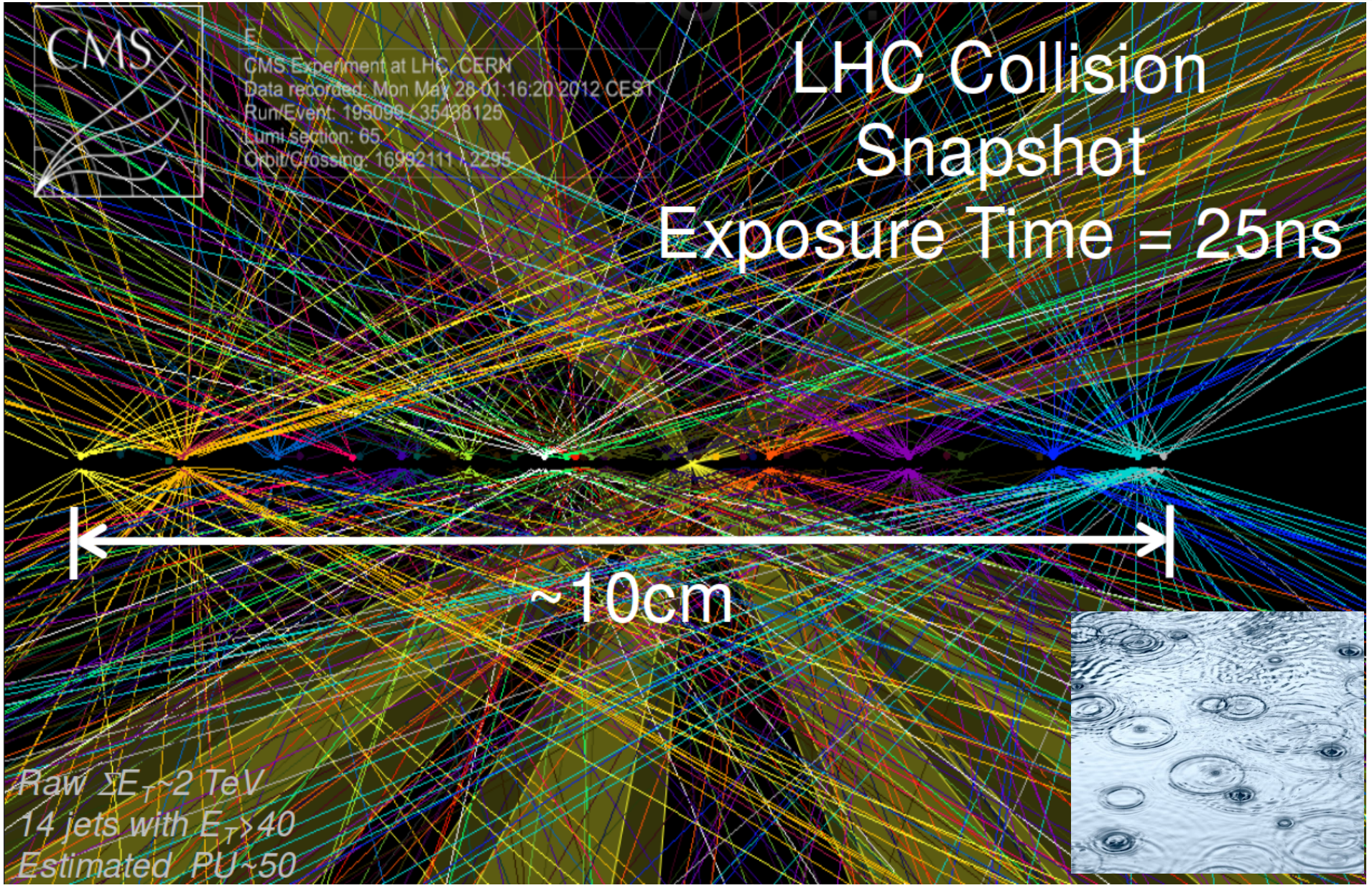
Lawrence Berkeley National Lab

CPAD 2017, UNM
Oct. 13, 2017

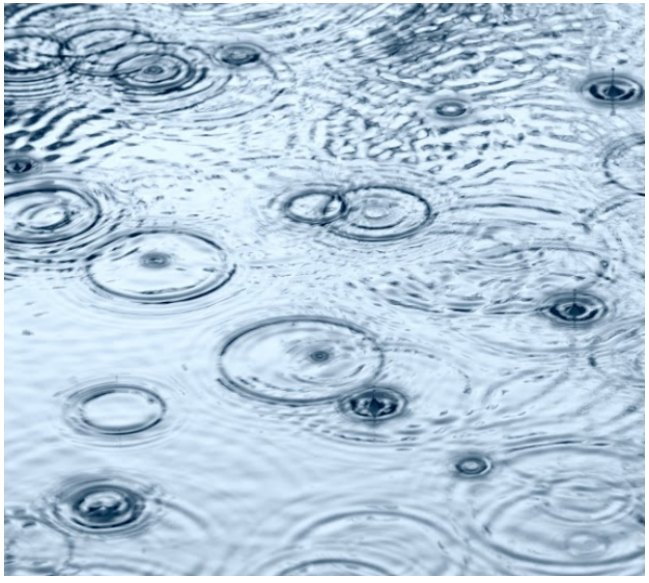
Obligatory Pileup Slide



Rate

Particles / Hits

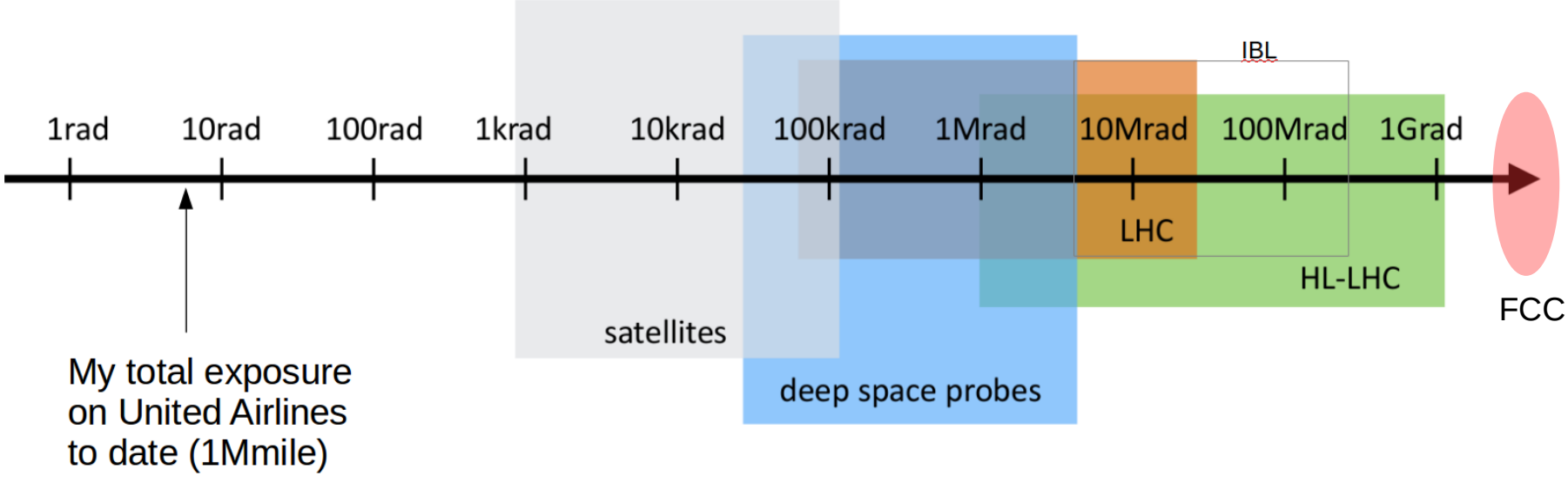
LHC



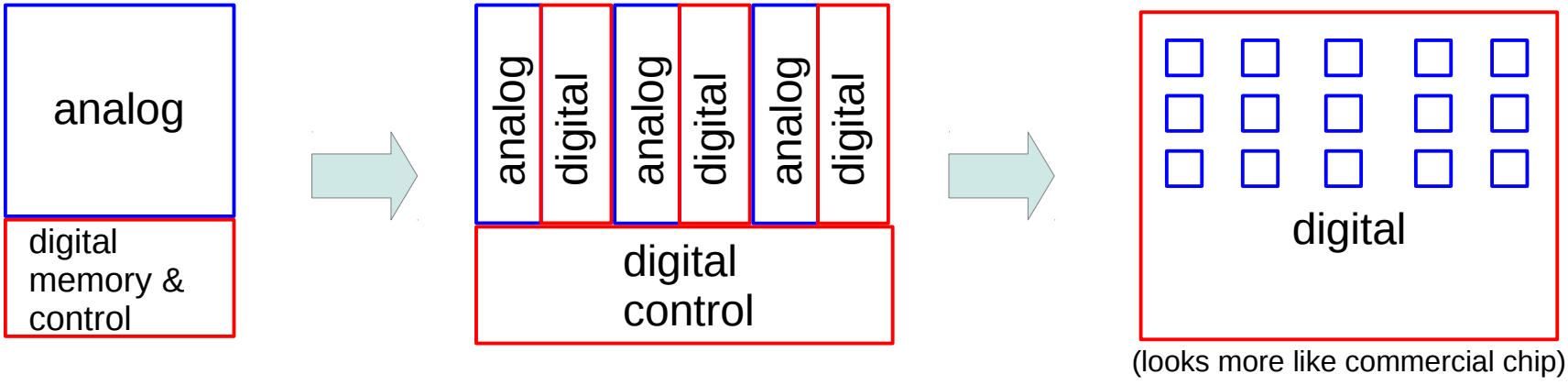
HL-LHC

* Store full time sequence of drops until trigger (not collect in a bucket)
* Can quantify rate as memory bits / area / time
  (note: no mention of pixel size)

Radiation


IBL
1rad
10rad
100rad
1krad
10krad
100krad
1Mrad
10Mrad
100Mrad
1Grad
LHC
HL-LHC
FCC
satellites
deep space probes
My total exposure
on United Airlines
to date (1Mmile)

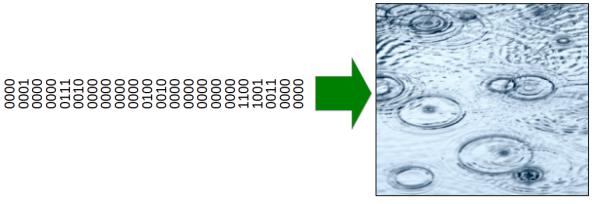
Readout Chip Evolution



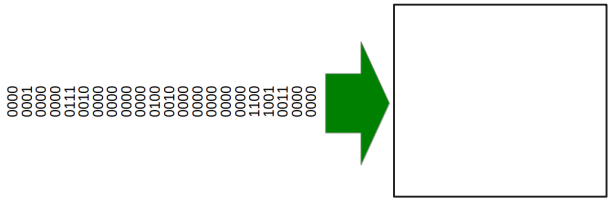
10 yrs ago

today

HL-LHC



<1 Gbps/cm^2

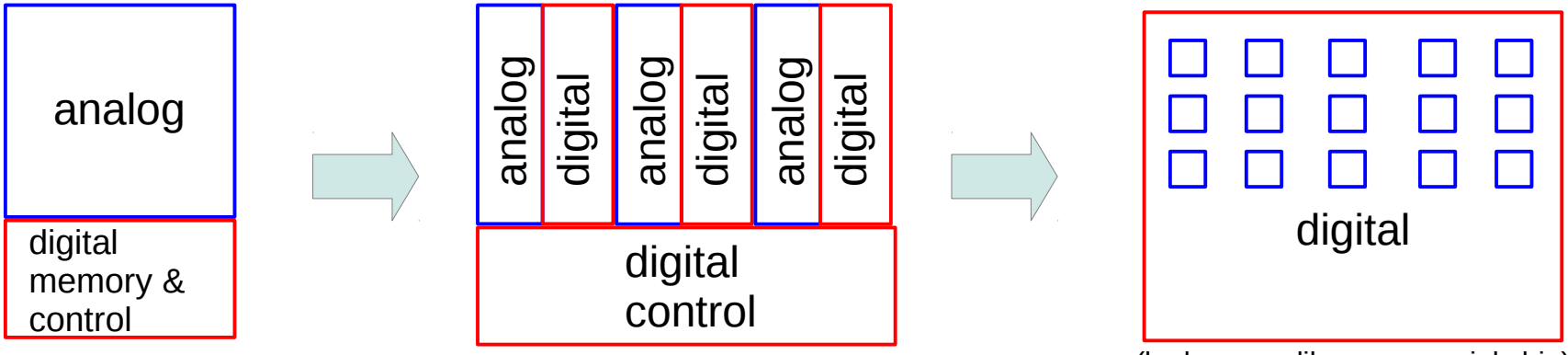


5 Gbps/cm^2

40 Gbps/cm^2

Another way to say memory per unit area: Logic Density.
We follow Moore's Law.

Collaborative Design



(looks more like commercial chip)

Single institute team

Participating institutes:

Bonn: D. Arutinov, M. Barbero, T. Hemperek, A. Kruth, M. Karagounis.

CPPM: D. Fougeron, M. Menouni.

Genova: R. Beccherle, G. Darbo.

LBNL: S. Dube, D. Elledge, M. Garcia-Sciveres, D. Gnani, A. Mekkaoui.

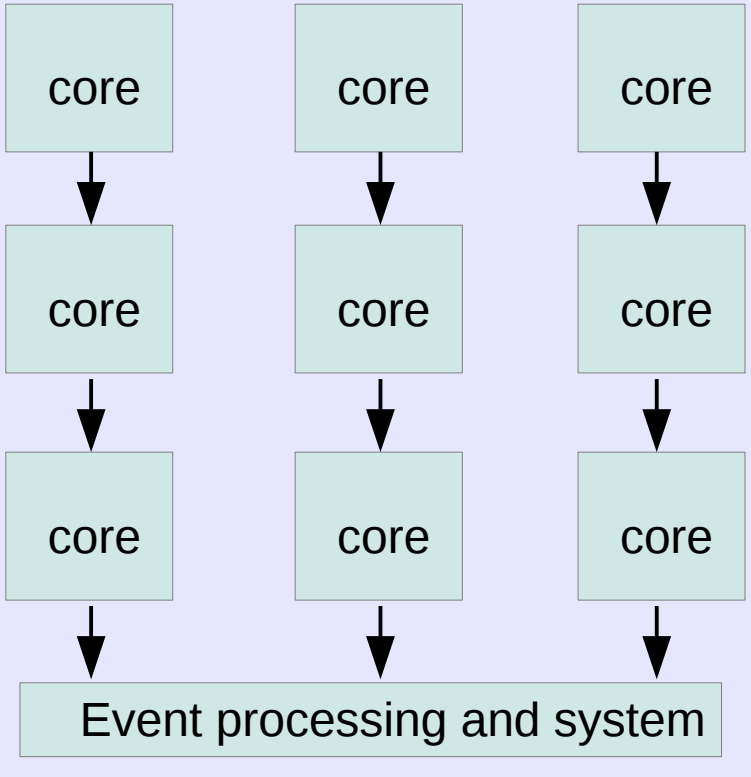
Nikhef: V. Gromov, R. Kluit, J.D. Schipper

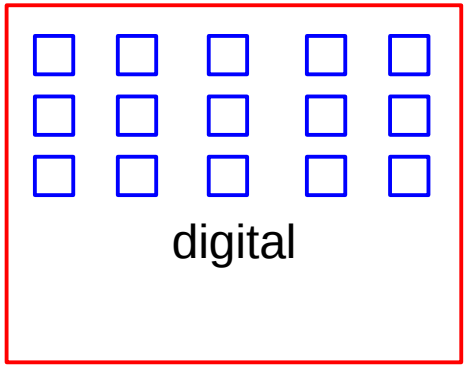
2nd RD53 meeting. Oxford 2014

Digital on Top

Design procedure is closer to writing and compiling code
Than to drawing.
Heavy use of automated tools and modeling

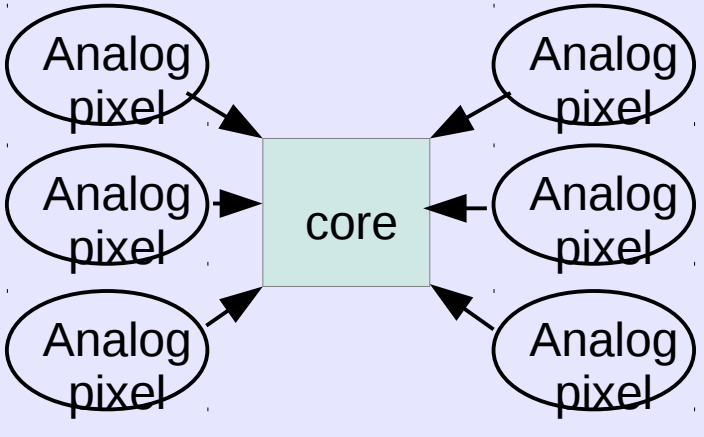
Concept Slide from Pixel 2012



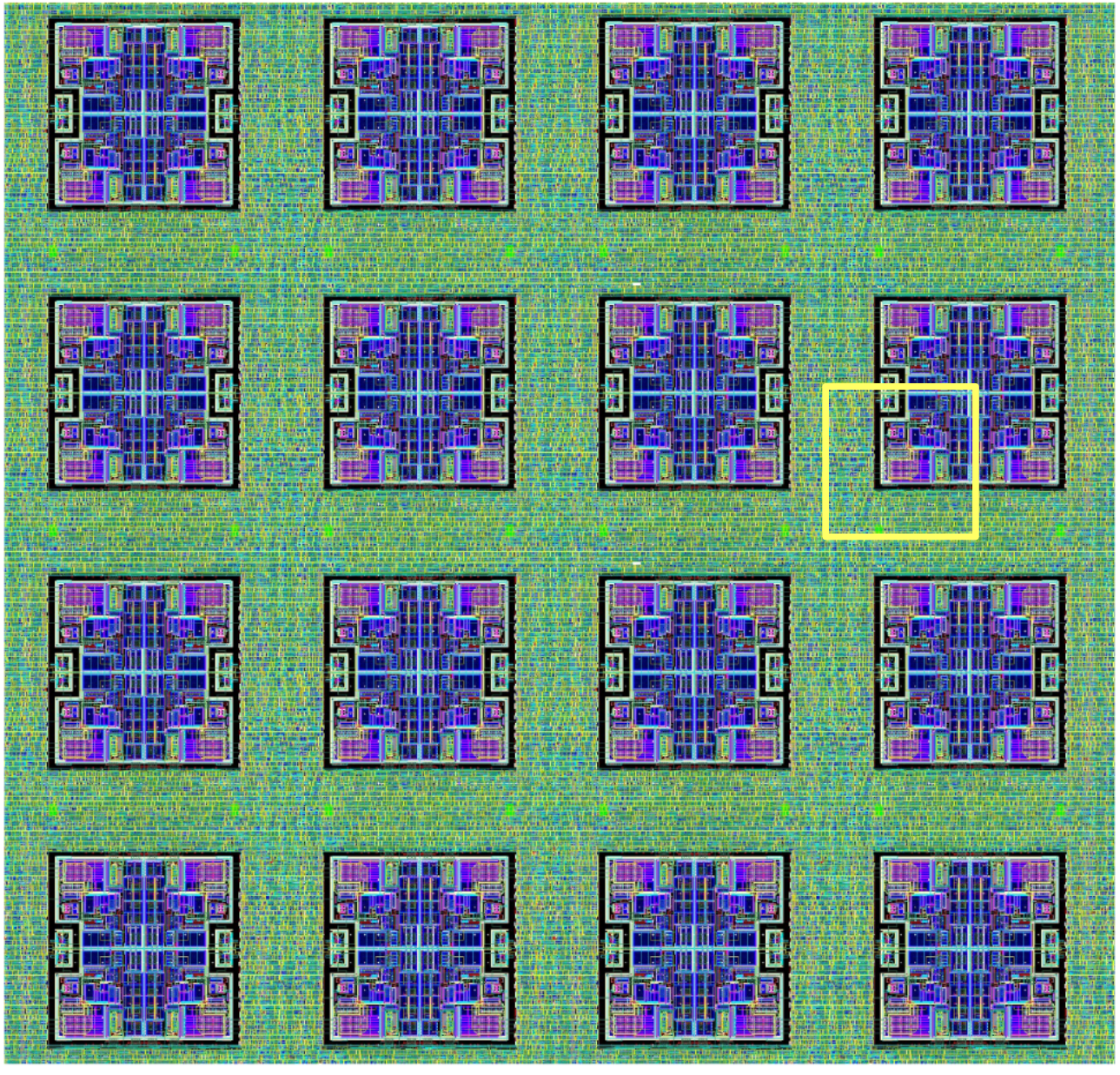


(looks more like commercial chip)

HL-LHC



One RD53A Chip Core



One flat synthesized circuit
Each pixel is different !

Whole block is stepped and repeated

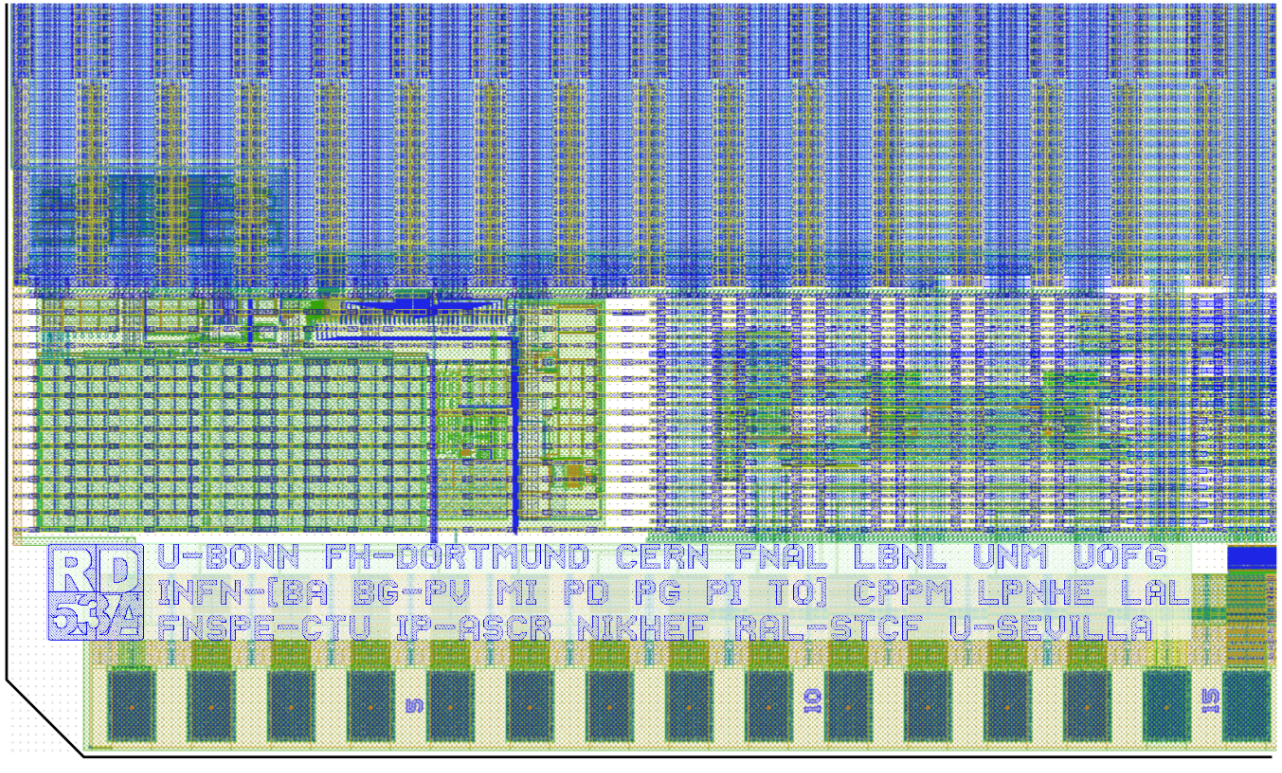
~ 200k transistors
Size chosen so it CAN be SPICE simulated
(ask Dario how long it runs)

(routing dominated re: metal stack)
(both A and D substrate isolation)

RD53A submitted

1.2cm

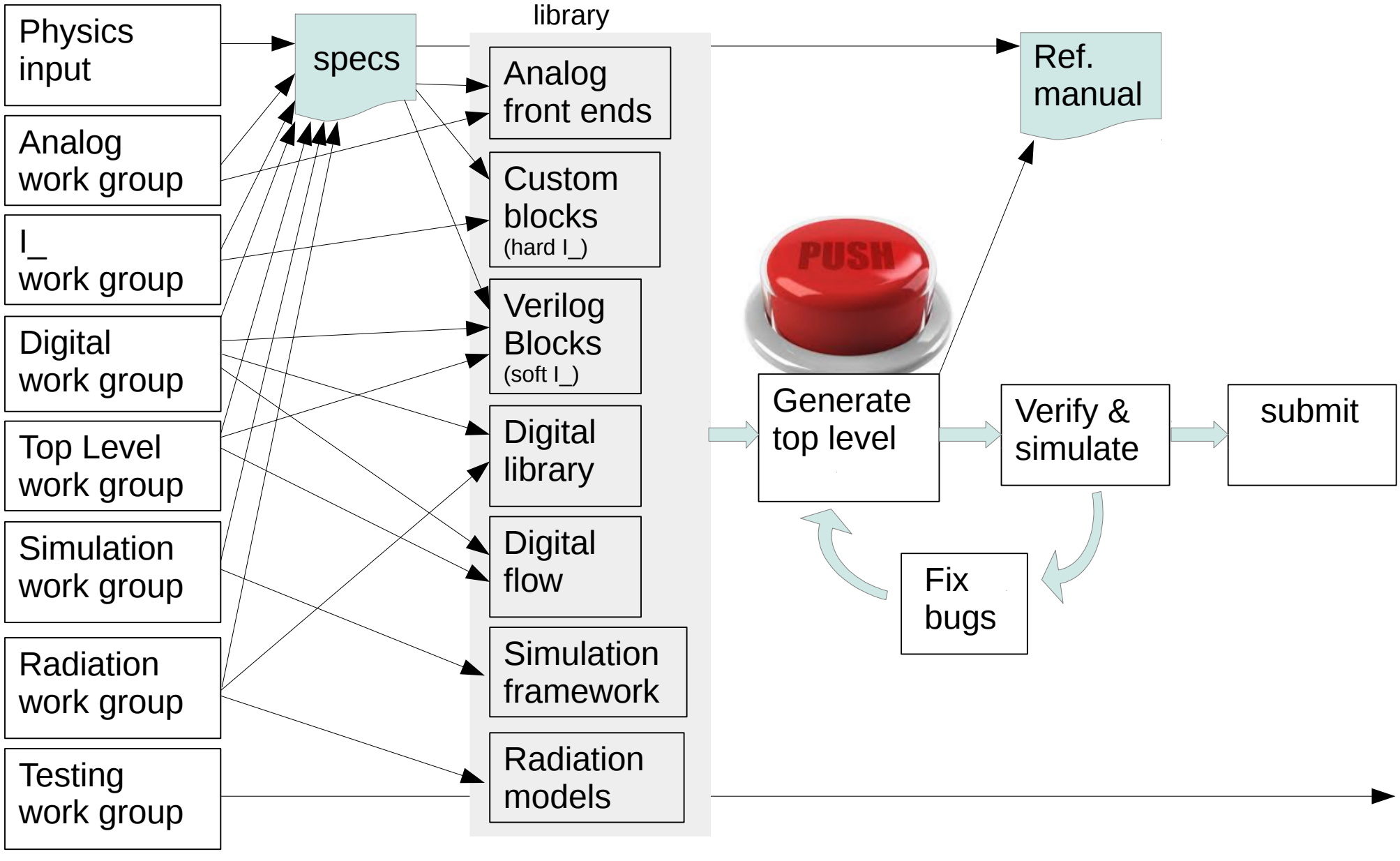
400 x 192 pixels



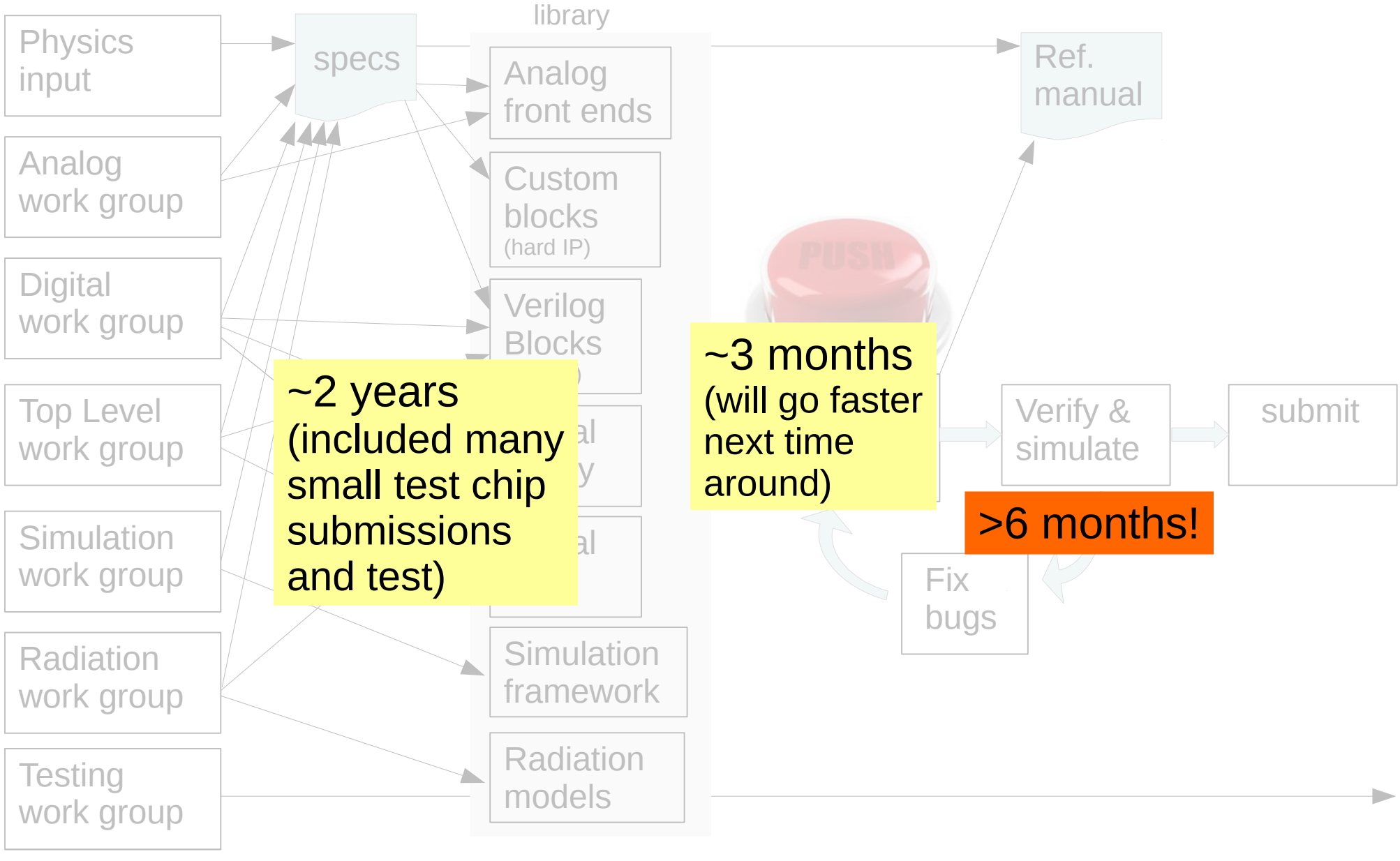
2cm

Expect delivery of 12 wafers (300mm dia.) late November

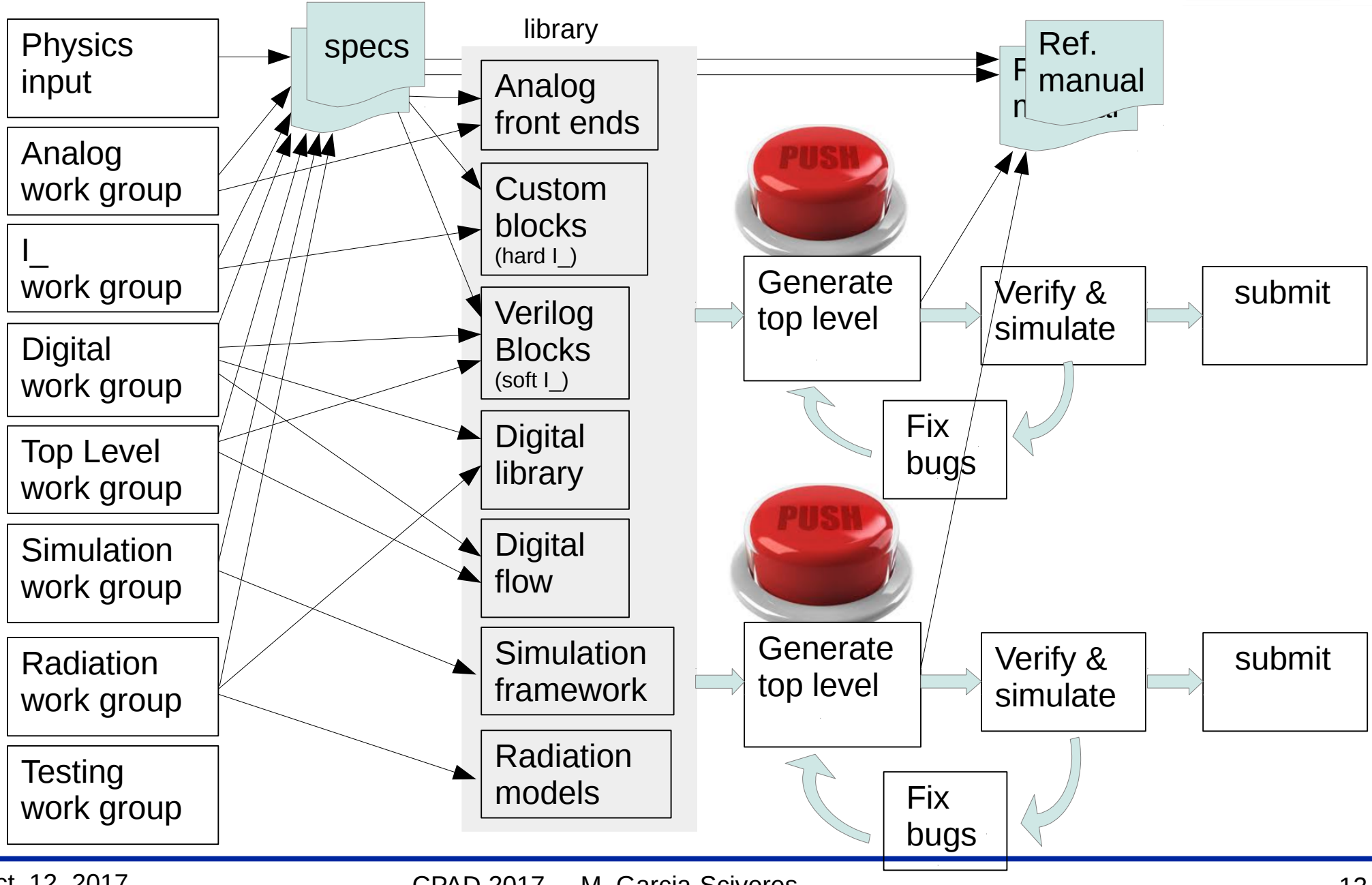
Development Model



Development/Design Time



Multiple Chips



Rad Hard Logic Density Scaling

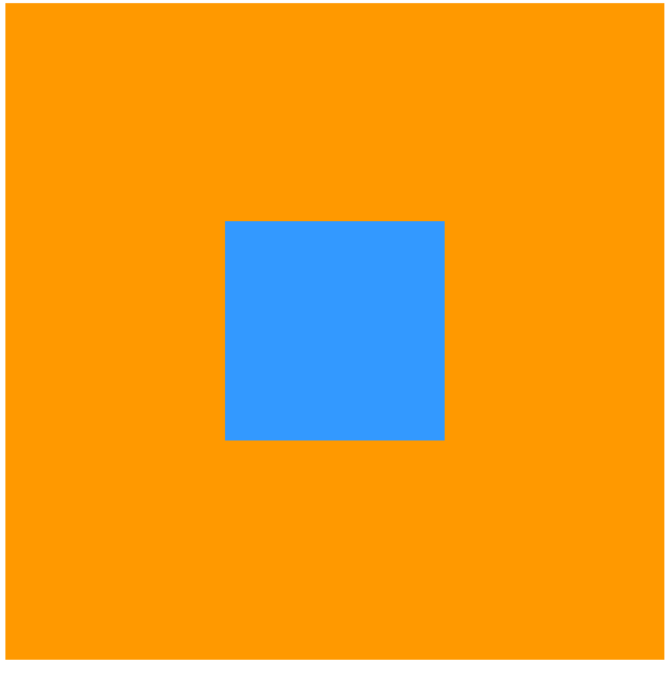
28nm ?

65nm

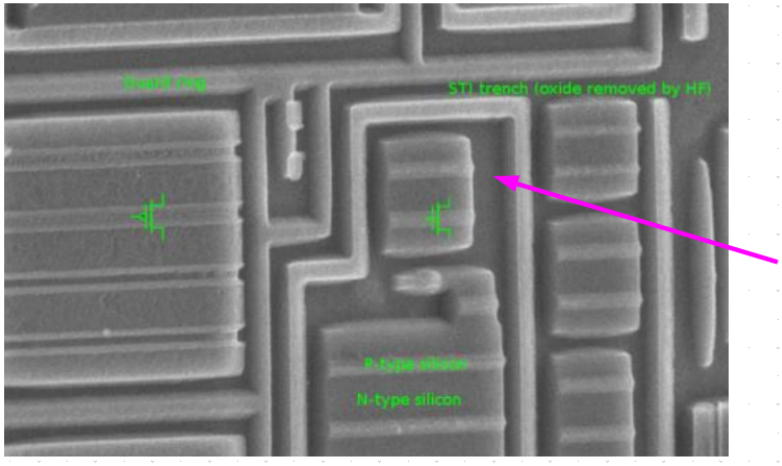
Not quite minimum size due to pesky radiation damage

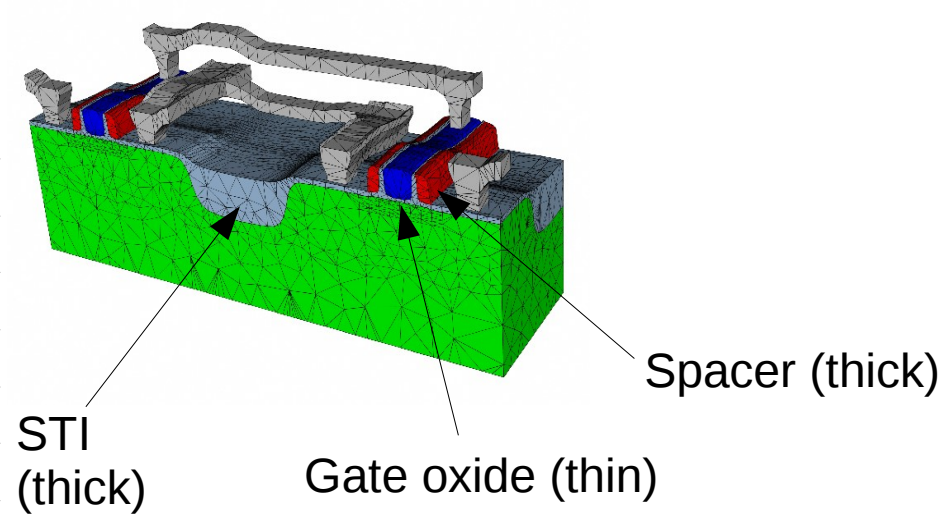
130nm

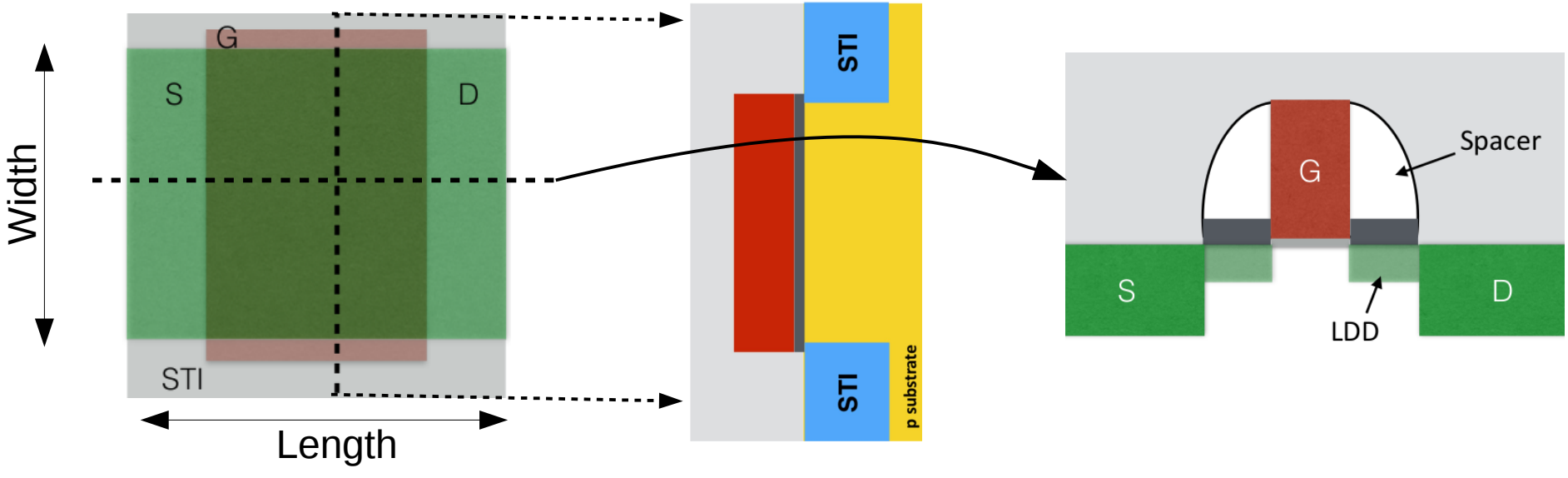
0.25um
ELT



STI, Gate, Spacer



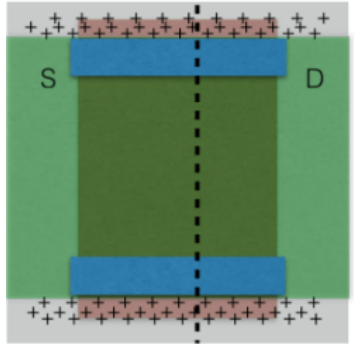


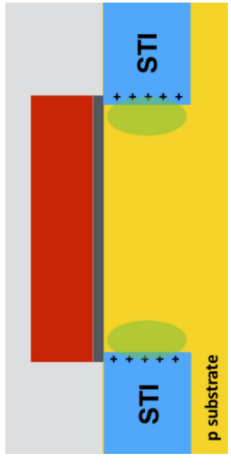


RINCE: STI damage

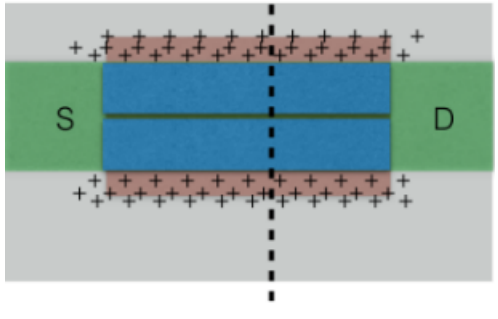
Radiation Induced Narrow Channel Effect

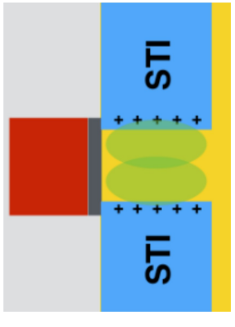
Wide Transistor

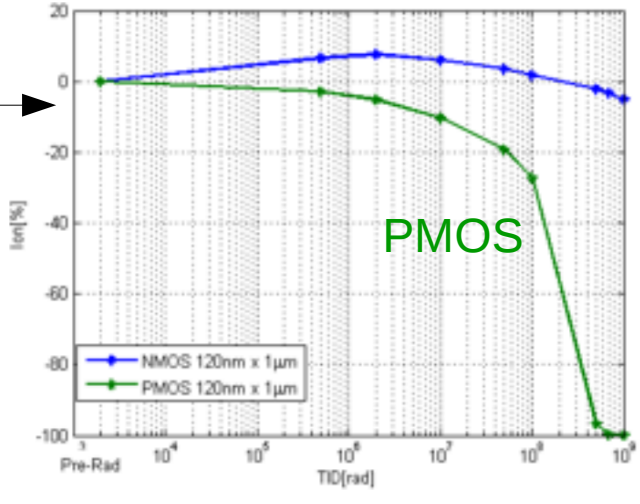




Narrowest Transistor







NMOS

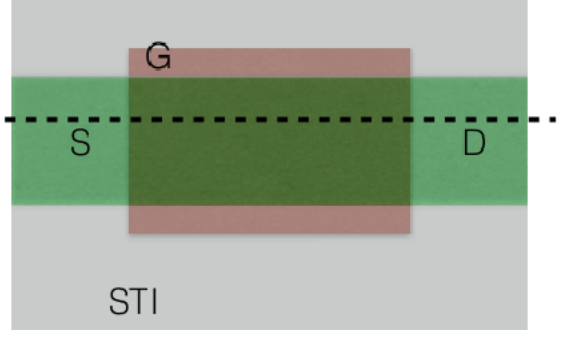
PMOS

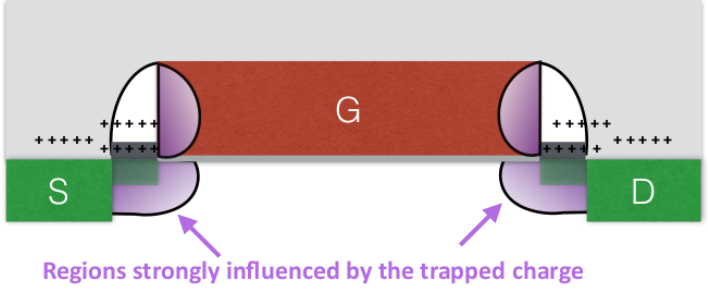
1Grad

RISCE: spacer damage

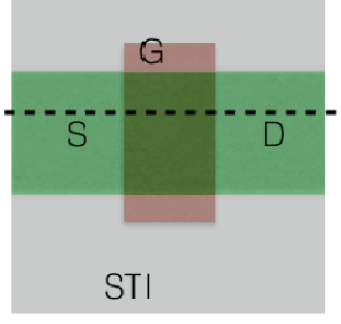
Radiation Induced Short Channel Effect

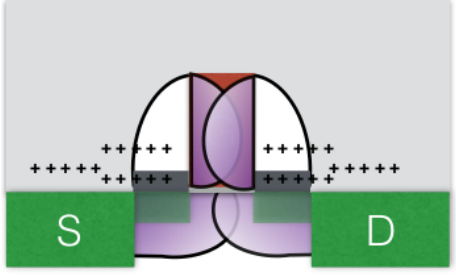
Long Transistor

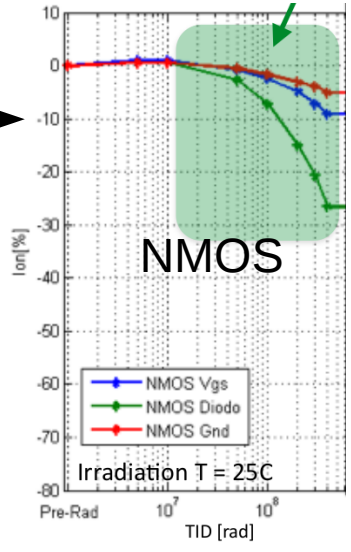


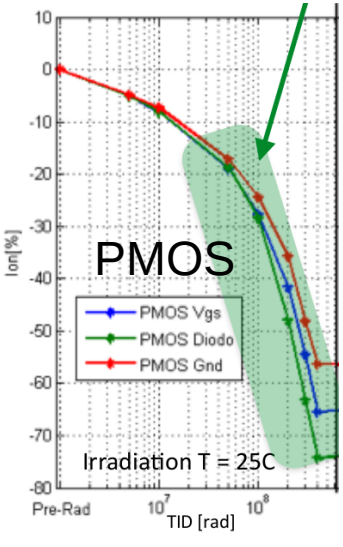


Shortest Transistor









Temperature, Time, Dose rate, Process

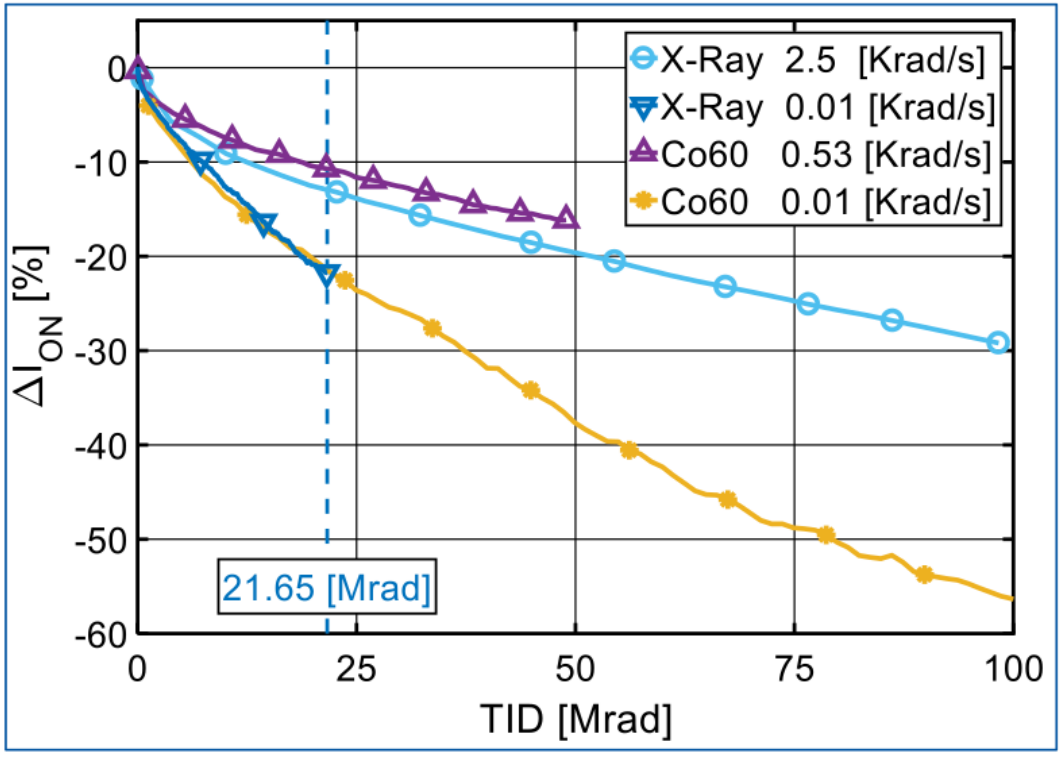
It DOES work up to 1Grad

Analog circuits no problem. Several test chips irradiated this high and work fine

Digital (small transistors)
If you operate cold, you don't heat it up under power (just like sensors),
low dose rate is not worse than expected, and you don't get unlucky with process

We will have RD53A chips working after 1Grad (if it works at all), but we only guaranteed specs up to 500Mrad. See Sandeep's talk

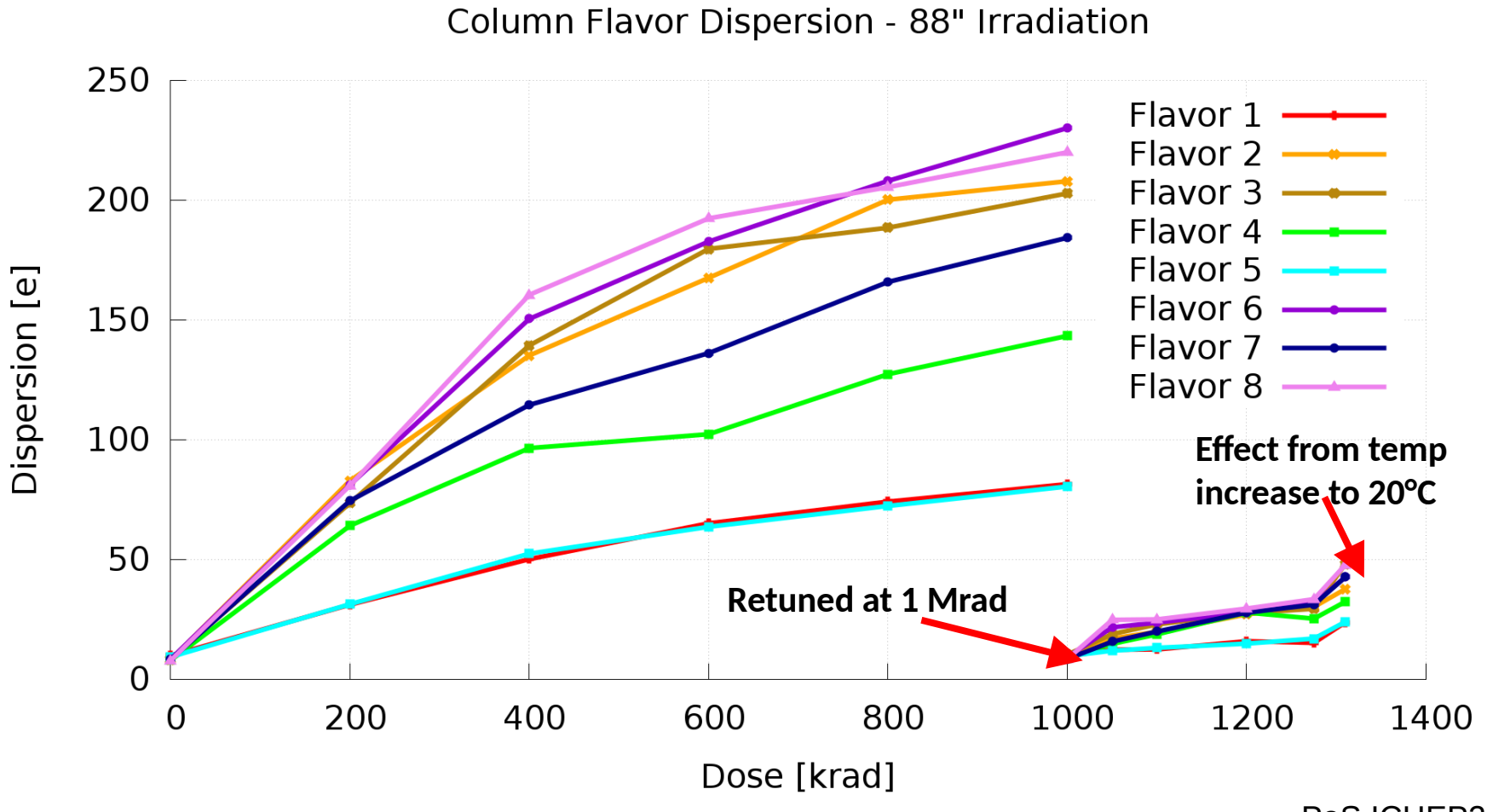
Radiation damage must be simulated and treated like other design corners



New concerns: Low dose rate is not so low

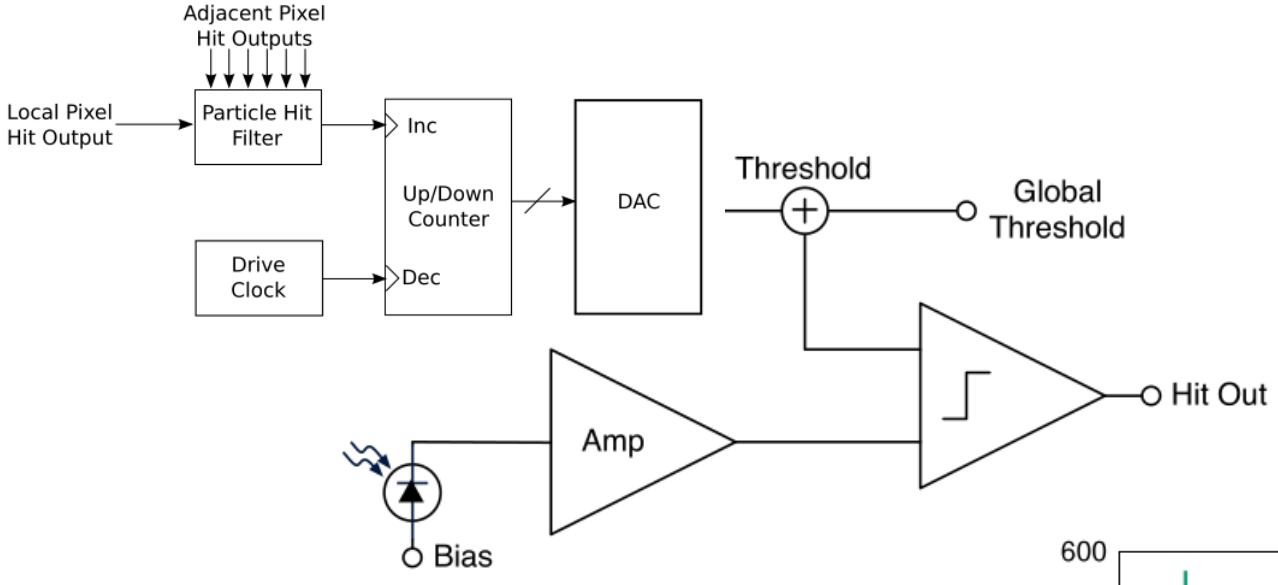
1 Mrad per run at HL-LHC ! But dose rate here was ~5x higher than at HL-LHC

Threshold Dispersion vs. Dose

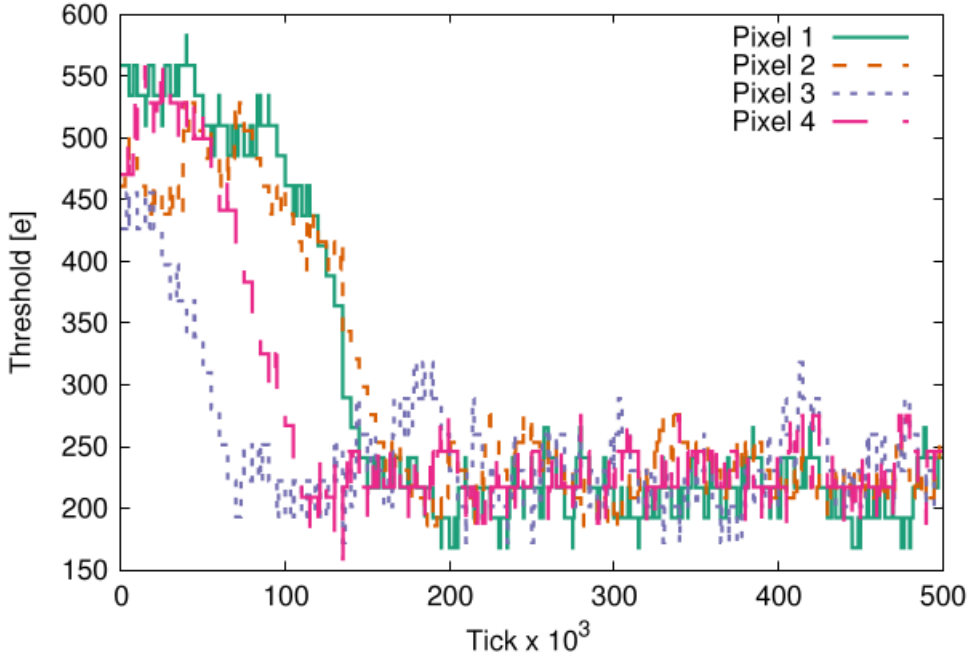


PoS ICHEP2016 p. 272

Self-tuning threshold



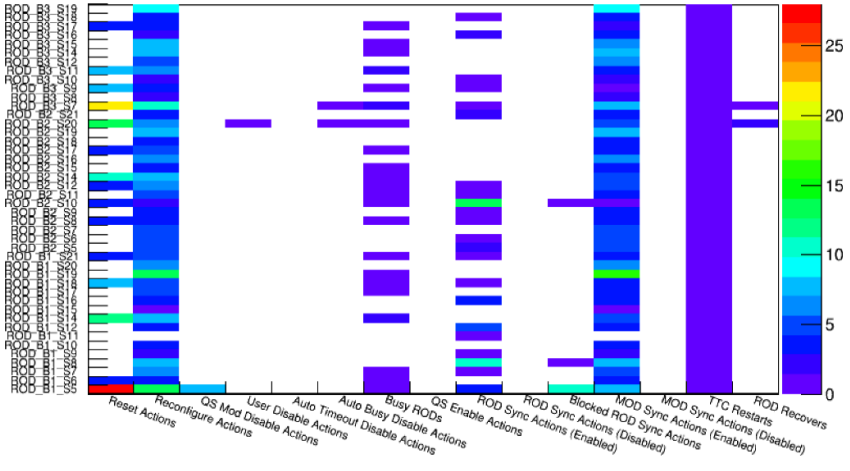
- Adjust each pixel threshold to a constant rate of noise hits
- Noise hits are selected by topology (isolated)
- Selection does not need to perfect- can be quite poor even.

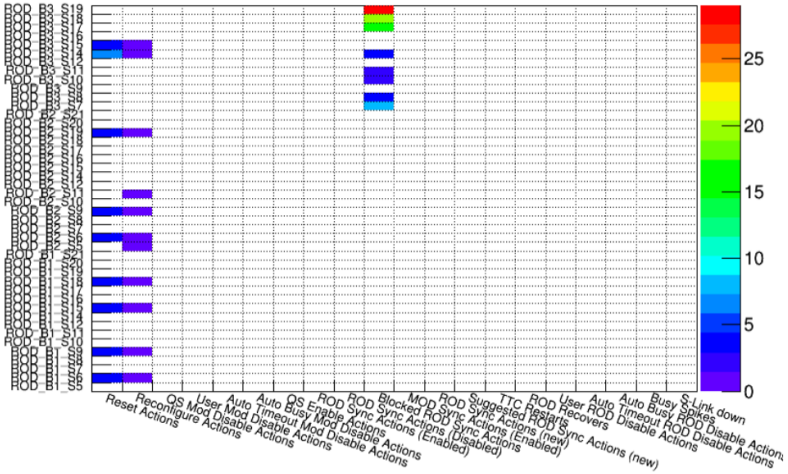


Nucl. Instrum. Meth. A867 (2017) p. 209-214

SEU

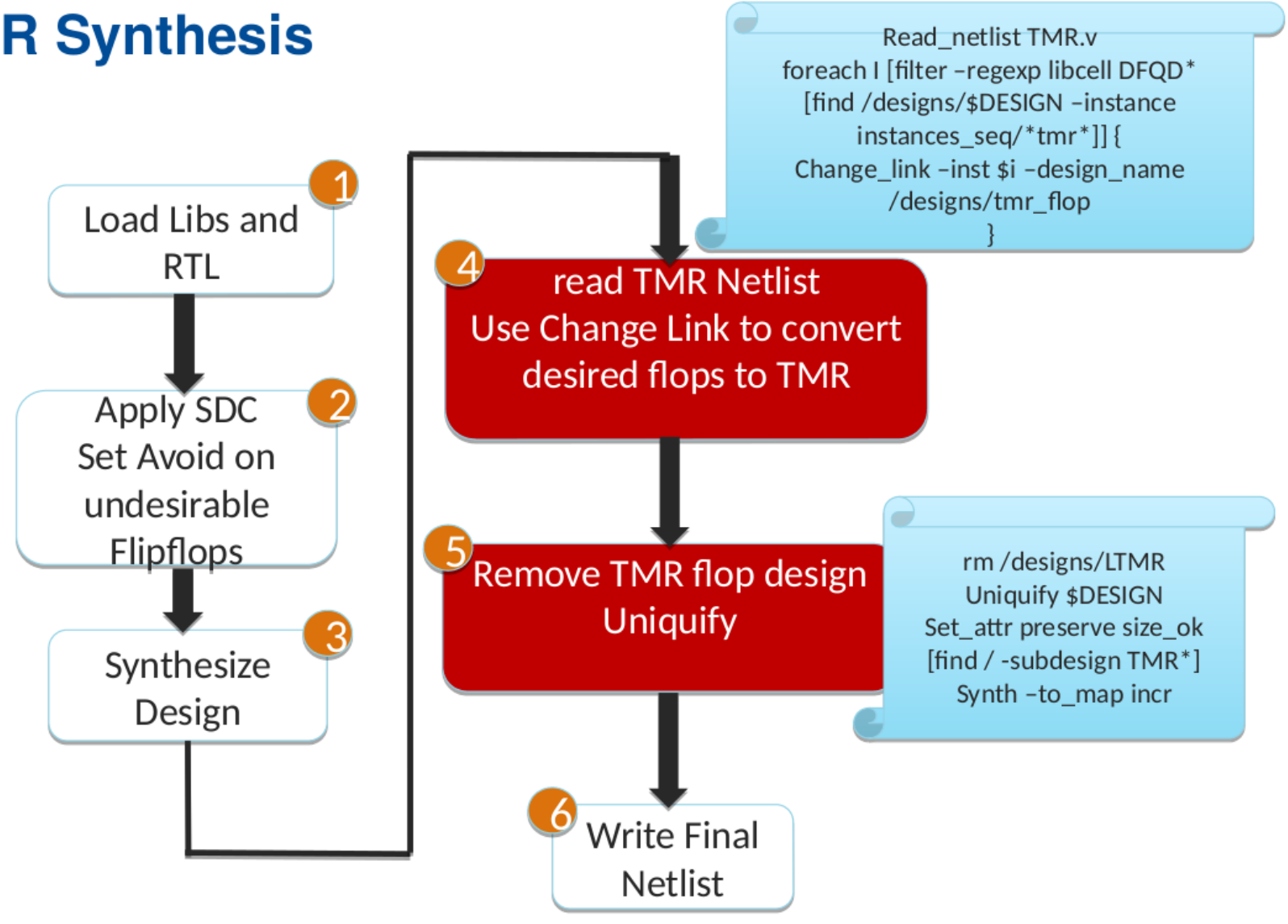
- Traditional approach of memory SEU hardening is dead
  - Upset rate gets too high even with hardening
  - Still need to harden logic / controls: incorporated into synthesis
- A digital chip does not need SEU-hard storage
  - Continuously reprogram everything
    - Plenty of bandwidth, plenty of processing power to handle triggers and reconfiguration at the same time
  - Interestingly, ATLAS pixel operation already trying to do this as best we can. Not the way operation was envisioned, but reset/reconfigure everything one can every 5s gives most stable operation





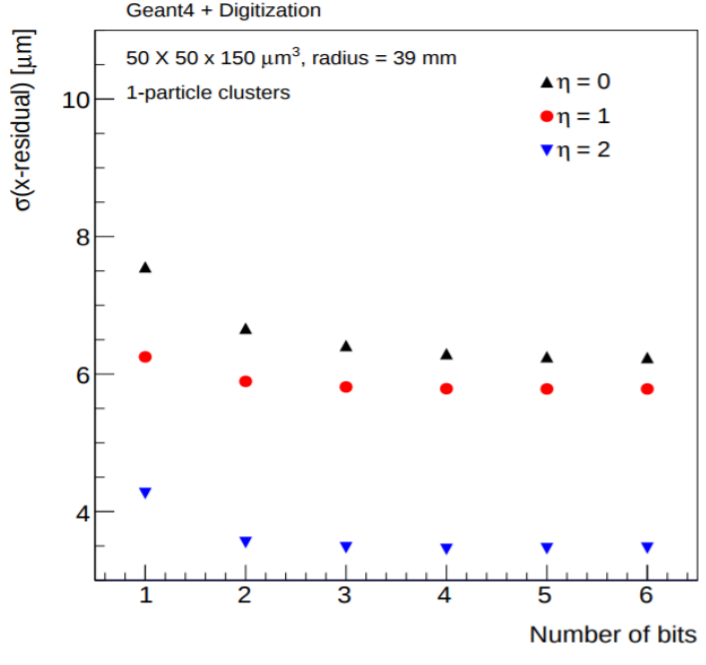
SEU hardened logic synthesis

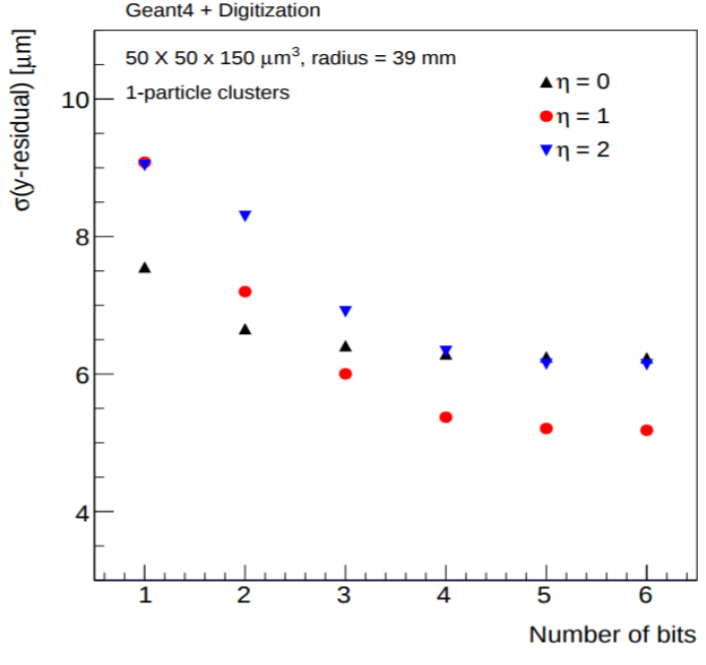
TMR Synthesis



Other points (not rate or radiation)

- Single pixel gets “easier” due to smaller capacitance (eg. no timewalk)
- But total power budget gets more challenging (capacitance per unit area goes up- scales with perimeter, not area)
- At what point should we go binary?
- High bandwidth data transmission. Data compression.





arXiv:1710.02582

Where next?

- Higher logic density
- Higher radiation dose
- Smaller pixels
- More functionality

- R&D into smaller features
- Followed by another collaboration to make next gen. chip

28nm to 1Grad

after C.Zhang et al., "Characterization of GigaRad Total Ionizing Dose and Annealing Effects on 28 nm Bulk MOSFETs", accepted for publication in IEEE TNS, to be published soon

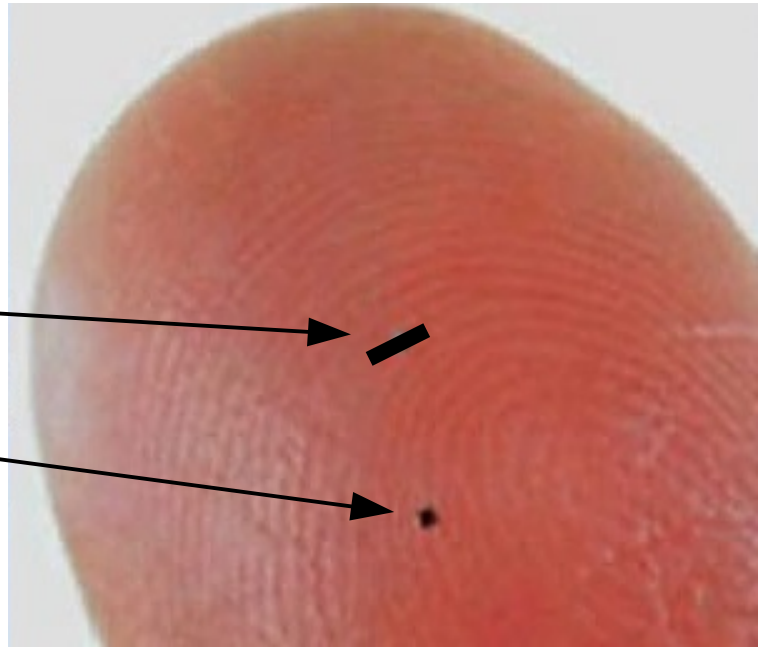
Conclusion

- Model worked well, but aske me again end of November after we have the chip back
- RD53 has now been promoted to “job shop” to deliver production chips to ATLAS and CMS
- Model was set up to allow multiple “top levels” from the begining

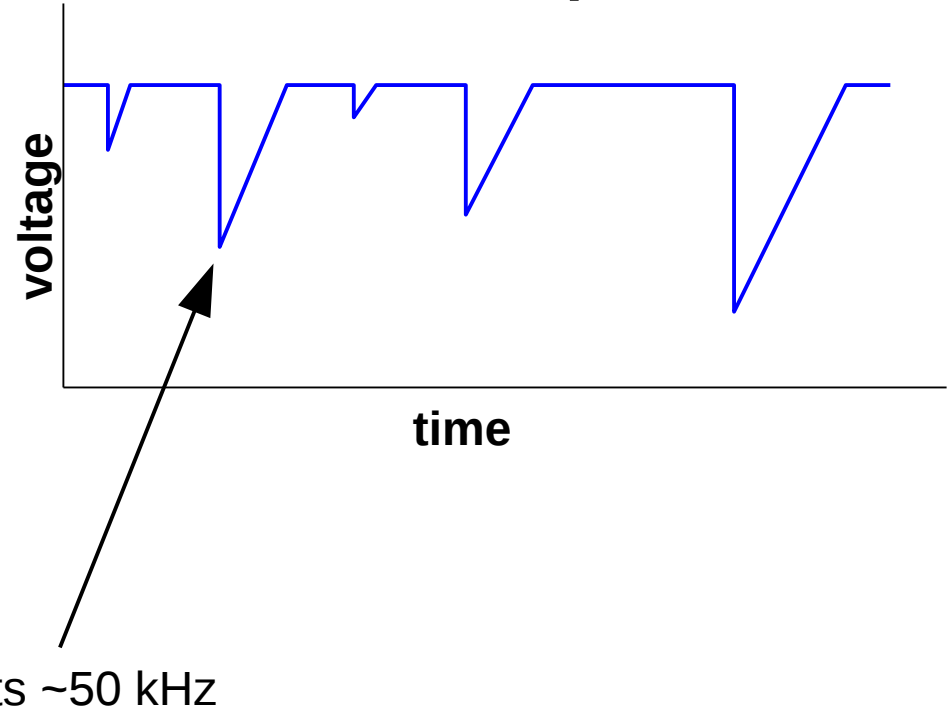
B A C K U P

Single Pixel Perspective

Pixel size

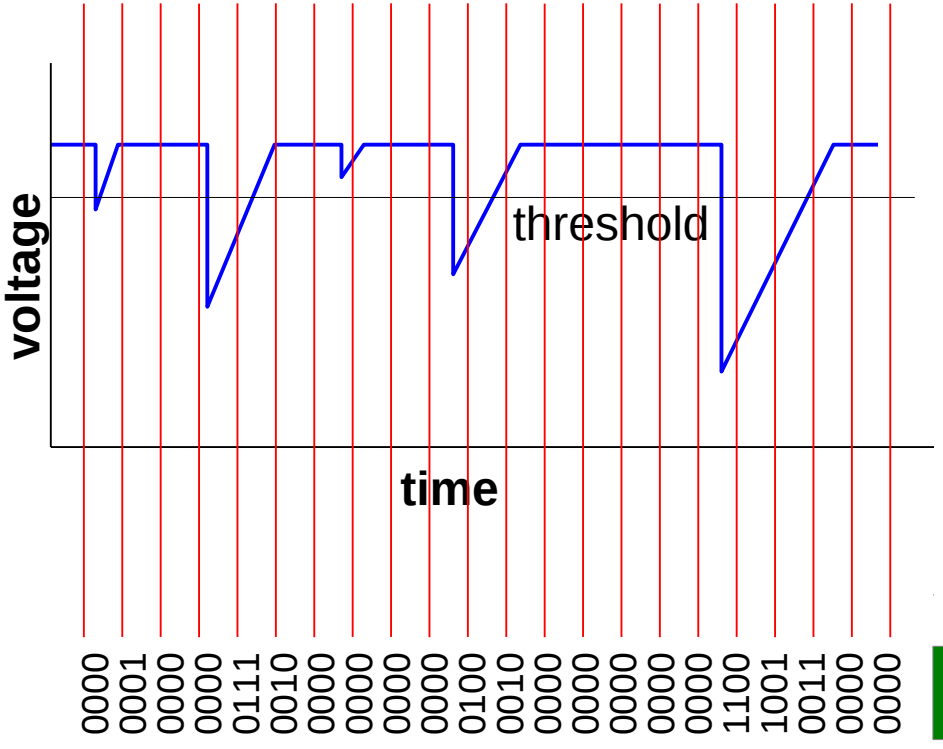


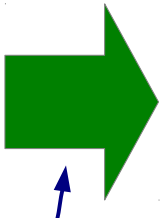
Pixel output

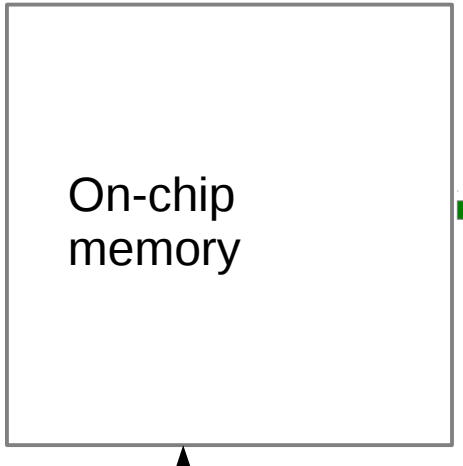


- For 50um x 50um HL-LHC pixels up to 3Ghz / sq. cm. In ATLAS / CMS
- Need to save these hits FOR ENTIRE TRIGGER LATENCY (12µs up from 6µs)

On-Chip Storage and Trigger







Readout
~5Gbps
cable limit

Storage of all
individual hits
W/ ADC value

Triggers (selected slice times)

IC Electronics Radiation Damage

- Change in effective doping is insignificant, because doping levels in CMOS transistors are very high.
- All radiation damage effects to CMOS are due to parasitic electric fields form charge trapped in oxides and oxide-silicon interfaces
- Meet the oxides:
  - Gate oxide
  - Field Oxide
  - Buried Oxide (only for SOI)
  - Shallow trench Isolation (STI)
  - Gate Spacer