SUMMARY/HIGHLIGHTS OF TRIGGER & DAQ

Darin Acosta, Jinlong Zhang

Agenda

12:30 **LHCb TDAQ** *30'*

A major upgrade of the LHCb detector and DAQ systems is planned for the LHC long shutdown II (2019-2020). For this upgrade a purely software-based trigger system is being developed to replace the current multi-stage hardware and software trigger. The new system will process the full 30 MHz bunch-crossing rate delivered by the LHC while running at five times the present instantaneous luminosity. The physics reach of the upgraded detector will be enhanced by the Turbo paradigm, where high-level reconstructed objects are persisted along with a subset of the raw event data.
In this talk we will describe the LHCb detector upgrade and discuss the plans and progress towards performing event reconstruction and selection at 30 MHz using modern CPU architectures.

Speaker: Olli Lupton (CERN)
Material: Slides

13:00 **ATLAS Trigger Upgrade Plans for the High Luminosity LHC** *25'*

By 2026 the High Luminosity LHC will be able to deliver 14 TeV proton-proton collisions with an order of magnitude higher instantaneous luminosity than the original design, at the expected value of 7.5 × 10^34 cm−2s−1. The ATLAS experiment is planning a series of upgrades to prepare for this new and challenging environment, which will produce much higher data rates and larger and more complex events than the current experiment was designed to handle. The broad physics program planned for this fourth LHC run is driving the full upgrade plan, which will involve major changes in the detectors as well as in the trigger system. One key aspect driving the trigger system design is the need for rate reduction, which will be based on easily identifiable high momentum electrons and muons. However, hadronic final states are also becoming important for investigations of the full phase space of the Standard Model and beyond. This motivates the inclusion of both higher resolution first-level trigger information and a new hardware tracking system. This presentation will describe the baseline architecture established for the High Luminosity LHC, while also detailing the new system components and their interconnections.

Speaker: Stephanie Majewski (University of Oregon)
Material: Slides

13:25 **Overview of the HL-LHC Upgrade for the CMS Level-1 Trigger** *25'*

The High-Luminosity LHC will open an unprecedented window on the weak-scale nature of the universe, providing high-precision measurements of the standard model as well as searches for new physics beyond the standard mode Such precision measurements and searches require information-rich datasets with a statistical power that matches t high-luminosity provided by the Phase-2 upgrade of the LHC. Efficiently collecting those datasets will be a challengi task, given the harsh environment of 200 proton-proton interactions per LHC bunch crossing. For this purpose, CMS is designing an efficient Level-1 hardware trigger that will include tracking information and high-granularity calorimet information. The system design is expected to take full advantage of advances in FPGA and link technologies over the coming years.

Speaker: Richard Cavanaugh (University of Illinois at Chicago and Fermilab)
Material: Slides

13:50 **ATLAS DAQ Upgrade** *20'*
Speaker: Alexander Paramonov
Material: Slides

14:10 **CMS DAQ R&D for HL-LHC** *20'*

I describe the evolution of the CMS DAQ system from today to the baseline system envisioned for the high-luminosi LHC. R&D projects for novel approaches for energy-frontier DAQ systems are discussed.

Speaker: Dr. Remi Mommsen (Fermilab)
Material: Slides

13:30 - 15:30 Data Flow Techniques V: Trigger and Data Acquisition
Conveners: Jinlong Zhang (ANL), Prof. Darin Acosta (University of Florida)
Location: Fiesta Room

13:30 **ANL TDAQ Roadmap** *30'*
Speaker: Alexander Paramonov (Argonne National Laboratory)
Material: Slides

14:00 **BNL TDAQ Roadmap** *30'*
Speaker: Kai Chen (Brookhaven National Laboratory)
Material: Slides

14:30 **Fermilab TDAQ Roadmap** *30'*
Speaker: Sergo Jindariani (Fermilab)
Material: Slides

15:00 **SLAC TDAQ Roadmap** *30'*
Speaker: Mr. Ryan Herbst (SLAC)
Material: Slides

08:00 - 10:00 Data Flow Techniques VII: Trigger and Data Acquisition
Conveners: Jinlong Zhang (ANL), Prof. Darin Acosta (University of Florida)

08:00 **DUNE Trigger and DAQ** *25'*
Speaker: Mathew Graham

08:25 **LZ Trigger and DAQ** *25'*
Speaker: Eryk Druszkiewicz

08:50 **Trigger and DAQ for UHE Neutrino Detection** *20'*
Speaker: Eric Oberla

09:10 **The Data Acquisition of the sPHENIX Experiment at the Relativistic Heavy Ion Collider** *20'*

We will present the design of the sPHENIX data acquisition system, which will implement a streaming readout for the TPC.

Speaker: Martin Purschke
Material: Slides

09:30 **DAQ Workshop Summary** *30'*
Speaker: Kurt Biery

Also DOE DAQ (Pre) Workshop

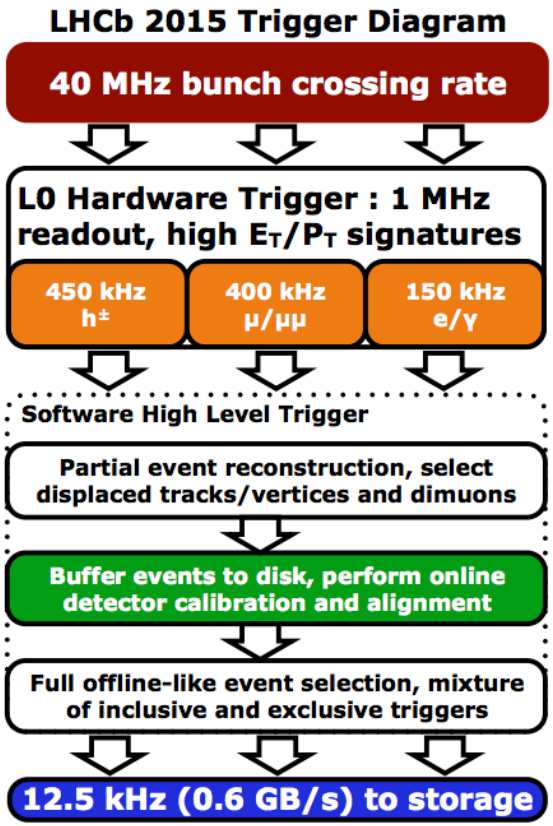
Agenda

Full agenda here: https://indico.fnal.gov/event/14744/timetable

Summary:

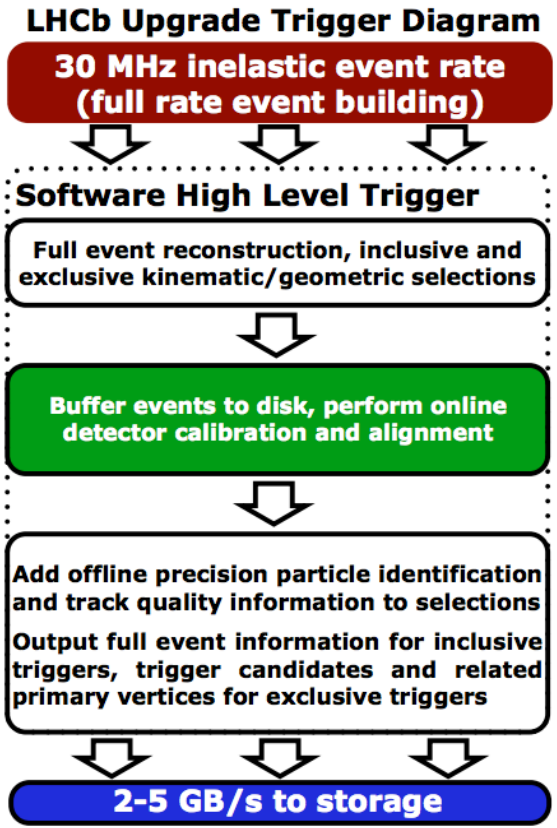
- Cosmic Frontier DAQ Needs, Paul O'Connor (BNL)
- Energy Frontier Trigger and DAQ Needs, Wesley Smith (U. Wisconsin)
- Future DAQ Needs for the Intensity Frontier, Josh Klein (U. Penn)
- Testbeam and Test Stand DAQ Needs, Mandy Rominsky (FNAL)
- Future FPGA Architectures, Ryan Herbst (SLAC)
- Future Process Architectures, Chris Green (FNAL)
- DAQs for cryogenic detectors in Cosmology, Gustavo Cancelo (FNAL)
- Tech Trends and R&D Ideas for a Post HL-LHC Energy Frontier, Paul Padley (Rice)
- Future Technologies for the Intensity Frontier in Trigger and DAQ, Wes Ketchum (FNAL)
- Technologies for Test Beam and Test Stand DAQ, Ryan Rivera (FNAL)
- Participant roundtable
- Working groups and discussion

LHCb phase I upgrade – trigger scheme



→ HW Triggerless →

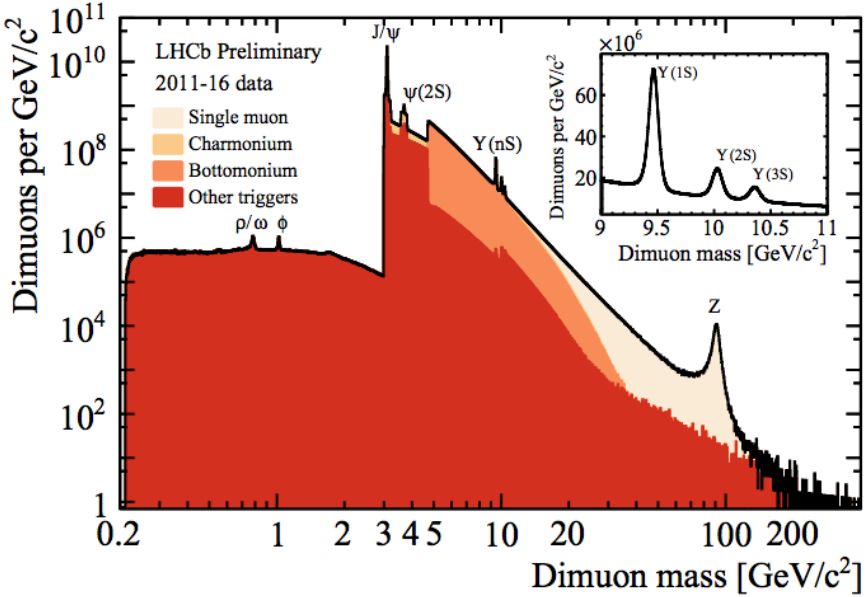
- Upgrade: $\mathcal{O}(40\,\text{Tbit/s})$ readout
- Calibration takes $\mathcal{O}(\text{minutes})$
- Events buffered for $\mathcal{O}(\text{days})$
- No futher offline reconstruction



The Turbo paradigm

- Basic idea: do physics analysis using trigger output directly[1]

- Real time alignment and calibration
  $\Longrightarrow$ no "better" offline reconstruction
- No offline processing
  $\Longrightarrow$ full raw event not always needed
- Bandwidth is the limit
  $\Longrightarrow$ smaller events mean more events

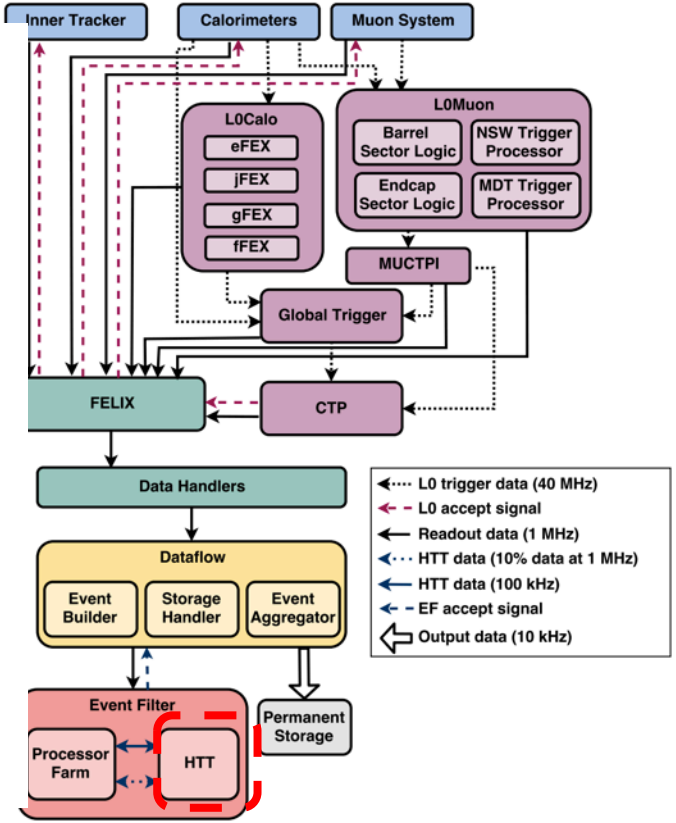


[1] R. Aaij *et al.*, "Tesla: an application for real-time data analysis in High Energy Physics", Comput. Phys. Commun. **208**, 35–42 (2016), arXiv:1604.05596

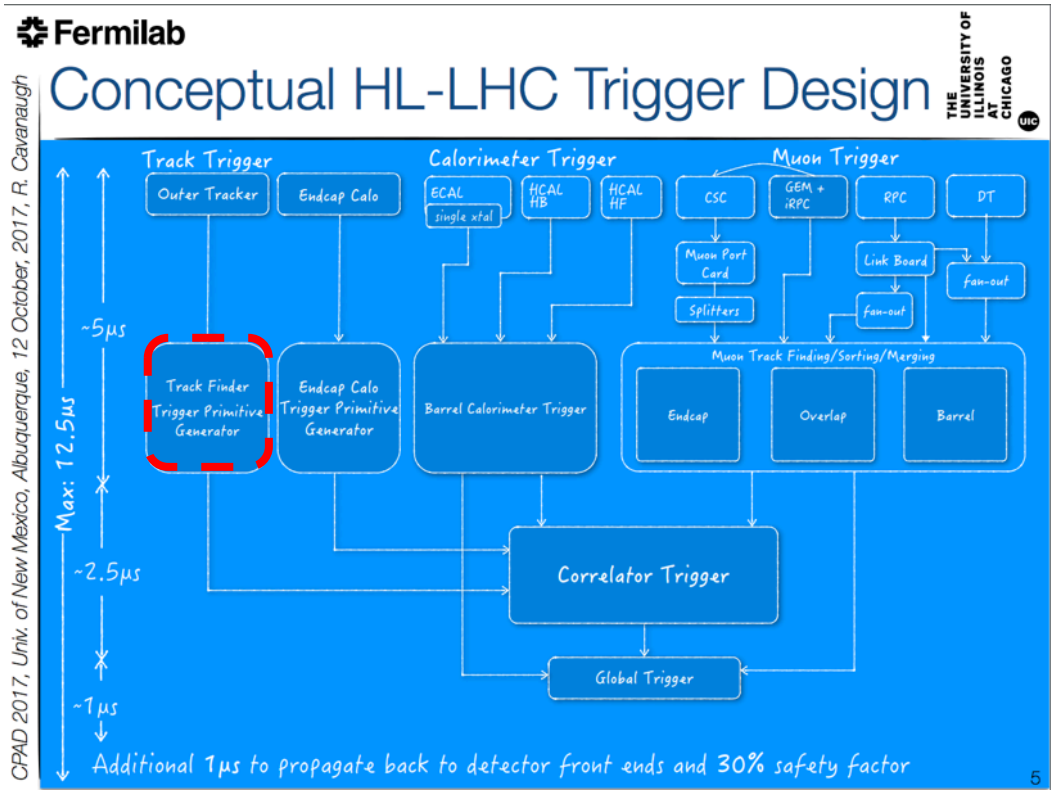
[2] LHCb, "LHCb dimuon and charm mass distributions", LHCb-CONF-2016-005 (July 2016)

ATLAS/CMS HLLHC Triggers

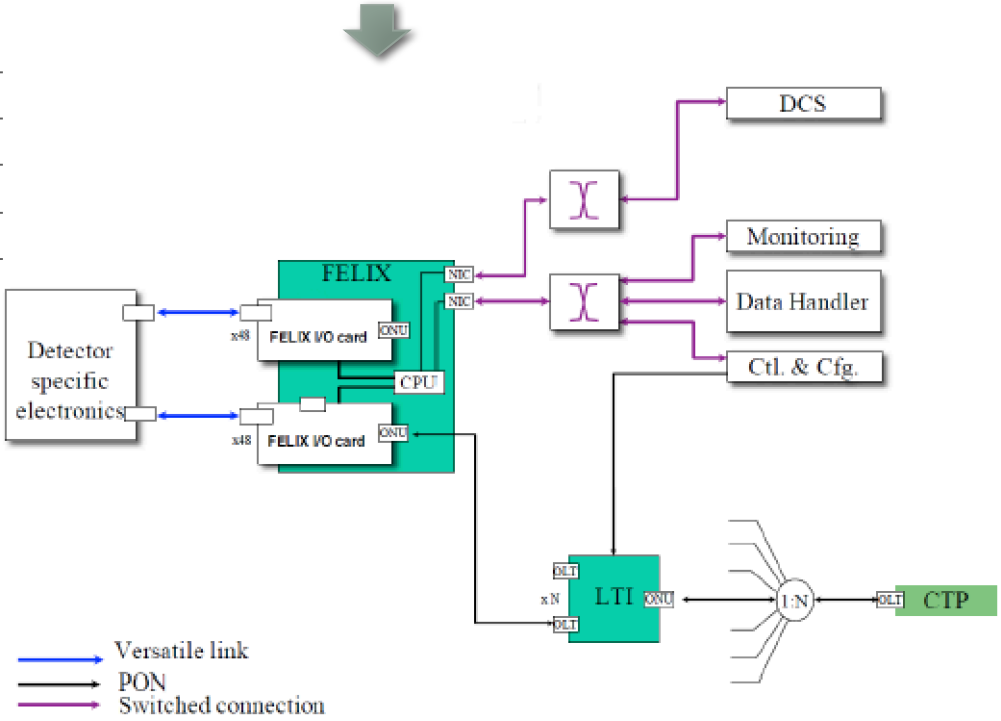
- Not HW triggerless
- Complementary Track Trigger approaches (trigger level and technology)



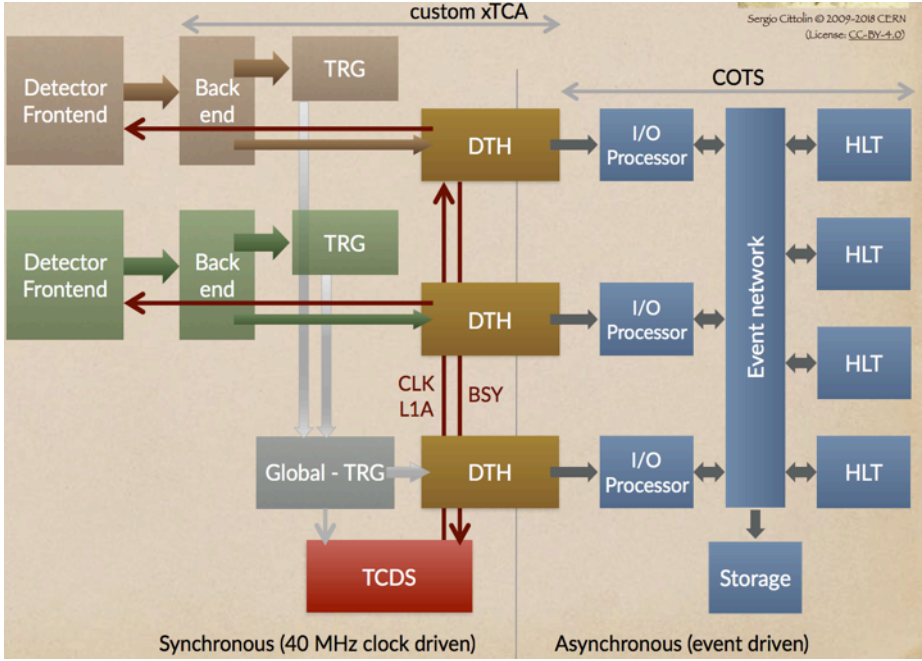
S. Majewski, CPAD 2017 9



ATLAS and CMS HL LHC DAQs

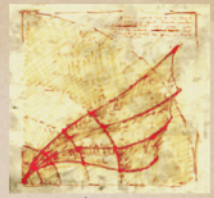


A.Paramonov



R. Mommsen

No Event Building (?)



Sergio Cittolin © 2009-2018 CERN
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Large key-value store

- Insert data from each fragment keyed with run/event/id
- Potentially stored for several hours or days

HLT processes query data when needed

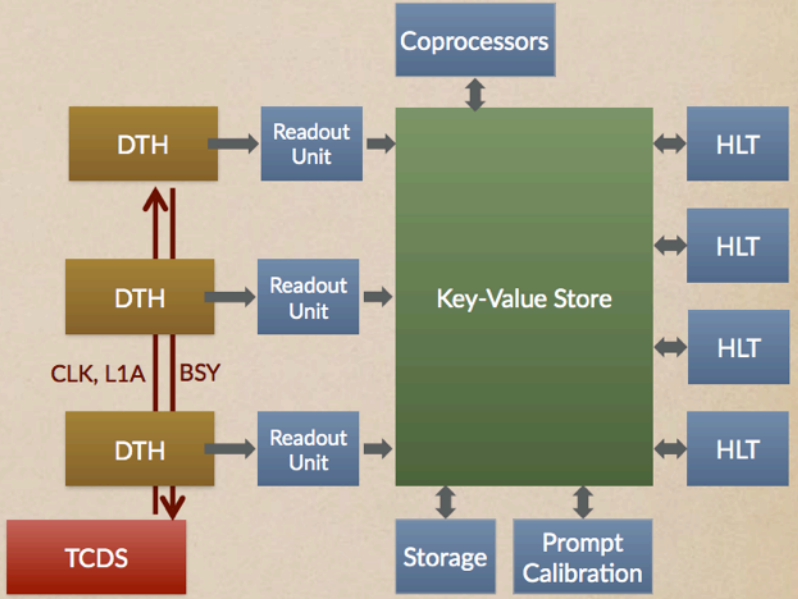
- Reduced time-coupling of HLT resource needs to LHC cycle
- Coprocessors could be easily attached to handle subsets of data
- Long storage time would allow to run prompt calibration before (final) event selection

Event assembly only after events are accepted

- Reduces amount of data moved through the system

Intel Poland is developing a commercial solution

- Phase-2 requirements should be met
- Collaboration under CERN openlab umbrella being set up
- Interest from CERN, ATLAS and CMS



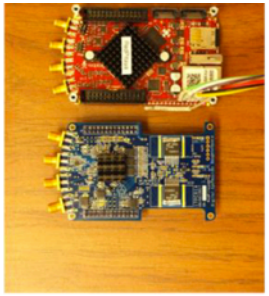
Points from LHC Session

- How to effectively make use of coprocessors
  - “A versatile software framework could be a game changer”
- From HL LHC to HE LHC and FCC:
  - R&D for rad hard high speed data links from the detectors
  - R&D for wireless data transmission

Lab Roadmap Highlights: ANL

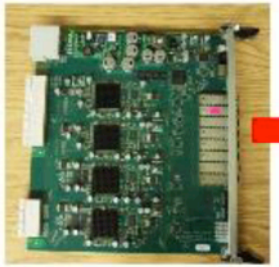
ATLAS TileCAL @ CERN
– Low Voltage Power Supplies for Phase 2 Upgrade

LBNE (DUNE) @ FNAL (35-ton prototype)
– Front End Electronics for Photon Detectors
Now: 35-ton prototype; Next: CERN TB



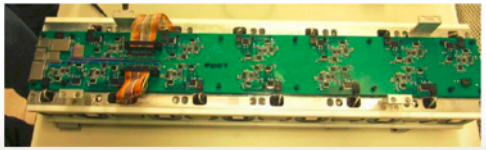
Synthesizer for a quantum computer

QIE front-end and HV distribition systems for ATLAS Tile Calorimeter



ATLAS TDAQ @ CERN
– FTK Readout Driver

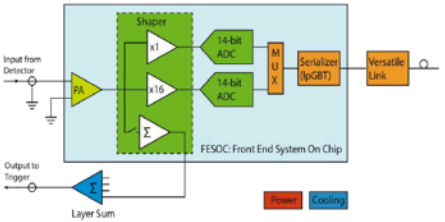
CTA
– L2 Array Trigger

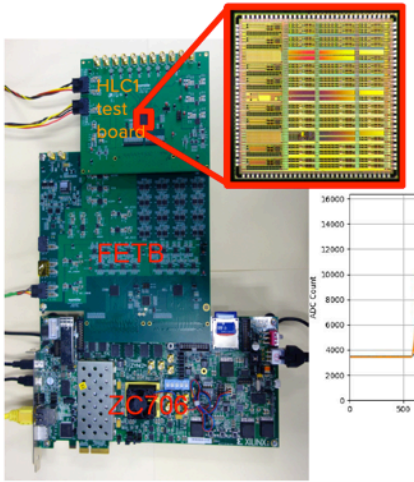


Lab Roadmap Highlights: BNL

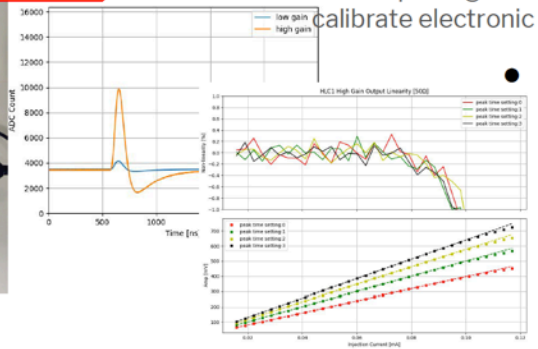
LAr Front-End System-on-Chip

- ***Preamplifier & Shaper ASIC Development***
  - fully differential low noise amplifier
  - engineered by Instrumentation Division Micro-Electronics Group
  - **65 nm CMOS process from TSMC**





- ***HLC1***
  - fabricated March 2017; delivered July 2017
  - summing for 4 or 8 input channels
  - simultaneous readout of two gain settings
  - **built-in driver to interface COTS or ASIC ADCs for testing**
  - built-in pulse generator & mask bit for individual channels to calibrate electronic response and perform crosstalk studies

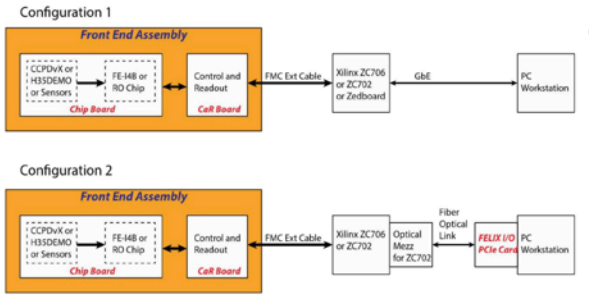


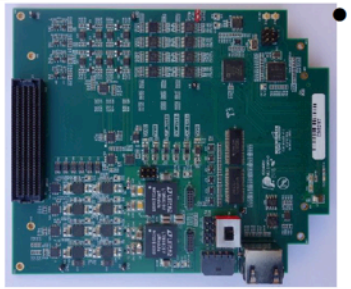
- ***Testing underway***
  - ZC706 (with ZYNQ) is used for the control and data readout.
  - **basic functionality verified**
  - **Performance test (linearity, ENI) for single channel finished;**

High-gain, 50 ohm: Non-linearity better than 0.3% within the designed dynamic range of 60uA for all peaking time settings;

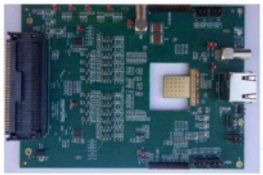
Lab Activity Highlights: BNL

Control and Readout Itk Board (CaRIBOu)



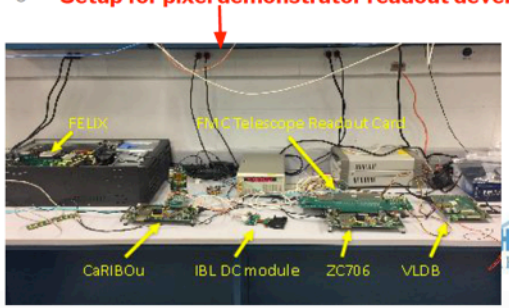


Control & Readout (CaR) board (v1.1)



board for FE-I4B and sensors

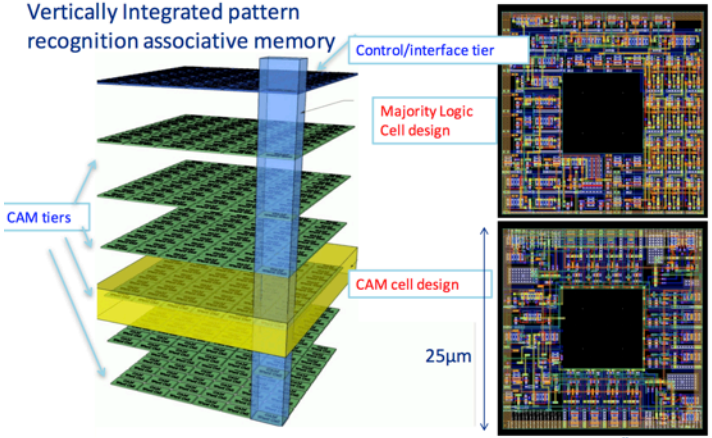
- ***Modular readout system for CMOS sensor R&D (LDRD program)***
  - open architecture with ZYNQ SoC to simplify firmware & software
  - easily adapted to various sensors under development
  - carefully defined interface to minimize design revisions
  - used in several test beams with FELIX readout at CERN
  - ***outgrowth of FELIX & LDRD efforts***
- ***Adapted for ATLAS HL-LHC Pixel Detector***
  - important for final development of pixel readout chain with FELIX
  - **Setup for pixel demonstrator readout development**



Lab Roadmap Highlights: Fermilab

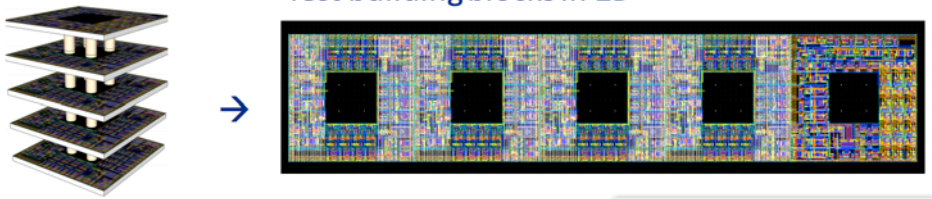
VIPRAM – a step in the "extra dimension"

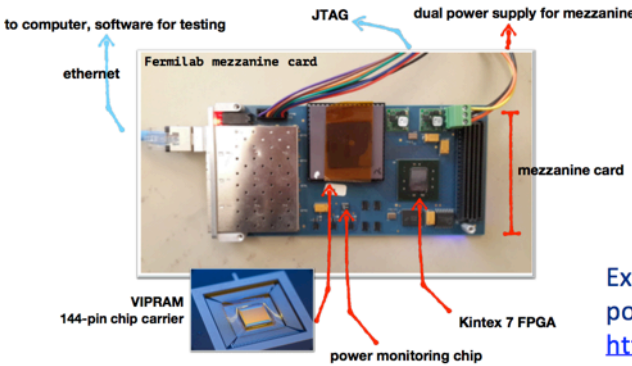
Vertically Integrated pattern recognition associative memory



protoVIPRAM00 performance

Test building blocks in 2D





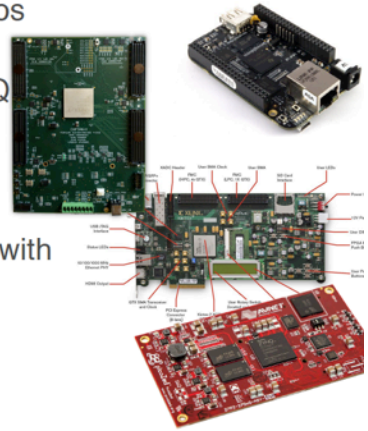
Freq(MHz)	Found/Expected Avg.
50	100
66	100
71	100
76	100
83	100
90	100
100	100
111	99.76489028
125	95.29780564

Extensive performance and power consumption studies: https://arxiv.org/abs/1709.08303
Submitted to TNS

Lab Roadmap Highlights: Fermilab

otsdaq and *artdaq* Data Acquisition Toolkits

- *otsdaq* is a Ready-to-Use DAQ solution aimed at test-beam, detector development, and other rapid-deployment scenarios
  - *otsdaq* uses the *artdaq* framework under-the-hood, providing flexibility and scalability to meet evolving DAQ needs
  - Library of supported front-end boards and firmware modules implementing custom protocol
  - Provides Run Control and readout software that works with *otsdaq* firmware

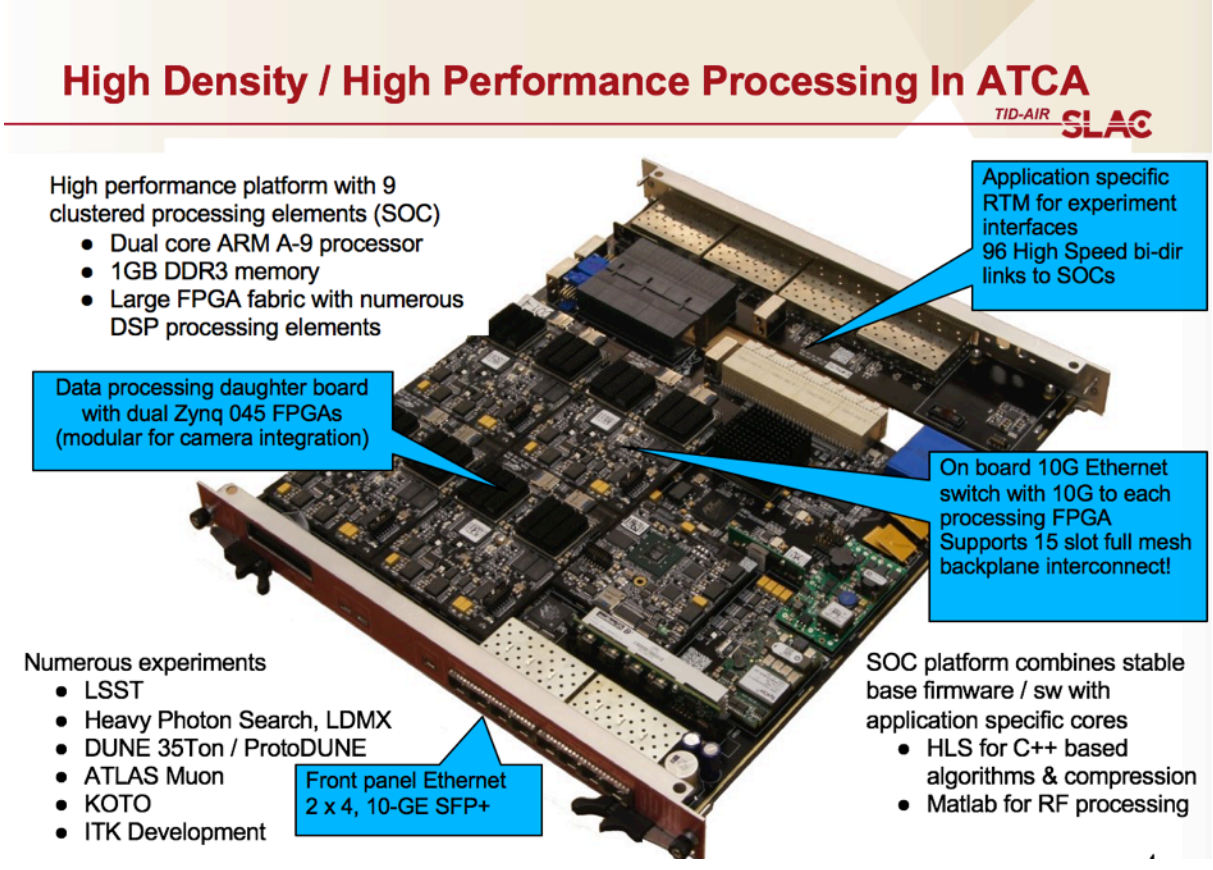


- *artdaq* is a plugin-based DAQ framework, used by several Fermilab experiments such as DUNE and mu2e
  - Flexible design allows for different detector technologies and event selection
  - Allows for data to be analyzed mid-stream for software triggers
  - Configurable asynchronous readout
  - *artdaq* filtering modules are compatible with the *art* analysis suite

DUNE
DEEP UNDERGROUND NEUTRINO EXPERIMENT

MU2E

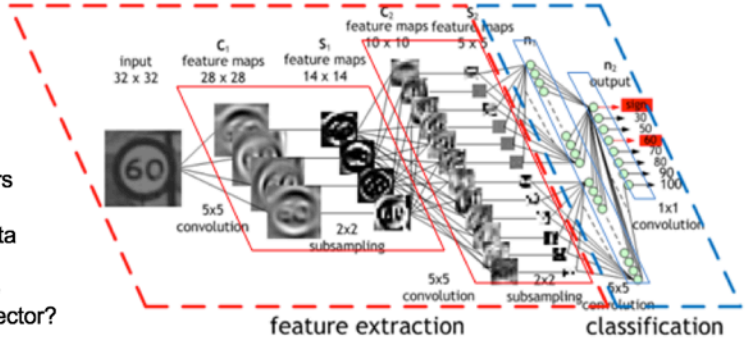
Lab Roadmap Highlights: SLAC



Lab Roadmap Highlights: SLAC

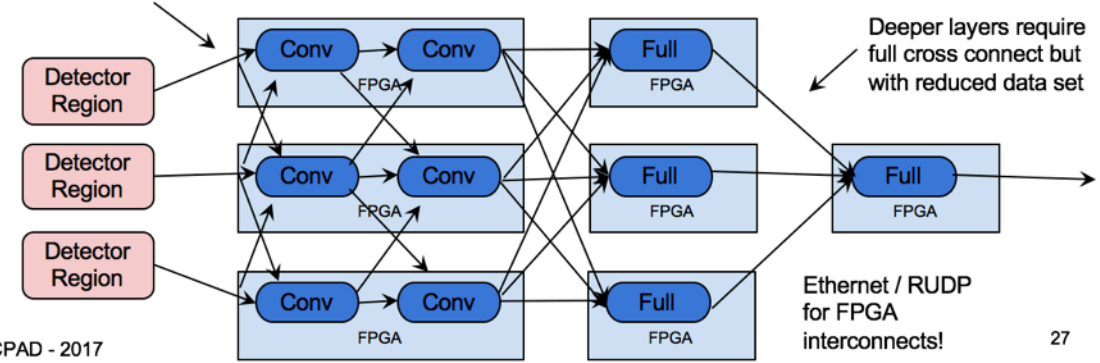
Deploying Machine Learning In DAQ & Trigger Systems
Matching Deployment To Common DAQ Structures

SLAC



Convolution layers need minimal cross connect data

First level feature extraction on detector?



CPAD - 2017

27

Points from Lab Reports

- To establish framework for collaborating in firmware development
- To balance the commonality vs flexibility in the testbeam /teststand environment and support
- To strengthen the university lab collaboration

(proto)DUNE Trigger/DAQ

DUNE Trigger/DAQ

Selected data rates from the TPC (1 10kT single phase)

SLAC

Source	Event Rate	Event Size	Data Rate	Volume/year
all ^{39}Ar	11.2 MHz	150 B	1.6 GB/s	53 PB
all in-spill				159 TB
with-beam-ν				79 GB
cosmic-μ	0.259 Hz	2.5 MB	647.4 kB/s	20 TB
beam-ν	8770 year^{-1}	2.5 MB	0.69 kB/s	22 GB
SNB cand. (ZS)	12 year^{-1}	16.7 GB	6366 B/s	201 GB
SNB cand. (FS)	12 year^{-1}	46.1 TB	17.5 MB/s	553 TB

assumes 2.4 drifts/readout → 5.4ms

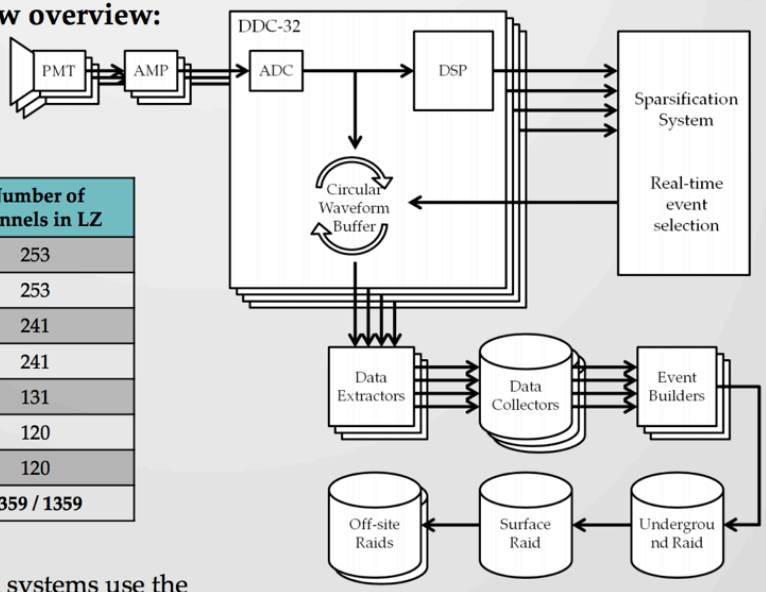
FS="Free Streaming"
ZS="Zero Suppression"

- ^{39}Ar endpoint is ~0.5MeV; this probably sets the threshold
- next 5 rows assumes zero suppression below this 0.5 MeV
- SNB cand. (FS) → no zero suppression, full detector for 10s
  - we would really like to have the capability to do this…requirement?
- The 12/year is ~ upper limit for false positives…need to tune the SN trigger to meet this

LZ Trigger and DAQ

LZ – DAQ and Trigger System Overview

System flow overview:



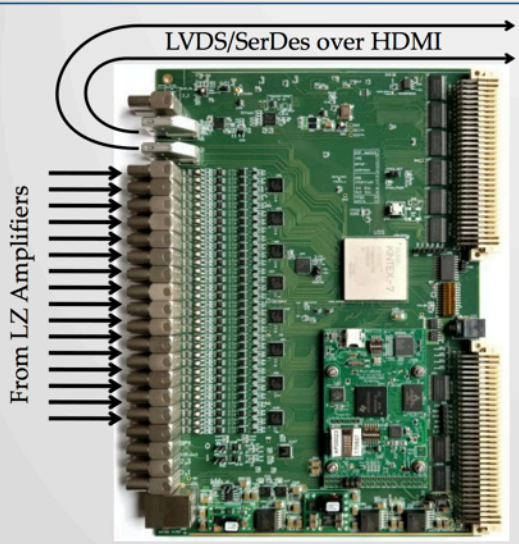
Channel count:

Channels	Number of channels in LZ
TPC Top High Gain	253
TPC Top Low Gain	253
TPC Bottom High Gain	241
TPC Bottom Low Gain	241
Skin	131
Outer Detector High Gain	120
Outer Detector Low Gain	120
Totals (DAQ / Trigger)	**1359 / 1359**

• The DAQ and Sparsification systems use the same digitized waveforms, thus reducing the hardware footprint and simplifying the system performance evaluation.

Expected total collected data volume:
> 3 PB

LZ – DDC-32 Digitizers



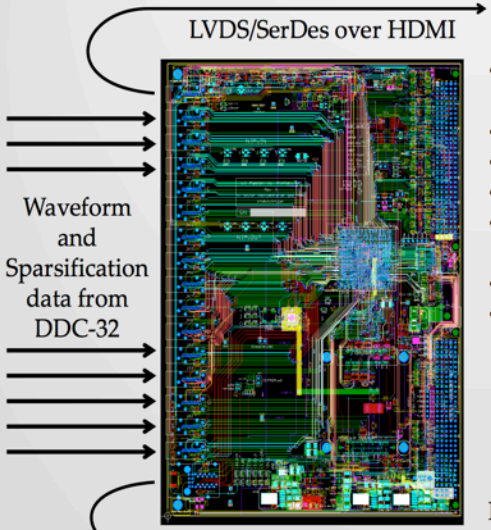
Reduced quantities to Data Sparsifiers

Waveforms to Data Extractor

- 32 ADC channels:
  - 14-bit resolution
  - 100 MHz sampling
  - 2V input range
  - +/-1V adjustable baseline
- 2 DAC channels (14-bit/100 MHz)
- Kintex 7 Xilinx FPGA
- AM335x running Linux with Ethernet and RS-232
- 2 Serial links over HDMI
- ADC board temperature monitoring
- Remotely reprogrammable:
  - FPGA and AM335x Processor
  - No need to extract and program boards one by one

Hardware designed by Wojtek Skulski.

LZ – DS and DE Logic Boards



Higher level of Data Sparsifiers/Masters

- One HW platform for Data Extractors and Data Sparsifiers
- 16 Serial links over HDMI
- 1 Gbit Ethernet link directly from FPGA
- Kintex 7 Xilinx FPGA
- AM335x running Linux with Ethernet and RS-232
- Current and voltage monitoring
- Remotely reprogrammable:
  - FPGA and AM335x Processor
  - No need to extract and program boards one by one.

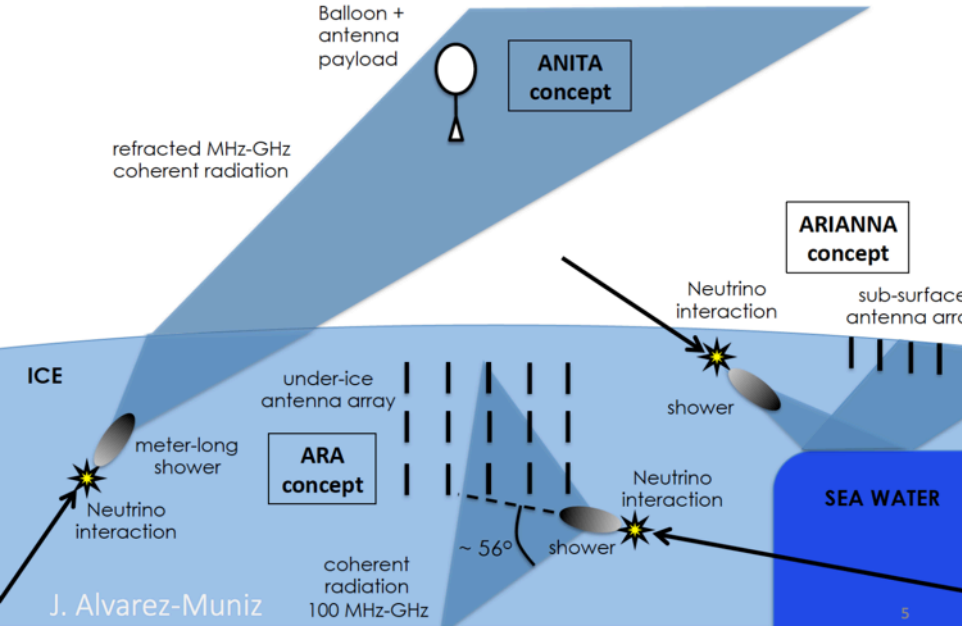
In proto production.

Hardware designed by Wojtek Skulski.

Waveform data to Data Collectors

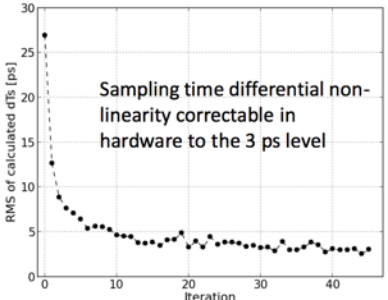
Trigger & DAQ for UHE Neutrino

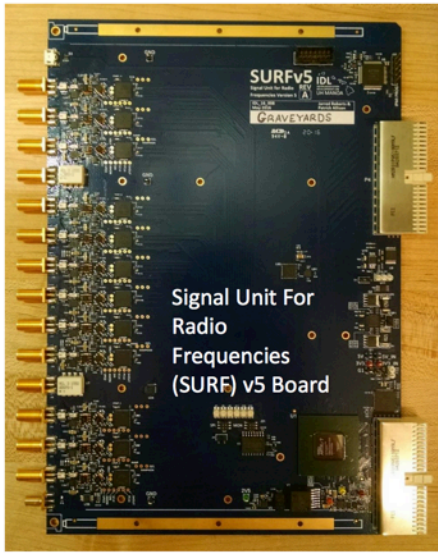
Radio Detectors using Dense Media: Ice



ANITA Data Acquisition

- ANITA flights 1-4 flew with the basically the same DAQ using the LABRADOR3 ASIC waveform sampler (2.6 GSa/s, 260 samples)
- A new system is ready for ANITA5 using the new LAB4D ASIC (Varner, UH)
  - 3.2+ GSa/s with 1024 samples per buffer and 4 buffers.
  - > 1 GHz analog bandwidth
  - Trim DACs on each sample allows for correcting sampling time non-linearity



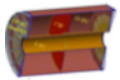


[Varner, et al NIMA 583 2007],
[P. Allison, EO, J. Roberts, G. Varner, in prep]

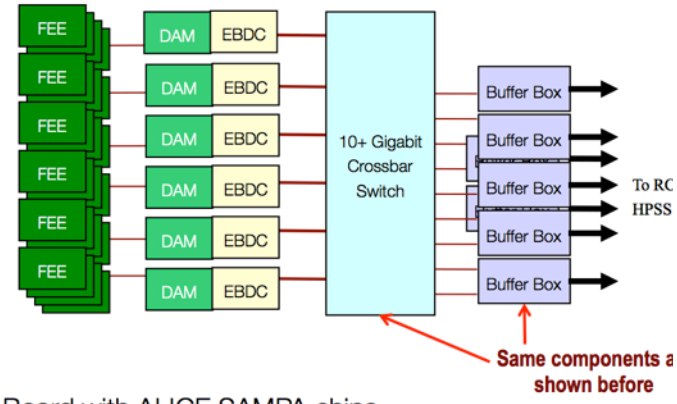
E.Oberla

sPHENIX

The streaming TPC readout

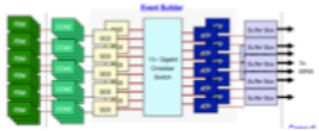


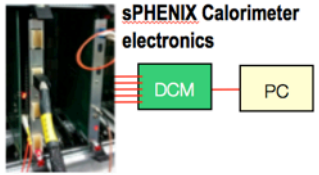
TPC



- FEE Board with ALICE SAMPA chips
- DAM Data Aggregation Module
- EBDC Event Buffering and Data Compressor

RCDAQ - R&D-themed part of the system





- **The RCDAQ DAQ System**
- Cut out the event builder (not much need right now)
- Log data at the EVB "input point" instead
- Same technology, reading out our front-end here will seamlessly integrate into the big thing
- Addt'l support for a large variety of non-sPHENIX gear
- Powerful scripting/automation features
- Compatible with the sPHENIX data standard – experience gained during test beams re-usable
- "Real" online monitoring often has it roots in test beam code
- ~20 RCDAQ copies around in the sPHENIX orbit
- About a dozen more in use by external groups
- Supported on high-end 32core PC to Raspberry Pi

M.Purschke

Software framework and support

Points Neutrino, DM, RHIC Session

- DUNE and DM experiments become PB data scale expts, and will require sizable computation

DAQ Workshop Summary

- Find Kurt's summary here:
  - https://indico.hep.anl.gov/indico/getFile.py/access?contribId=110&sessionId=30&resId=0&materialId=slides&confId=1185
- Report will be written

Recommendations

- To augment R&D on wireless data and power transmission (revolutionary)
- To Develop high-speed rad-hard optical links (>> 10 Gb/s) (evolutionary)
- To establish framework for collaborating in firmware development
- To utilize more hardware platforms such as CPU-FPGA, GPU, etc, and machine learning