Proposal from the Solid State Technologies / Silicon Detector Session

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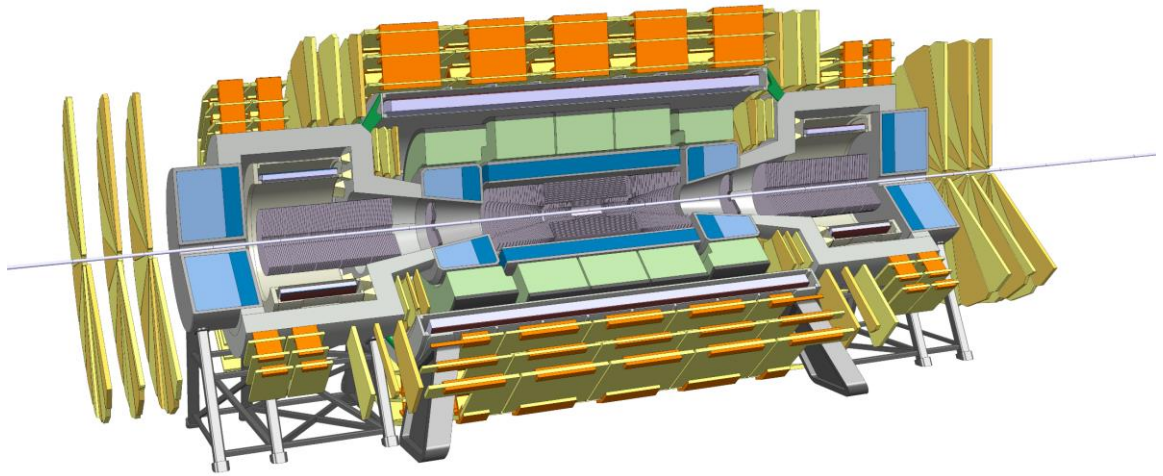
Tracking / calorimetry systems with high granularity using Si as sensitive medium

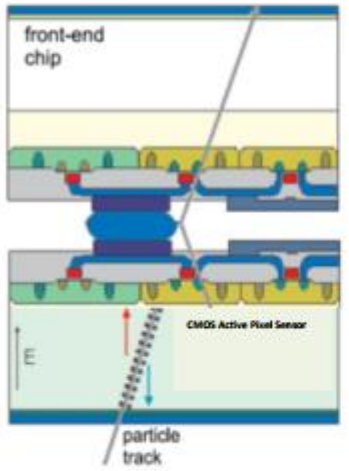
- Could consider multi-purpose detector for next generation of hadron colliders as motivation for developments of Si based detector
  - Technology developments also apply for any high intensity experiment (examples: LHCb @ 2E34, mu2e – 2nd gen, e^+e^- @E37,…..)
- Reduce cost of detector systems
- Increase channel count and address bandwidth / dead material / power issues
- ASIC development
- Include timing information
- Radiation hardness
- Scalability and reliability



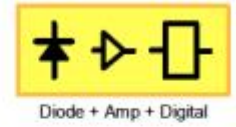
Reduce cost

- HVCMOS development
  - Advantage: produced in commercial foundries (higher throughput, lower costs)
  - Demonstrate radiation hardness and acceptable signal levels (short term goal)
  - Integrate at least preamp inside the sensor
  - Possibly include digital processing
- Other sensor technologies for large area detectors with reduced granularity (calorimeters)
  - Even cheaper ways of fabricating large area sensors

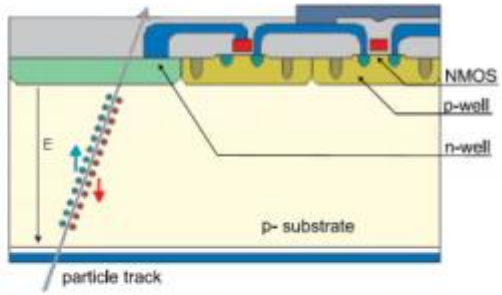
CMOS Active Hybrid



Bumped or glued

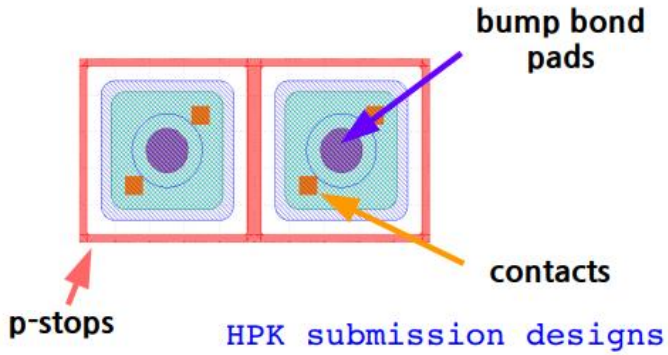


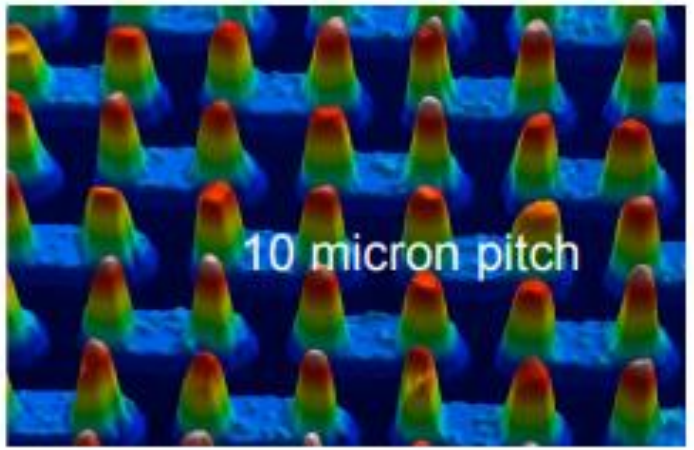
Depleted Monolithic



Increase channel count (i) / ASICs

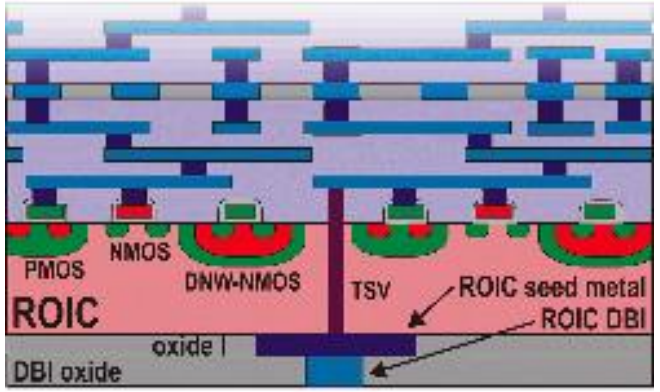
- Investigate minimum pixel size that can be fabricated
  - Aim for 5-10 µm pixel sizes
- Readout ASICs
  - Start a “RD53-like” consortium in the US
  - Investigate next step in feature size (28 nm ?)
    - Start with understanding radiation hardness of simple transistors and basic blocks for chip design
    - In parallel set up consortium of universities and lab to share tools, training, and develop larger IC blocks that can be shared for design of multiple ASICs to be used in multiple experiments / frontiers

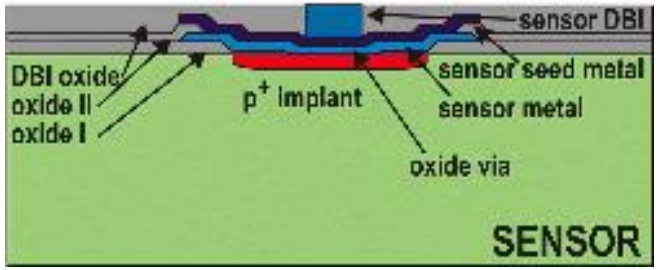


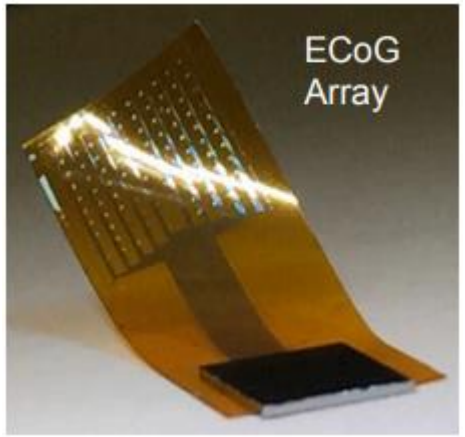


Increase channel count (ii)

- Increase of channel counts
  - cannot come with increase in detector mass, cables/fiber plant
  - requires increase in density of interconnects
- Specialized technologies to be used in areas with largest interconnection density (ex: vertical interconnect)
- New technologies to reduce costs (ex: conductive adhesives)
- Increase available bandwidth of E-links / fibers, rad hardness of opto-converters
- Move clustering / track segment finding into the front-end

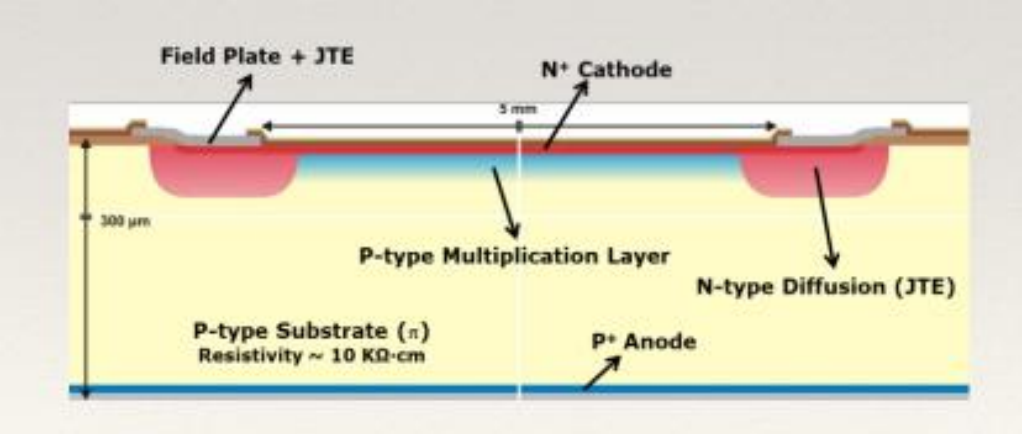


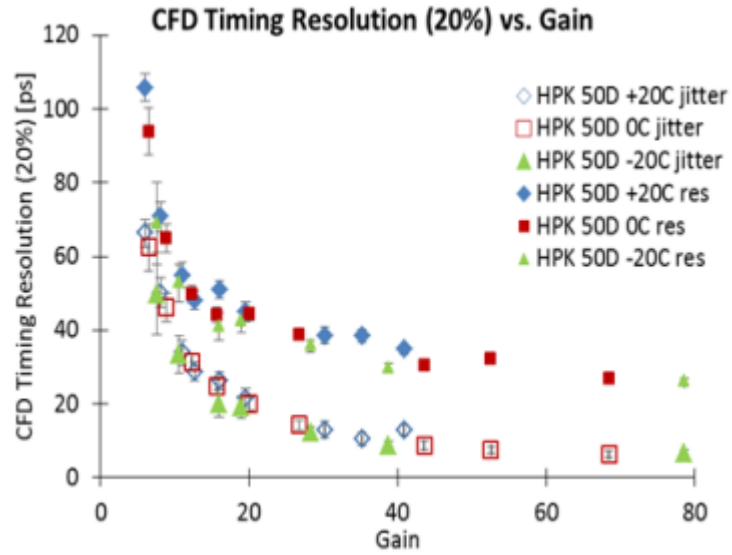




Adding Timing Information – New Dimension

- Short term: qualify LGAD detectors, add timing capability for MIPs
  - Address radiation hardness, inactive area, detector size and integration
- Longer term: develop timing detectors for multiple uses
  - Tracking layers
  - Calorimeters
- Understand needs for spatial / timing resolution
  - Not clear that same detector should provide ultimate resolution on both
  - 4D Kalman-filters vs 4D pattern finding





Specific Proposals

- Cheaper sensors:
  - 1st step: HV/HR-CMOS
  - 2nd step: alternative materials / cheaper processing
- ASIC consortium: investigate next feature size in ASIC design
  - 1st step: qualify transistors / basic building blocks
  - 2nd step: build library of components for generic ASICs
- 4D tracking / calorimetry: include timing information
- High density / high bandwidth connections: 3D integration, low mass connectors, high throughput/rad hard E-link to optical conversion

- Let's make pigs fly…..
  - Send us your suggestions / comments for CPAD proposals, help planning deliverables and milestones