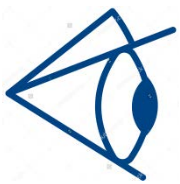
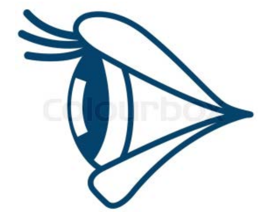
# Precision Timing in HEP Experiments

An 8-fold way…



黄色い！



绿色!

Orange

Grün!


Gary S. Varner

University of Hawai'i



HEPiC 2017

UNIVERSITY of HAWAI'I® MĀNOA

# (x,y,z;t) – As a neverending student

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- Learn ‘Time’ is a fiction

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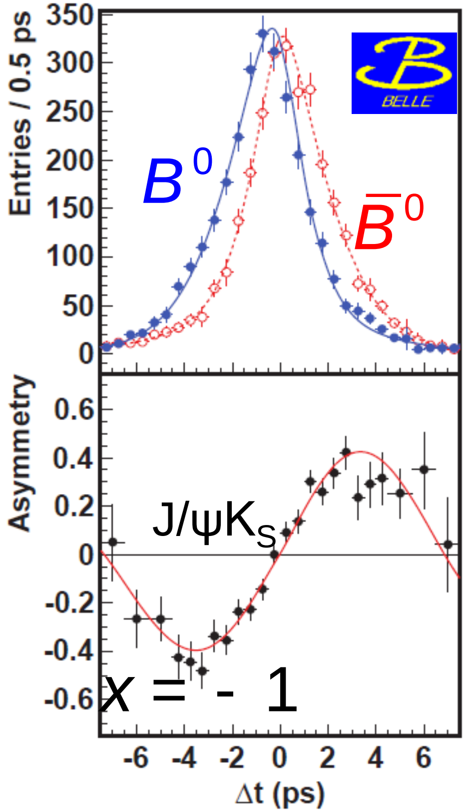
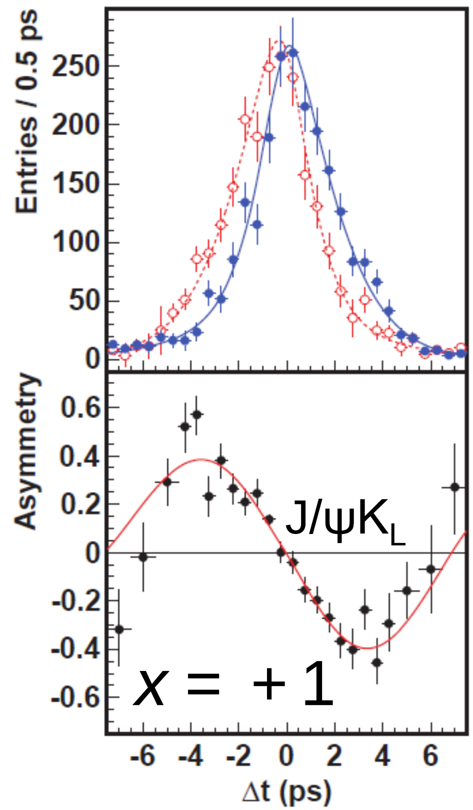
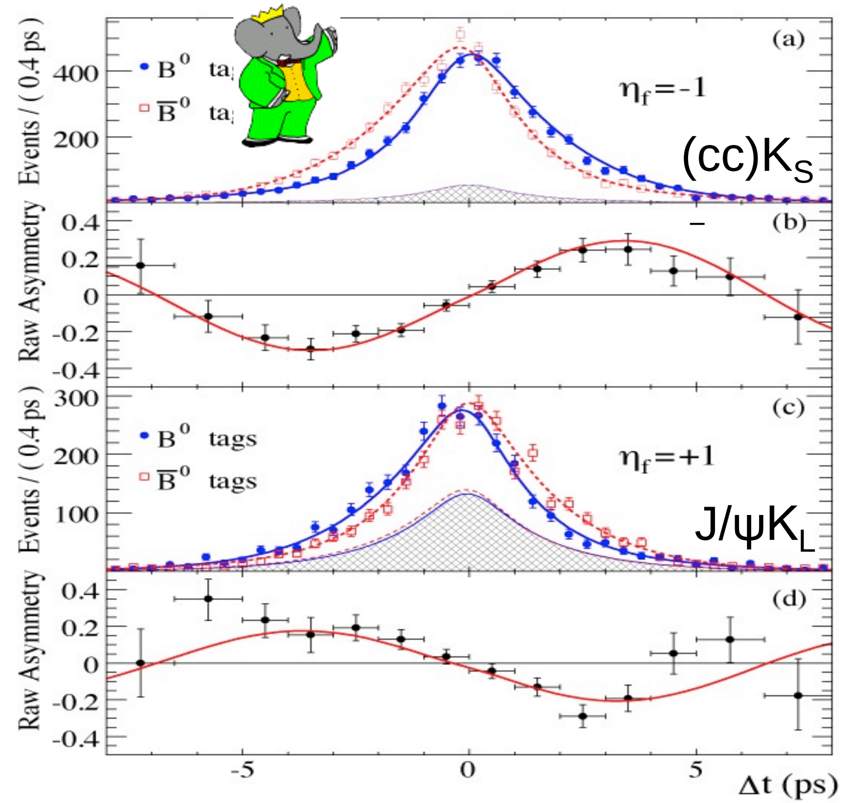
小林 益川

$$V_{\mathrm{CKM}} \equiv V_L^u V_L^{d\dagger} = \begin{pmatrix} V_{ud} & V_{us} & V_{ub} \\ V_{cd} & V_{cs} & V_{cb} \\ V_{td} & V_{ts} & V_{tb} \end{pmatrix}$$

# Measurement of $\sin(2\varphi_1)/\sin(2\beta)$ in $B \rightarrow$ Charmonium $K^0$ modes




$\sin 2\varphi_1 = 0.667 \pm 0.023 \pm 0.012$

$A_f = 0.006 \pm 0.016 \pm 0.012$

PRL108,171802 (2012)

$\sin 2\varphi_1 = 0.687 \pm 0.028 \pm 0.012$

$A_f = -0.024 \pm 0.020 \pm 0.016$

PRD79,072009 (2009)

Overpowering evidence for CP violation (matter-antimatter asymmetries). >>>> The phase of $V_{td}$ is in good agreement with Standard Model expectations. *This is the phase of $B_d$ mixing.*

# ‘Precision Timing’ – 3 realms

- 10’s of ps
- ~1ps
- Sub-ps (femtosecond)

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Trailokya (Sanskrit: त्रैलोक्य; Pali: tiloka, Wylie: khams gsum) has been translated as "three worlds,"[1][2][3][4][5] "three spheres,"[3] "three planes of existence,"[6] "three realms"[6] and "three regions."[4] These three worlds are identified in Hinduism and appear in early Buddhist texts.

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3 options: 2^3 Combinations (8)

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**My difficulty**

(1) Null set

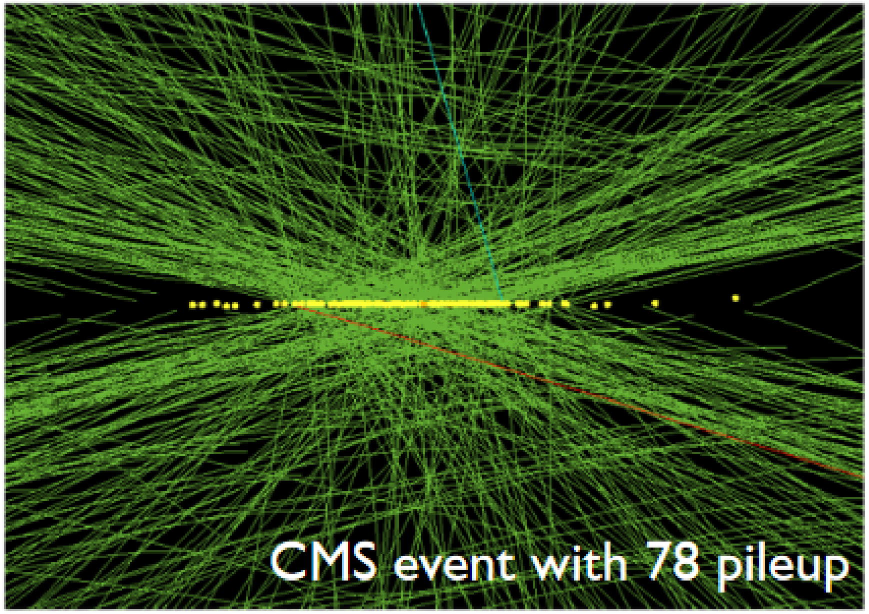
(3) Focus

(3) Mix of 2

(1) Overview of each

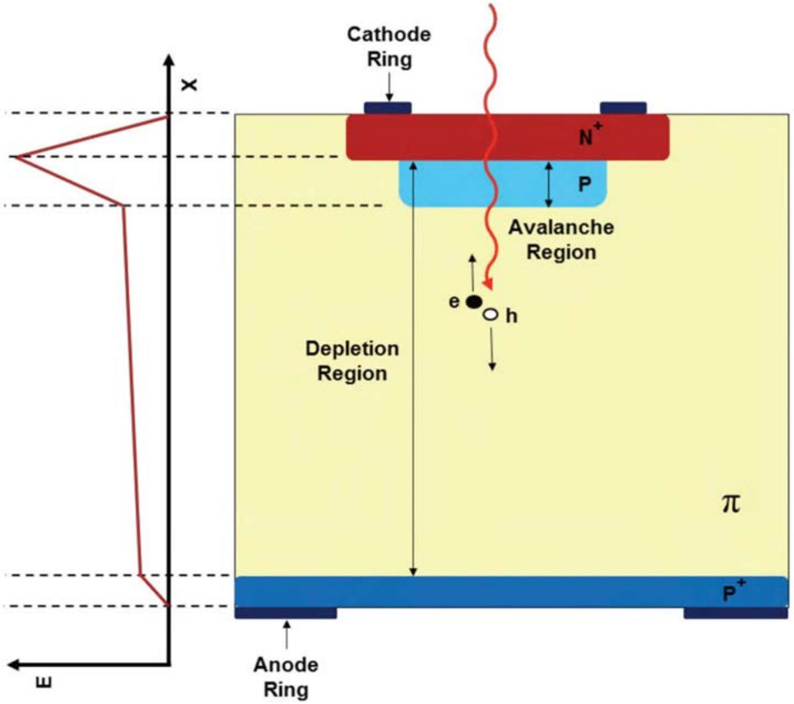
# The canonical example: HL-LHC

- Luminosity of $5x10^{34}cm^{-2}s^{-1}$ corresponds to an *average* pileup of 140 events
  - Upper estimate of average number of pileup events for this lumi - partly accounts for bunch-to-bunch variation
  - Average of a Poisson distribution with a sigma of about 12 events
- Key questions:
  - Can the detectors work with even higher (average) pileup to allow 3000 /fb to be delivered more quickly?
  - Can a longer beam spot help pileup mitigation?
- Need to take into account in-time pileup (same bunch crossing) and out-of-time pileup (previous crossings) - particularly for ATLAS colorimeter and for muon spectrometers



# Low-Gain Avalanche Detectors (LGAD)

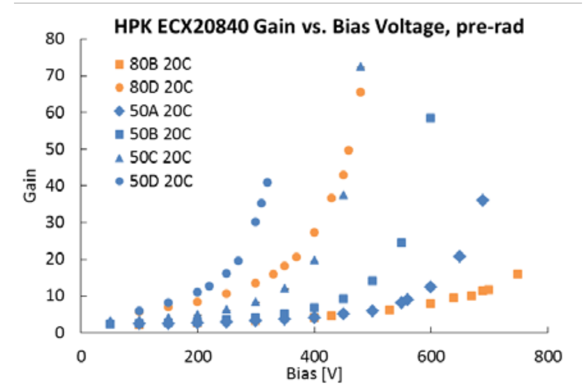
Hartmut F.-W. Sadrozinski, UFSD, TWEPP, Sep 13 2017



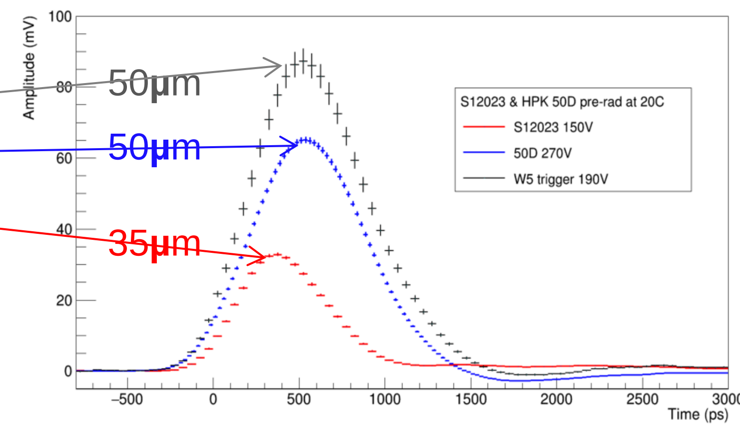

Principle:

Add to n-on-p Silicon sensor an extra thin p-layer below th junction which increases the E-field so that charge multiplication with **moderate gain** of 10-50 occurs without breakdown.

High Doping Concentration: High Field




Average pulse Shapes




**Manufacturers of LGAD (30 µm – 300 µm):**

CNM Barcelona (RD50, ATLAS-HGTD)

HPK Hamamatsu

FBK Trento (INFN)

**very similar behavior with exception of breakdown voltage and special design features .**

# “Beam test results of a 16 ps UFSD timing system”

N. Cartiglia et al., “Beam test results of a 16 ps timing system based on ultra-fast silicon detectors”, NIM. A850, (2017), 83–88.

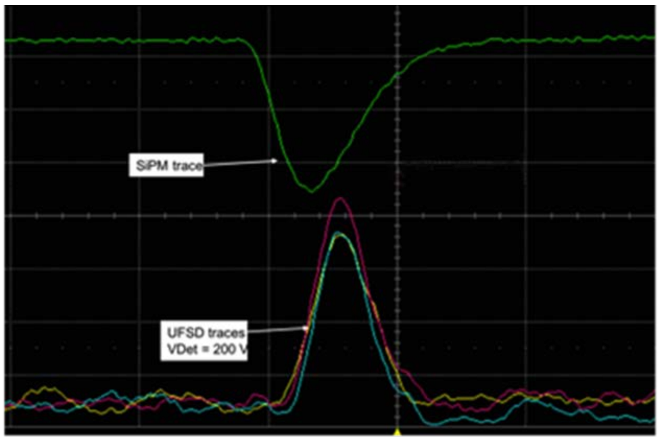


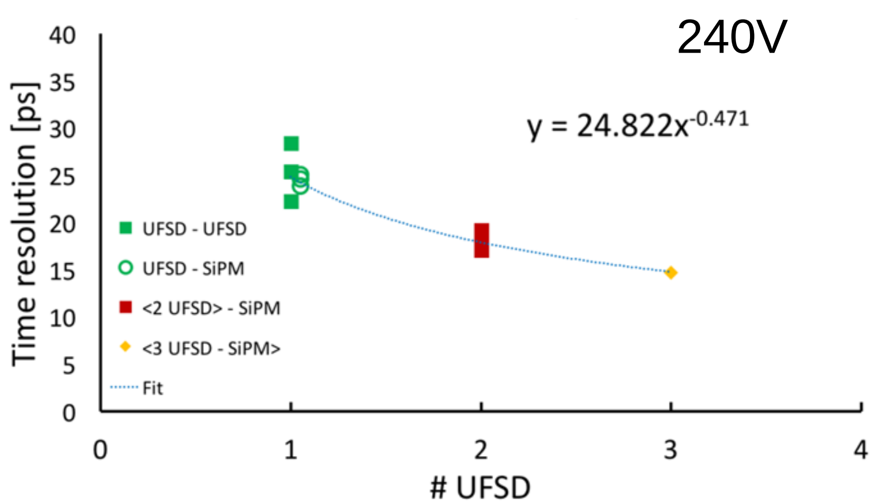

Figure 1 Screenshot of one event, showing the signals of 3 LGAD biased at 200 V and the SiPM at 28 V. Each horizontal division corresponds to 2 ns, while each vertical division is 100 mV.

**3 identical 45 μm thick 1.3x1.3 mm² LGAD produced by CNM**

**To extract the time stamp of the LGAD employ constant-fraction discrimination (CFD) to correct for time walk (CFD ≈ 20%).**

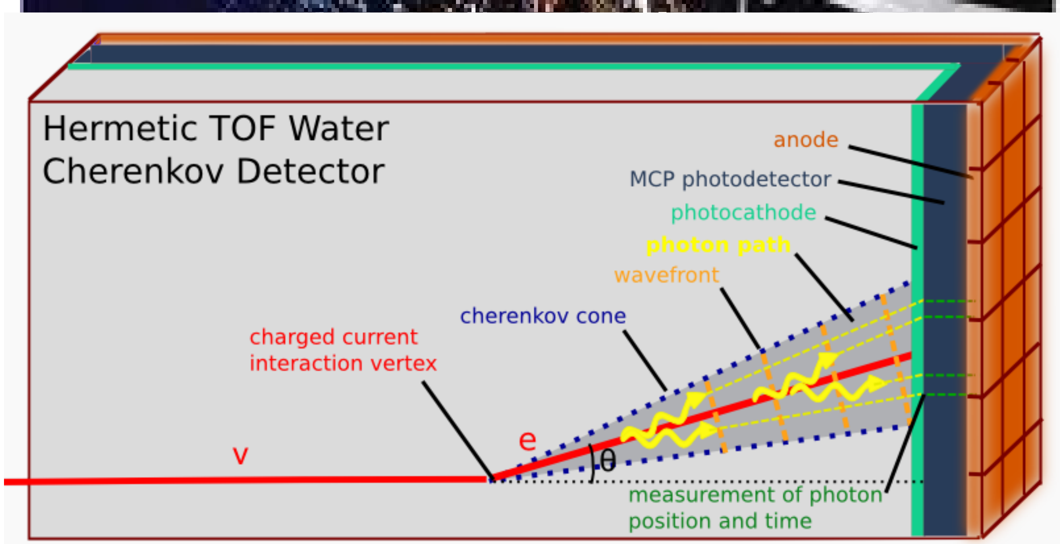
**Important: this can be reliably implemented in an ASIC.**

**Timing resolution vs. # of UFSD averaged**




- **Good matching of three LGAD**
- **Time resolution of single UFSD:**
  **~ 25 ps (240V)**
- **Time resolution of average of 3 UFSD:**
  **20 ps (200V) & 16 ps (240V)**
- **Timing resolution agrees**
  **with expectation $\sigma(N) = \sigma(1)/N^{0.5}$**

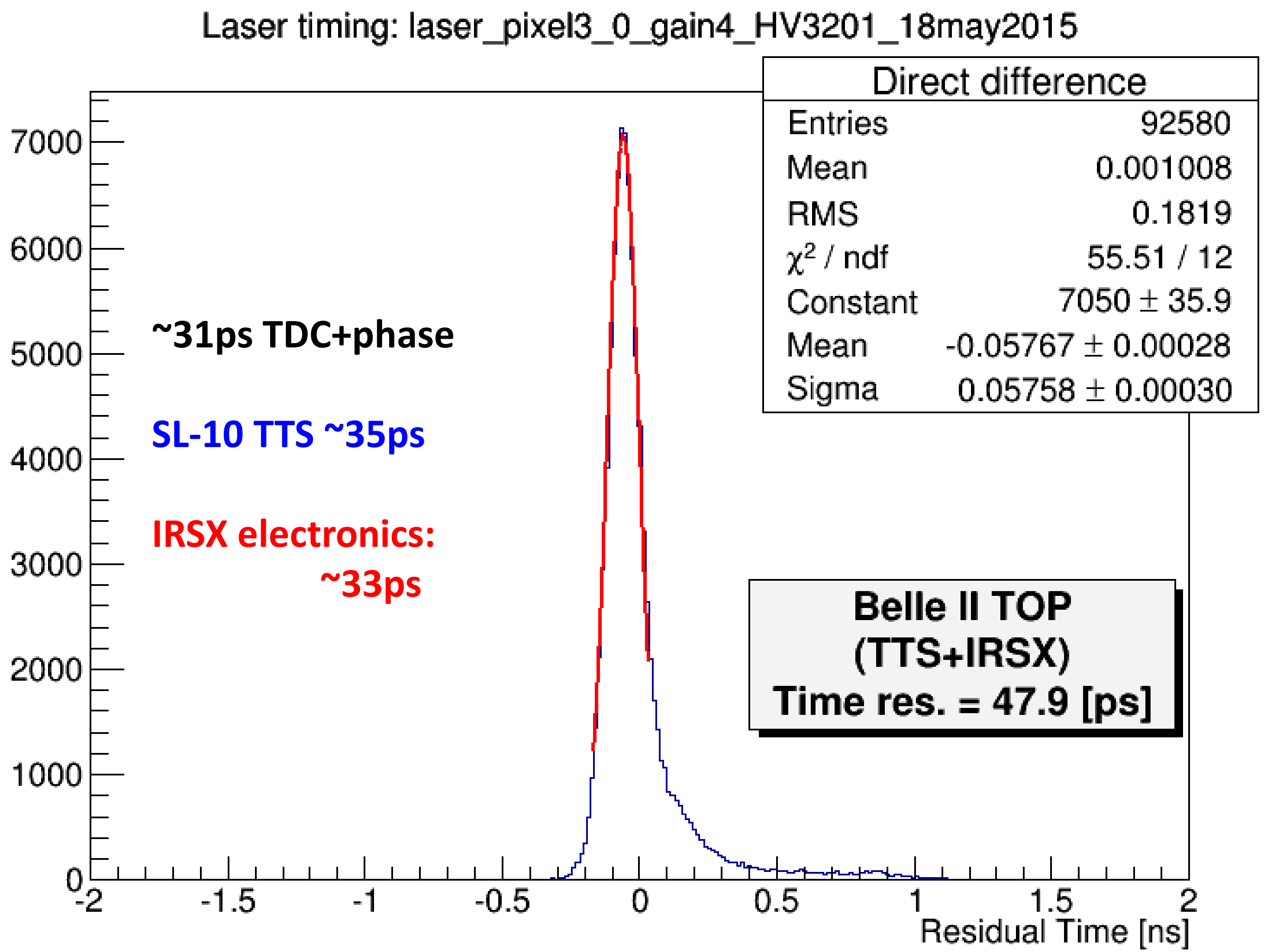
# LAPPDs -> MCP timing




- Each 'pixel' is 20"
- Fragile, expensive
- Few ns timing
- Neutrino cross-section can't be fooled
- 40% photocathode coverage

➢ **< 100ps timing**
➢ **< cm pos. resolution**
➢ **Significantly larger number of voxels**
➢ **Larger fiducial volume**

# Production single photon testing



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- Electronics for Physicists
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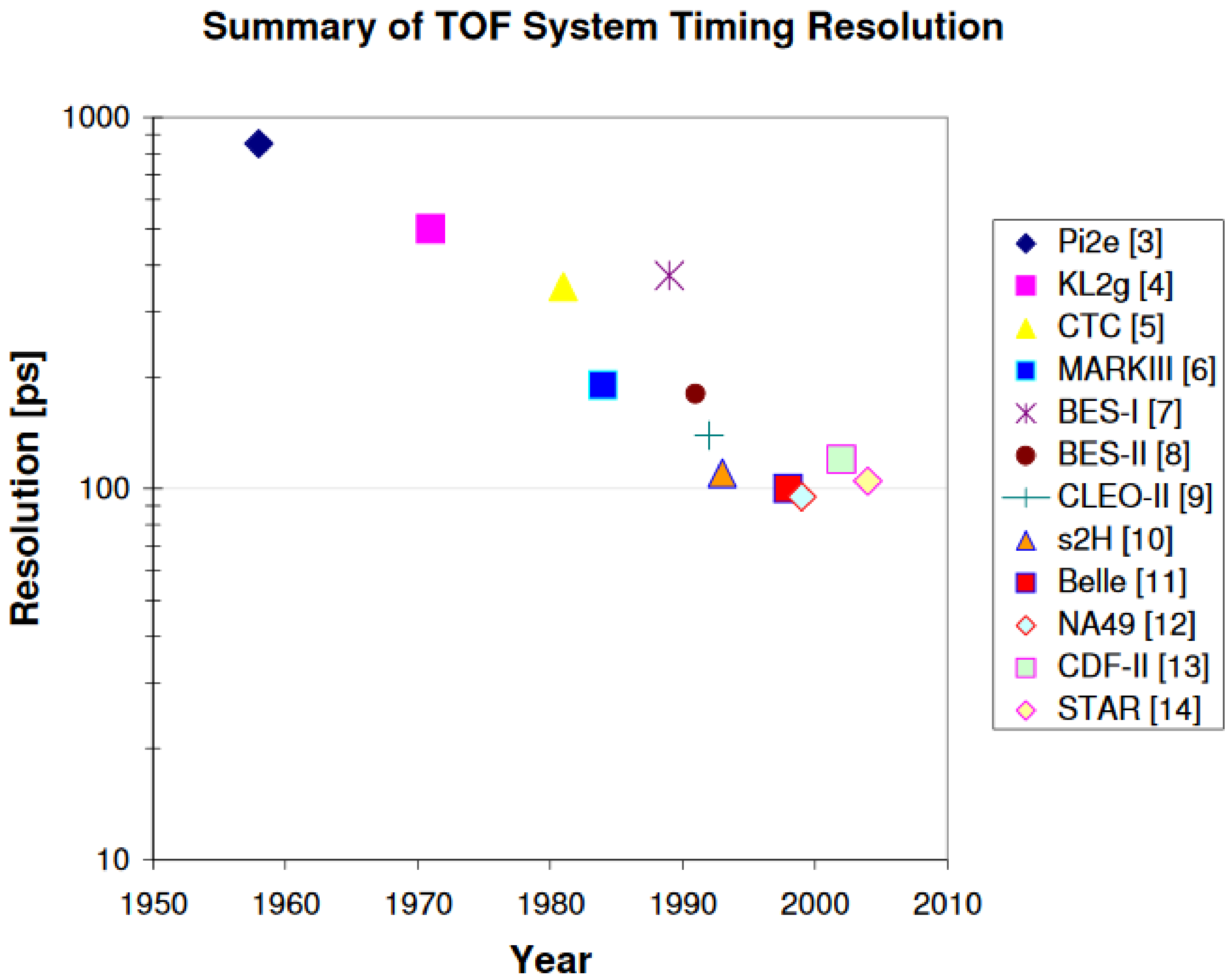
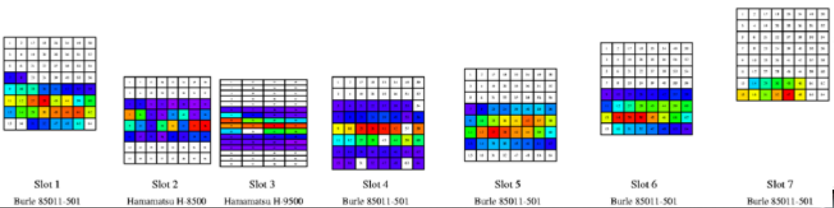
- Student projects
  1. Actually build test circuits
  2. High quality analog difficult
  3. **Sub-10ps not so difficult**

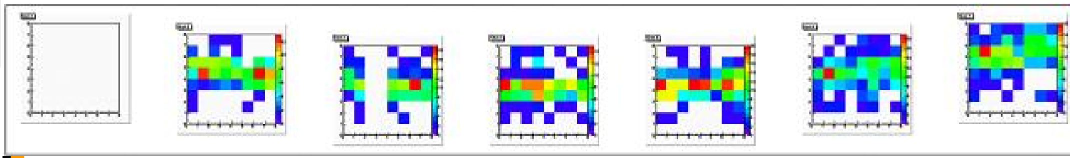
# So What is the Disconnect?

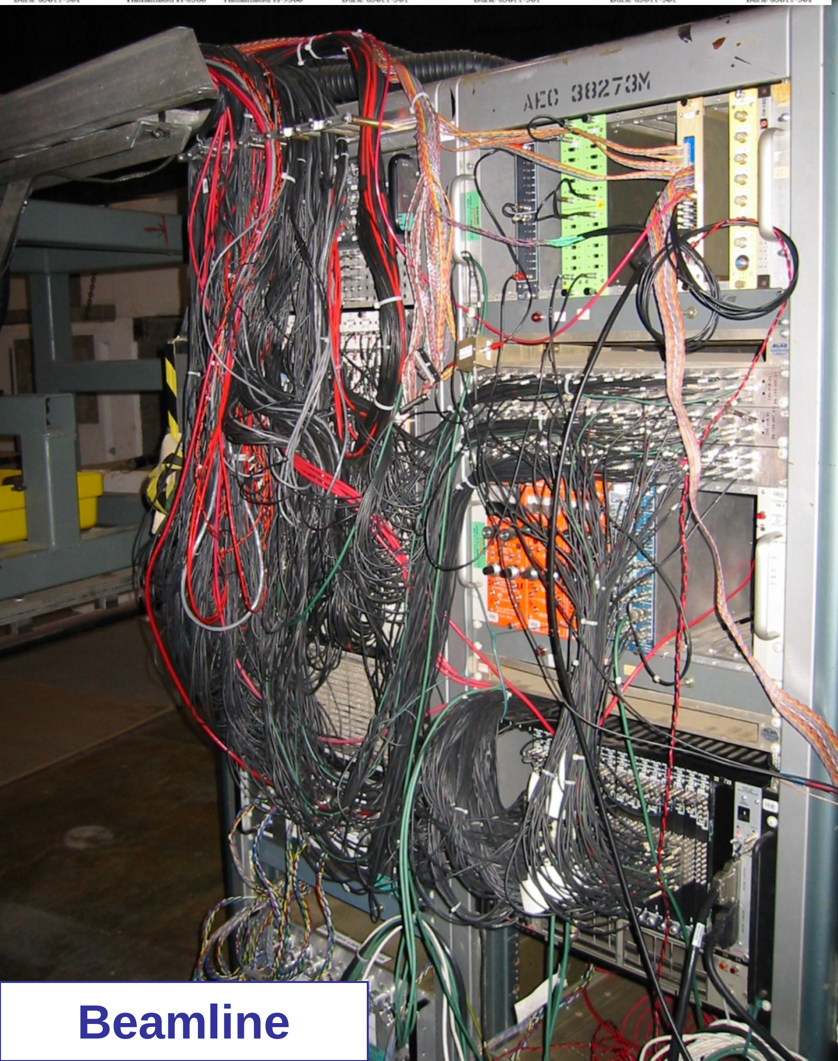



L. Ruckman, G. Varner, NIM **A602** (2009) 438-445

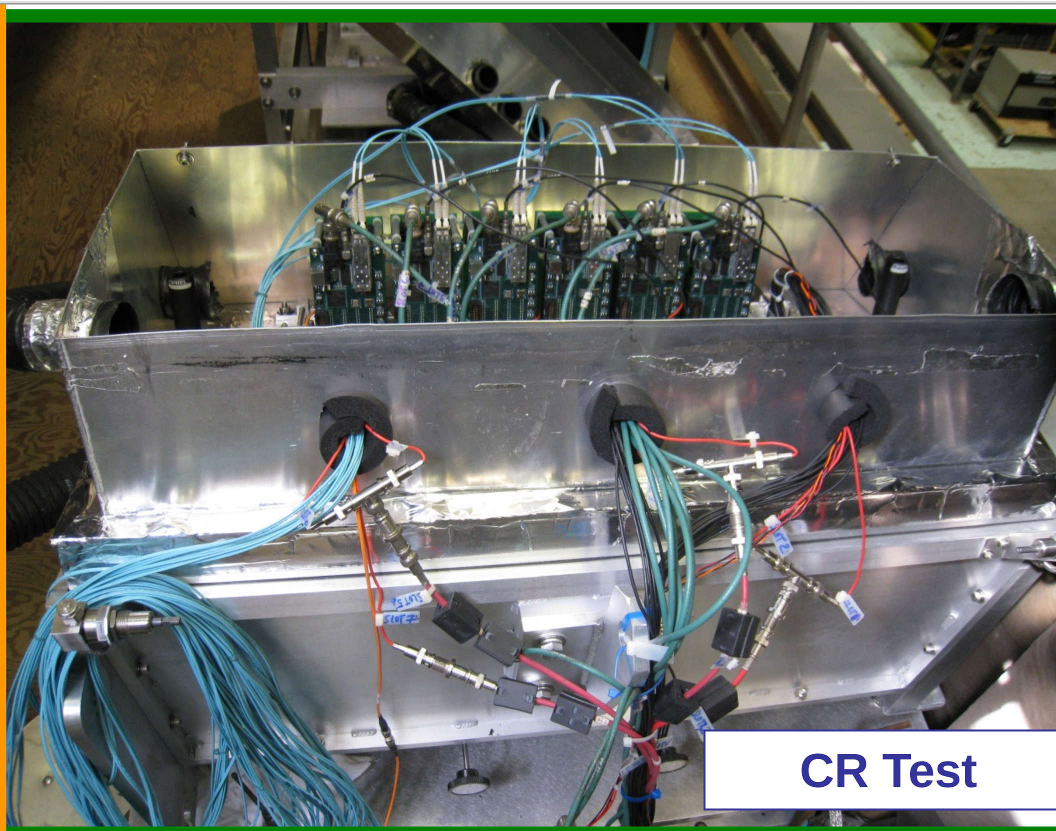
# Fast, Focusing-DIRC Experience






Beamline



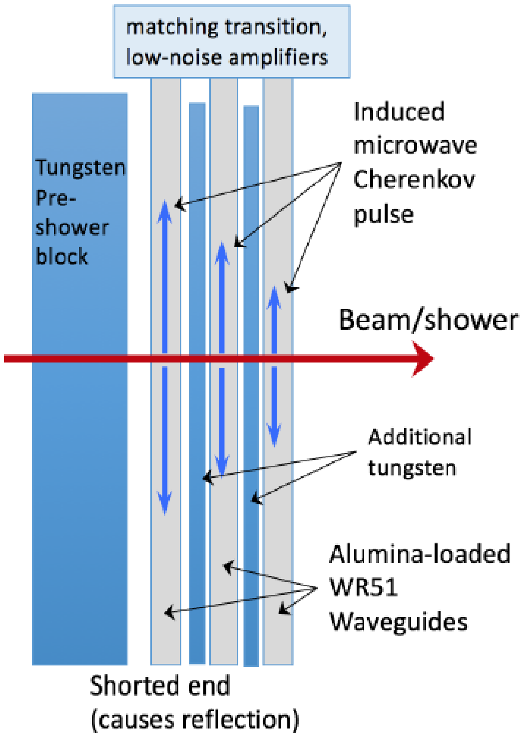
CR Test

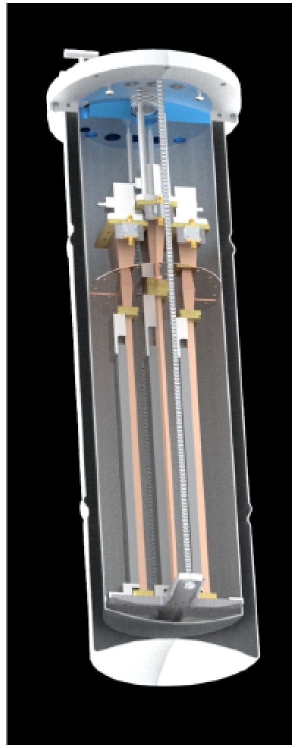
**“25ps CFD in lab”**

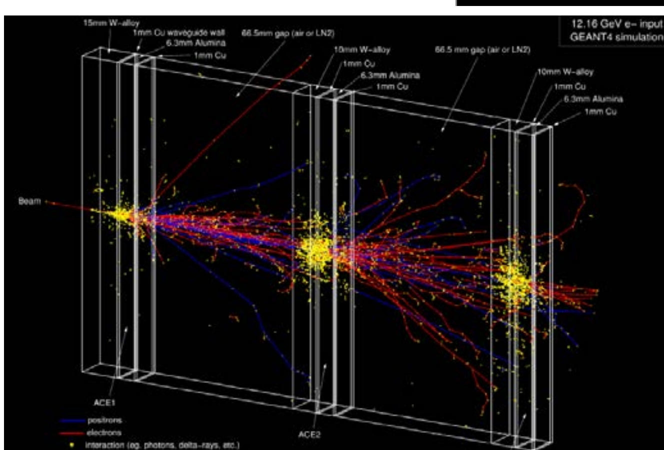
**-End Station A environment**

# Picosecond needs

## Askaryan Calorimeter Exp (ACE)



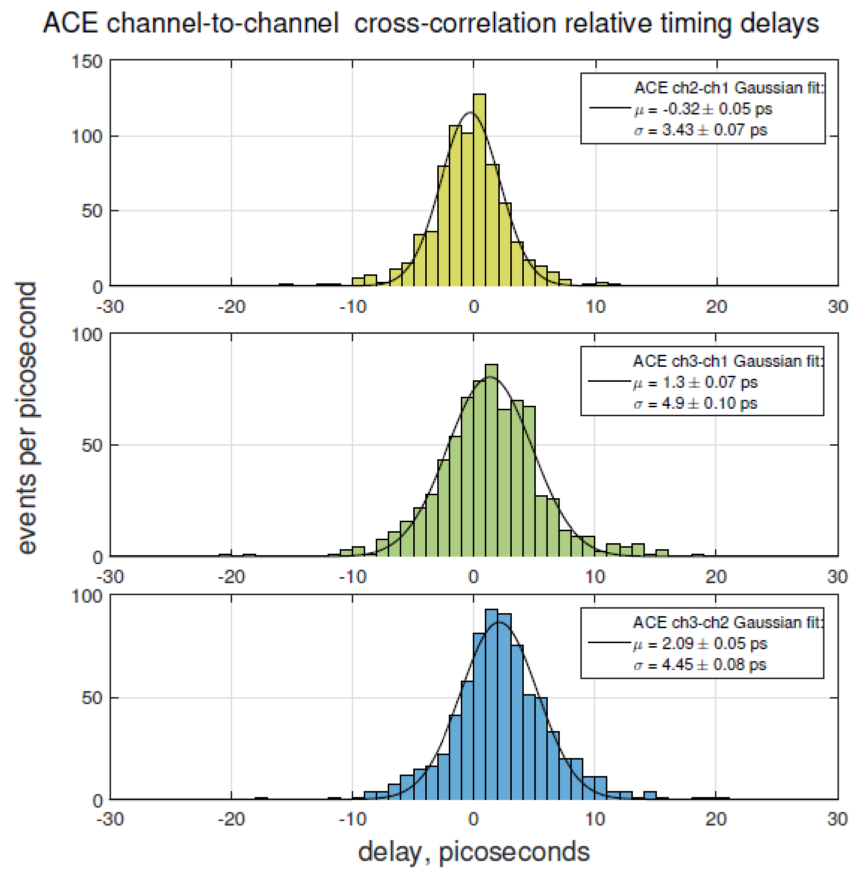



## Radio (mm wave)

**arXiv:1708:01798 (5-AUG-2017)**

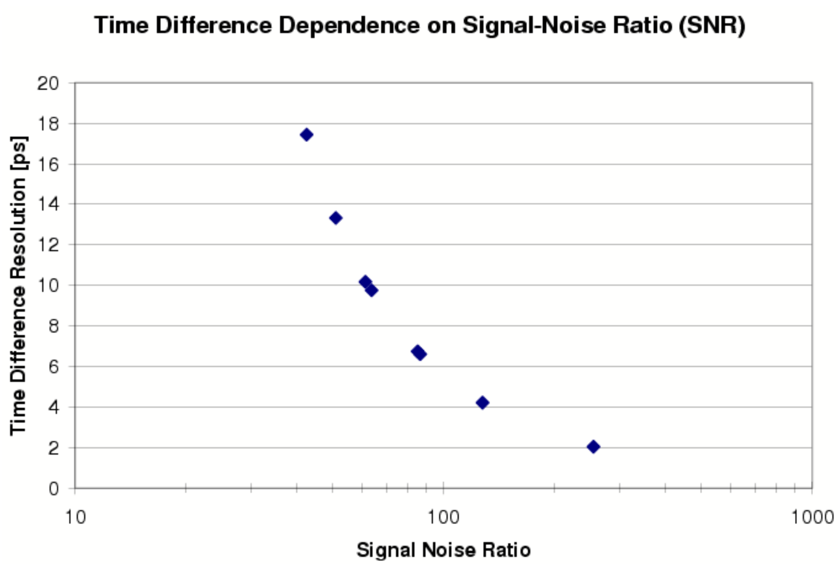
**2.3ps intrinsic timing resolution**

**(SLAC ESTB measurement)**



# Predictions from the last decade …

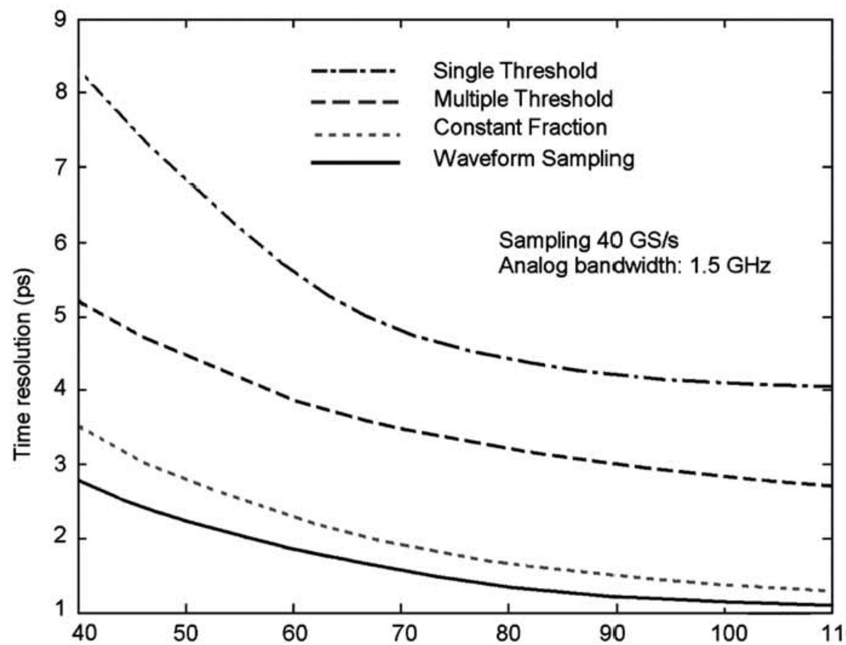
1GHz analog bandwidth, 5GSa/s




G. Varner and L. Ruckman

NIM A**602 (2009) 438-445**.

Simulation includes detector response

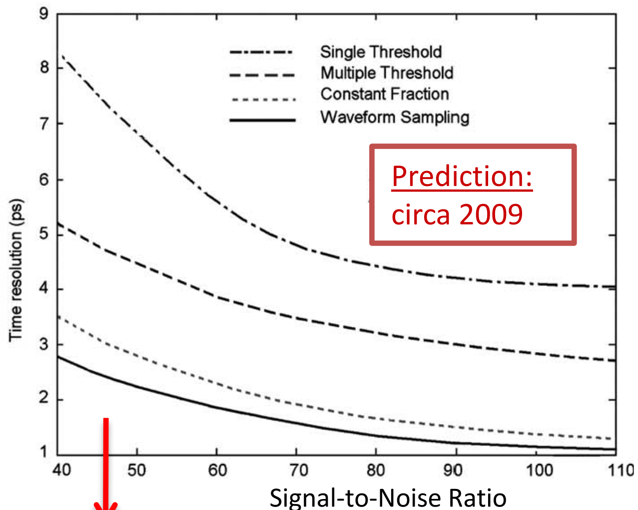


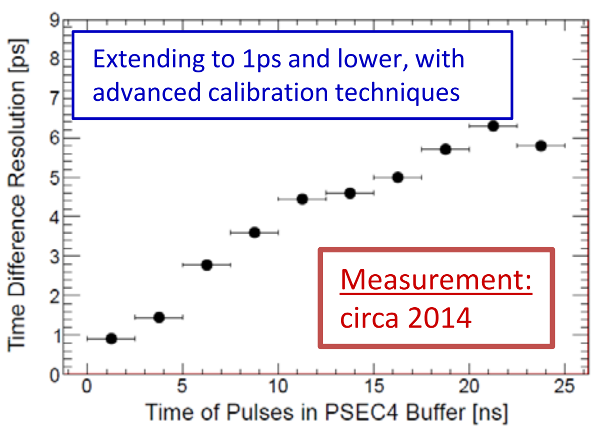

J-F Genat, G. Varner, F. Tang, H. Frisch

NIM A**607 (2009) 387-393**.

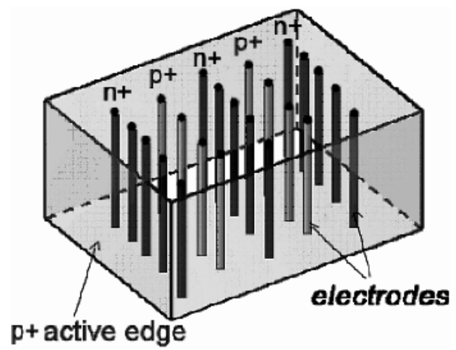
# Interest in exquisite space-time Resolution

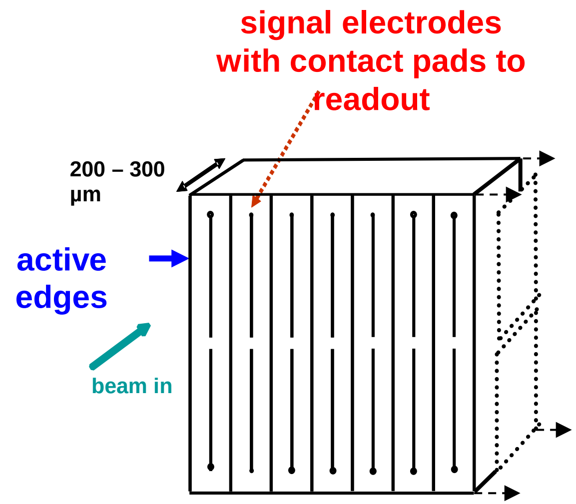
In a number of communities (future particle/astroparticle detectors, PET medical imaging, etc.) a growing interest in detectors capable of operating at the pico-second resolution and μm spatial resolution limit (for light 1 ps = 300 μm)

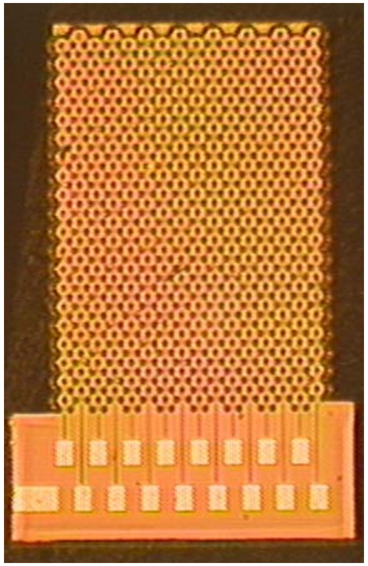



Front-End Electronics



Fast signal collection x-ray detectors

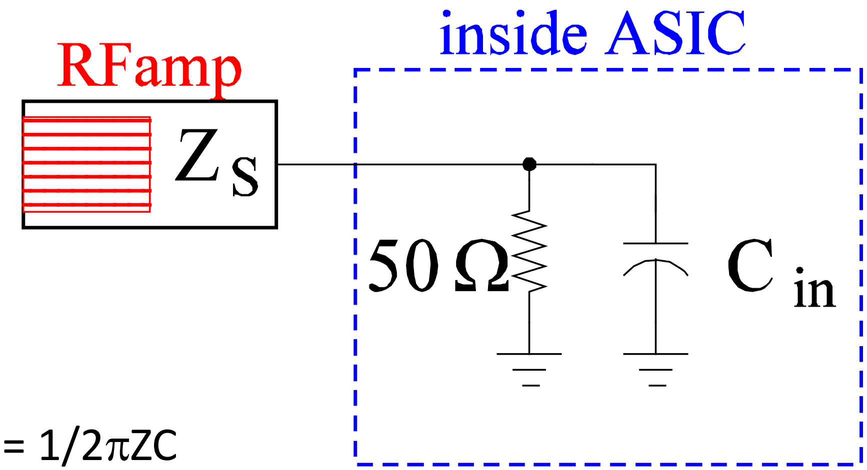
# Toward increased timing precision

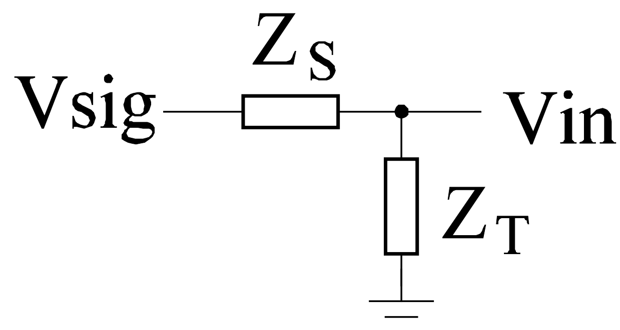
| ASIC | # chan | Depth/chan | Time Resolution [ps] | Vendor | Size [nm] | Year |
|---|---|---|---|---|---|---|
| LABRADOR 3 | 8 | 260 | 16 | TSMC | 250 | 2005 |
| BLAB | 1 | 65536 | 1-4 | TSMC | 250 | 2009 |
| STURM2 | 8 | 4x8 | <10 (3GHz ABW) | TSMC | 250 | 2010 |
| DRS4 | 8 | 1024 | ~1 (short baseline) | IBM | 250 | 2014 |
| PSEC4 | 6 | 256 | ~1 (short baseline) | IBM | 130 | 2014 |
| RITC3 | 3 | Continuous | TBD | IBM | 130 ? | --- |
| PSEC5 | 4 | 32768 | TBD | TSMC | 130 | --- |
| DRS5 | 8/16? | 128x32 | TBD | UMC | 110 | --- |
| SamPic | 16 | 64 | ~few [pic 0] | AMS | 180 | [2014] |
| RFpix | 128? | TBD | <= 100fs (target) | TSMC | 130 ? | --- |

Very incomplete: missing S. Kleinfelder ASIC from yesterday

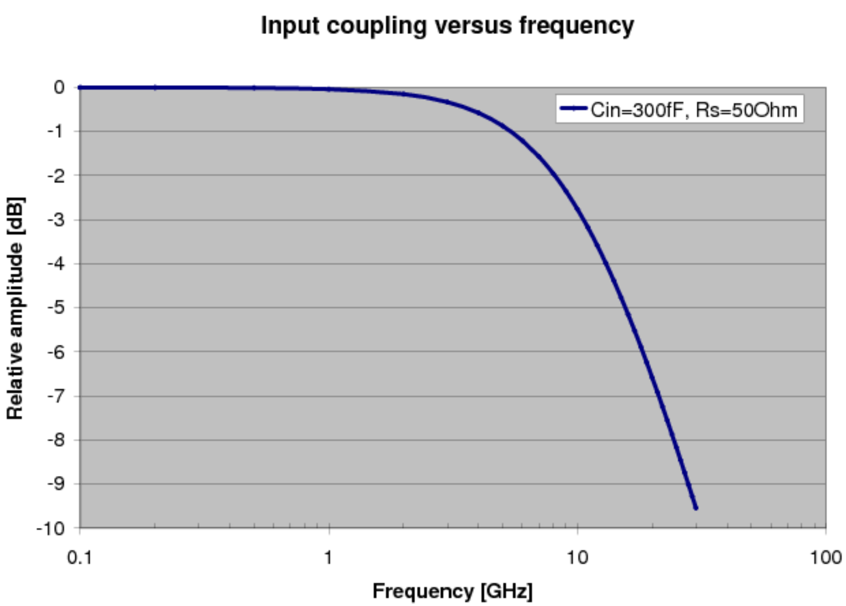
# Constraint 1: Analog Bandwidth

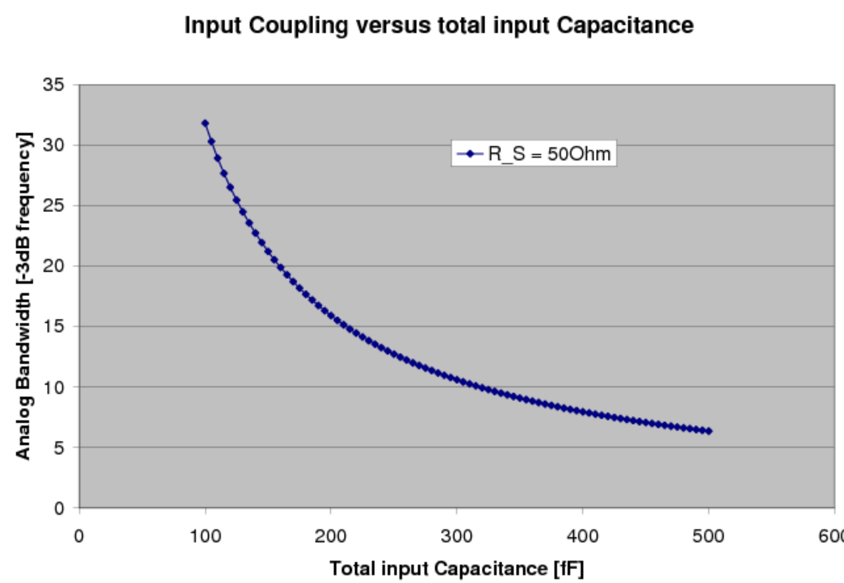
**Difficult to couple in Large BW (C is deadly)**



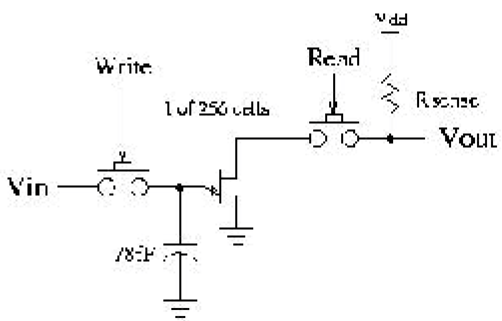

$f_{3dB} = 1/2\pi ZC$



# Constraint 2: kTC Noise

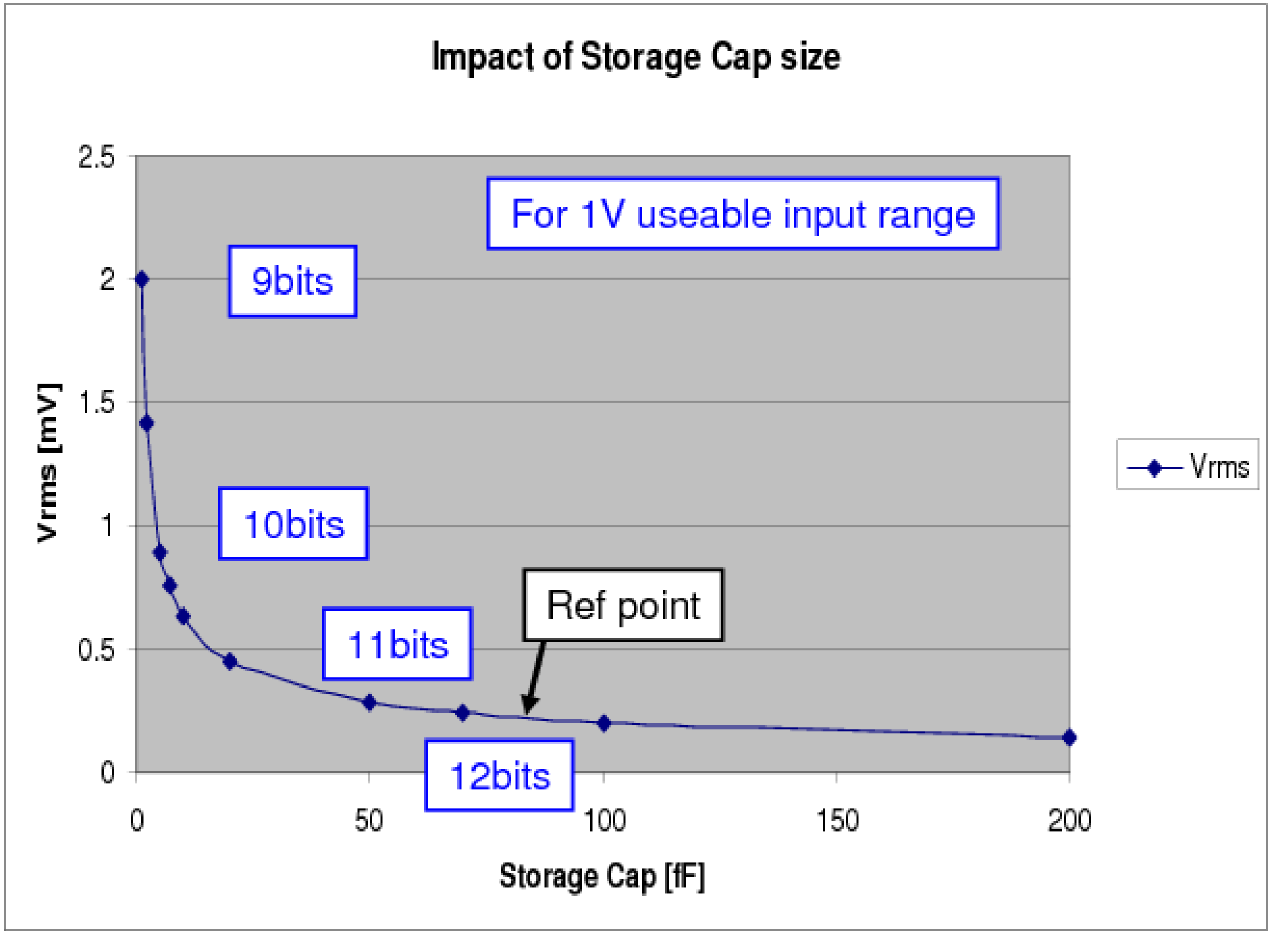
Want small storage C, but…




$$v_{rms} = \sqrt{\frac{kT}{C_{store}}} = 0.23mV$$

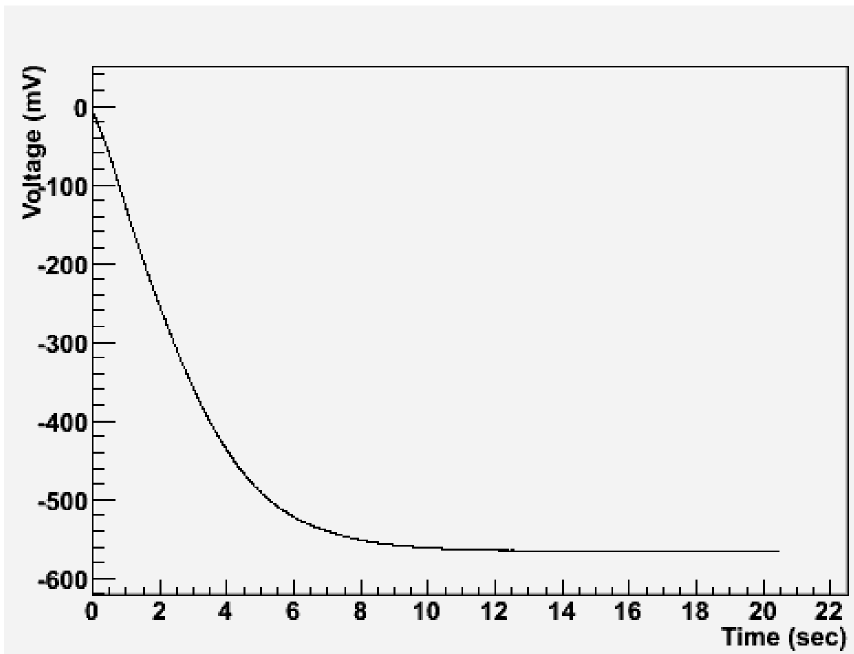
$C_{store}$ = 78fF

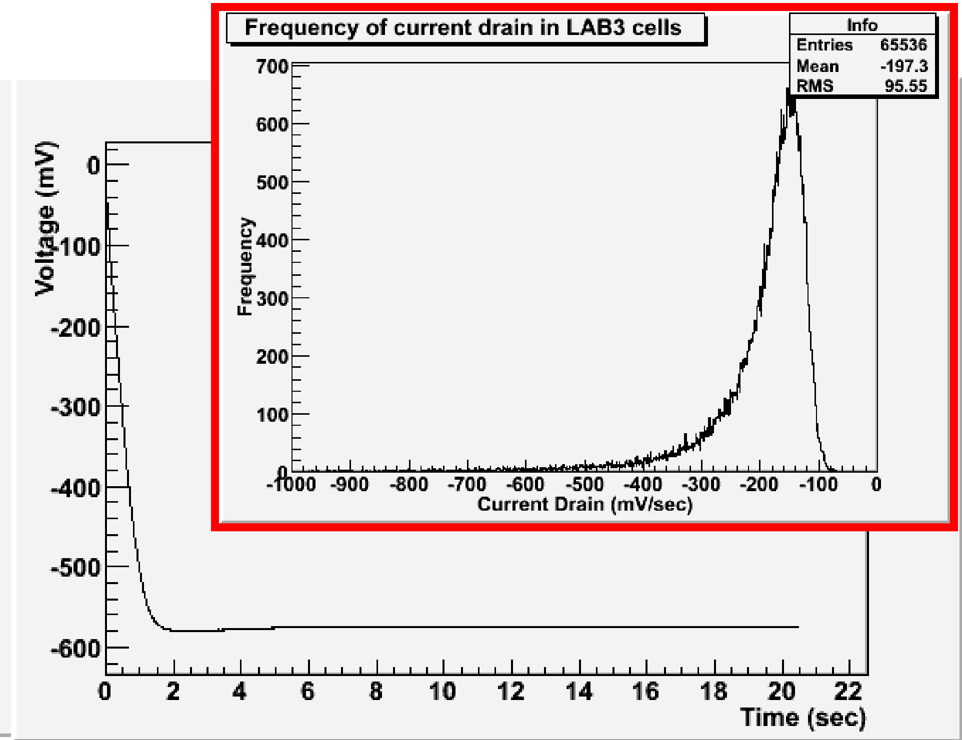
**1mV on 16fF is only 100e- !**



# Constraint 3: Leakage Current

Increase C or reduce conversion time << 1mV




Sample channel-channel variation

~ fA → nA leakage (250nm → 130nm)

# The ultimate Space-Time Limit

- How to measure something extremely precisely in HEP?

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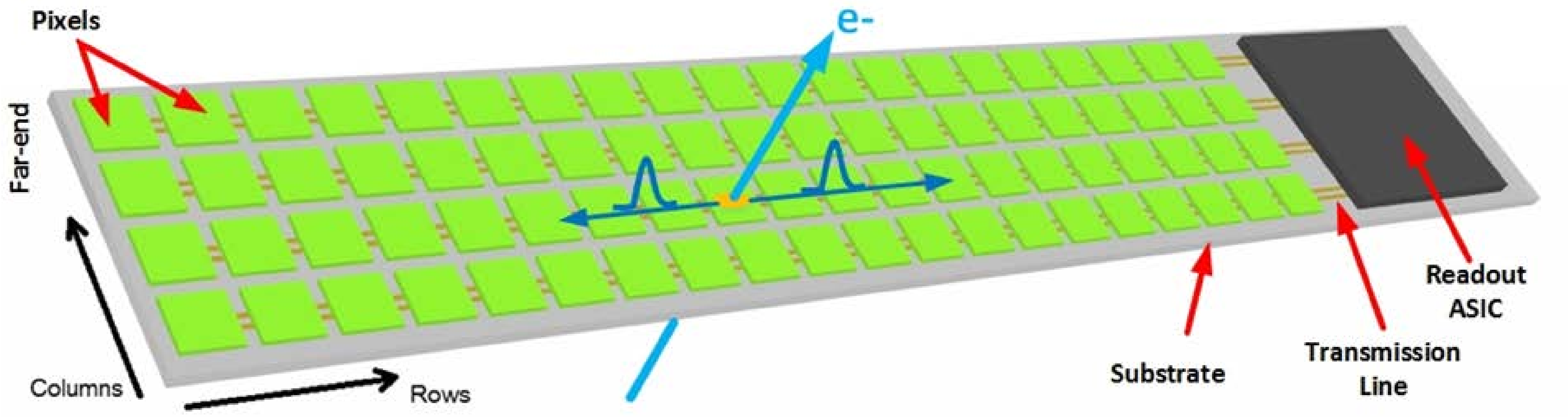
- How to measure something extremely precisely in HEP?

Cancel systematic errors in ratio

# What would it take?



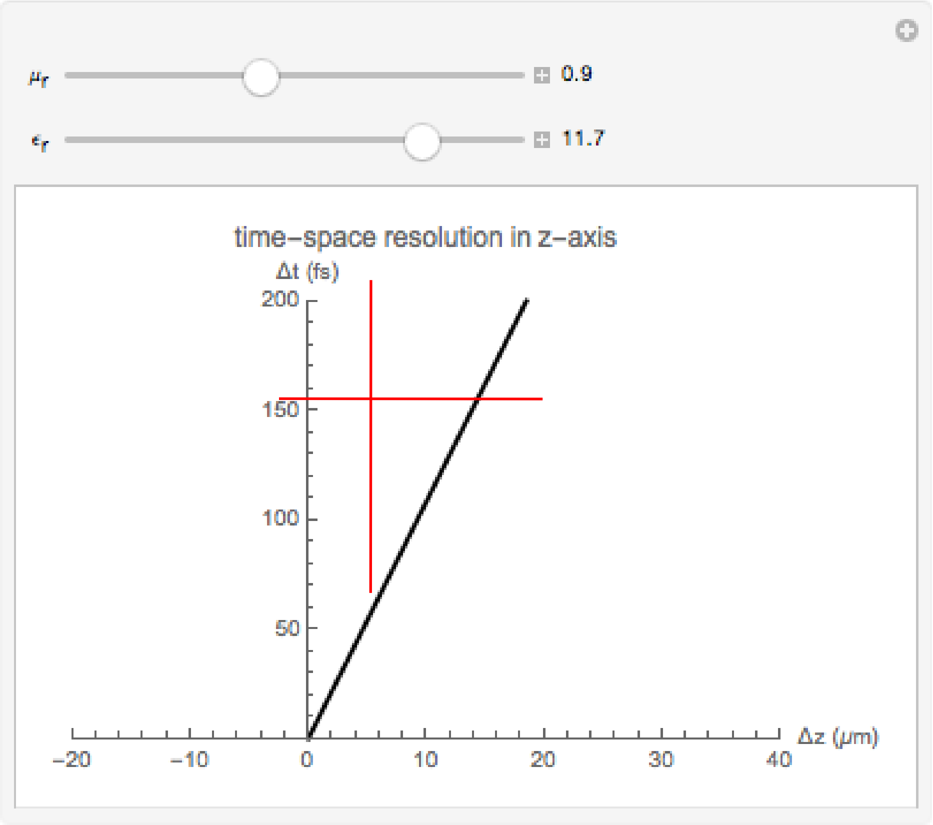

- Micron spatial pixel resolution (using timing)

→ Fast timing brings many benefits:

  - ***Minimal pile-up (fast clearing)***
  - ***Improved event timing (direct T0 for TOF/TOP measurements)***
  - ***Belle II data archiving!***

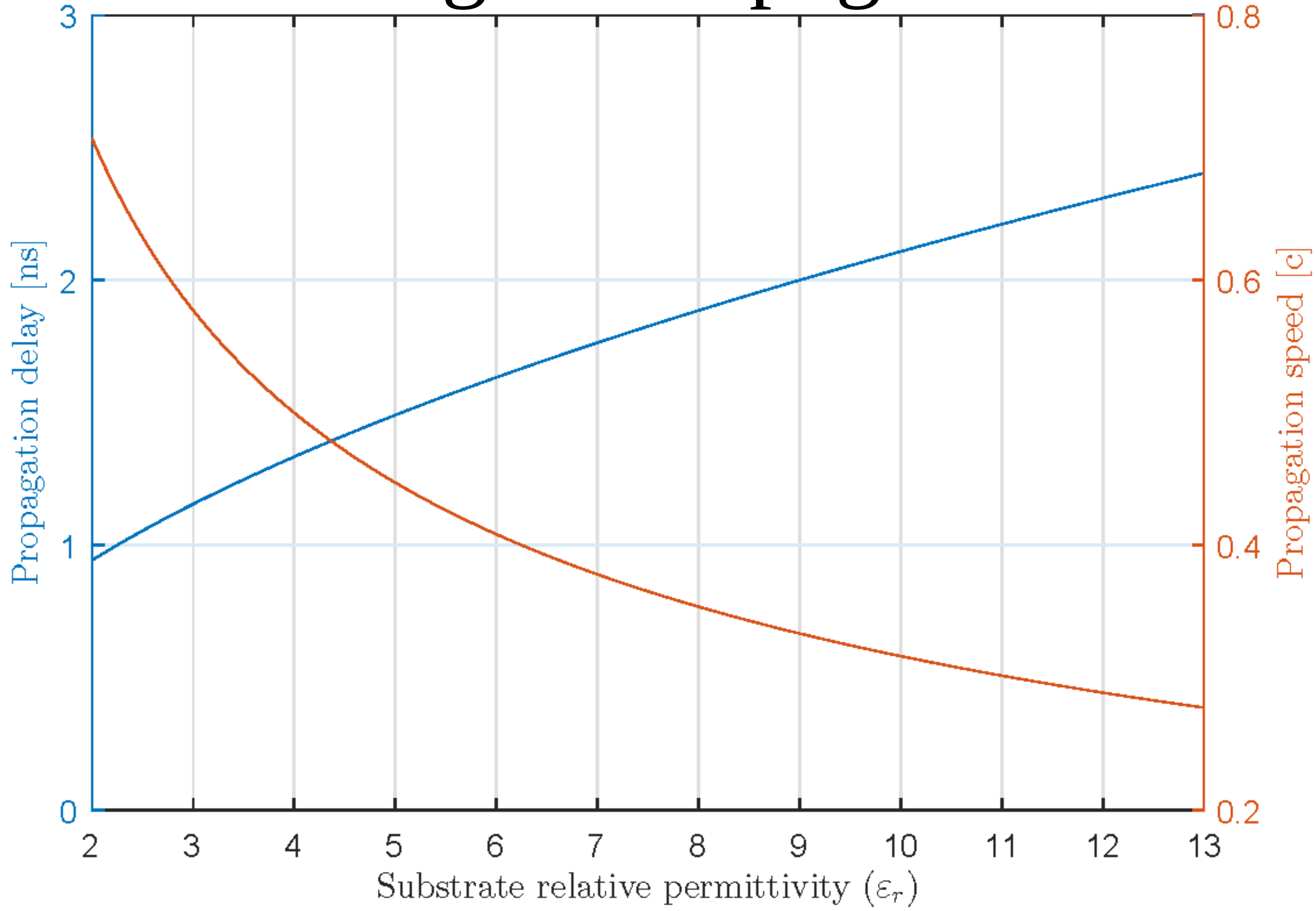
# Exploration of the space-time limit

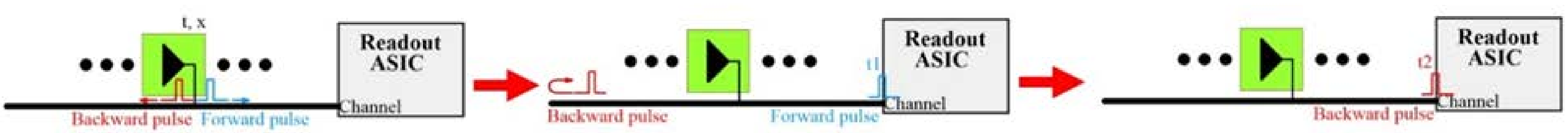
-Sampling at high sampling rate and high bandwidth
-Resolve small distances
Current Goals: Spatial resolution of 10μm in z and 20μm in rφ
In Silicon 10μm in z corresponds to timing resolution of about 100fs
20μm in rφ will depend on the SNR



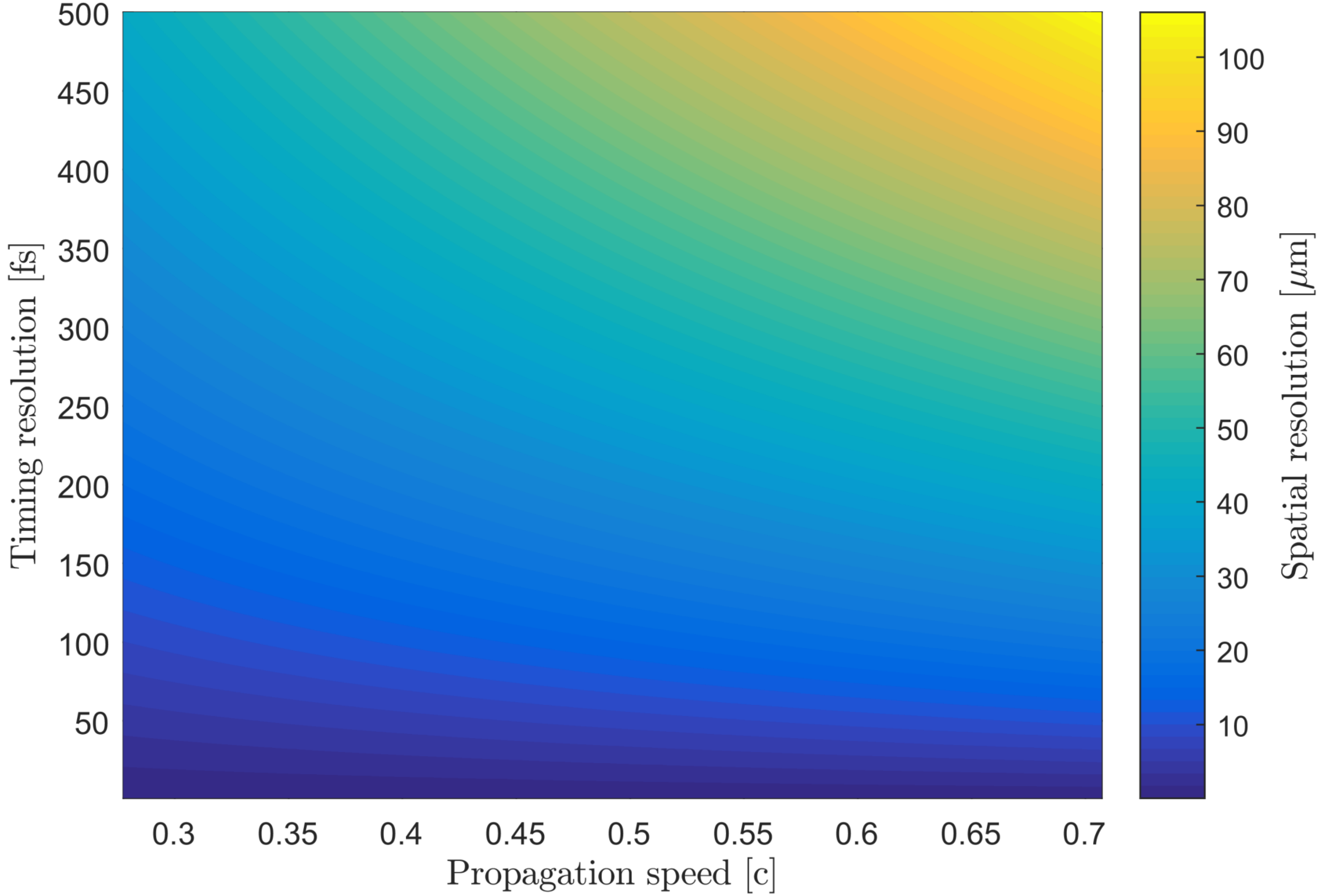

Pixel detector (PDX) at SuperKEKB

# Signal Propagation

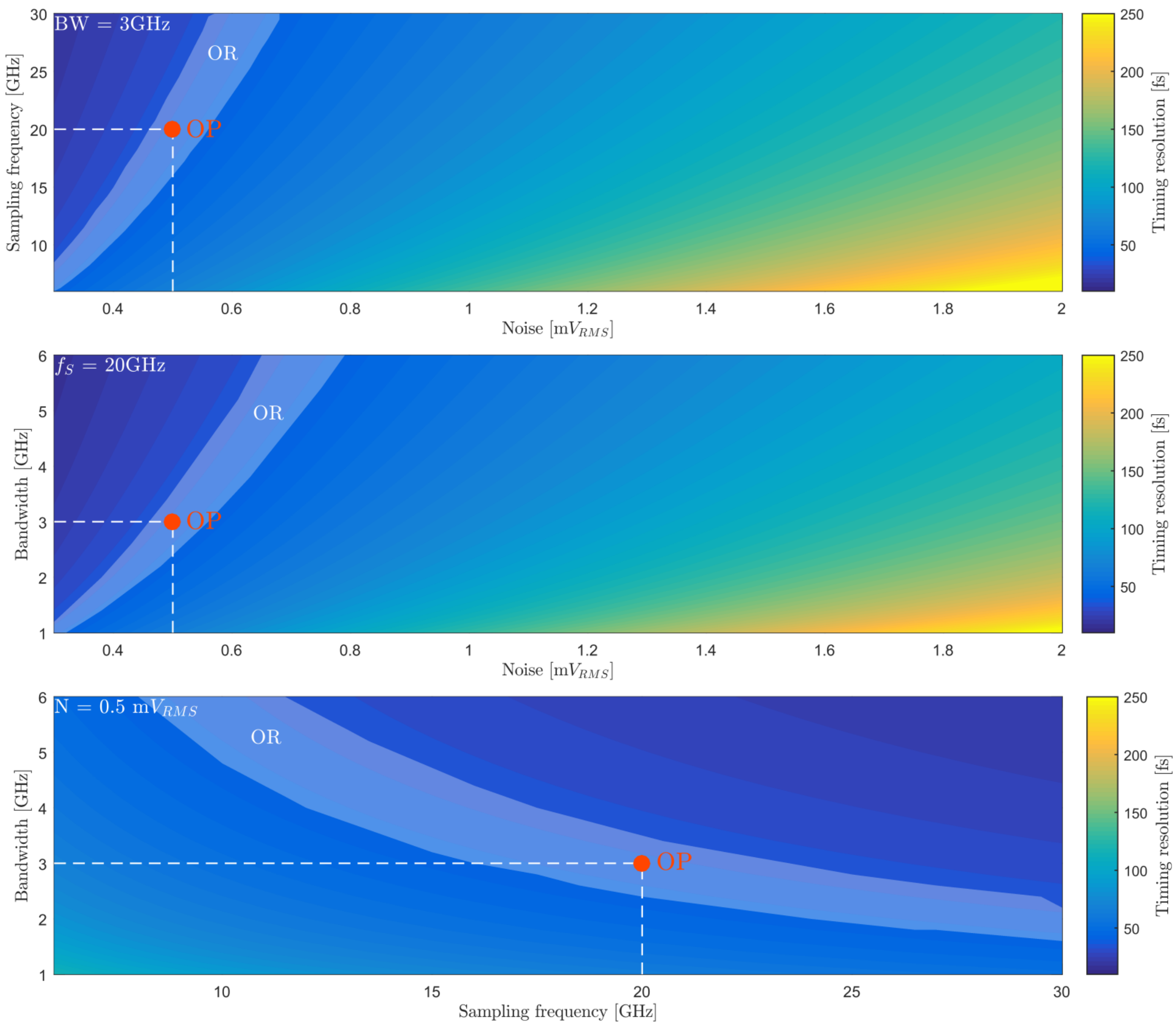


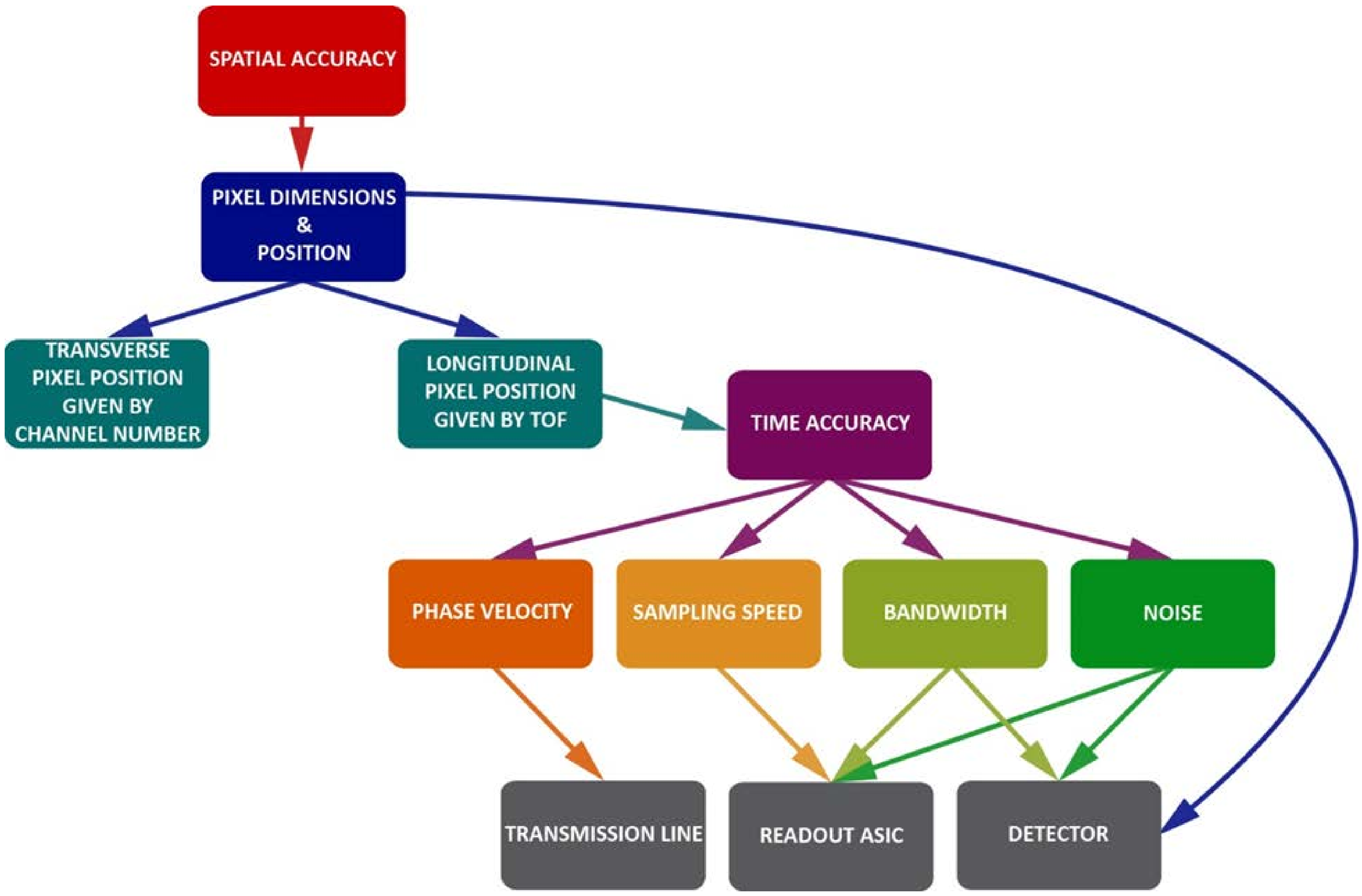
# Spatial resolution correlation



# Performance Parameter Space



# Overall optimization/interplay



# Target Specifications

| Parameter | Minimum desired value |
|---|---|
| Sampling frequency (ASIC) | 20 GHz |
| Bandwidth (Detector and ASIC) | 3 GHz |
| Signal to Noise Ratio (Detector and ASIC) | 58dB ($V_{signal}$=1 Volt) |
| Velocity of Propagation (Transmission Line/ strip line) | 0.35c |
| Number of Bits of Resolution | 9.4 bit |

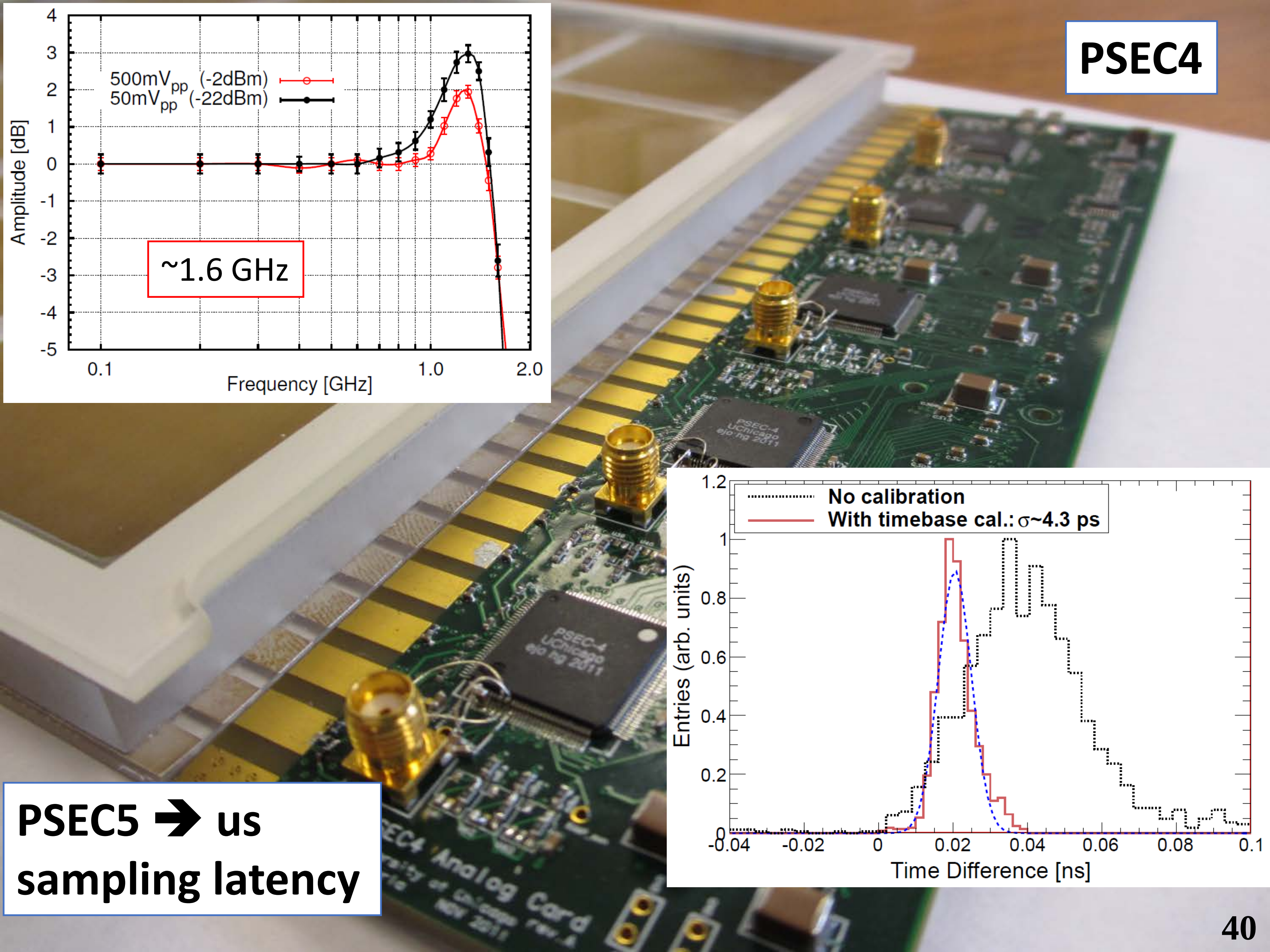
**This is an ongoing study – snapshot**

**PhD student needs to finish → focus on ASIC**

**A device with <=1ps (independent of aperture) interesting**

**PSEC4 design as a reference → PSEC5 design**

# PSEC4



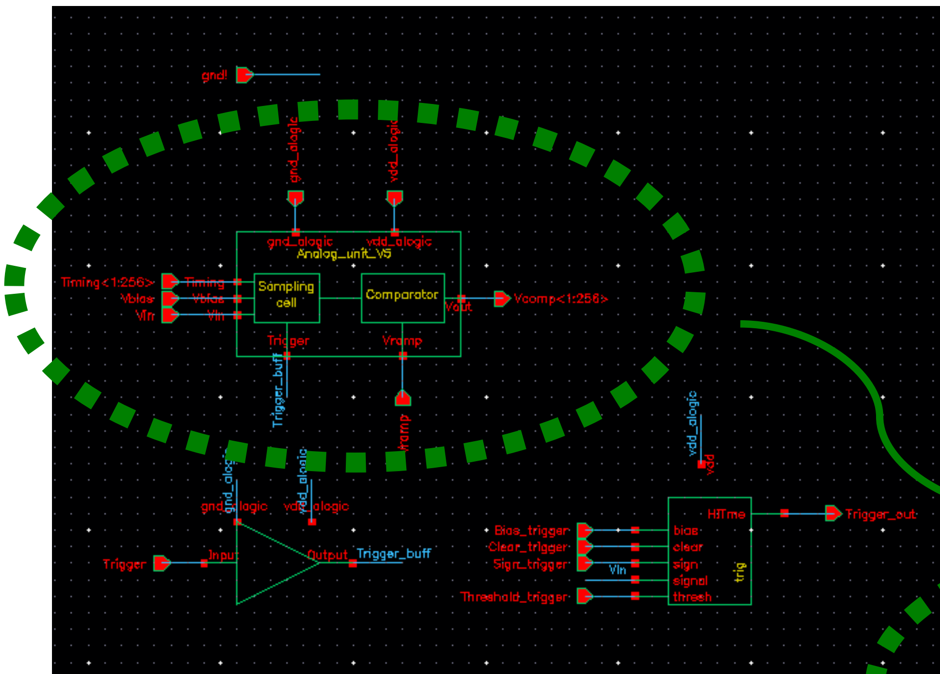

**PSEC5 ➔ us sampling latency**

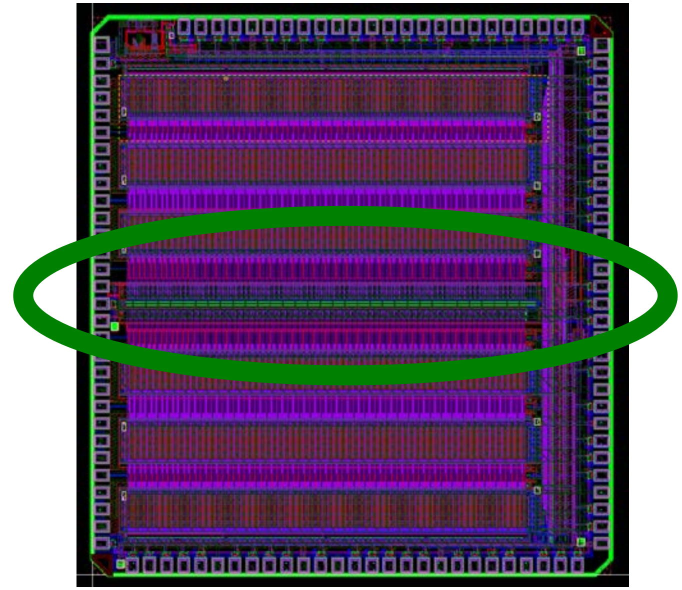
# PSEC4: Sampling Analysis

Utilizing PSEC4's SCA as starting place

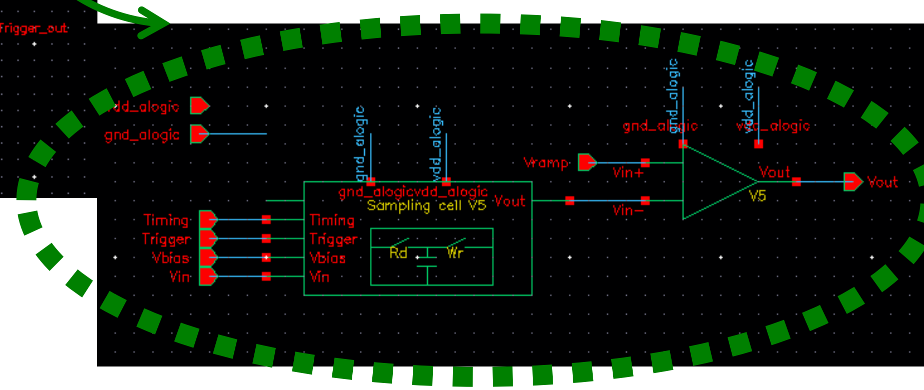
-Adjustable Sampling rate between 4-15 GSPS

-1.6 GHz bandwidth





x256



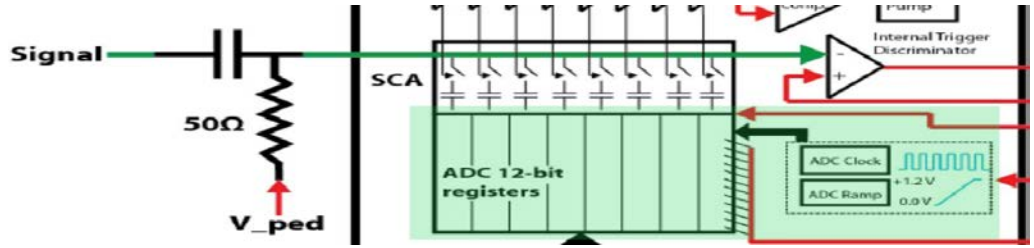
also

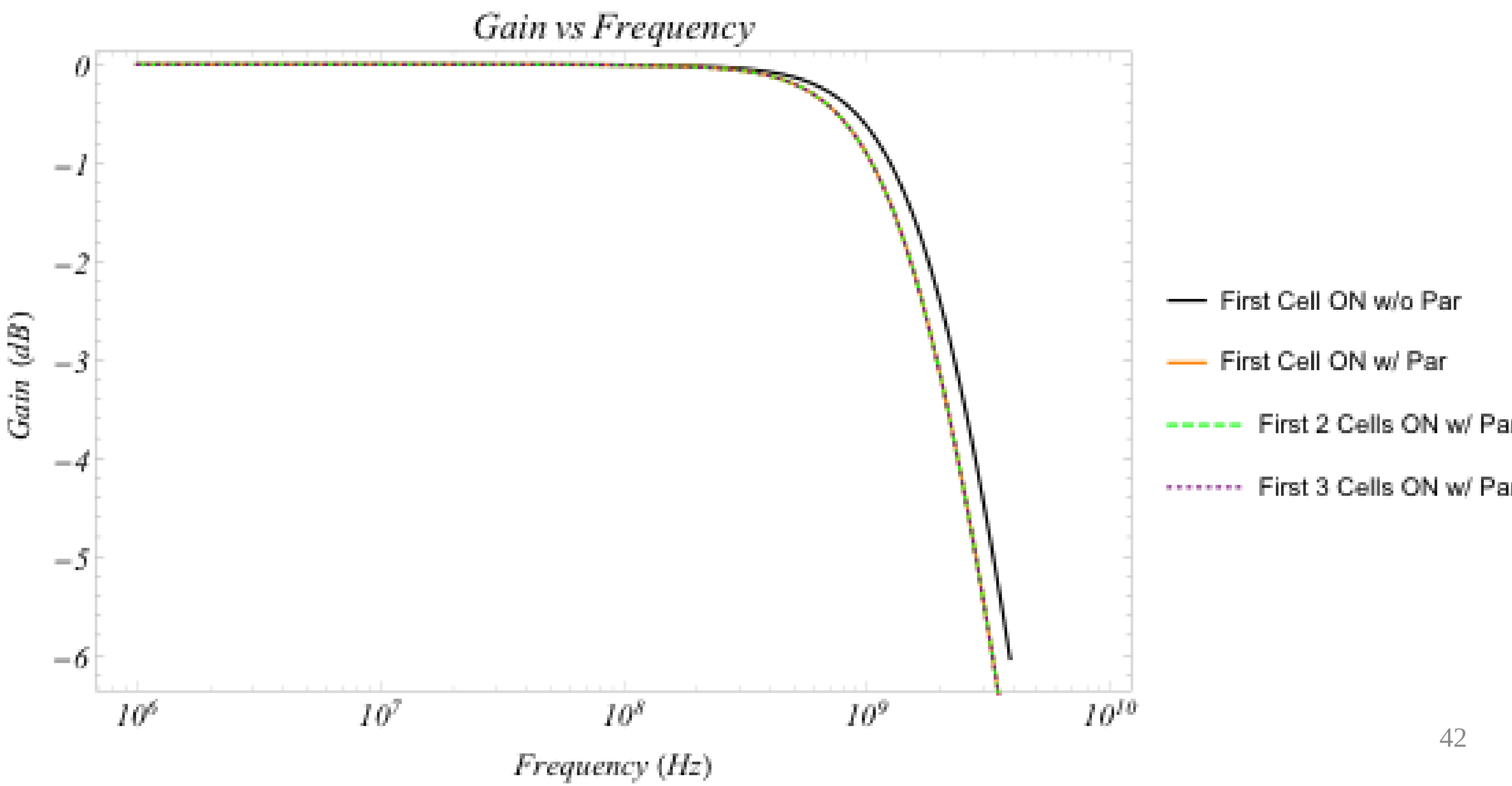
-0.13µm CMOS (IBM-8RF)

-10.5 bit  DC dynamics

# Equivalent Circuit

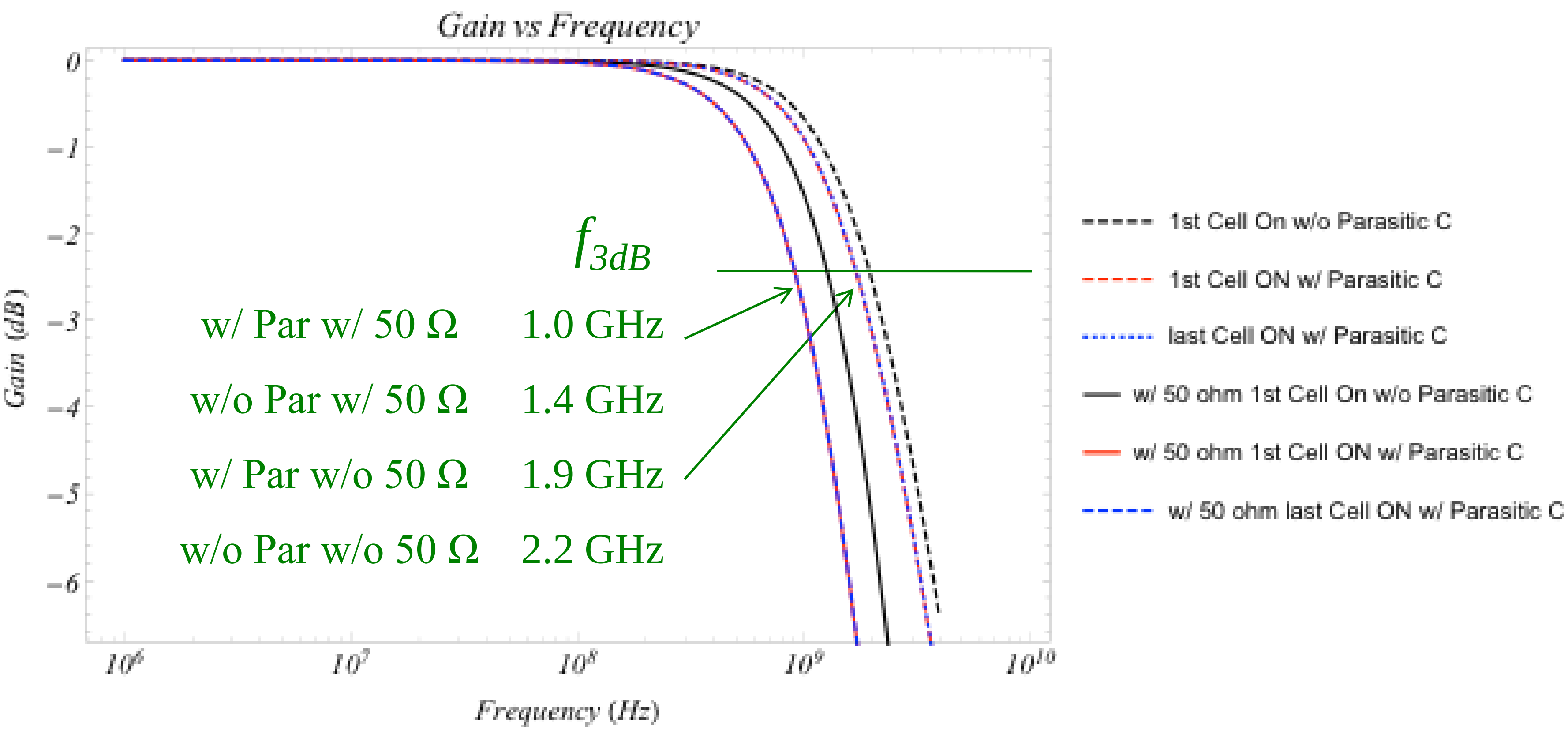
Multichannel sampling array



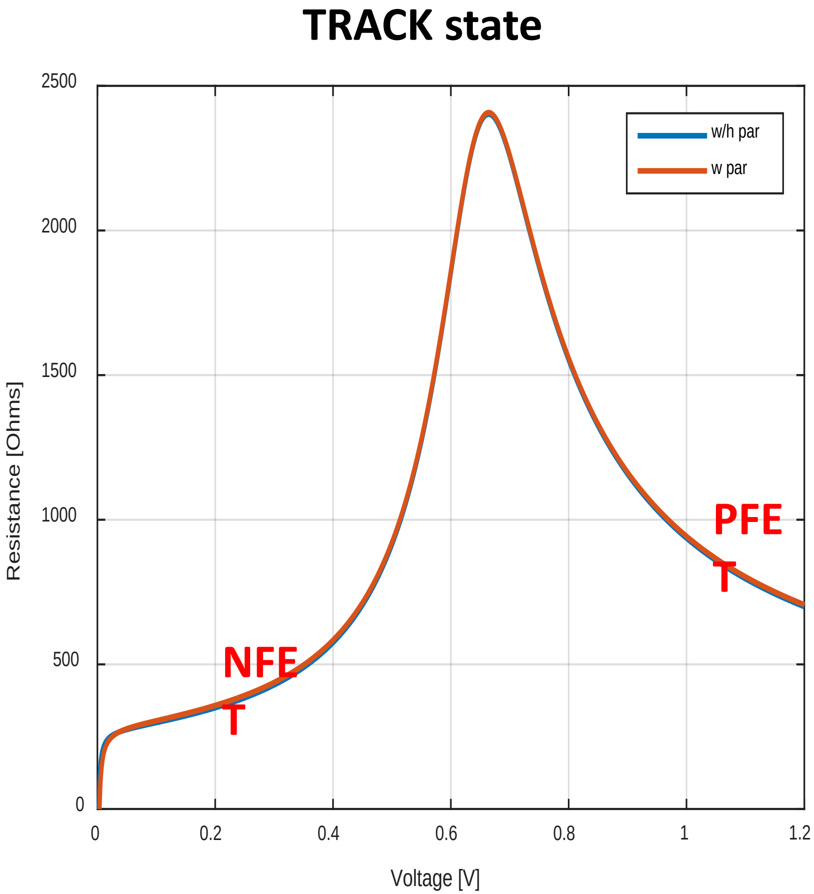



# Simulation Results: Bandwidth for worst case operating bias point

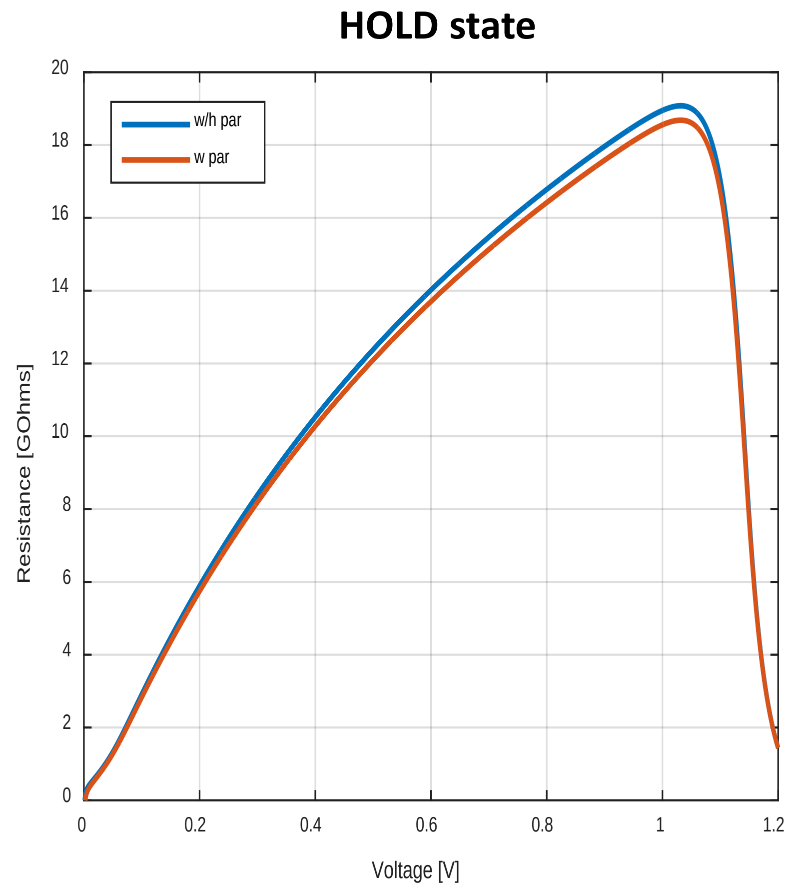
Whether the 1st switch is on or the last, Gain is the same



# Pass Transistor (Switch) Resistance




- **Ron=2.4k @665mVdc**

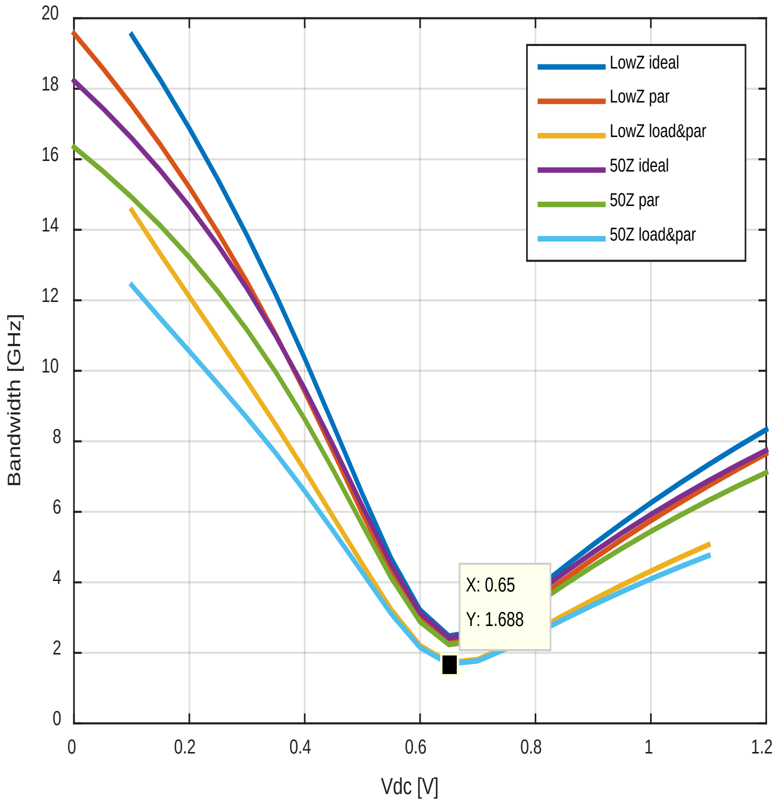



- **Roff is in GΩ**

- **The PFET and NFET are not matched and Ron varies considerably**

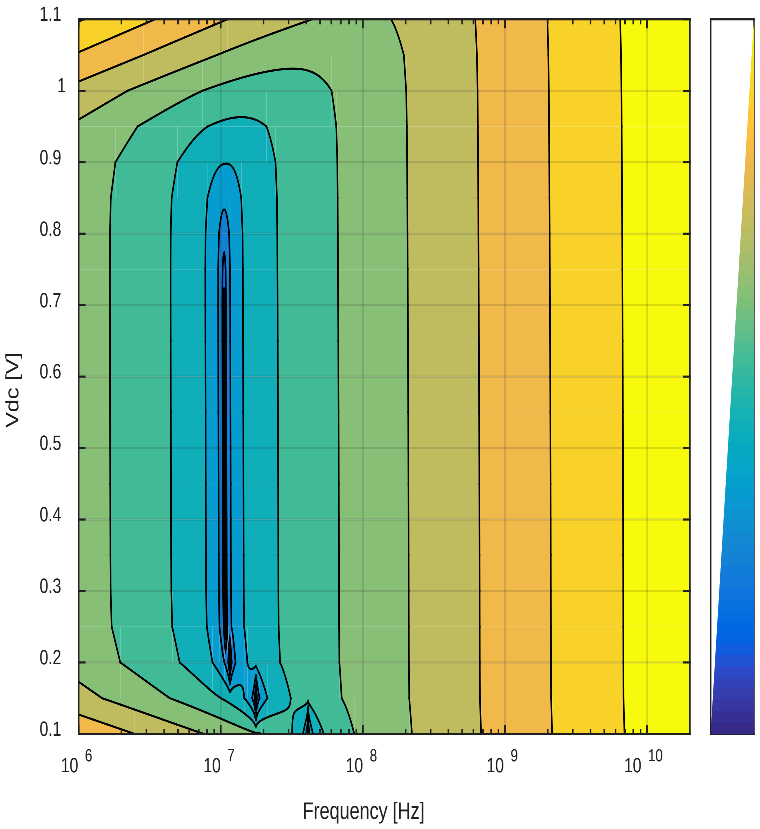
# Small signal frequency response

## Bandwidth




- **BWworst≈2.3GHz @665mVdc @LowZ drive**
- **BWworst≈1.7GHz @665mVdc @50Ω drive**

## Isolation



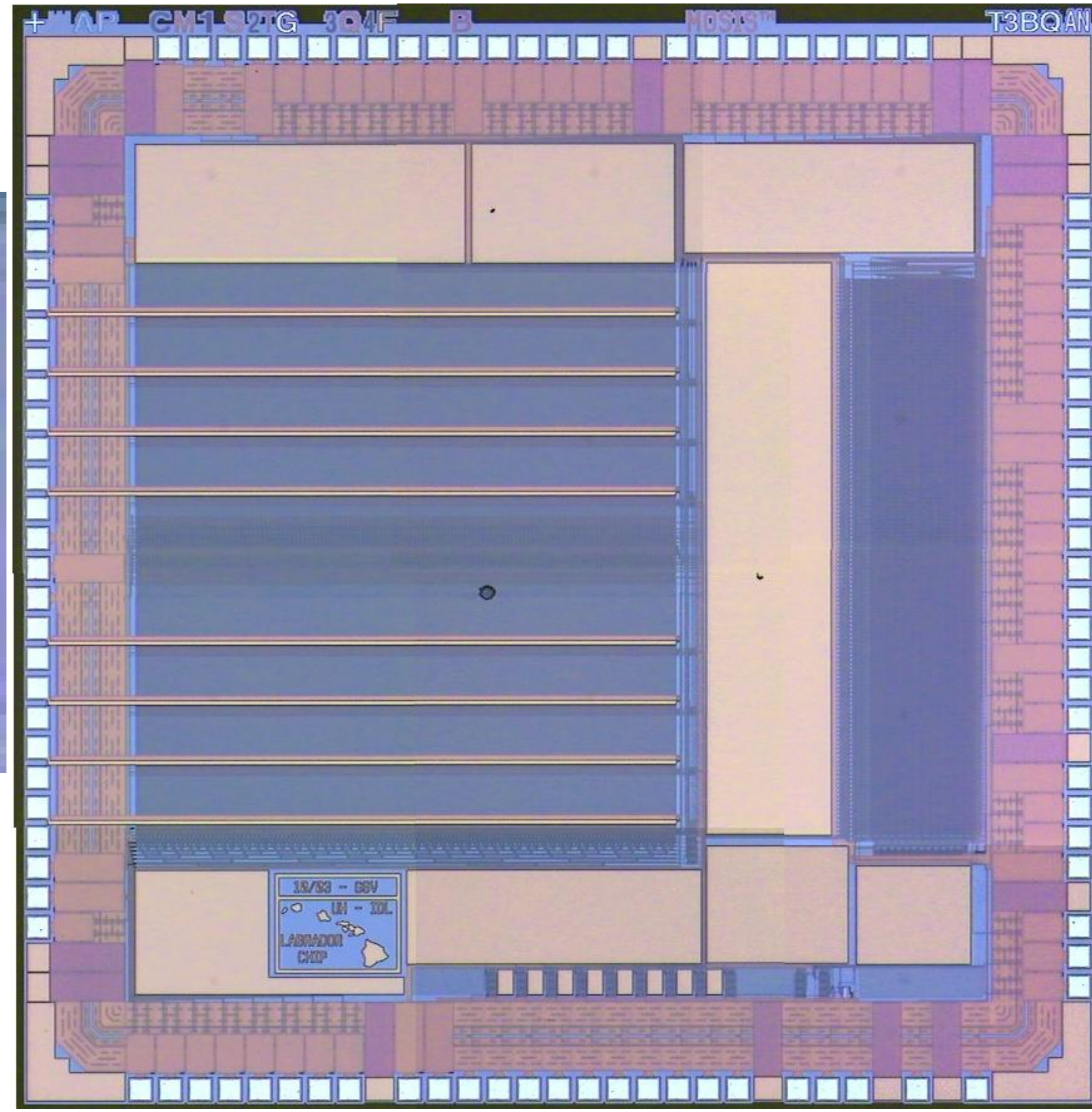

- **Isolation is over 60dB over all parameter space**

# Summary

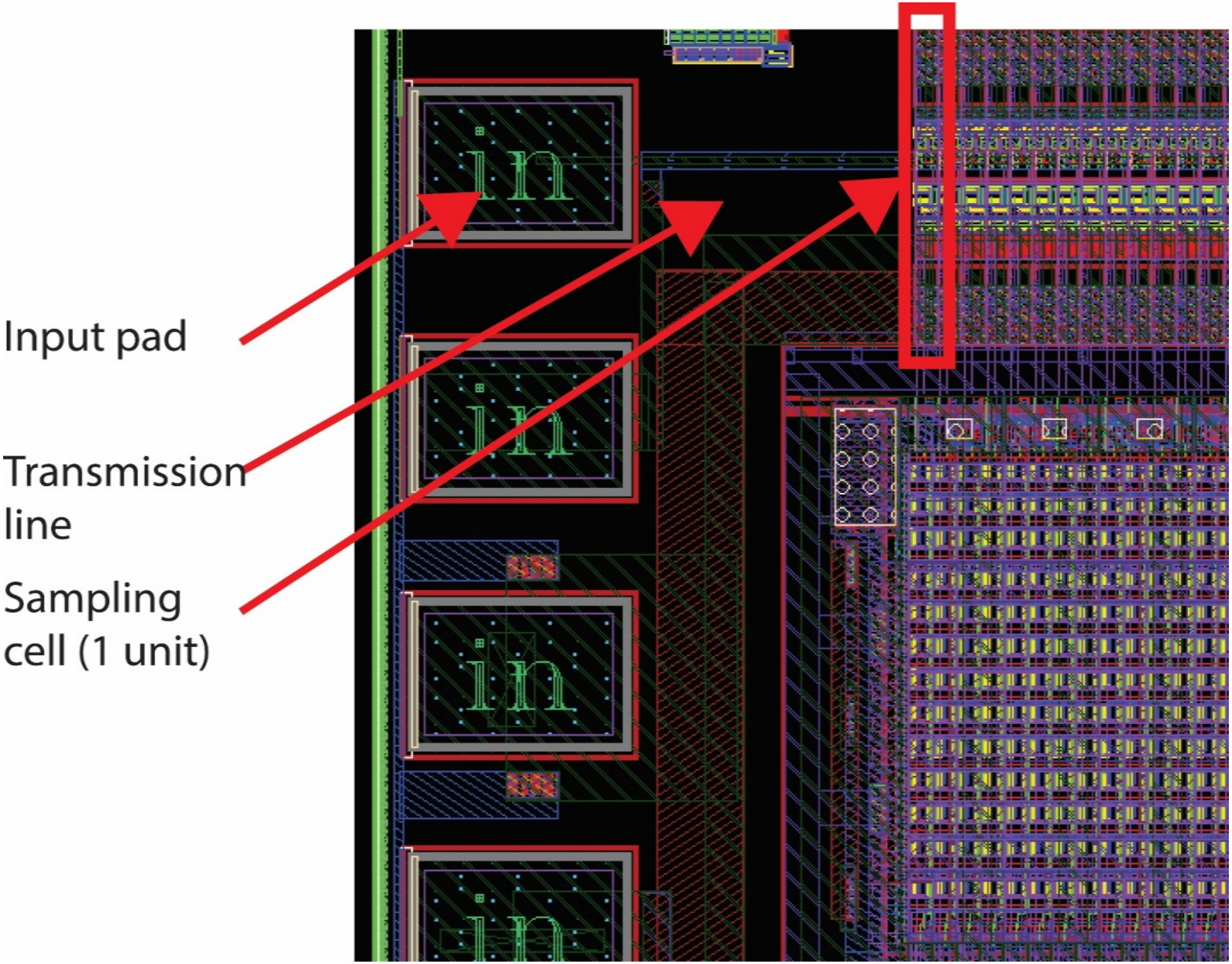
## ‘Precision Timing’ has different meanings

- **10’s of picoseconds:**
  - **HL-LHC, MCP-PMTs, TOF-PET**
  - **Many WFS, TDC options: amplifier challenge**
  - **System engineering**
- **~1ps:**
  - **Space-time Detector determined**
  - **Direct conversion techniques**
- **Femtosecond:**
  - **Differential techniques**
  - **Pushing the equivalent space-time limit**

# Back-up slides

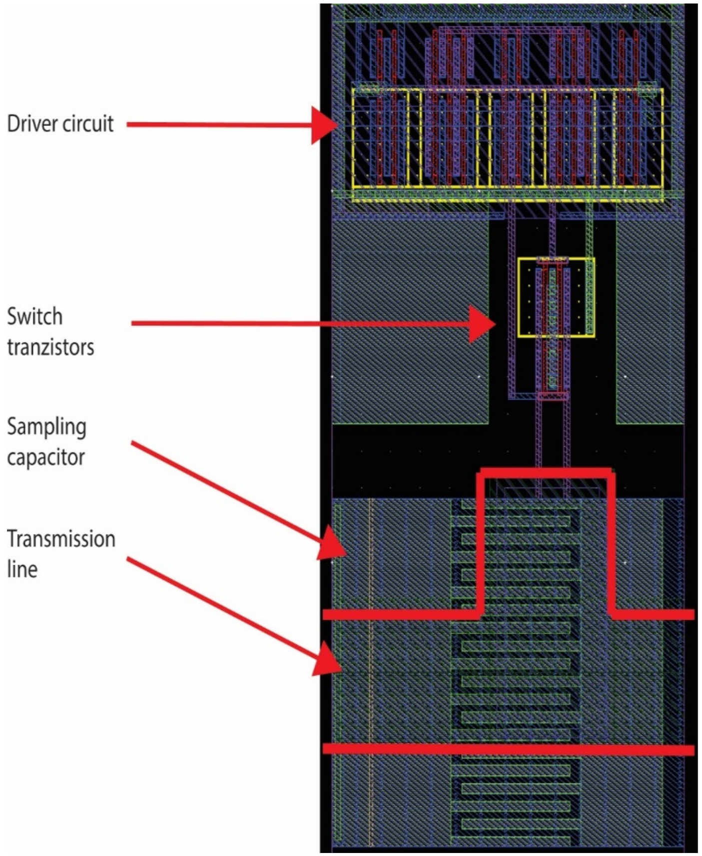
# PSEC4 Analysis: Single Sampling Cell



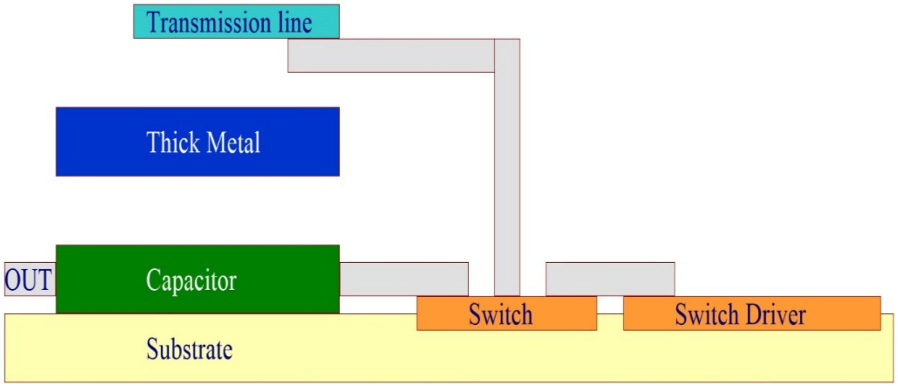
# PSEC4 Analysis: Single Sampling Cell

## Structure & Layout

**Top view**

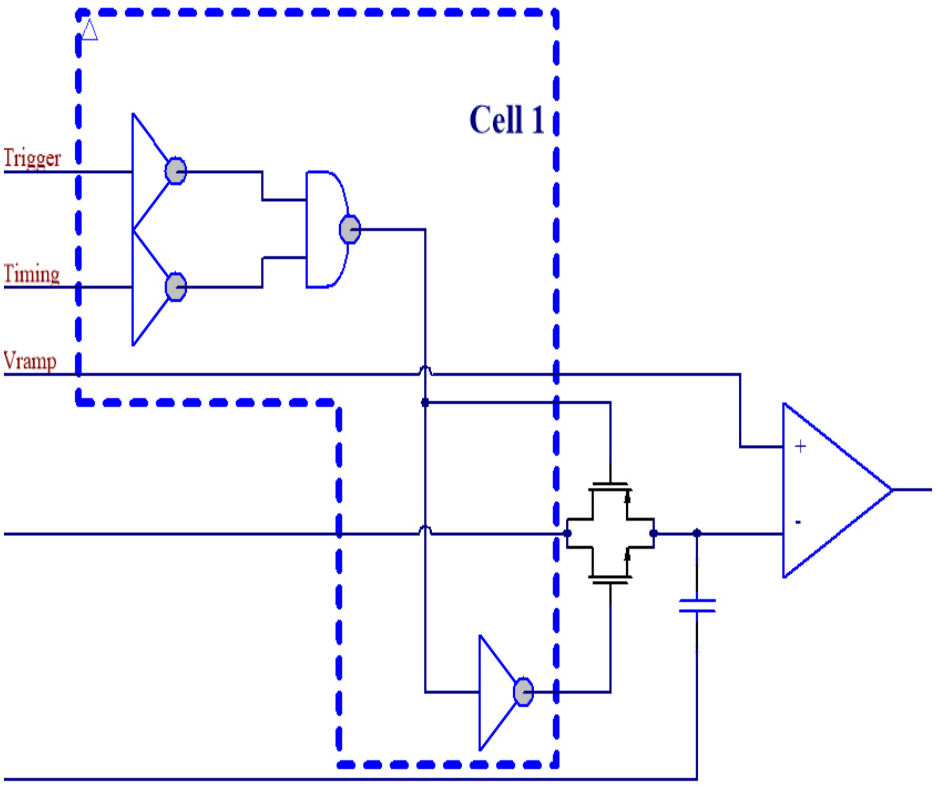



**Side view**



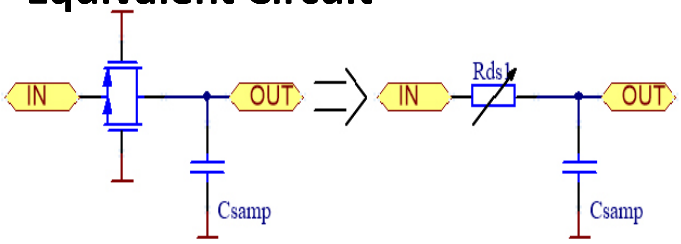
# Single Sampling Cell Coupling

**Simplified Schematic**




- Driver circuit
- Switch with n-p FET pair
- Sampling capacitor
- Comparator as load

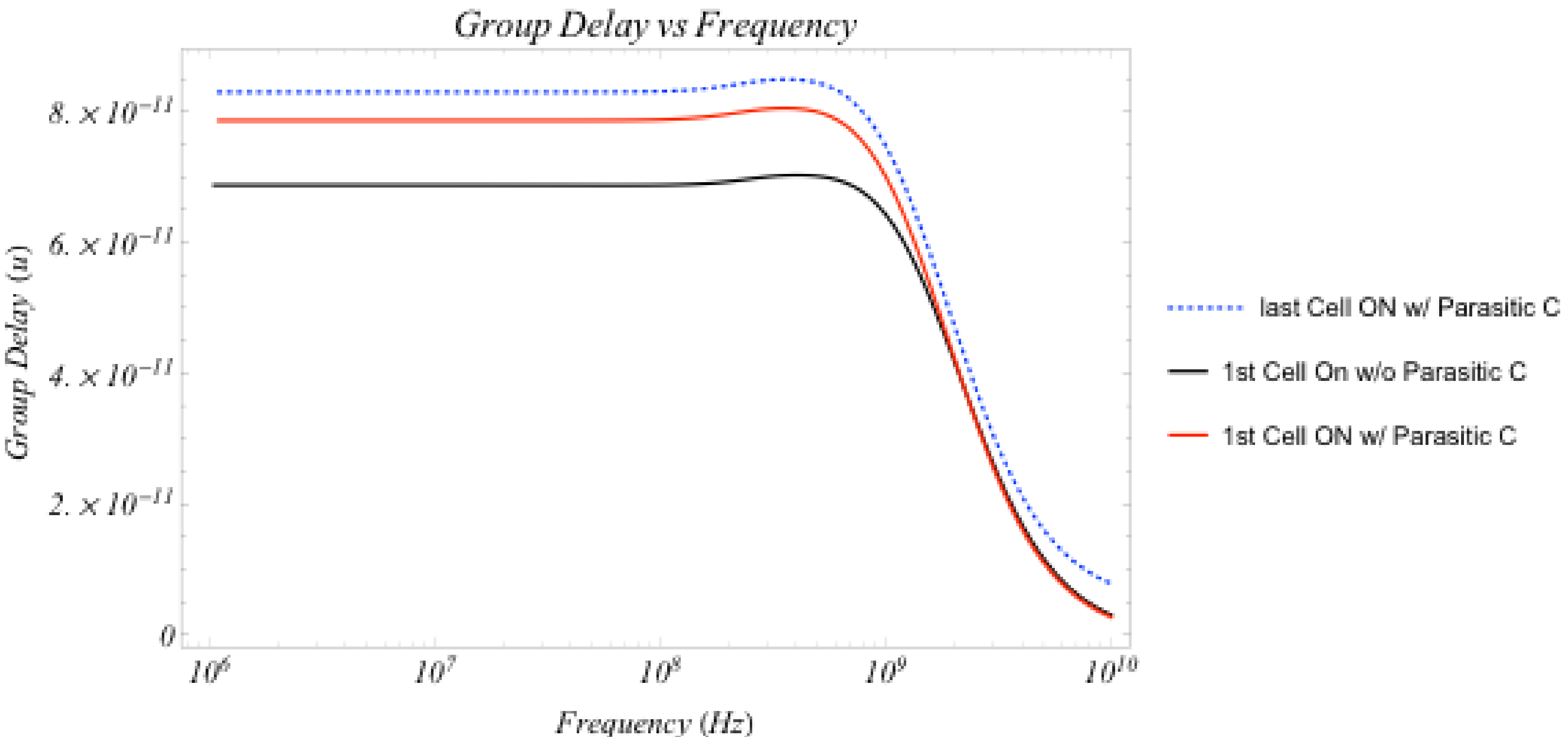
**Switch & Sampling Capacitor Equivalent Circuit**




- Check Csampling capacitance
- Identify Ron and Roff

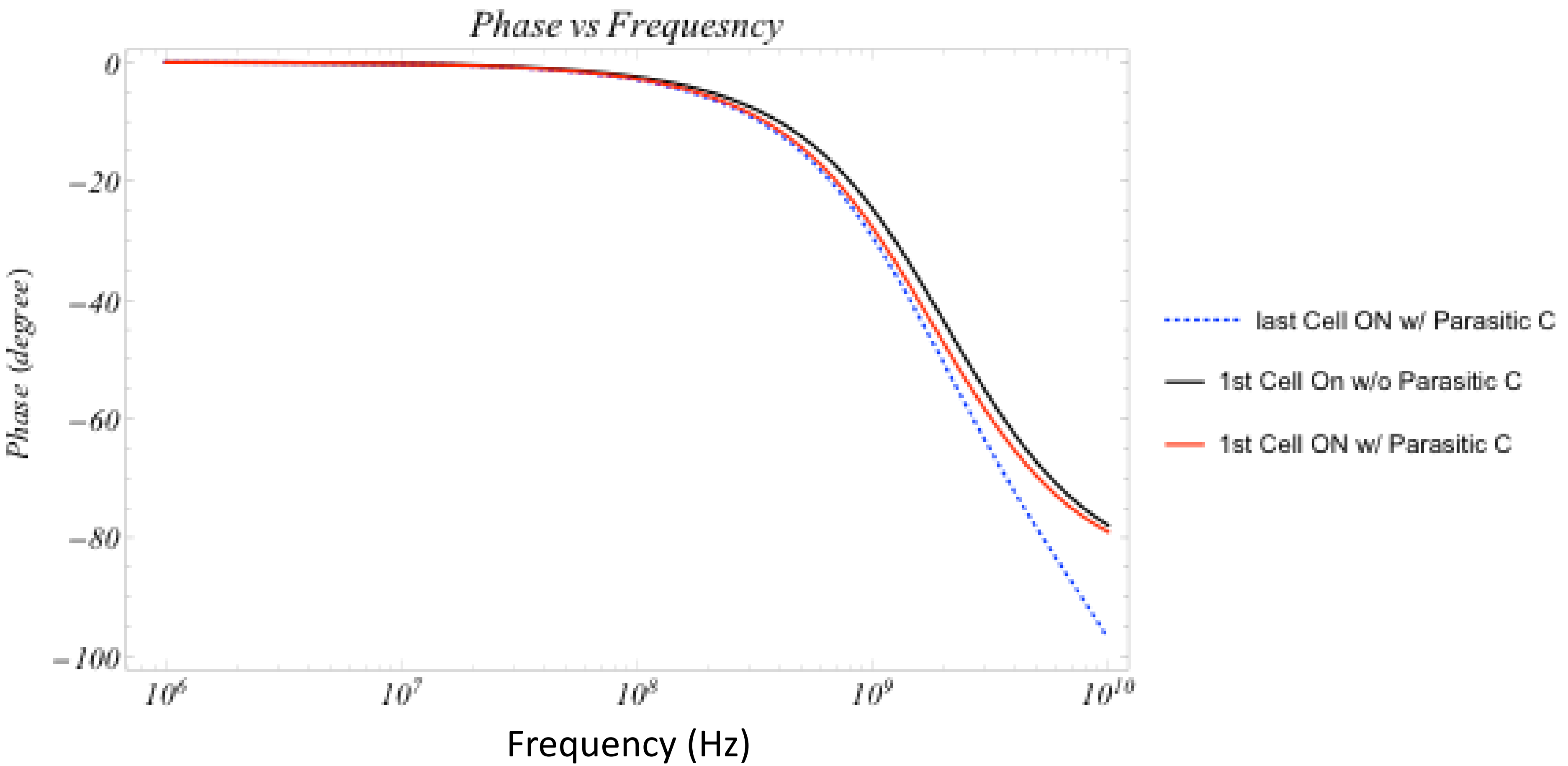
# Simulation Results: Group Delay

Group Delay does vary depending which switch is on by ~25ps which puts a constraint on sampling time window



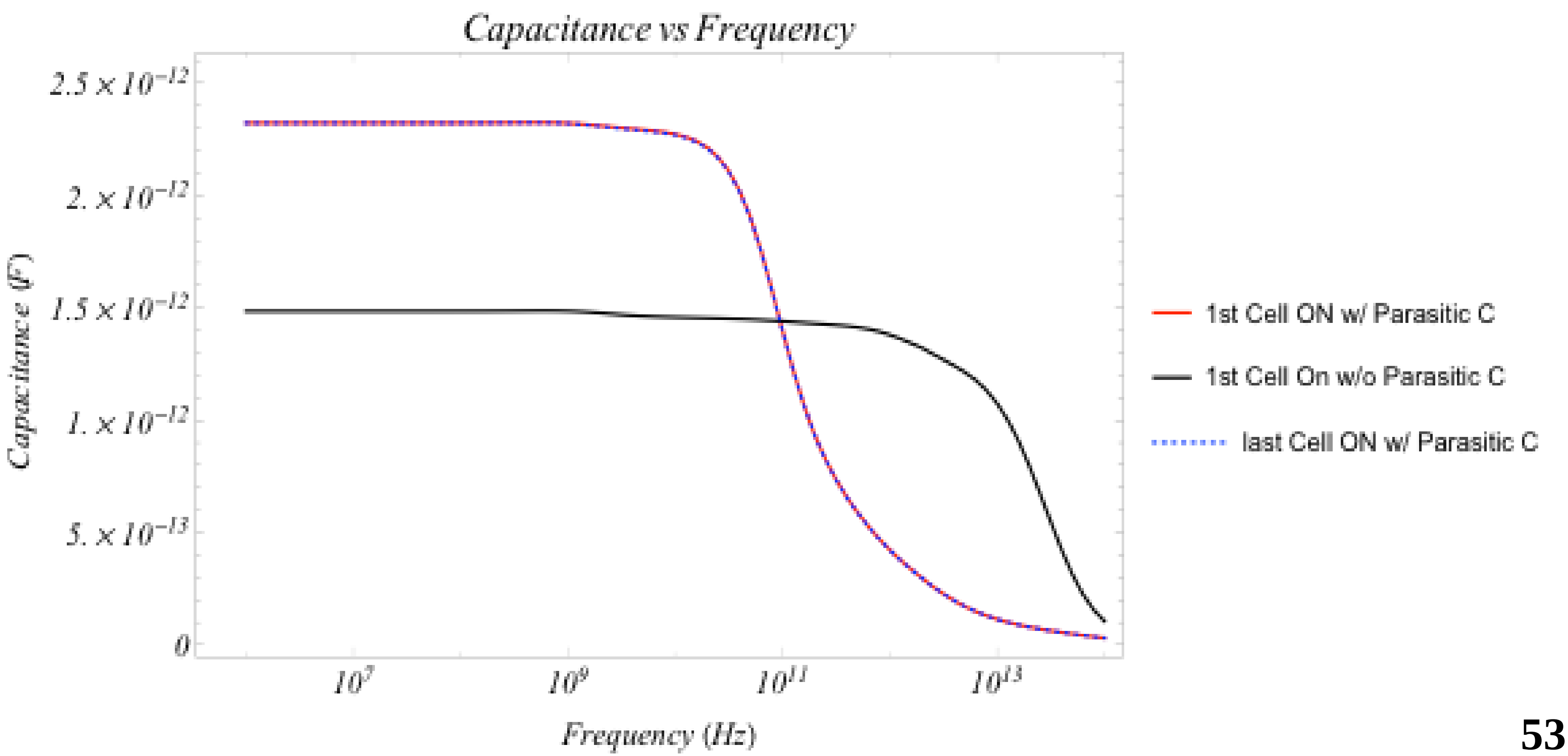
# Simulation Results: Phase

- At higher frequencies Phase vs freq behavior is also different and depends on which switch is on

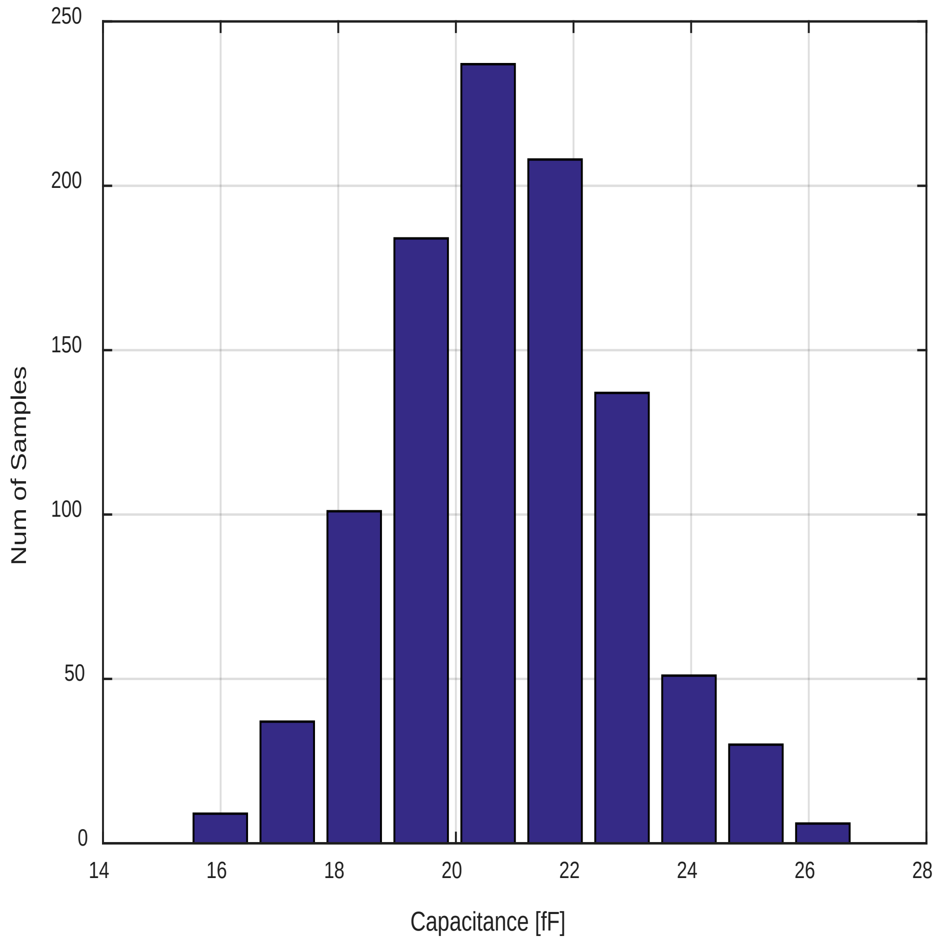


# Simulation Results: Capacitance

Capacitance is 2.2 pF and does not dependent on which switch is on



# Sampling Capacitor Spread



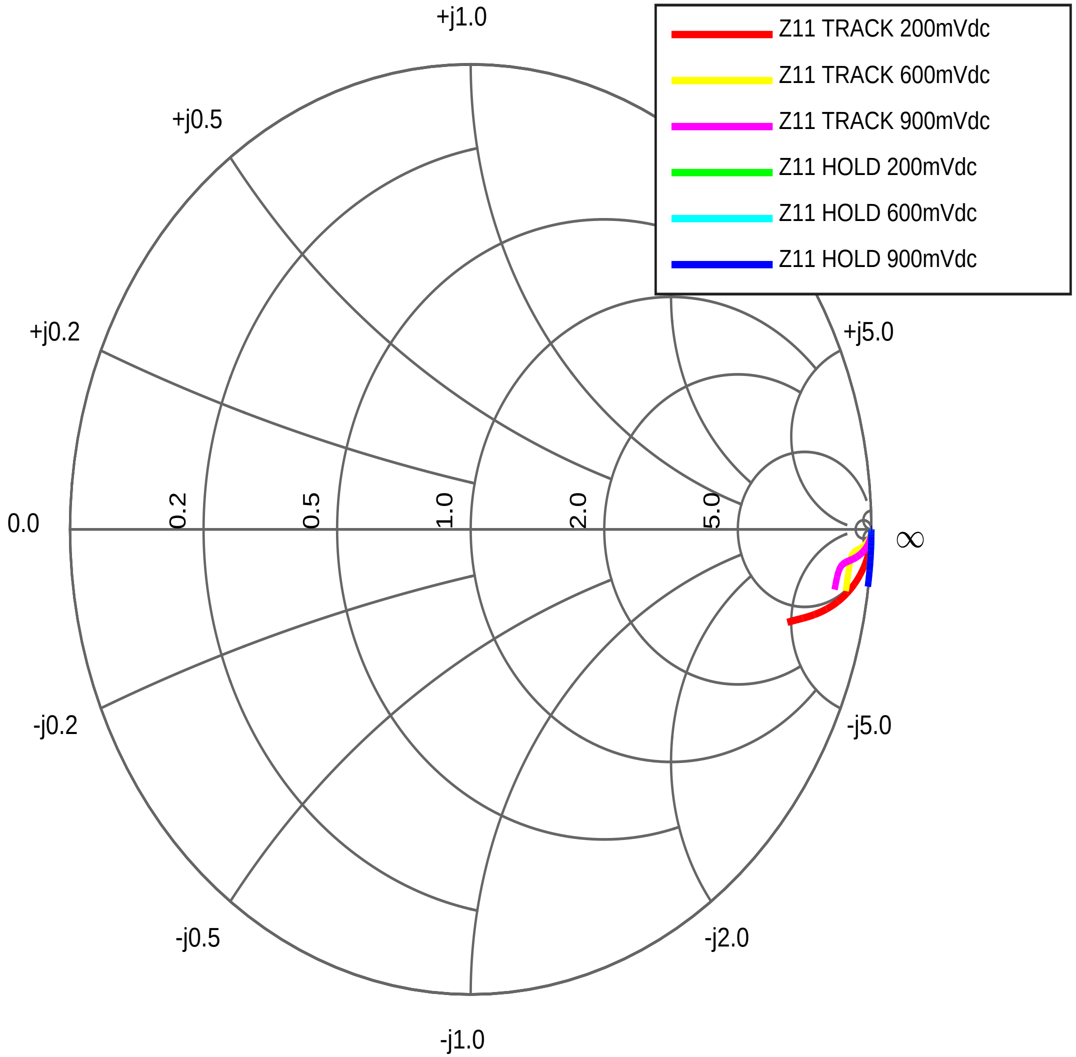

**Monte Carlo with process variation and mismatches shows a discrepancy between Csampling Schematic (13.5 fF) and Measured mean (20.27 fF).**

**The Spread is about 1.9fF which makes the Capacitor tolerance at about 9.3%**

| Num. of Samp. | MEAN | STD | MIN | MAX |
|---|---|---|---|---|
| 1000 | 20.27 fF | 1.89 fF | 14.86 fF | 26.24 fF |

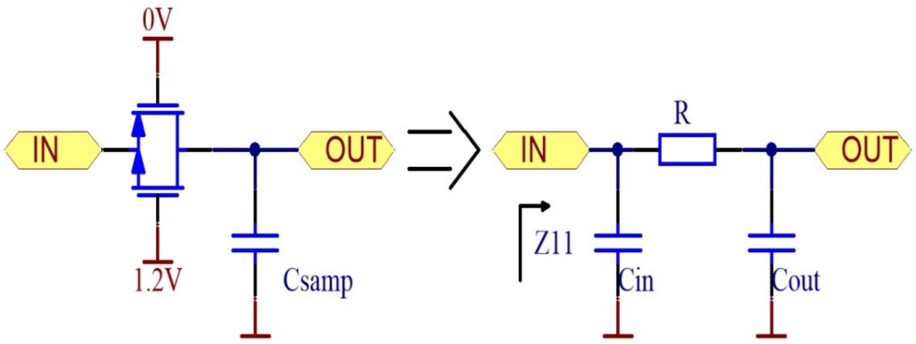
# Frequency Analysis

## Performance: S(Z)-parameter




**The input impedance is high and it is capacitive.**

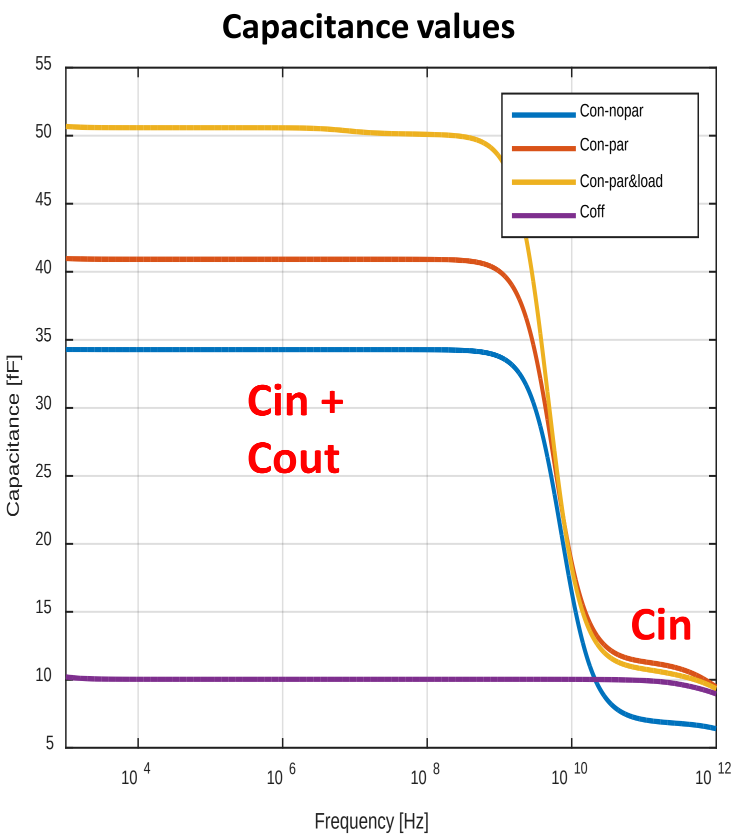
# Input coupling analysis




$$Z_{11} = \frac{1 + sC_{OUT}R}{s^2 C_{IN} C_{OUT} R + s(C_{IN} + C_{OUT})}$$

The transfer function parts:

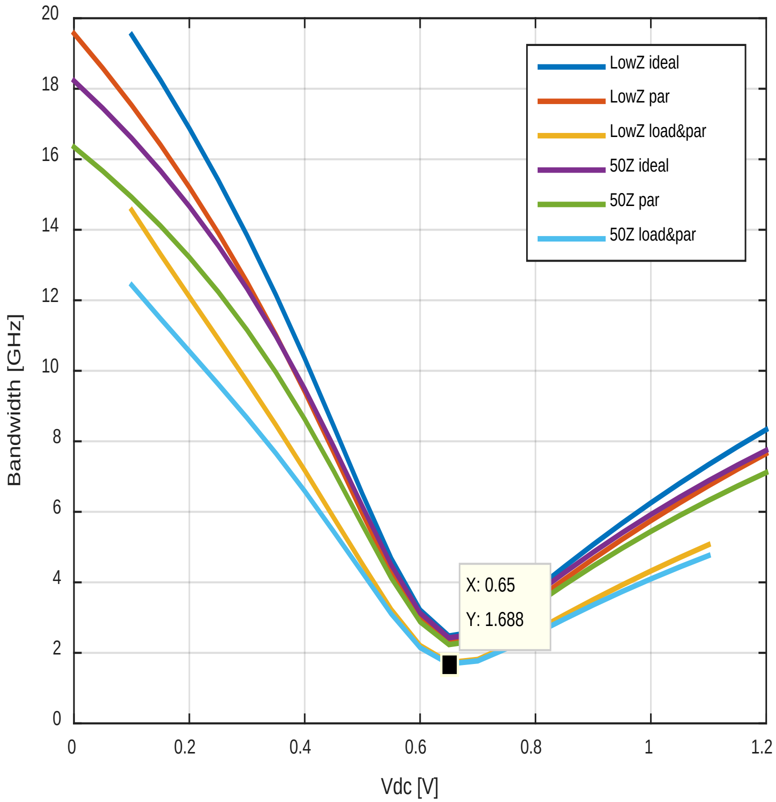
- input parasitic capacitance of the transistor plus capacitance of the transmission line section.
- Series resistance of the transistor channel (Rds)
- Output capacitance which is formed of the parasitic capacitance of the transistor, sampling capacitor and load capacitance



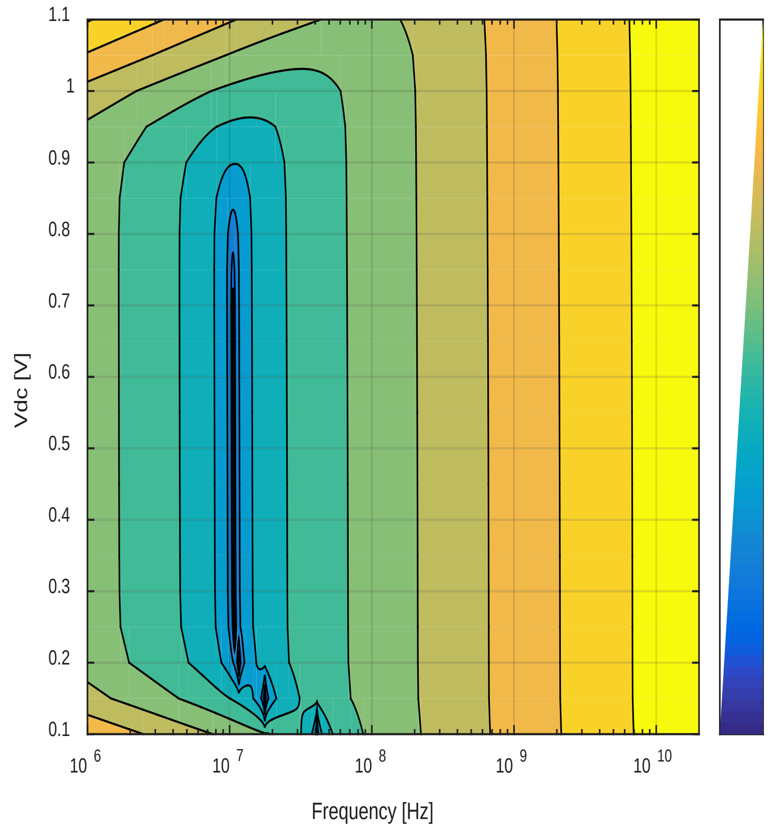

| Capacitance | Value [fF] |
|---|---|
| Cin_open | 8fF |
| Csw_out | 10fF |
| Csamp | 20.3fF |
| Cload | 13fF |

# Small signal frequency response

## Bandwidth




## Isolation

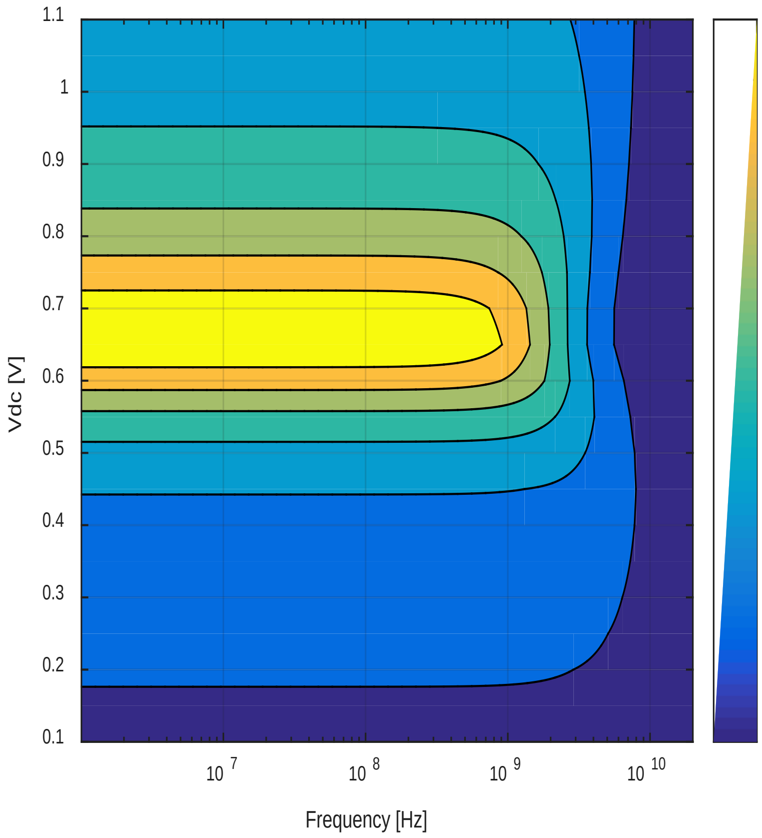



- **BWworst≈2.3GHz @665mVdc @LowZ drive**
- **BWworst≈1.7GHz @665mVdc @50Ω drive**

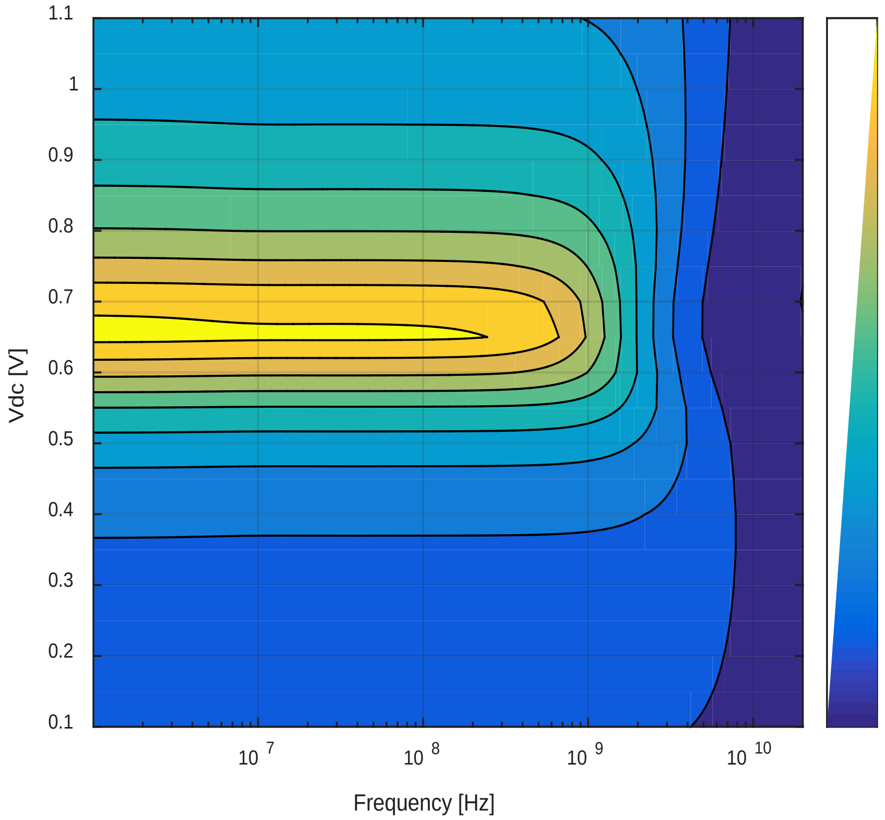
- **Isolation is over 60dB over all parameter space**

# Small signal phase analysis

**Group Delay without the load**

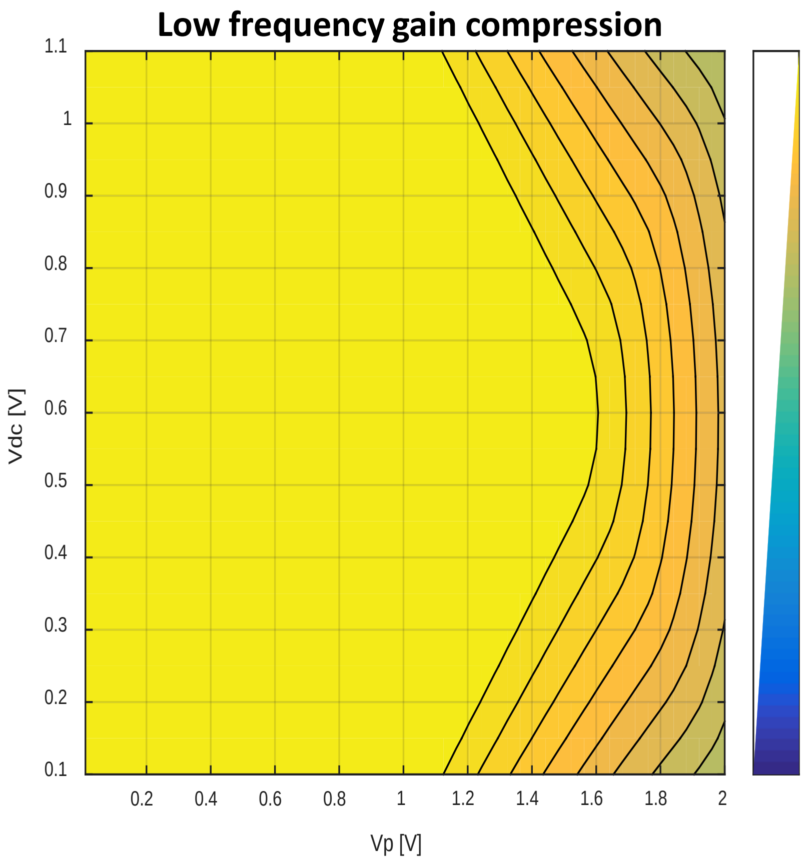


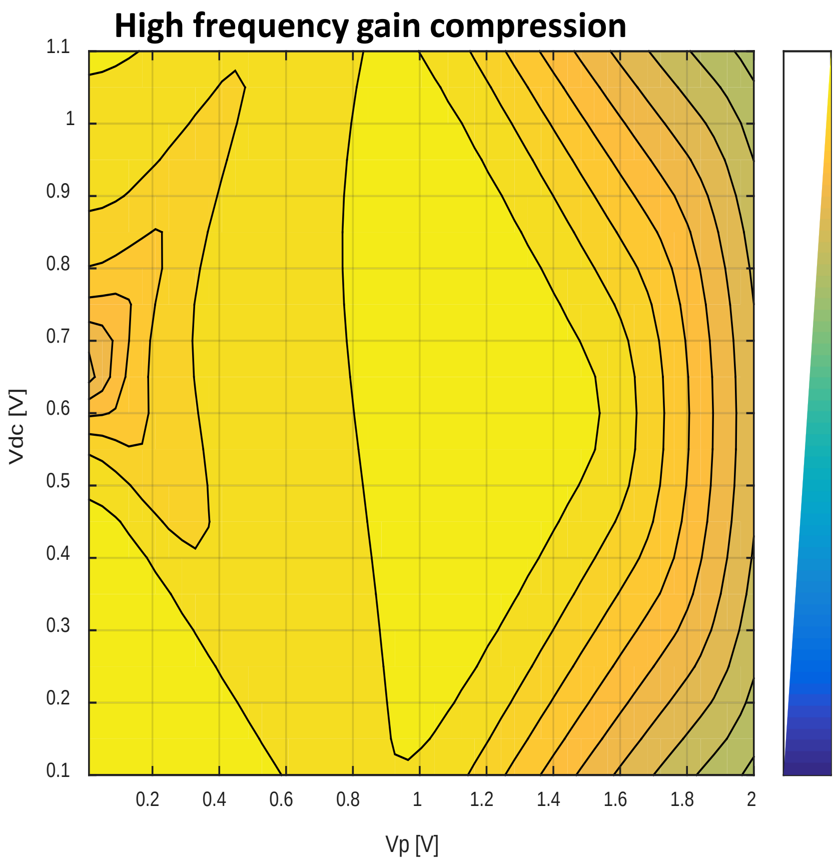

**Group Delay with the load**




**➔ Large group delay variation points to large distortion**

# Large signal response (I)



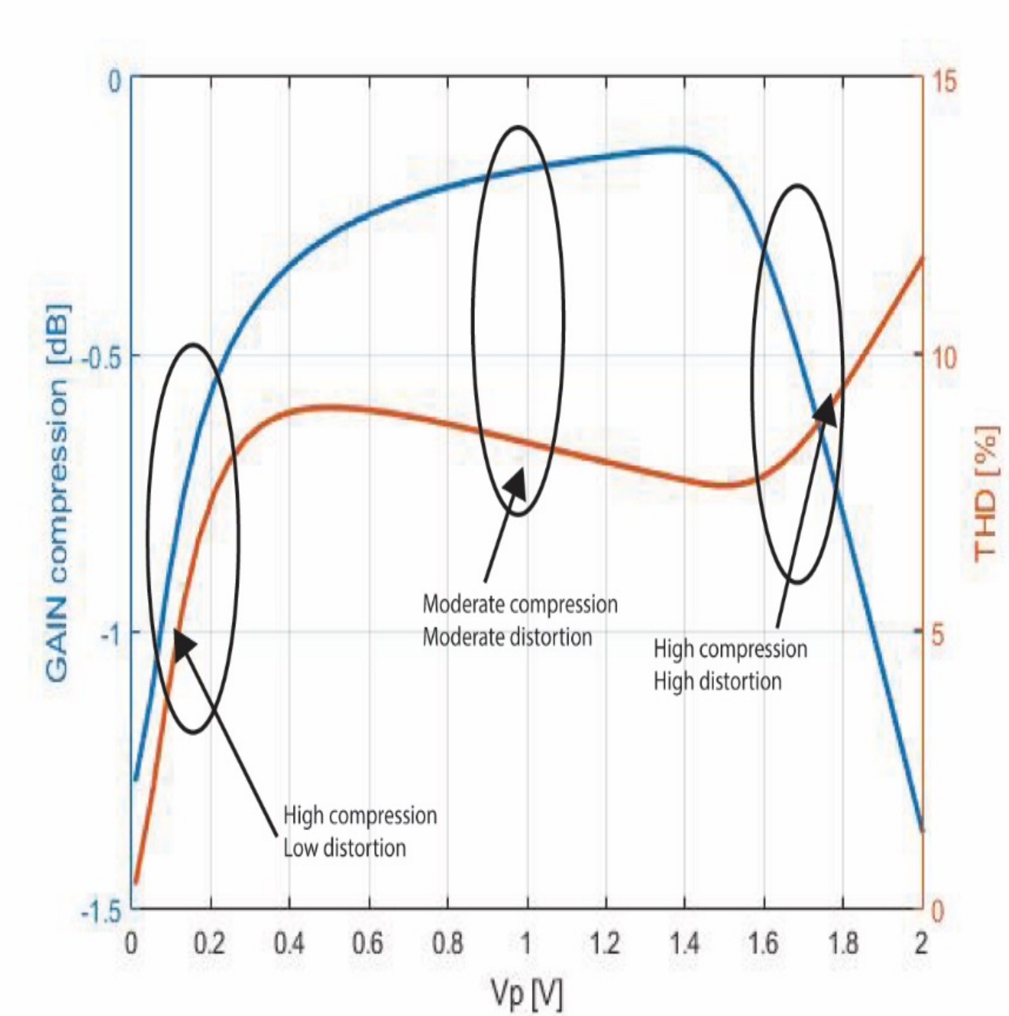




- **Full dynamic range at low frequency, compression appears when reaching the voltage threshold of the PN junctions at the drain/substrate barrier.**

- **Gain compression at lower and higher amplitudes**

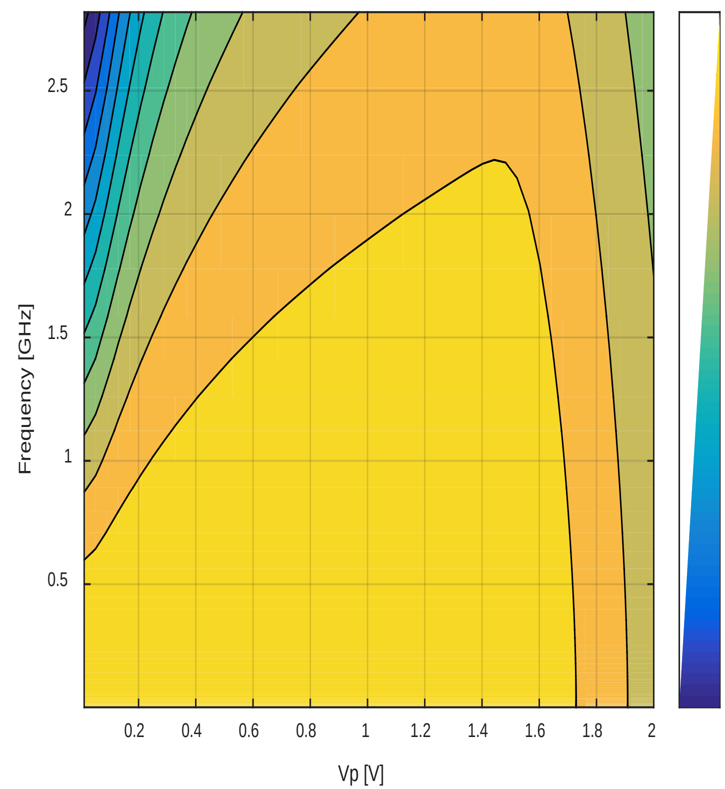
# Large signal analysis (II)

**High frequency gain compression & distortion**



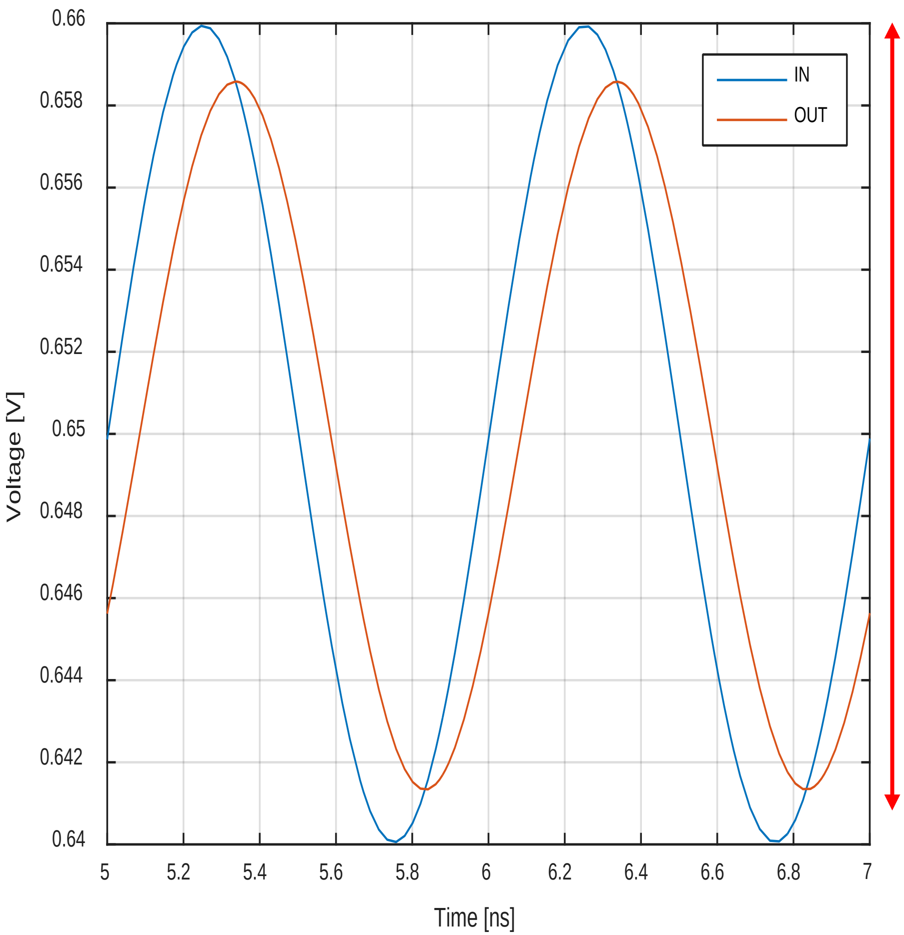

**Three region of operation:**

- **Low distortion & High compression**
- **Moderate distortion & Moderate compression**
- **High distortion & High compression**



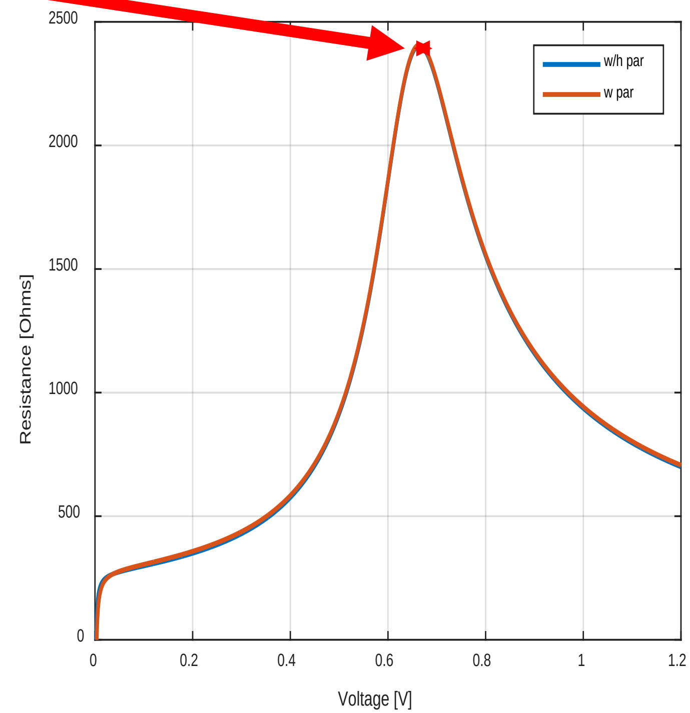
# Understanding signal response

**Low distortion & High compression**




- **Resistance of the channel does not vary much -> Low distortion**
- **At high resistance the bandwidth is limited -> lowering of the gain (compression)**

**TRACK state**

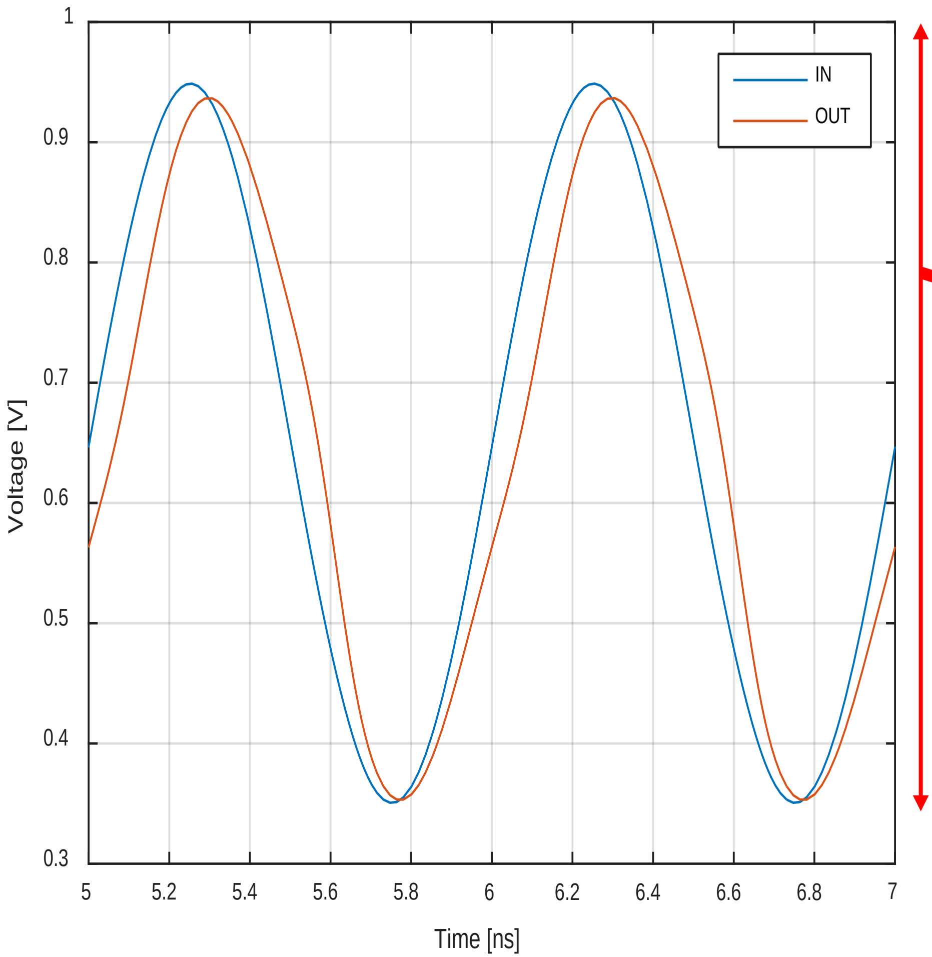


# Understanding signal response

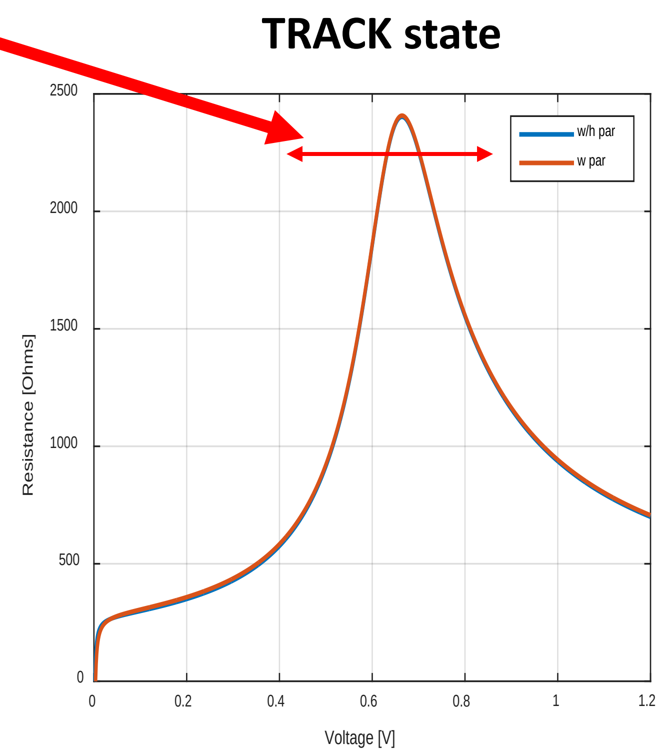
- **Resistance of the channel is varying**
  **-> The bandwidth at instantaneous values of the incident voltage waveform is different**

**-> In frequency domain this gives rise to higher harmonics, which interfere constructively hence increasing the overall signal amplitude but also increases distortion**

**Moderate distortion & Moderate compression**

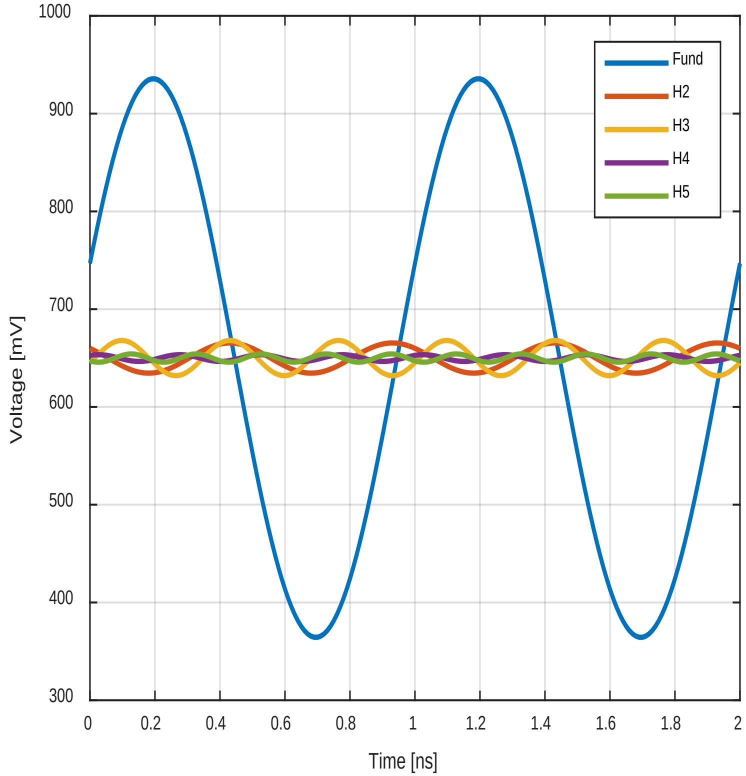



**TRACK state**

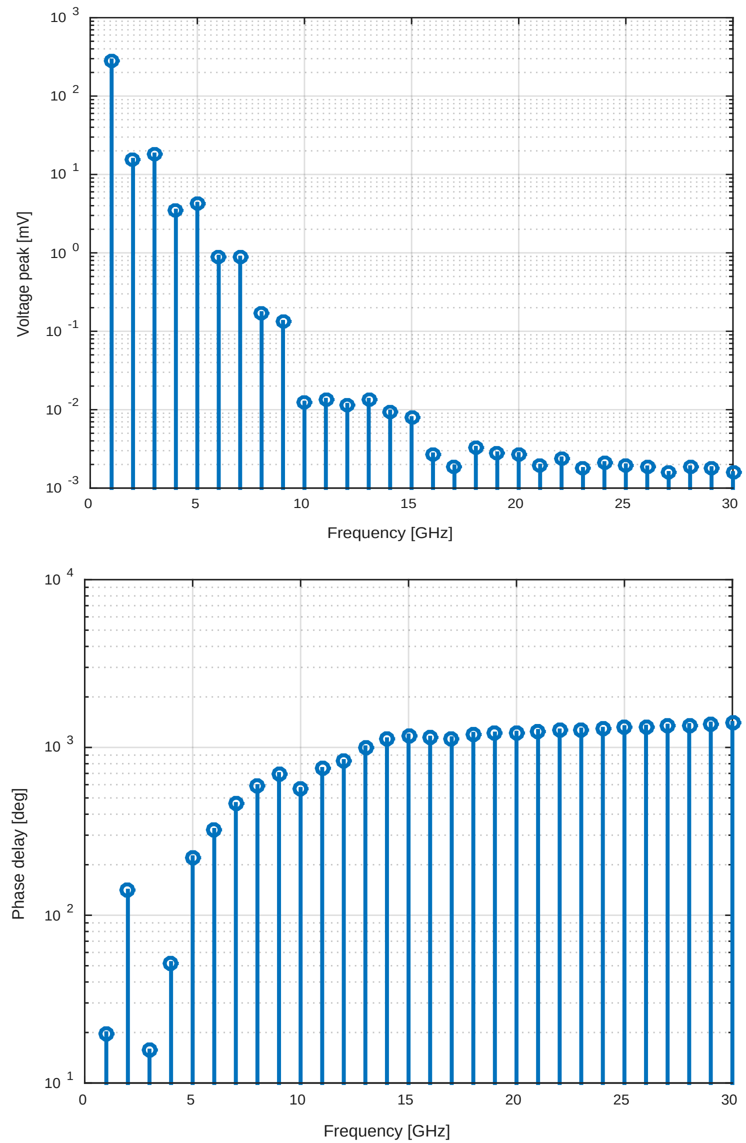


# Harmonic decomposition

## Time domain decomposition



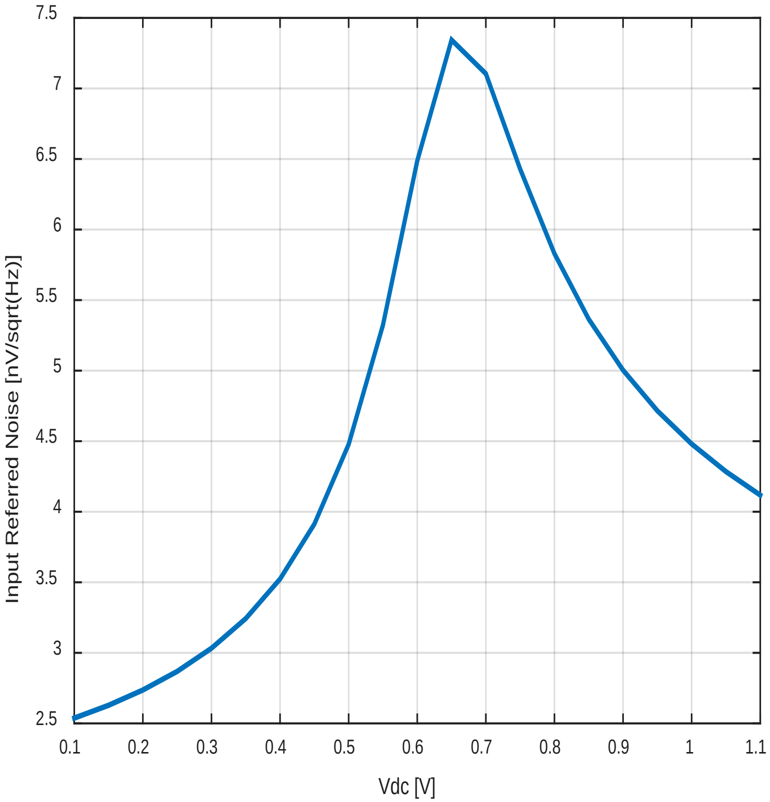

## Frequency domain decomposition



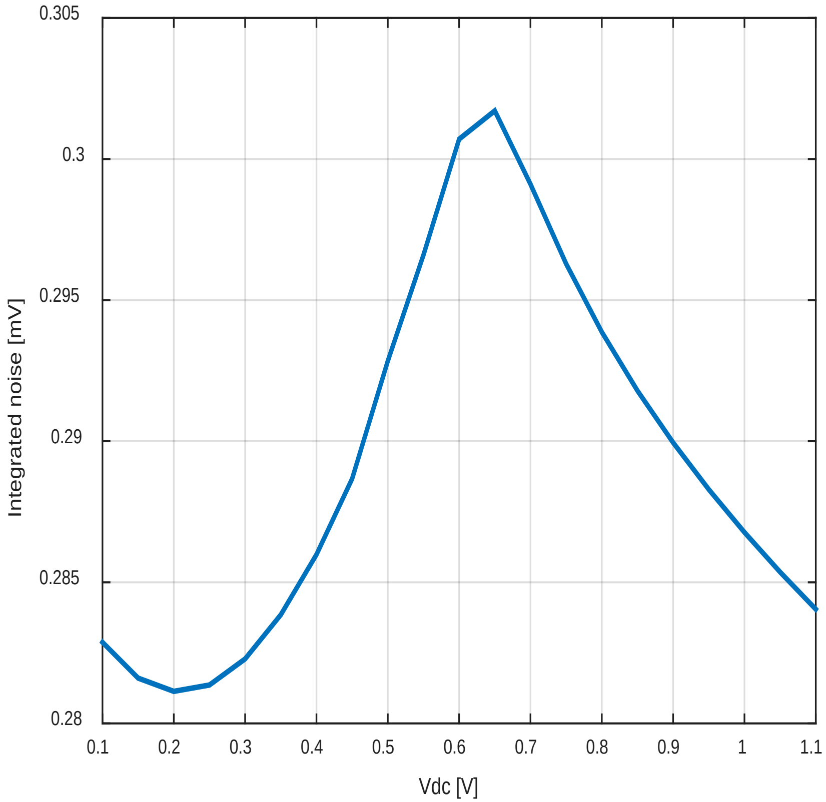

- **Constructive interference of odd harmonics and destructive interference of even harmonics at the peaks**
- **Constructive interference of second and third harmonics at zero crossing**

# Noise and Distortion

**Input referred noise**



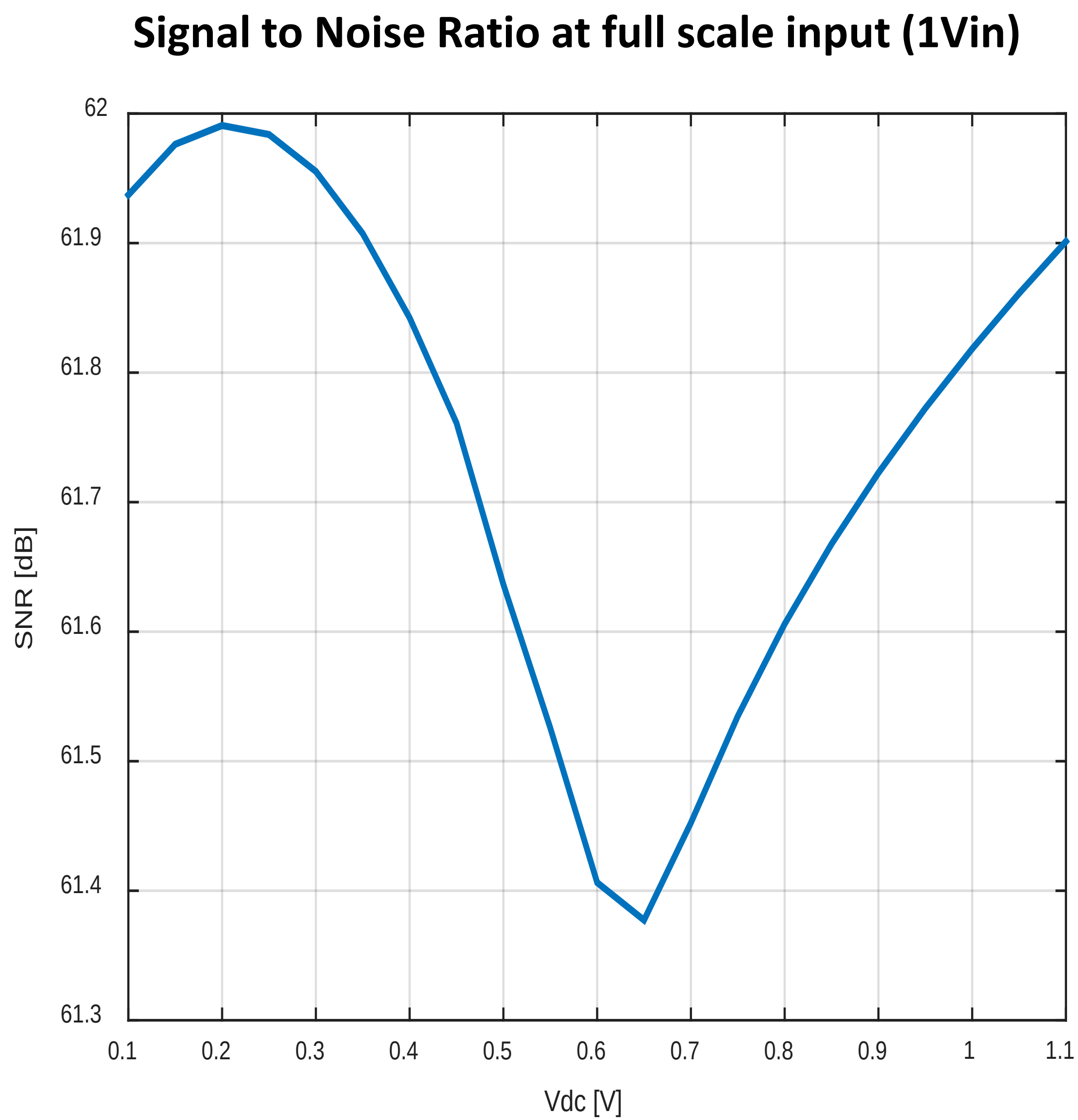

**Integrated referred noise**




- **Noise dominated by the ON resistance of the channel**

- **Total noise is around 0.29mV ± 0.01 mV**

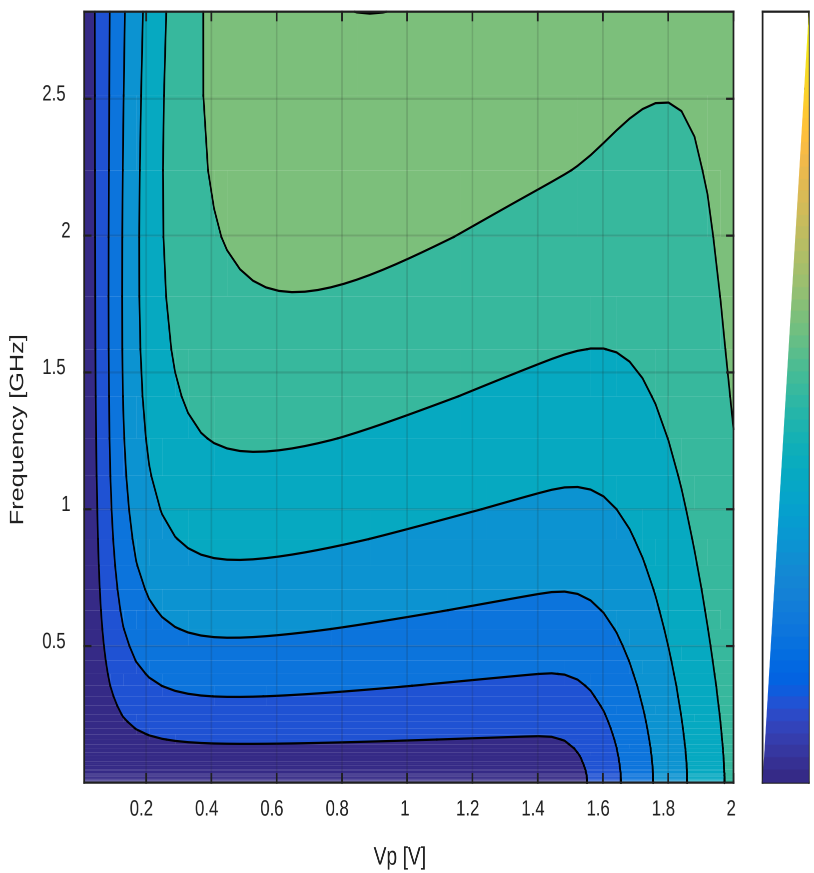
# Noise, distortion and dynamic range



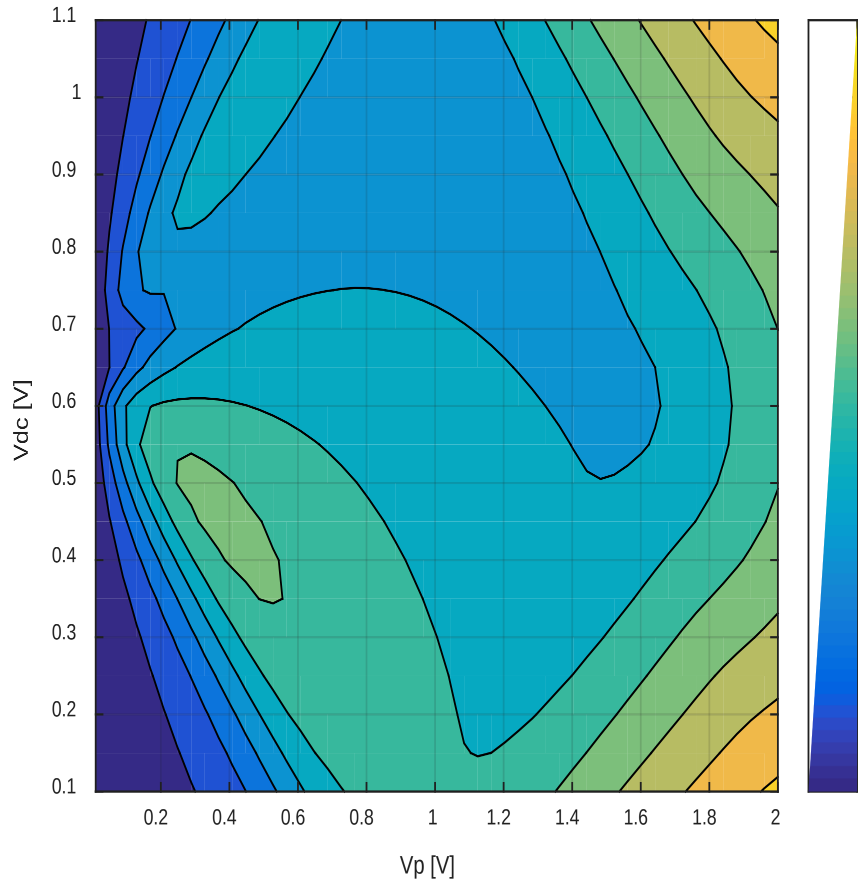

- **SNR is around 61.7dB ± 0.3 dB**

# Distortion analysis

## Distortion at fixed Vdc

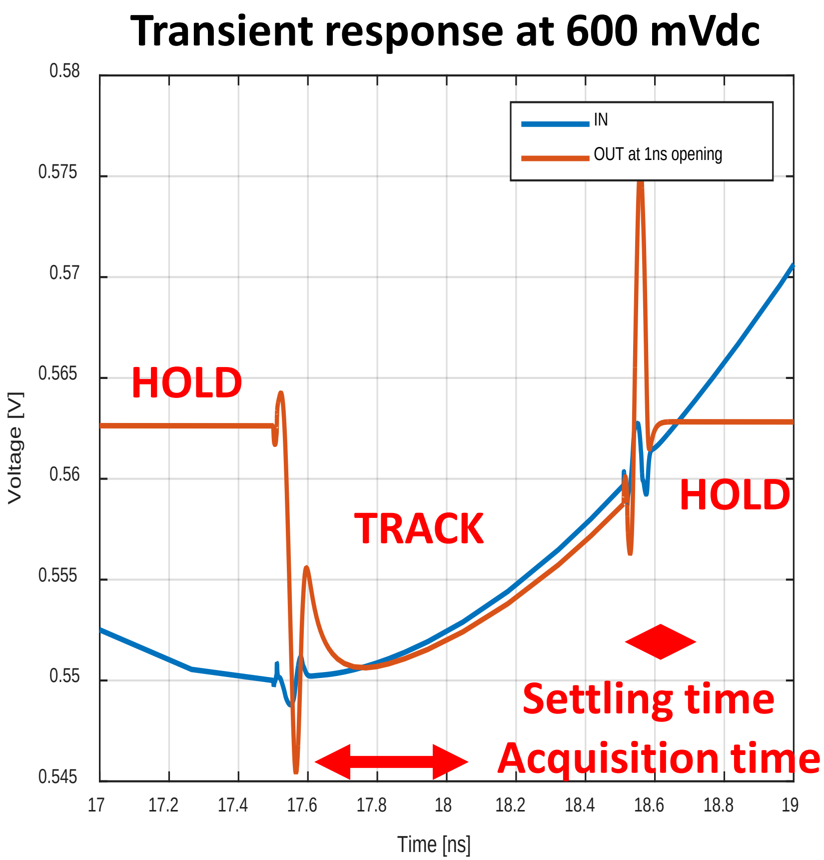


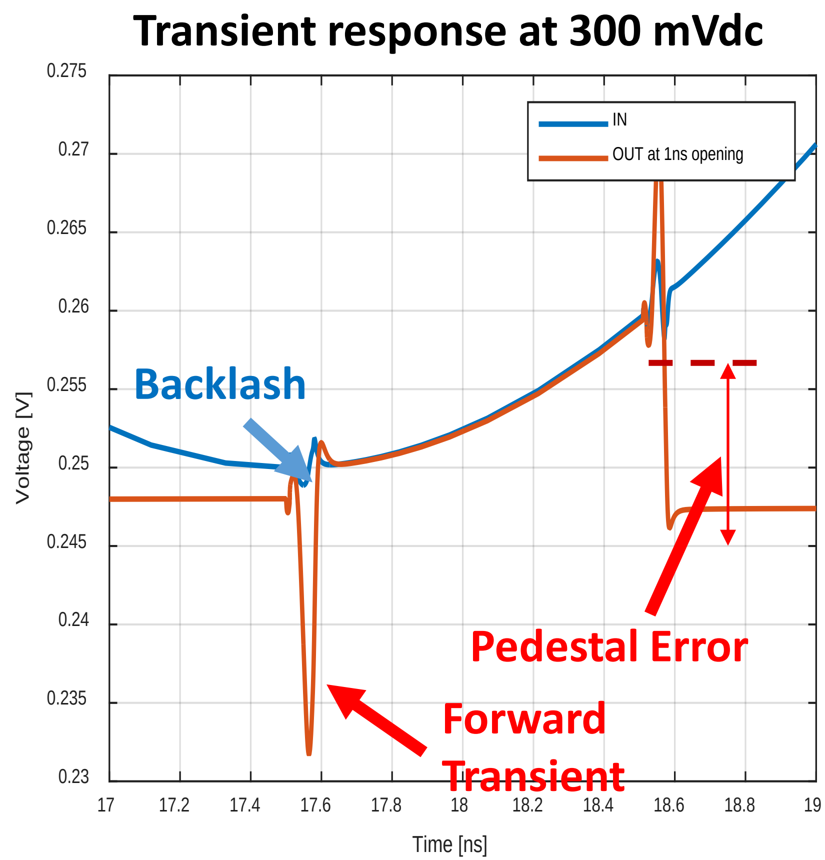

## Distortion at fixed Frequency




- **Most of the distortion comes from the Ron variation over the input voltage range**

# Transient Response




| Input Vdc voltage | Acquisition time | Settling time |
|---|---|---|
| 300mV | 0.14ns | 0.11ns |
| 600mV | 0.68ns | 0.11ns |
| 900mV | 0.52ns | 0.11ns |

- Worst case window time is 0.8ns or 1.25GHz -> due to low bandwidth
- Best case is 0.25ns or 4GHz

- 15% backlash at 30mV forward transient
- Pedestal error due to charge injection and transistor mismatch dominate

# Summary – Requirements comparison

| Parameter | Measured (worst case) | Requirement |
|---|---|---|
| Bandwidth | 1.7GHz @665Vdc @50Ω | 3GHz |
| SNR | 61.7 dB | 58dB |
| ENOB | 9.8 bits (small region) | 9.4 bits |

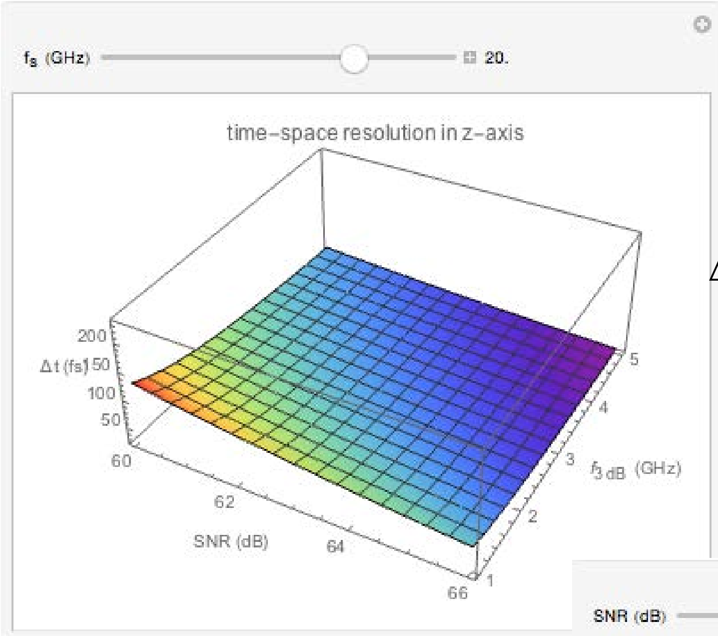
**Things to improve:**

- **Reduce Ron variance over the dynamic range to reduce distortion and increase the ENOB**
- **Timebase generator stability**
- **Bandwidth improvement:**
  - **Reduce Cin or reshape the channel to increase the bandwidth (first pole)**
  - **Reduce Ron overall value to increase the bandwidth (second pole)**
- **In summary:**
  - **Increase bandwidth**
  - **Need fast detector**
- **Use differential configuration to reduce pedestal error and increase noise coupling and crosstalk immunity**

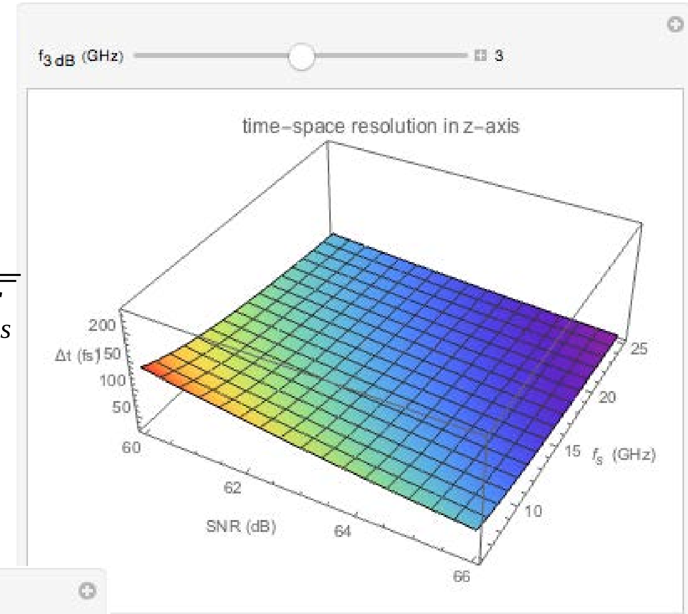
# Ongoing Plans

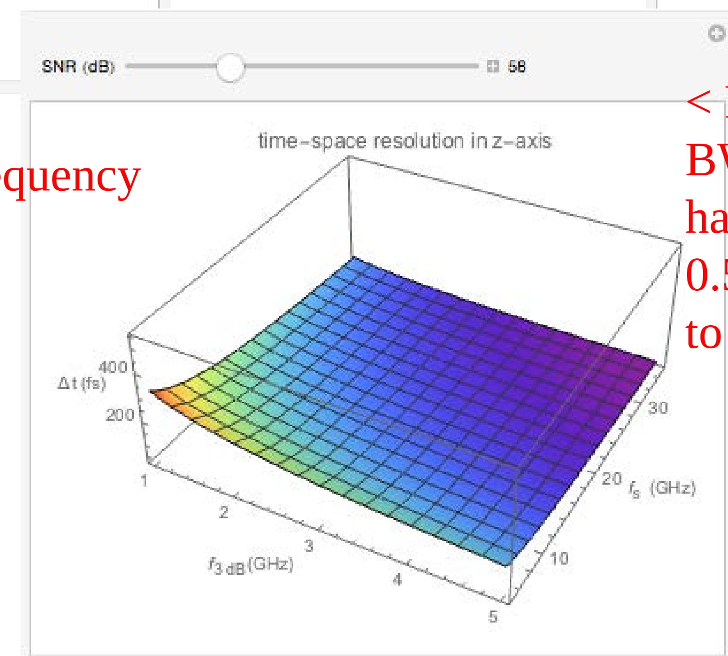
- "Pixel" vertex detector using precision timing?
- PSEC5 ASIC
  - 256 → 32k sample storage
  - Work to optimize bandwidth, ENOB
  - Persistence effects
- RFpix ASIC
  - Push limits of ABW, timing
  - Below 100-200fs, direct spatial measurement becomes interesting
  - Many practical issues, but none fundamental (CF 1ps)
- DRS5, SAMPIC ASICs
  - Will be interesting to see how well can perform

# Visualizing parameters for time resolution in z




$$\Delta t = \frac{\Delta U}{U}\frac{1}{\sqrt{0.34 * BW * f_s}}$$




^ Need to hold sampling frequency to least at 20 GHz to have timing resolution in 100fs range

< For the above sampling freq and BW integrated noise amplitude has to be in the range or less than 0.5mV to 0.6mV corresponding to SNR~58dB ($V_{pp}$=1volts)

SNR~58dB corresponds to 9.4 bits for 20μm resolution in rφ (Ideal ADC)

# Design Choices

- Input coupling
  - Differential versus single-ended input
  - Needed analog bandwidth
  - Gain needed?
- Sampling Options
  - On-chip PLL/DLL
  - External DLL
  - Analog transfer vs. interrogate in situ
- ADC and readout options
  - Sequential output select vs. random access
  - On-chip vs. off-chip ADC
  - Serial, parallel, massively parallel

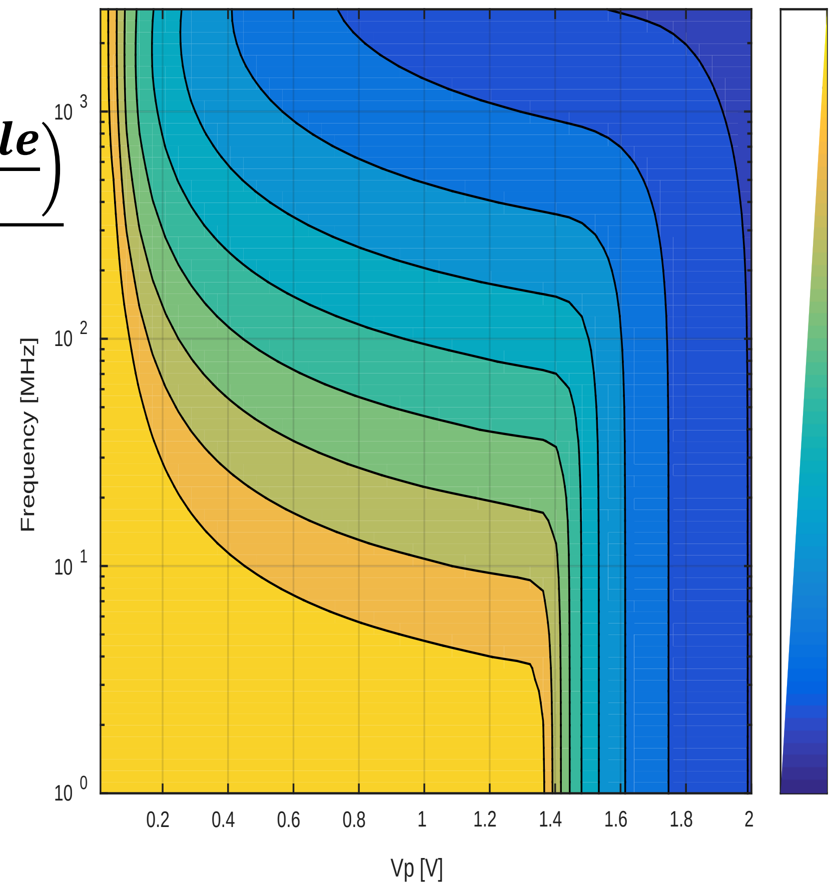
Many variants have been explored…

# SINAD & ENOB assessment

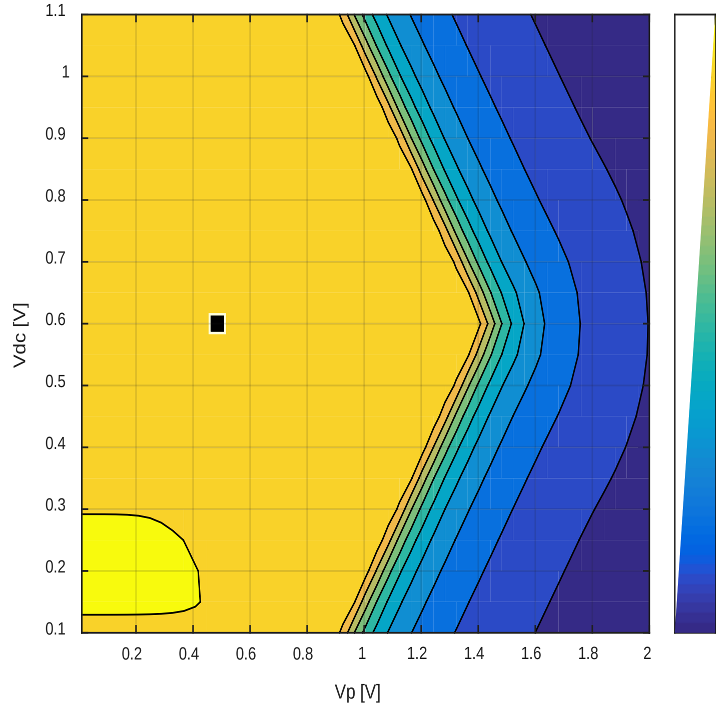
$$SINAD = -10\log_{10}\left[10^{-\frac{SNR}{10}} + 10^{-\frac{THD}{10}}\right]$$

$$ENOB = \frac{SINAD - 1.76 + 20\log_{10}\left(\frac{Fullscale}{Input}\right)}{6.02}$$

**ENOB versus frequency**



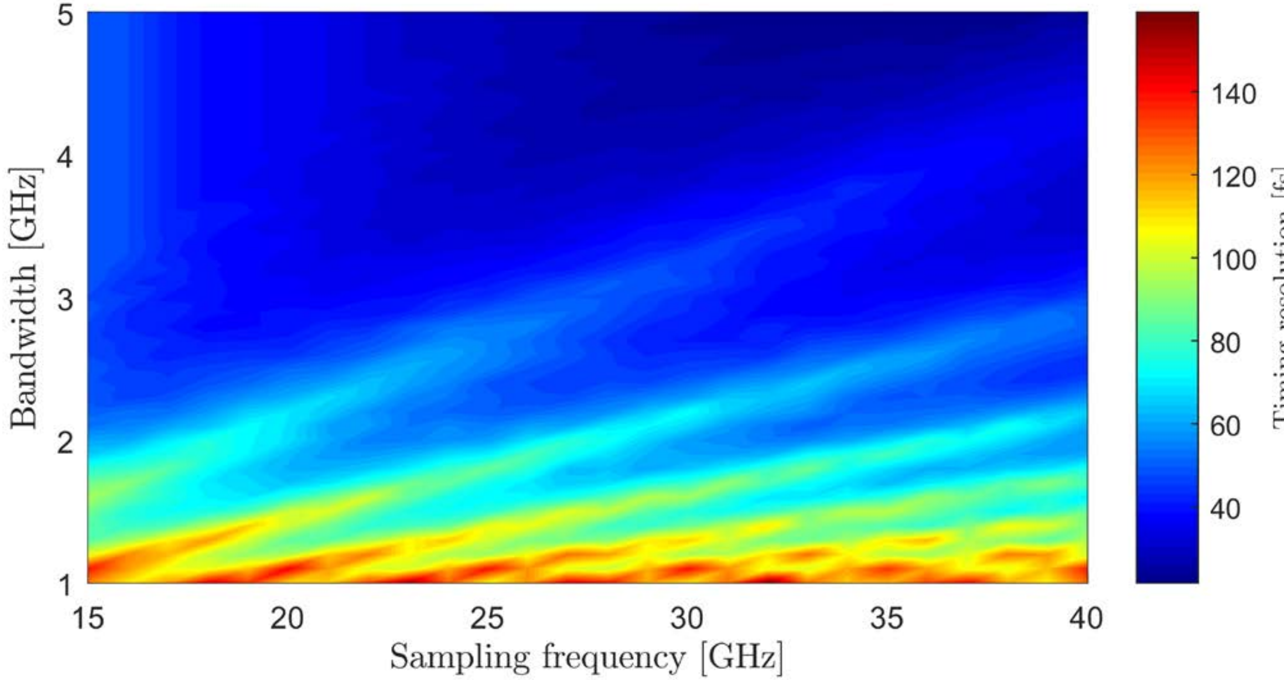

**ENOB at low frequency**




- **ENOB DOMINATED BY DISTORTION**

# Now pushing to the femtosecond regime

Pushing sampling speed and analog bandwidth




P. Orel, G. Varner and P. Niknejadi
NIM A**857 (2017) 31-41**.

And pushing the **space-time limit**
(new type of PID or DIRC devices?)

P. Orel and G. Varner

IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.