IP Sharing Experience - Columbia

- Three ASIC projects in past decade
  - 12-bit (11 ENOB), 40 MSPS quad ADC in 130 nm CMOS for ATLAS Phase-I upgrade ("NevisADC") - in production
  - Corresponding multiplexer-serializer chip, 16 ADC channels in (4 chips), 2 x 4.8 Gbps out ("LArTDS") - in production
  - 14-bit (11 ENOB), 40 MSPS octal ADC in 65 nm CMOS for ATLAS HL-LHC upgrade ("COLUTA ADC") in collaboration with UT Austin - first test chip
- In all cases, extensive benefit of IP sharing:
  - NevisADC: SLVS I/O drivers (CERN), PLL (modified from CERN/LHCb design), bandgap (NIKHEF), I2C slave verilog (CERN), ITAR "fuse"
  - LArTDS: GBTx serializer (CERN/U of Michigan), SLVS I/O drivers (CERN)
  - COLUTA ADC: bandgap and rad-hard I/O (Bologna)
- In a number of these, evolved the design for our application
  - Still a lot of effort saved

IP Sharing Moving Forward

- Plan to continue current mode of operation
  - Hope to benefit from a number of lpGBT building blocks (e.g. PLL)
- Would also be happy to share our work
  - Would be good to have easy way to share our modified versions of generic blocks
  - Also more advanced, e.g. NevisADC contains 8-bit SAR ADC block that could have been of use to others