Argonne NATIONAL LABORATORY

*HEPIC2017*

# ASIC Design & Development Activities at Argonne National Laboratory

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*SLAC*

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U.S. DEPARTMENT OF ENERGY

# About Argonne National Laboratory

- **Argonne is a Multi-Disciplinary Laboratory**
  - 14 Science Divisions
  - 22 Divisions/Sections/Facilities total
- **The HEP Division**
  - Medium-sized division at ANL - ~130 people
  - But arguably is the most aggressive in using leading-edge technologies, particularly high-level integration of FEE and detectors…

  ⇨ ***We have a need for ASICs in our research & collaborative work***
  ⇨ ***We have elected to not host an in-house ASIC design group***
  ⇨ ***Instead, we have formed a strategic partnership with FNAL…***
- **The Advanced Photon Source**
  - Has recently taken advantage of ANL/FNAL collaboration in ASIC design

**Fiscal Year 2016**
Budget: $770 million
Procurement: $300 million

**Workforce**
- 3,206 total employees (FTEs)
- 268 postdoctoral scholars
- 582 graduate and undergrad students
- 256 joint faculty
- 7,422 facility users
- 1,005 visiting scientists

**Research**
- 14 research divisions
- 5 national scientific user facilities
- Many centers, joint institutes, program offices
- Hundreds of research partners

**USER FACILITIES**
- Advanced Photon Source
- Argonne Leadership Computing Facility
- Argonne Tandem Linear Accelerator System
- Center for Nanoscale Materials
- Transportation Research and Analysis Computing Center

# A Few Examples of ASIC Development Work…

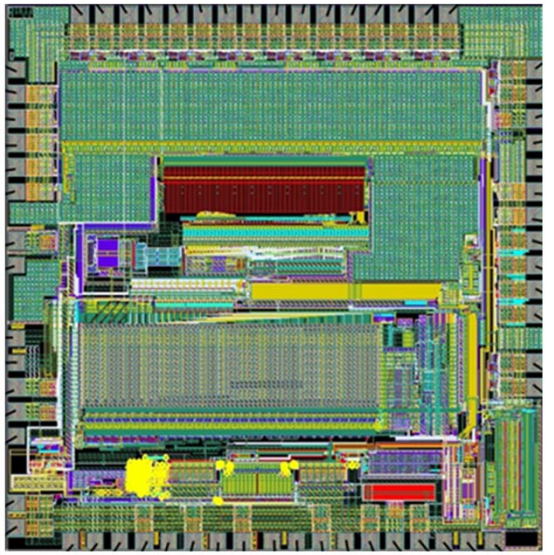
# QIE readout for the ATLAS Tile Calorimeter at the LHC

- **Current Electronics for ATLAS TileCal**
  - Uses pulse-shaping
  - Uses Hi Gain / Lo Gain 10-bit digitization
  - Triggered readout

- **For Phase 2 Upgrade**
  - New electronics required
    - End of life of current electronics
    - Need higher radiation tolerance
    - DAQ system architecture changes (no HDW trigger)
  - 3 FE options considered

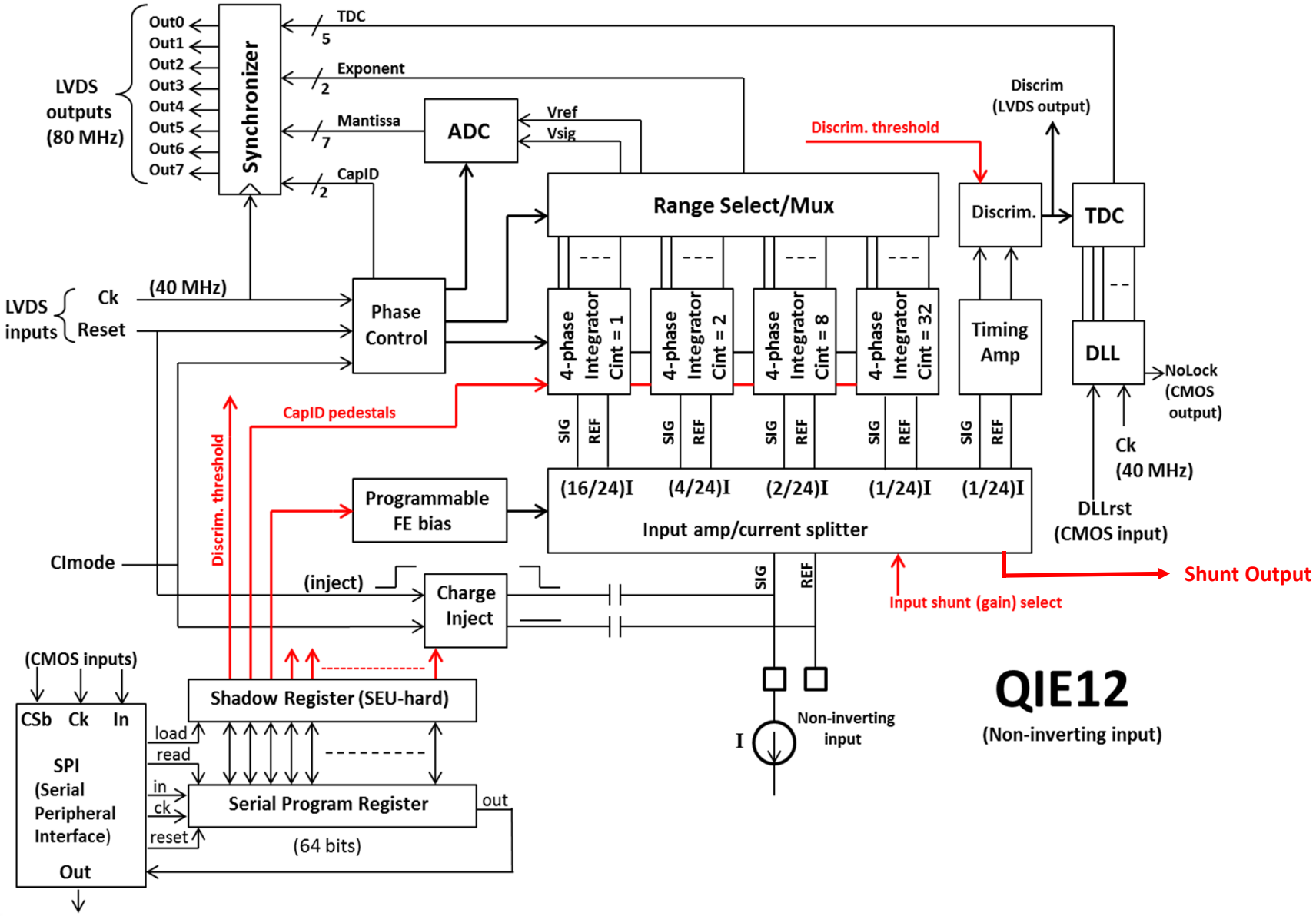
    ⇨ ***QIE proposed by ANL → QIE12***
    - "Enhanced" version of CMS QIE (QIE8/QIE10/QIE11)
    - 1.55 fC least count sensitivity
    - 17 bits of dynamic range
    - 1 nS TDC in each crossing
    - Current integrator (uses programmable shunt from the QIE)

  ⇨ ***Proposed work complementary with FNAL work on CMS***



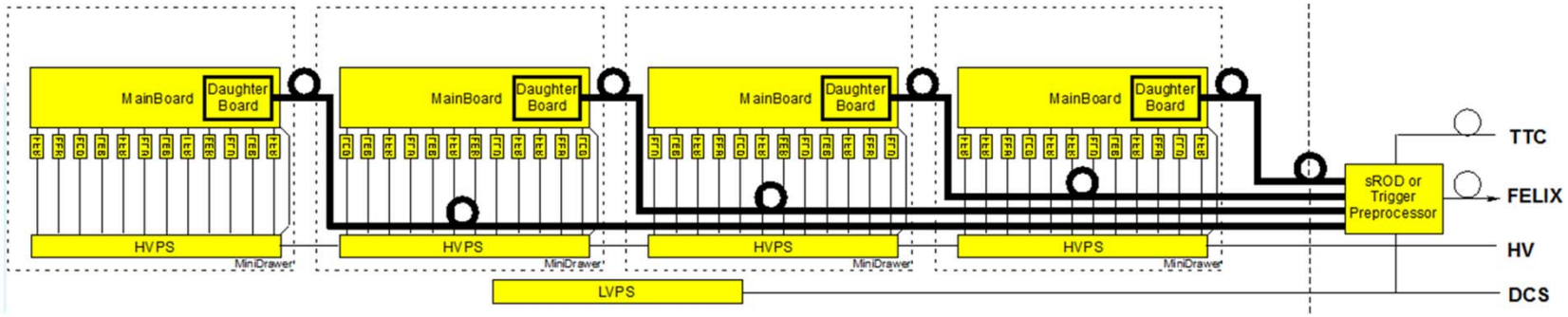
QIE12 Screen Shot from Tom Zimmerman

# Block Diagram of the QIE12 ASIC

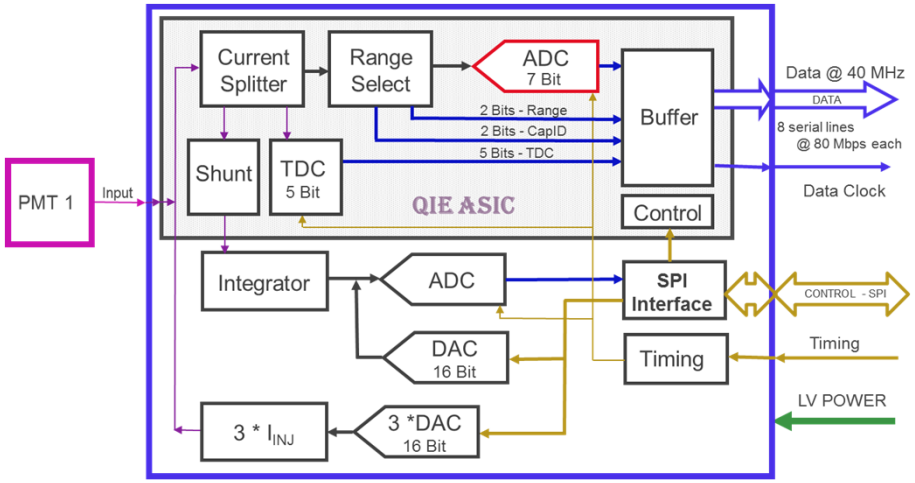


# QIE Readout for the ATLAS Tile Calorimeter at the LHC

- **Block diagram of readout system**



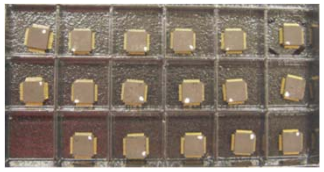

- **Block diagram of front-end board**



# Design Process of the QIE Front End

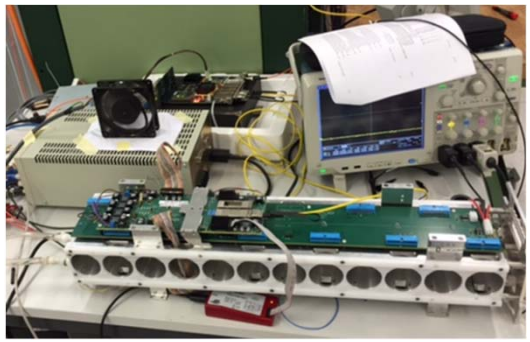
- **QIE12 Specifications:**
  - Begun ~2012 with specification for QIE10, Collaboration between ANL & FNAL
  - QIE12 realized ~2013-2014 by Tom Zimmerman, 2 versions
- **Bench Tests at ANL (2 versions, ~2013-2015)**
  - Characterize performance; Feedback on improvements
- **FE Design at ANL (~2014-2016, 2 versions)**
  - Design FE & readout system based upon QIE & DAQ interfaces
- **Prototype Design & Construction (~2015)**
  - Build 1 board → 12 boards for "Mini Drawer"
- **Small System Construction (~2016)**
  - Procured ~60 chips
  - Built 2 Mini Drawers, 24 channels
- **Test Beam Operation & Data (~2016)**
  - Successfully operated system in 2016 CERN test beam
  - Built 2 Mini Drawers, 24 channels

Chips

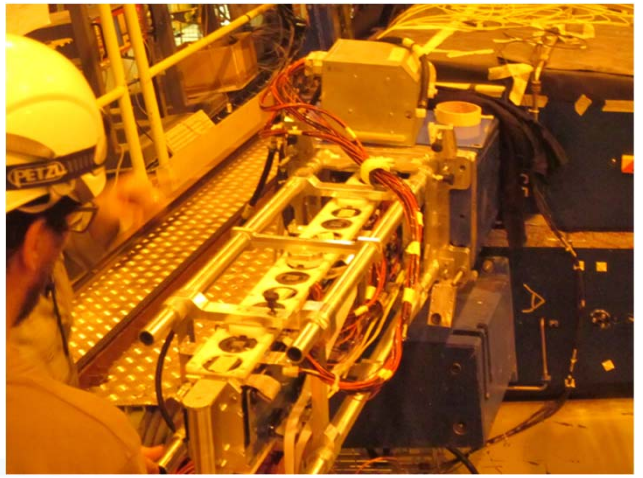


FE Boards


FEE on Mini Drawer



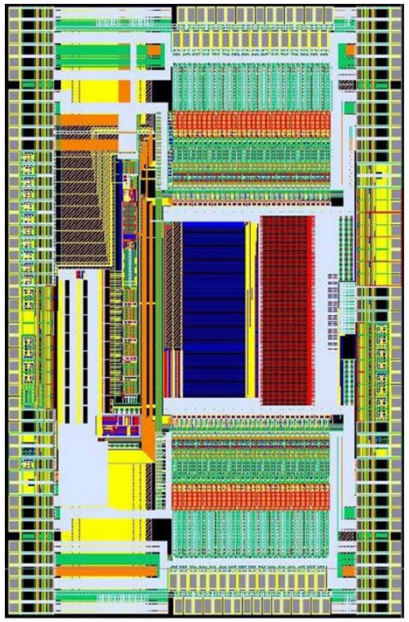
Full Mini Drawer



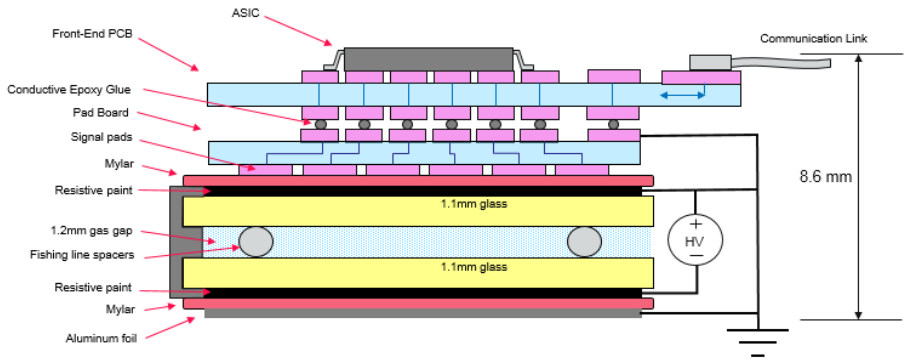
⇨ ***Nice Progression from Conception to Data***
⇨ ***Excellent Collaboration between ANL/FNAL***
⇨ ***Highly successful, but ANL has left TileCal…***

# DCAL Readout for the Tile Calorimeter at the ILC (CALICE)

- **Detector R&D Project using Particle Flow Algorithms**
  - Resistive Plate Chambers, 1 cm2 pads
  - Highly-integrated readout → DCAL ASIC
- **ASIC Requirements**
  - Capability for Self & ExternalTriggering
  - 20-stage pipeline ⍰ 2 mSec latency @ 100 nSec
  - Capability of FE to source prompt Trigger Bit
  - Capability to store up to 7 triggers in ASIC output buffer (FIFO)
  - Design for 100 Hz (Ext. Trig) nominal rate
  - Deadtimeless Readout
  - Zero-suppression implemented in front-end
  - On-board charge injection with programmable DAC
  - Design for 10% occupancy
  - Concatenate data in front-ends
  - Use serial communication protocols
  - Slow controls separate from data output stream
  - Compatibility with CALICE DAQ



DCAL3 Layout




⇨ ***Developed DCAL Chip with FNAL (Funded through ANL)***

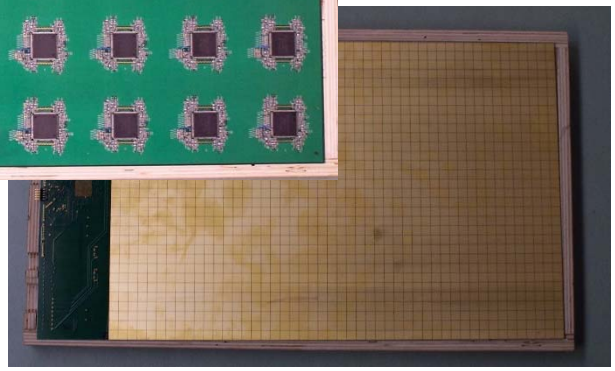
# Design Process of the DCAL System

- **DCAL Chip Development:**
  - Begun ~2004 with specification for DCAL chip Collaboration between ANL & FNAL
  - DCAL1 realized ~2006 by Jim Hoff
  - DCAL2 realized ~2007
  - DCAL3 realized ~2008
  - Production ~2009 → 10,000 chips
- **Bench Tests at ANL (3 versions, ~2006-2008)**
  - Characterize performance; Feedback on improvements
- **FE Design at ANL (~2008-2009, 2 versions)**
  - Design FE & readout system based upon DAQ interfaces
- **Prototype Design & Construction (~2010)**
  - Build 1 board → 6 boards for "Plane"
- **"Small" System Construction (~2010)**
  - Procured 11 wafers, ~10,300 chips
  - Built 240 boards, 40 planes, 400,000 channels!
- **Test Beam Operation & Data (~2011-2012)**
  - Successfully operated system in FNAL & CERN test beams

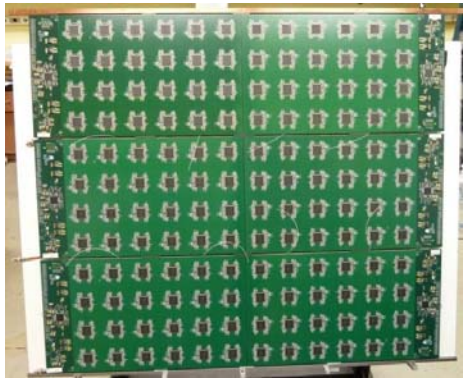
⇨ ***Nice Progression from Conception to Data***
⇨ ***Excellent Collaboration between ANL/FNAL***
⇨ ***Highly successful, viable technolgy for the ILC…***

**Chips**

**FE Boards**

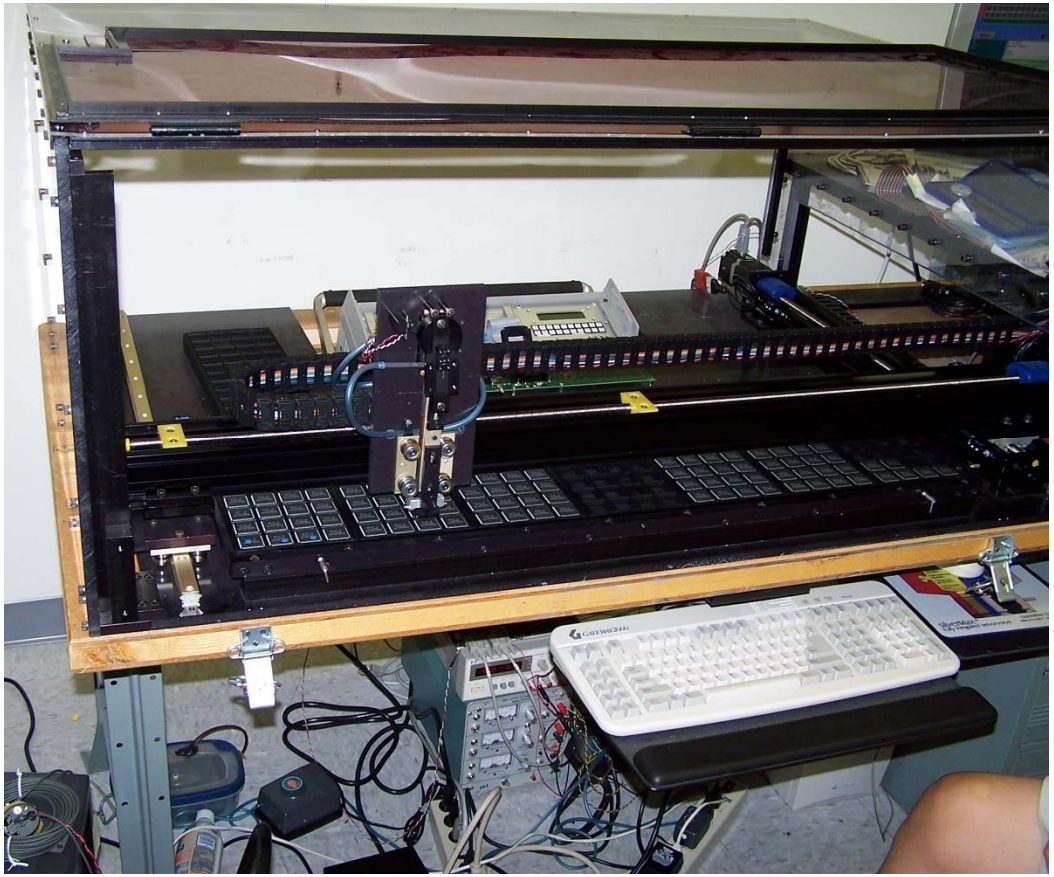


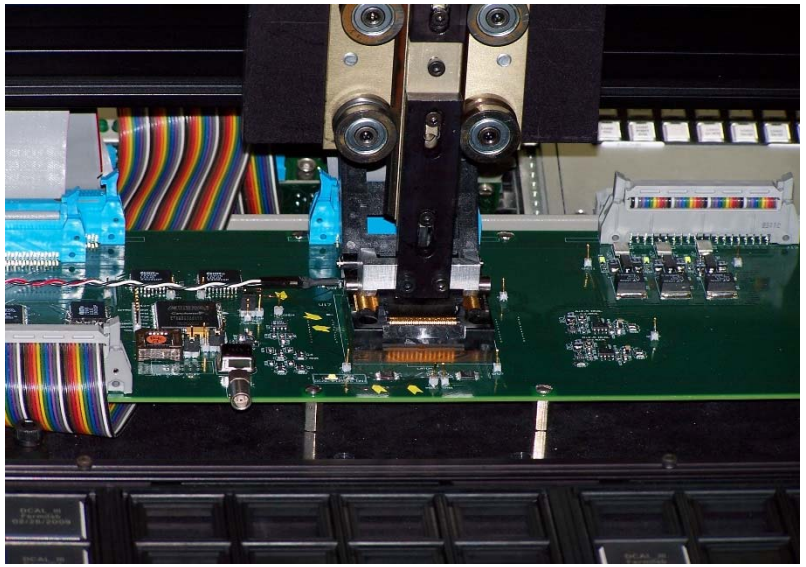
**Plane**



**Full Prototype Detector**

# DCAL Chip Testing at Fermilab



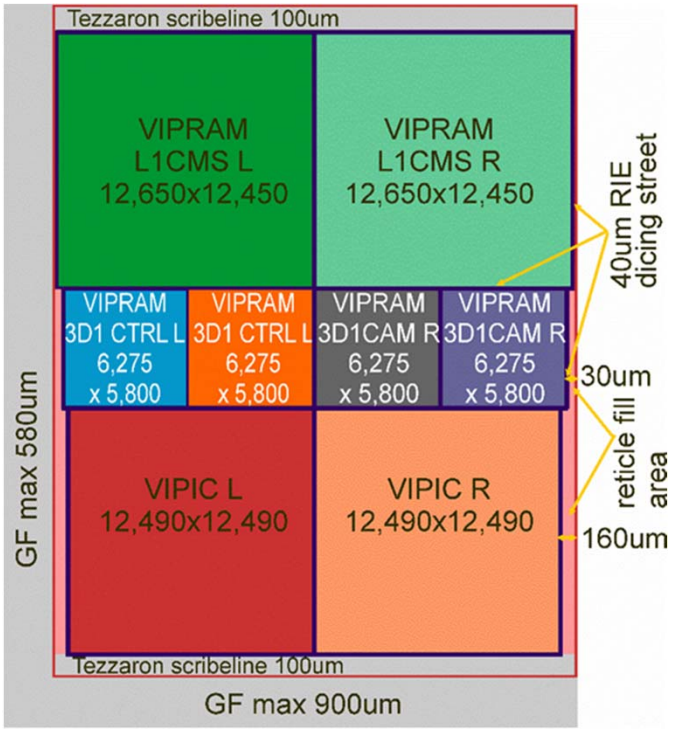


Fermilab

# VIPIC-L Camera for Photon Imaging at the APS Upgrade

- **VIPIC-L: Vertically-Integrated Photon Imaging Chip - Large**
  - Development of a photon imaging camera for use at the APS light source
  - 1.3M-pixel, single module camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays,
  - Funded by DOE Office of Science Office of Basic Energy Sciences
  - Collaboration between FNAL, BNL, & ANL
- **Roles & Responsibilities**
  - FNAL: Chip design - 3D ASIC (2 tiers 1.25×1.25cm2) in GF CMOS 130nm, design masks for 3D-integration processing for 3 interfaces (Tezzaron/Novati specification): ASIC tier-to-tier, ASIC digital back to PCB, ASIC analog front to sensor

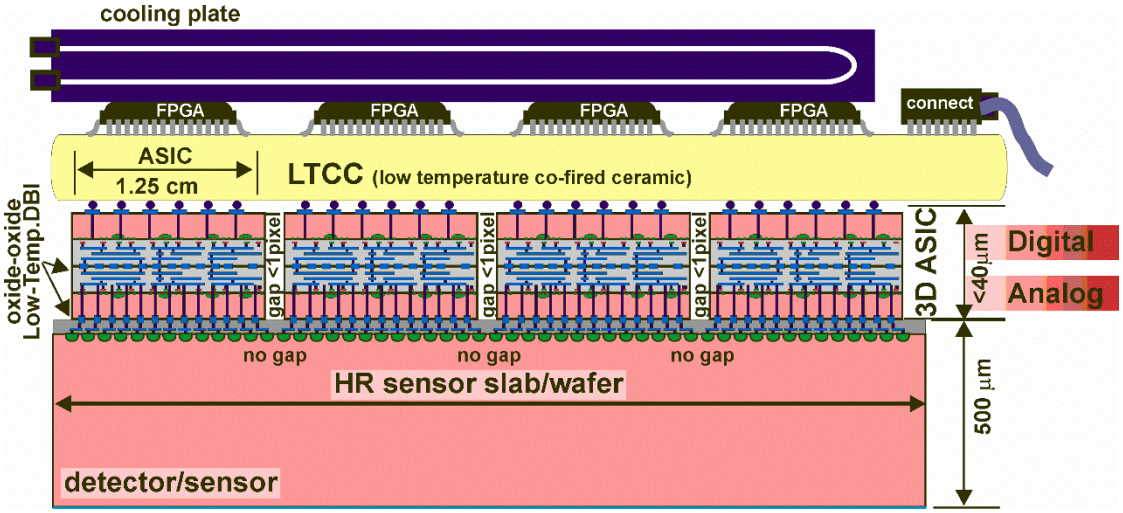
    ⇨ ***Part of 3D development program at FNAL***
    ⇨ ***Multi-project submission***
  - BNL & ANL: Back end DAQ; testing at light sources



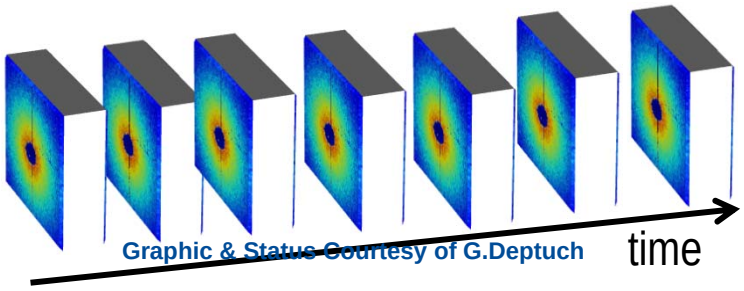

Graphic & Status Courtesy of G.Deptuch

# VIPIC-L Camera for Photon Imaging at the APS (Cont.)

- **The VIPIC-L Chip**
  - 3D ASIC (2 tiers 1.25×1.25cm2) in GF CMOS 130nm
  - ~120M transistor (largest ASIC built by any US National Laboratory) and 65 mm pixel pitch
  - 1 Mpixel = 3 slabs of 2×6 VIPIC-L LTD-bonded directly to a Si sensor wafer
  - Blind TSVs in both sides after thinning, wafer-to-wafer bonding of ASIC followed by die-to-wafer bonding of ASICs onto a Si sensor slabs
  - DAQ: 1 FPGA per VIPIC-L (fitting in its footprint) for on the fly data processing (up to 0.72 Tbps of raw data produced)



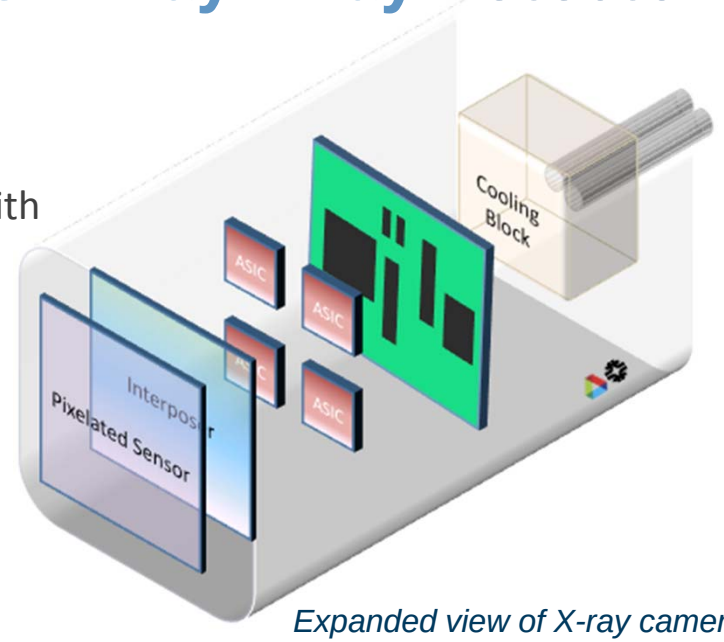

**X-ray back-side illumination**



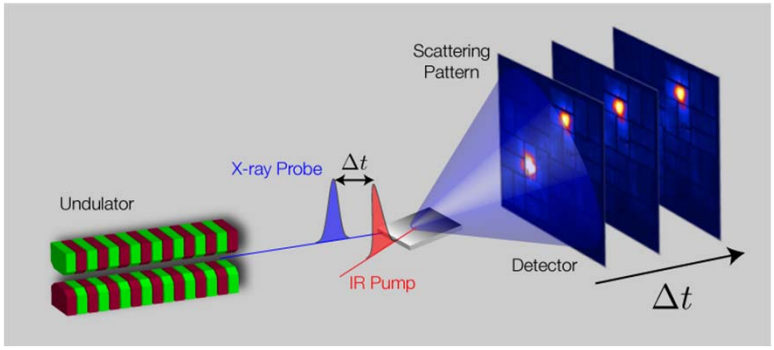

⇨ ***Chip design complete; Fabrication is in progress***
⇨ ***See FNAL & BNL talks for more details…***

# FASPAX: Fermi-Argonne Silicon Pixel Array X-ray Detector For the APS Upgrade

- **The APS Upgrade – New Regime in Area Detectors**
  - X-ray camera beyond the dynamic range of a CCD, with the sensitivity of a photon counting detector
    - Burst image rate (~13 MHz)
    - Large, fully active (seamless) area (15x15 cm2),
    - Small pixel size (100x100 mm2) for 2.2M pixels
    - Single frame - $10^5$ photon per image capability in small pixel footprint
- **Enabler of Science**
  - Studies of irreversible processes, time-resolved or high flux applications and high speed imaging (DCS)
    → Pump probe experiments
- **FASPAX - Versatile, Fast Integrating Area detector:**
  - MHz burst frame rates will record high-resolution movies of millisecond phenomena
  - Flexible dynamic range: on per pixel basis, gain for integrated signal – from single photon to $10^5$ photon/pixel




*Expanded view of X-ray camera*



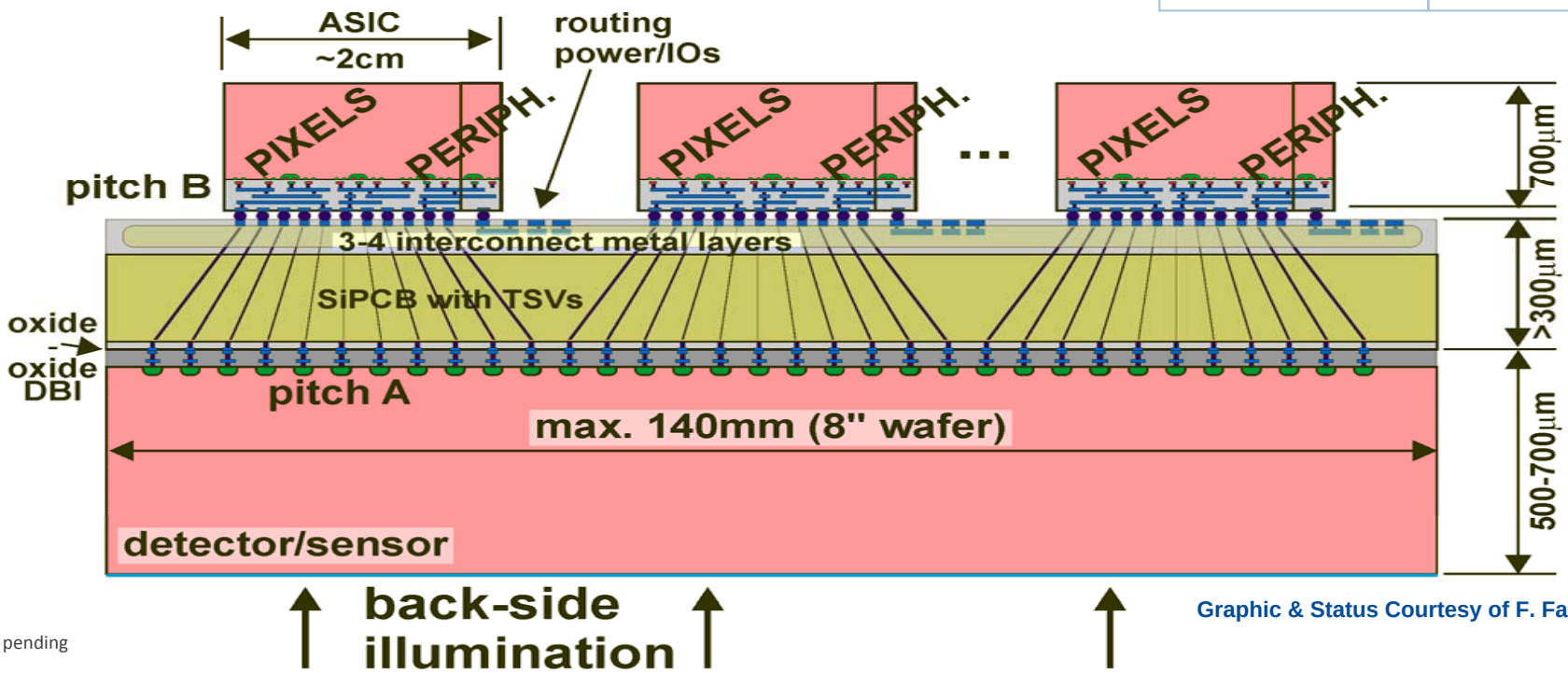

http://unlcms.unl.edu/physics-astronomy/fuchs-group/pictures/pump_probe_setup.png

⇨ ***Exceeds the capability of any existing X-ray detector***

# FASPAX Pixel Camera for the APS

- **Approach uses 3D integrated technology**
  - Provides seamless, wafer-scale detector
  - Back-illuminated to detect X-rays
  - Interposer adapts sensor pixel to ASIC pitch
  - ASICs in SiGe process, bump-bonded to interposer
  - 500 mm thick Si X-ray detector

| Parameter | Value |
|---|---|
| Pixel size | 100x100 $\mu m^2$ |
| Buffer depth | 24 – 256 |
| Range | 1 – $10^5$ $\gamma$'s |
| Detector area | ~15x15 $cm^2$ |
| Frame Rate | 13 MHz |
| Well depth | 1fC – 100 pC |
| Si Thickness | 500-700 $\mu m$ |

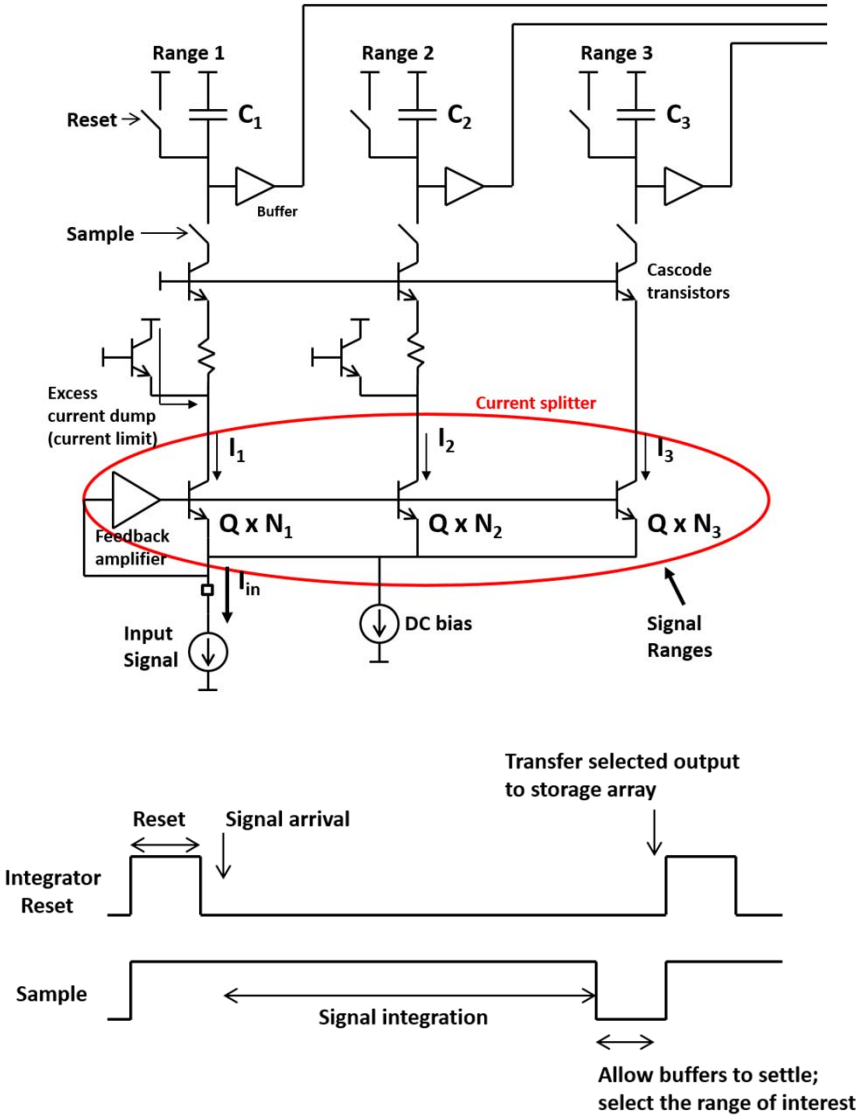



Graphic & Status Courtesy of F. Fahim

Patent pending

# FASPAX Pixel Camera for the APS Upgrade

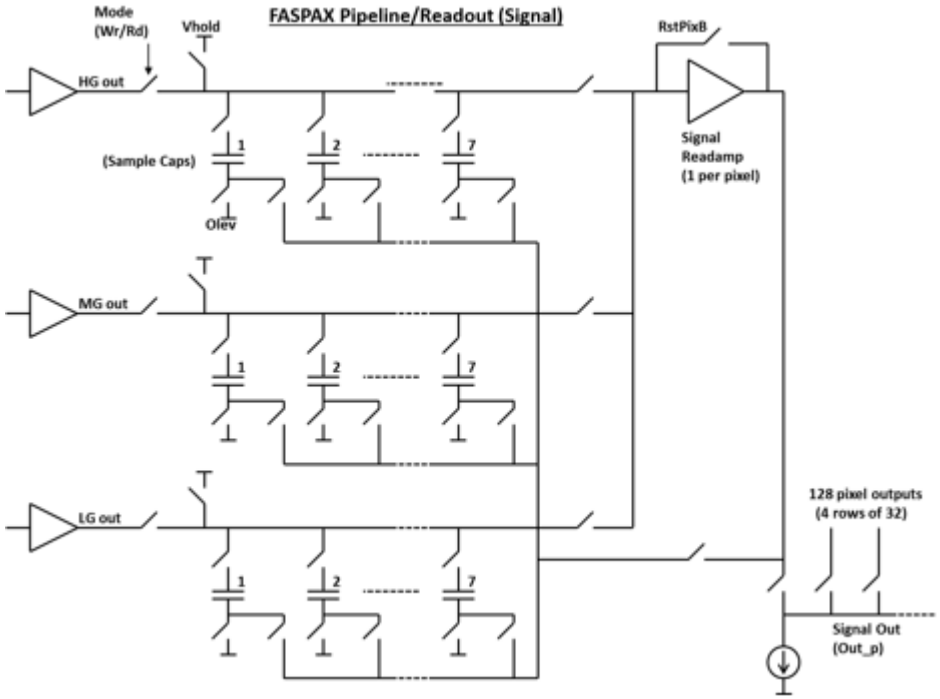
- **FE – Uses QIE-based Current Splitter on each Pixel:**
  - NPN current split ratios are set with multiple instances of unit-size transistor Q.
  - Splitter base is driven by a feedback amplifier in order to provide low input impedance and maximum bandwidth.
  - Splitter outputs pass through current limiters on the lower ranges: with a large input signal (lower ranges will not be selected), most of the input current is shunted away ("dumped").
  - Cascode transistors isolate current splitter output capacitance from integrators
  - Use passive integrators: simple! No power required, the signal does all the work!

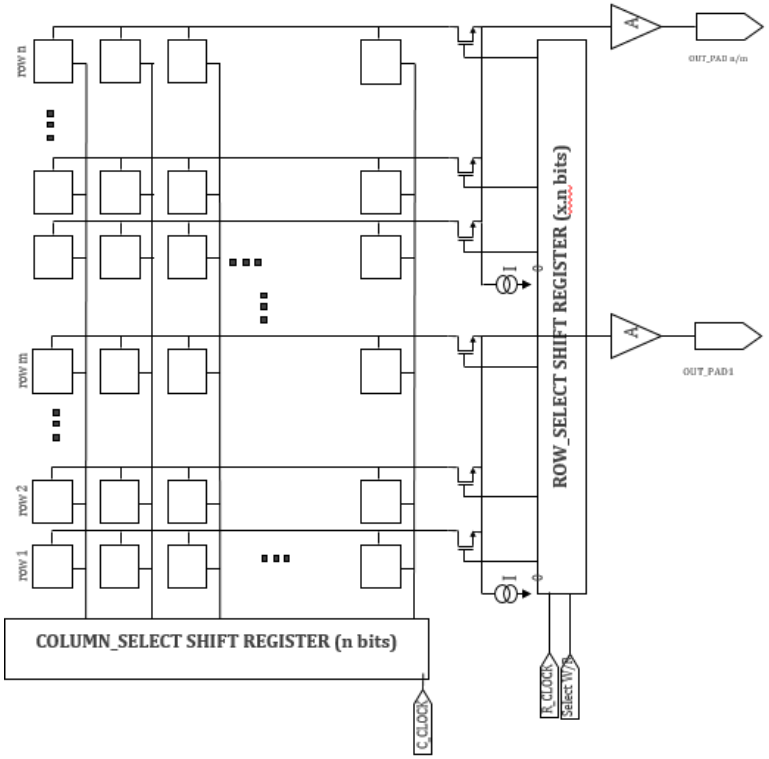



Graphic Courtesy of T. Zimmerman

# FASPAX Pixel Camera for the APS Upgrade

- **Readout Block Diagram**
  - Store (8*3)24 samples, then read
  - 4 rows grouped together per analog output




⇨ ***Chip design complete; Working on commercialization…***
⇨ ***See FNAL talks for more details…***

# Summary

- **Argonne has been developing ASICS over last ~20 years, primarily through partnership and collaboration with Fermilab**
  - Highly successful program
  - Has allowed us to develop sophisticated, leading-edge instrumentation systems contributing to the national HEP program
  - HEP has benefitted significantly;  APS starting to benefit;  PHY in the future (FRIB?...)

- **Excellent example of complementary use of national laboratory resources**
  - Leverages expertise from a large, highly-successful ASIC design group with wide breadth & depth of skills
  - Reduces licensing costs
  - Promotes collaborative atmosphere

- **But we could be doing more…**
  - **There are still barriers in inter-laboratory relations**
    - Overheads → Work for Others contracts
    - MOU / SOW/ general red tape
  - **European groups have figured out how to reduce these barriers**

    ⇨ ***This conference has the potential to make this better!!!***