



---

Managed by Fermi Research Alliance, LLC for the U.S. Department of Energy Office of Science

---

# ASIC Development Group at Fermilab

G.W. Deptuch, October, 2017

# Outline:

---

- Composition of the Group
- Mode of Operation and Projects
- List of Current Projects
- Access to Fabrication Processes
- Project Lifetime Cycle
- IC Design Flow and CAD/EDA Tools
- Infrastructure
- Current Project Highlights
- Summary

ASIC = Application Specific Integrated Circuits, developed for desired functionality of reading out detectors or processing of data, often required to operate in extreme environments, e.g. radiation or cryogenic temperature

# Composition of the Group:

## Fermilab ASIC Development Group, PPD/EED 14WHW

James Hoff

Sandeep Miryala

Tom Zimmerman

Alpana Shenai

Farah Fahim

Davide Braga

Grzegorz Deptuch



- ASIC Design current headcount: 7 ASIC designers - including 4 PhDs
  - 3 senior-leader engineers, 1 pursuing PhD, 1 providing maintenance of CAD/EDA tools, licenses, scripts, etc.
- ASIC testing: 1 senior test eng., 1 eng. assoc., 2 technicians + 1 PCB drafter (shared)
- occasional support from PPD/EED, CD + other departments at Fermilab and incidental invitees (guest/visitor) – testing often bottle-neck
- HIRING: 1 application physicist to enforce testing + need of 1 ÷ 2 ASIC designers

# Mode of Operation and Projects:

---

- **Role of the ASIC Development Group:**
  - Provide integrated circuits for detectors to run experiments,
  - R&D on detectors for future (*develop strategic solutions and establish reference*).
- **Acquisition of Projects:**
  - usually brought directly to the Group by/from physicists involved in experiments,
  - started internally or in response to external requests based upon the reputation of the group and portfolio of explored technologies,
  - in response to project calls (DOE-BES).
- **Areas of operation:**
  - primarily: instrumentation for HEP,
  - secondarily: where synergies present and where appropriate, i.e.
    - leverage technologies for other fields and work through collaborations (domestic: ANL, BNL, SLAC, Southern Methodist University, UPenn, NWU international: CERN, AGH-UST Krakow Poland, U. of Bergamo Italy).
- **Importance of an ASIC Group in Nat'l Lab system:**
  - maintain core competences for niche designs in extreme environments (cold, radiation)
  - maintain legacy projects and provide long term expertise on designed chips
  - provide base for collaboration with Universities

# Mode of Operation and Projects:

---

- **Core set of projects:**
  - ASICs for HEP (and NP - smaller degree)
    - pixels, strips, stripixels, wires, SiPM, PMT readouts, data transm. and auxiliary circuits:
      - *FPHX for Phenix at RHIC with LANL and BNL - completed 2009,*
      - *Front End Electronics for the NOvA Neutrino Detector - completed 2010,*
      - *charge integrating, floating point digitizer for CMS (FNAL) and ATLAS (ANL) QIE 10/11 – completed 2016)*
  - ASICs for R&D in HEP
    - Content-addressable memory circuits for track-triggering at HL-LHC
    - Readout ASICs for tracking with trigger participation in HL-LHC
    - Cryogenically-operated electronics for liquid Ar TPC (neutrino experiments - DUNE)
    - Radiation hardness of 65nm CMOS for HL-LHC ( $1\text{Grad}, 10^{16} n_{1\text{MeVeq}}/\text{cm}^2$ )
    - Synchronous front-end for pixel readout for CMS HL-LHC and RD-53
  - ASICs for DOE-BES (X-ray Photon Science)
    - Large area pixel detector systems: VIPIC-L, FASPAX, FLORA
- **Handling of external projects** Fermilab Office of Partnerships and Technology Transfer:
  - Field Work Proposals – funds received directly from funding agencies, e.g. DOE-BES
  - Collaborative Agreements, Statement of Work (SOW) - funds received from other entities, e.g. National Laboratories, Universities, Companies, etc.



# List of Current Projects:

---

## *High Energy Physics*

### **COLDATA: COLD DATA Transmission ASIC for DUNE**

Data transmission from cryostat to warm side at 1.2Gbps over up to 30m of Cu links and for control of Front-End and ADC chips, collab. with SMU and BNL

### **COLD ADC: for DUNE**

12b, 2Msps ADC for DUNE liquid Ar TPC, collaboration with LBL, BNL

### **FanTastIC: Fast Timing Integrated Circuit for CMS forward Calorimeter**

4 × 24 pixel RO IC providing ~20ps resolution for 1 × 3 mm<sup>2</sup> pixel LGAD sensors, collab. w. SLAC?, UCSC?

### **VIPRAM: Vertically-Integrated Pattern Recognition Associate Memory**

3D-integrated hardware tracking for Phase 2 CMS Upgrade, (Fermilab, NWU) funded through KA25 and CMS

### **HGCalConcentrator: High Granularity Calorimeter Data Concentrator for CMS**

72 × 1Gbps → 4 × 10Gbps transceiver for trigger data and event data readout, collab. w. CERN, Omega France

### **FCP130/iFCP65 and RD53A: Fermilab CMS Pixels (RD53 collaboration)**

Pixels for CMS Phase2 Upgrade + CERN RD53 in TSMC 65nm process, Univ. of Bergamo Italy (iFCP), KA25

## *Photon Science*

### **VIPIE-L: Vertically-Integrated Photon Imaging Chip - Large**

Fully 3D-integrated, 1.2M pixel camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays, 0.7Tbs of data (BNL, ANL, Fermilab), DOE-BES (FWP)

### **FLORA: Fermilab-LCLS CMOS 3D-integrated with Autogain**

Soft 0.2-2 keV X-rays, high speed 10kfps, high dynamic range 10<sup>3</sup>, 2M pixel camera for LCLS II, (Fermilab-SLAC) 2-year R&D funded by DOE-BES (FWP)

### **FASPAX: Fermi-Argonne Silicon Pixel Array X-ray**

Extremely high dynamic range (up to 10<sup>5</sup> photons/pixel/pulse) pixel camera for 8-12 keV X-rays, (started as funded by APS-ANL Upgrade – SOW, now: Phase I commercialization SBIR grant with FieldViewers)



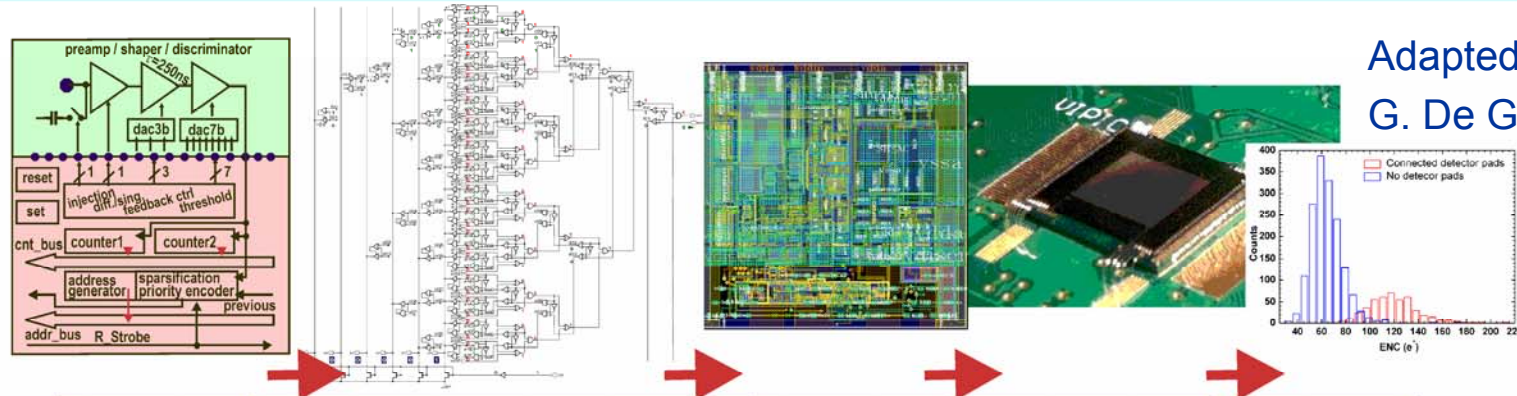
# Access to Fabrication Processes:

---

- Signed Non-Disclosure Agreements (NDA) and various License Agreements (DLA, PLA) with brokers (MOSIS, Europractice, IMEC-CERN) and individual companies for IC fabrication processes, sensor fabrication and integration (bump-bonding, 3D-IC, HDI)
- **Current portfolio of fabrication processes (MixedMode, LowPower):**
  - experience with:
    - GF (IBM) CMOS 250nm, TSMC CMOS 250nm
    - AMS SiGe BiCMOS 350nm
    - GF CMOS 130nm
    - GF (IBM) SiGe BiCMOS 130nm
  - growing experience with:
    - TSMC CMOS 65nm (member of RD53)
    - 'Leading CIS foundry' CMOS OPTO 180nm/130nm
  - Readiness (access to PDKs and CAD/EDA tools)
    - TSMC CMOS 45/40nm
    - GF CMOS 55nm
- **NDA signed for civil applications (excluding usage in weapons, medical applications, etc.), if needs of other uses emerge - special agreements needs to be established and signed**
- **Familiarity with handling ITAR issues**

# Project Lifetime Cycle:

Adapted from  
G. De Geronimo



<u>phase 1</u>	<u>phase 2</u>	<u>phase 3</u>	<u>phase 4</u>	<u>phase 5</u>
system level design	transistor level design	masks layout	fabrication boards / test environment preparation	tests
~ 2 months	~ 6 months	~ 2 months	~ 3 / ~ 2 months	~ 2 months

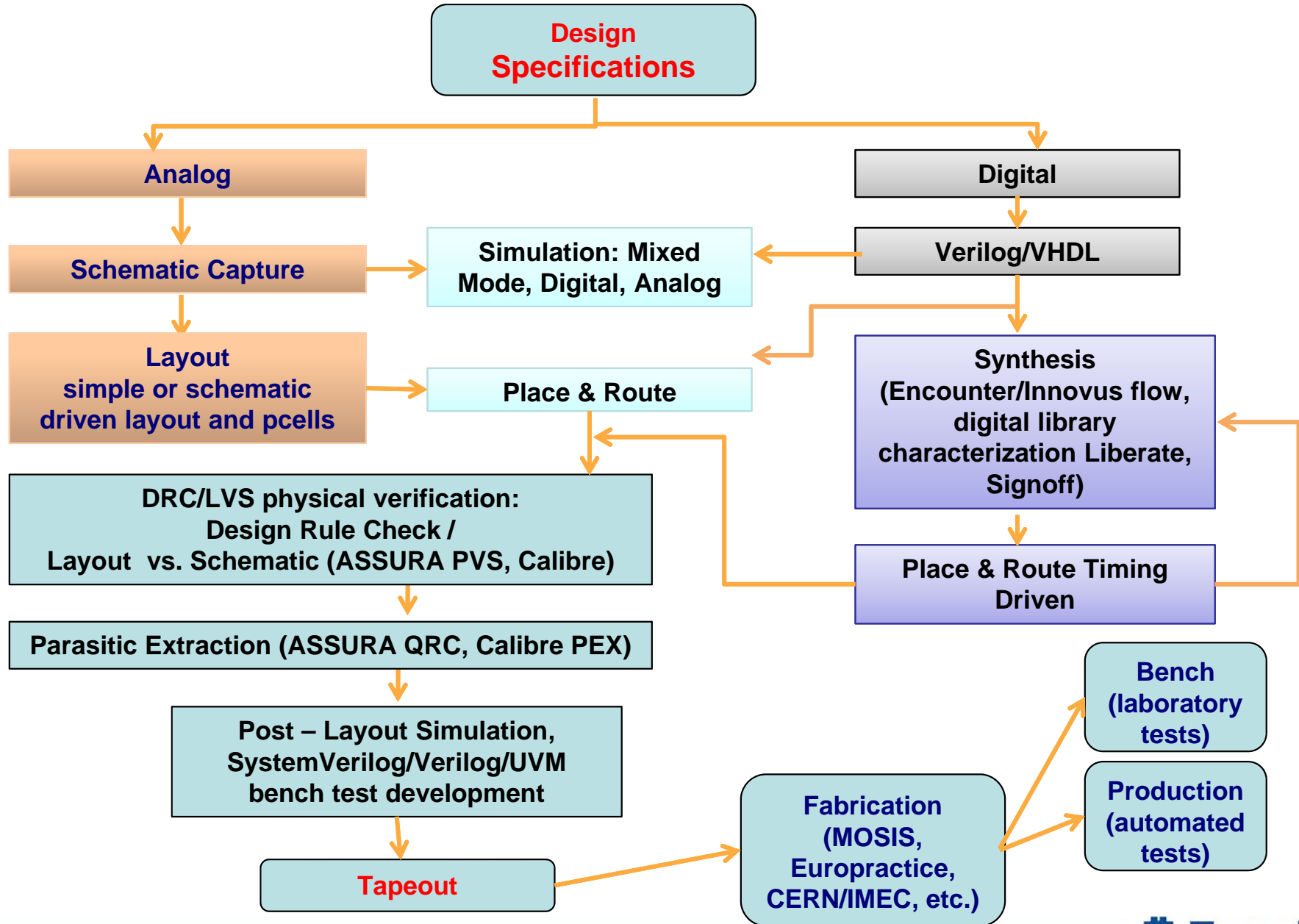


from concept to ready for production design it takes:  
1 - 2 cycles, 2 - 3 years, 3 - 6 FTE  
(but more complex designs require more)

higher complexity, more integrated functionalities translate to:  
more resources, higher level of expertise, longer development time



# IC Design Flow:



# Cadence/Menthor CAD EDA Tools (DFII Cadence 6.1X):

**Commercial/Research license portfolio that is not limited to degree-delivering educational purposes**

- **Full Custom Flow**
  - multiple seats of Schematic Editor with handling of constraints
  - Analog Design Environment capable of handling multi-thread Spectre (some Eldo), APS simulations, including MonteCarlo (process corners, mismatch and yield)
  - Mixed Mode simulation using Config View and SystemVerilog/Verilog + Spectre or APS (complex, multimillion transistor simulation can be handled), transient noise, WReal...
  - multiple seats of Layout Editor with schematic driven capabilities + space-based P&R
- **Digital-on-Top Flow**
  - Virtuoso Digital Implementation, Innovus Implementation System and Tempus Signoff – full Encounter flow capability (from Verilog, through Synthesis to silicon implementation)
  - NC Verilog, Incisive-Enterprise with test bench and UVM capability
  - Digital library characterization with Liberate (create full digital library with timing models)
- **Verification**
  - Cadence ASSURA DRC/LVS/QRC,
  - Cadence PVS DRC/LVS/QRC (90nm and below, used for 65nm)
  - Menthor Calibre DRC/LVS/PEX
- **Other**
  - SOS Cliosoft Design Manager (used for all projects)
  - Silvaco (TCAD, Device Level Simulations)

# Test Instrumentation:

- **ASIC test lab spaces**



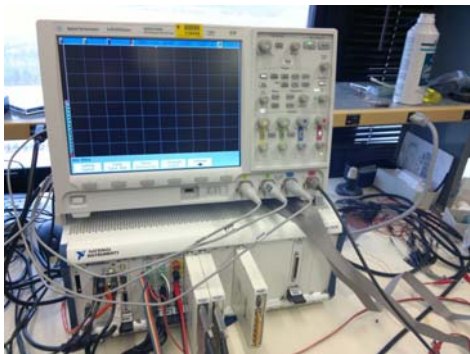
- + “clean room” (semi-auto probe stations /one capable 8”/ and measurement instruments)

- + 6 labs (PXIe chassis with FlexRIO National Instruments LabVIEW FPGA systems and test equipment + lab. radioactive sources)

- + robotic chip testing station (needs upgrade)

- + manual bonding station

- + PCB components mounting lab



**strategic: avoid custom FPGA-based systems for bench/beam tests (to test chips not testing setup)**

- Requisition of four PXI/PXIe FlexRIO National Instruments digital and analog (ADC, DIO LVDS, DIO CMOS, DAC, SMU, DMM, power, etc.) systems based on LabView – to fulfill hardware needs for testing of chips

- DC-3GHz spectrum analyzer – intended for noise measurement bench – crucial but needs development!

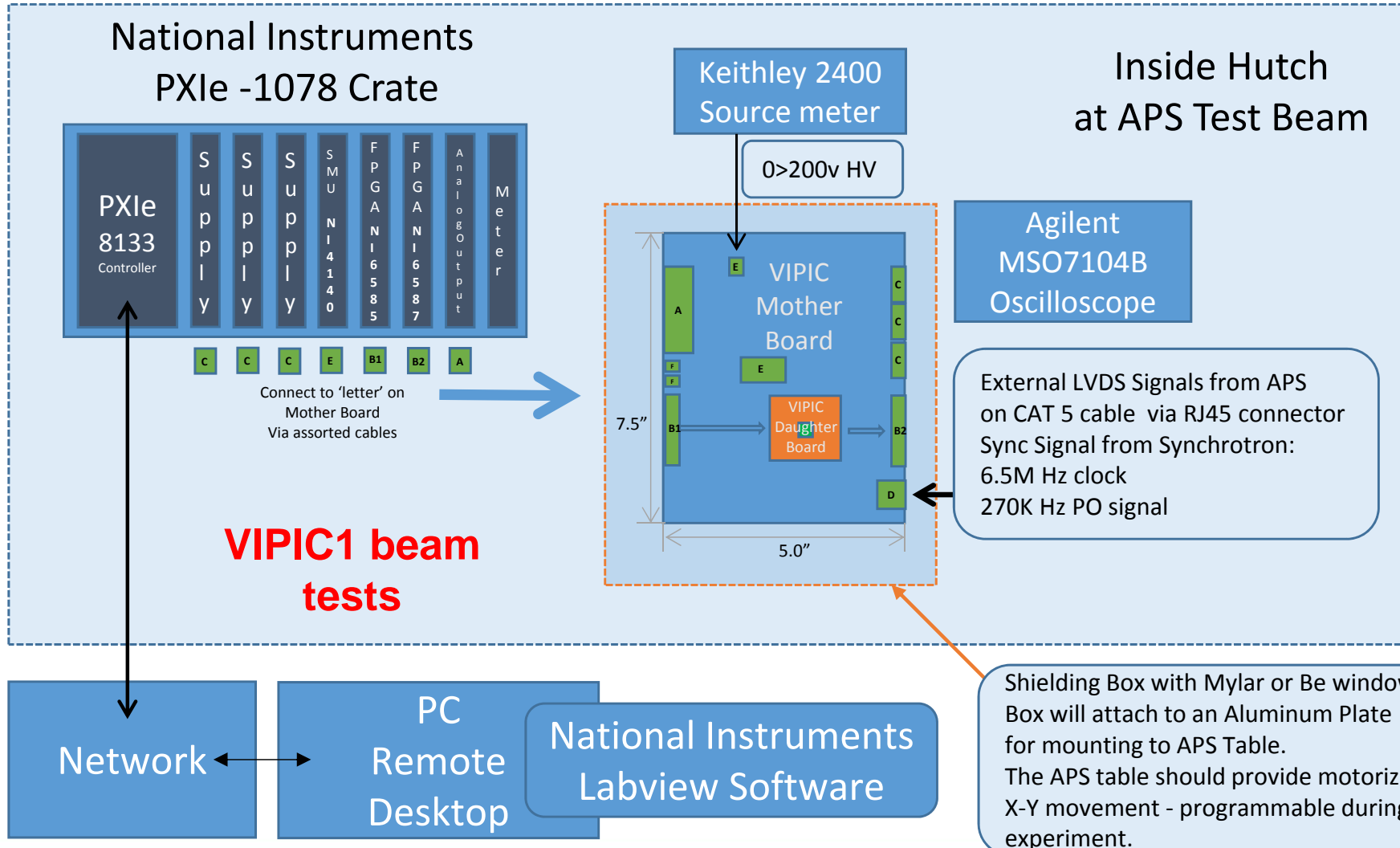
- Other instruments: static parameter / LCR / Logic / network analyzers/ V / I source, pA, digital oscilloscopes, etc.



# Test Instrumentation (example):

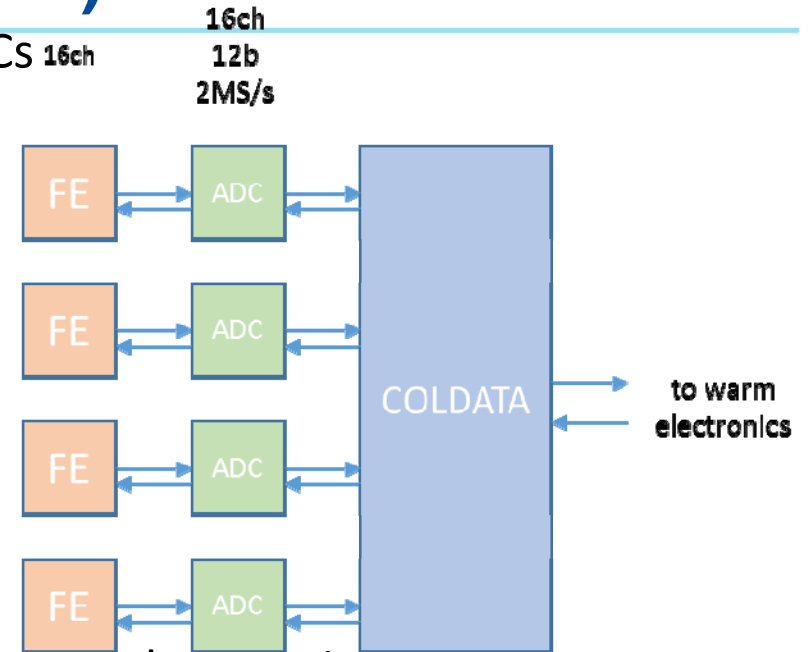
Crate Dimension : 40cm x 40 cm x 25cm tall  
 The cables coming out of the modules will extend out of the modules about 10cm before they can bend.  
 The shortest cables are 1 meter in length(they are custom cables from National Instruments).

**Complete testing of ASICs, including beam tests, cryogenic operation, gamma irradiations, etc.**



# Current Projects Highlights (COLDATA)

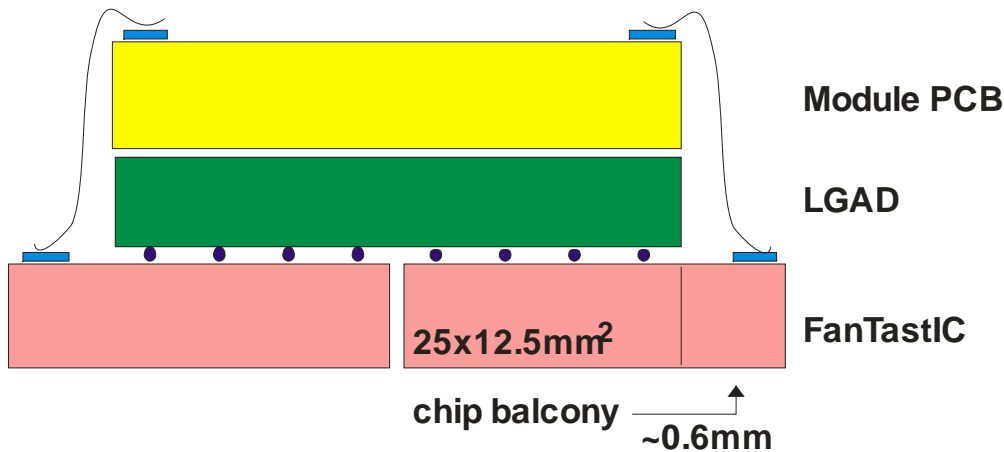
- Data concentrator and readout chip for DUNE LAr TPCs
  - 1.5Gbps In , 2x 1.2Gbps Out
  - data readout and control between cold and warm electronics
  - system clock interface
- Digital chip with mixed-signal components
- **Challenges:**
  - Low power/high speed: 65nm CMOS process
  - Reliability: operate at 89K for >25 years without maintenance
    - custom logic library designed to avoid premature degradation
    - custom models for accurate simulation provided by external company from Fermilab test structure
    - accurate cold timing models provided by UPenn
  - Fully digital chip:
    - new workflow/EDA tools
    - clock domains synchronization
    - test coverage and verification



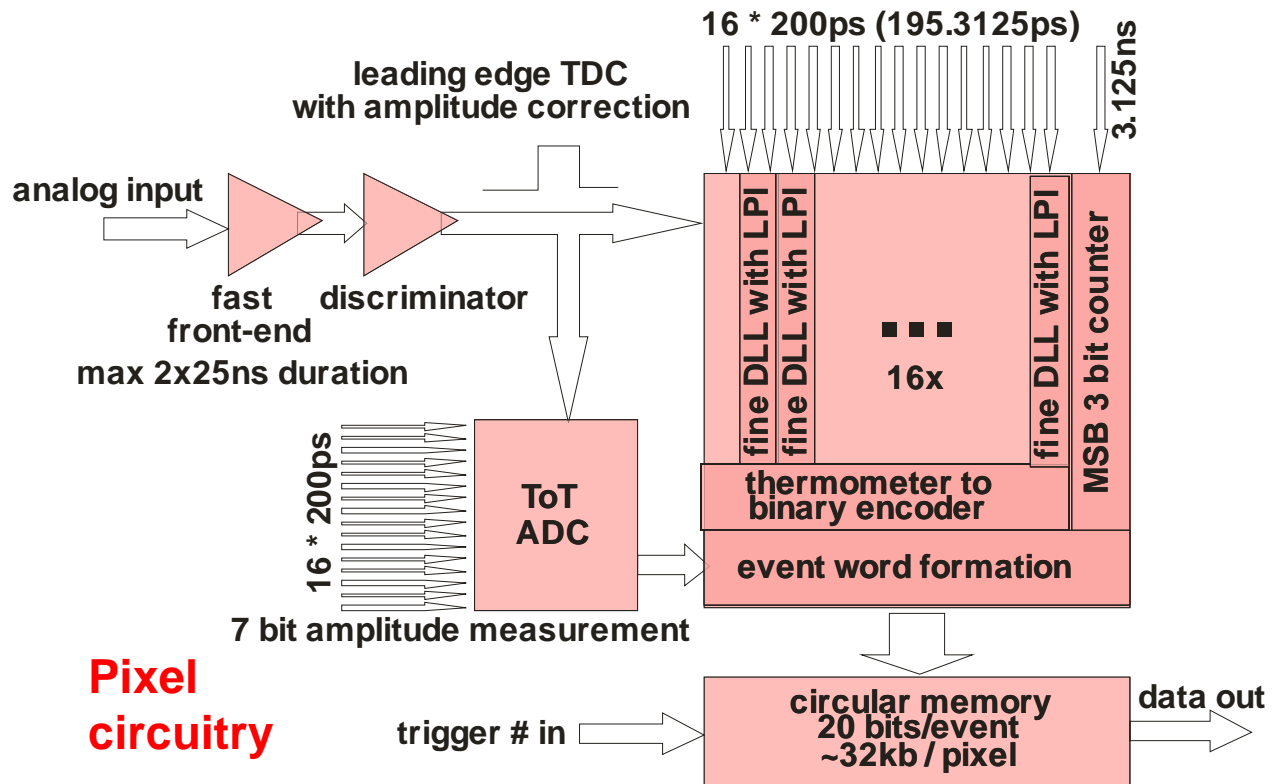
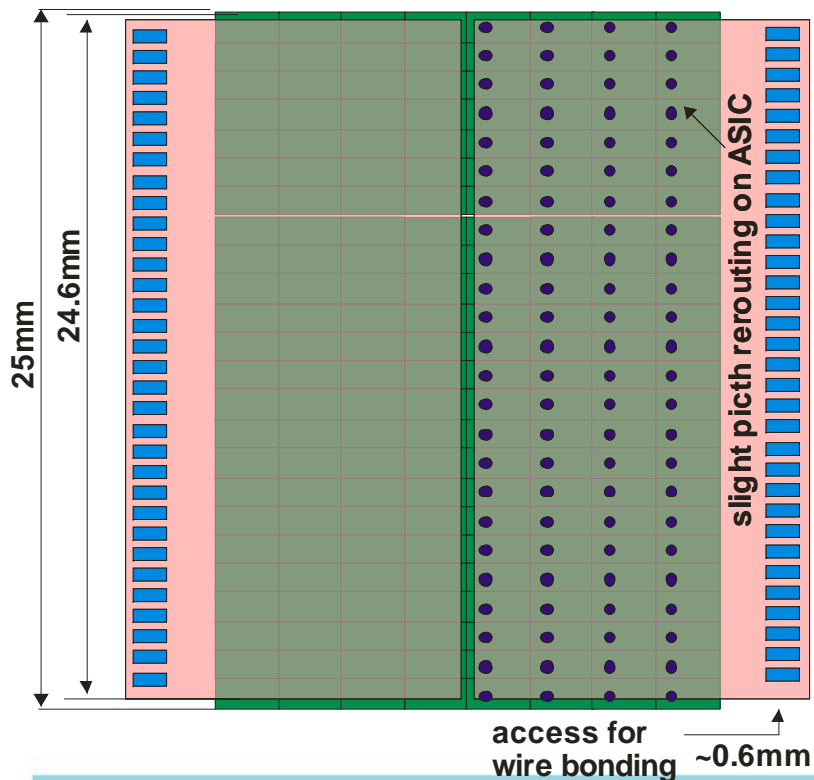
Fermilab ASIC group responsible for most of the chip design, plus top level assembly and verification; collaboration with Southern Methodist University (PLL and Line Driver) and University of Pennsylvania (library characterization).



# Current Projects Highlights (FanTastIC)



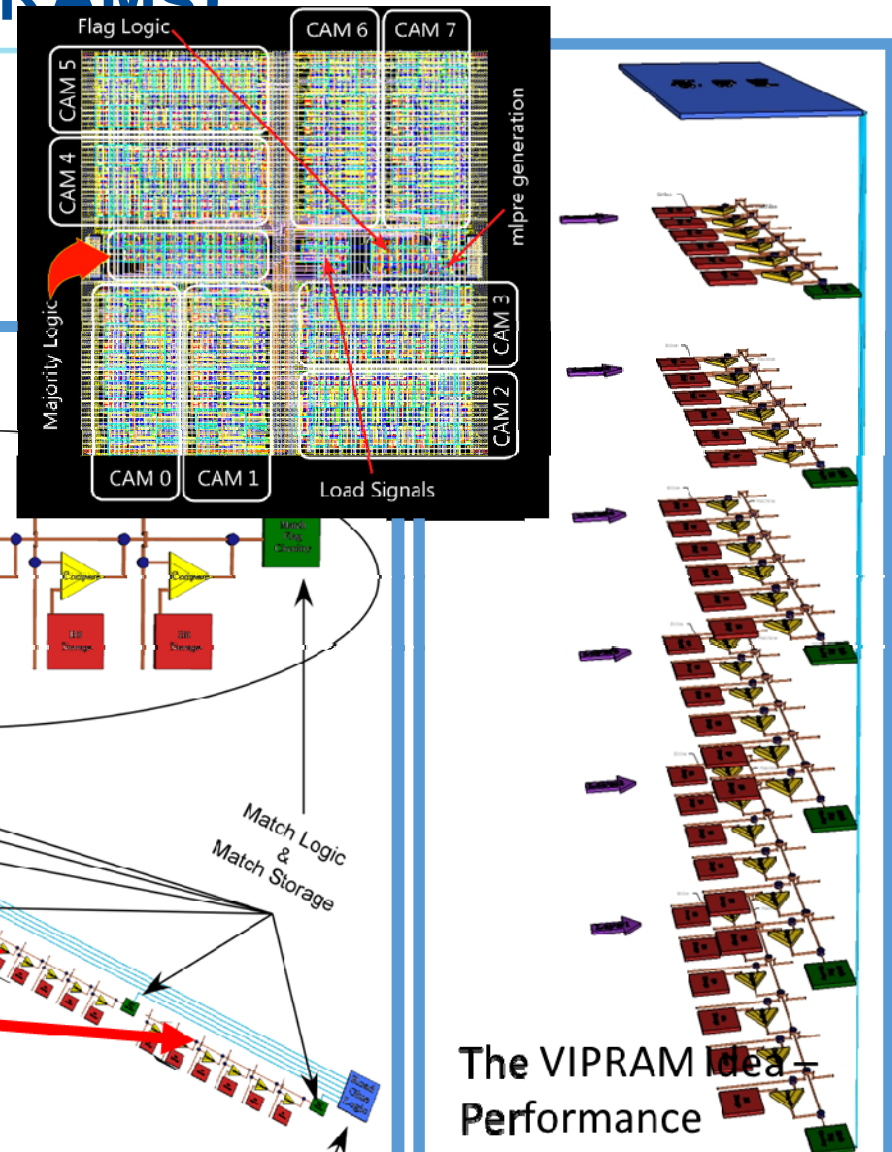
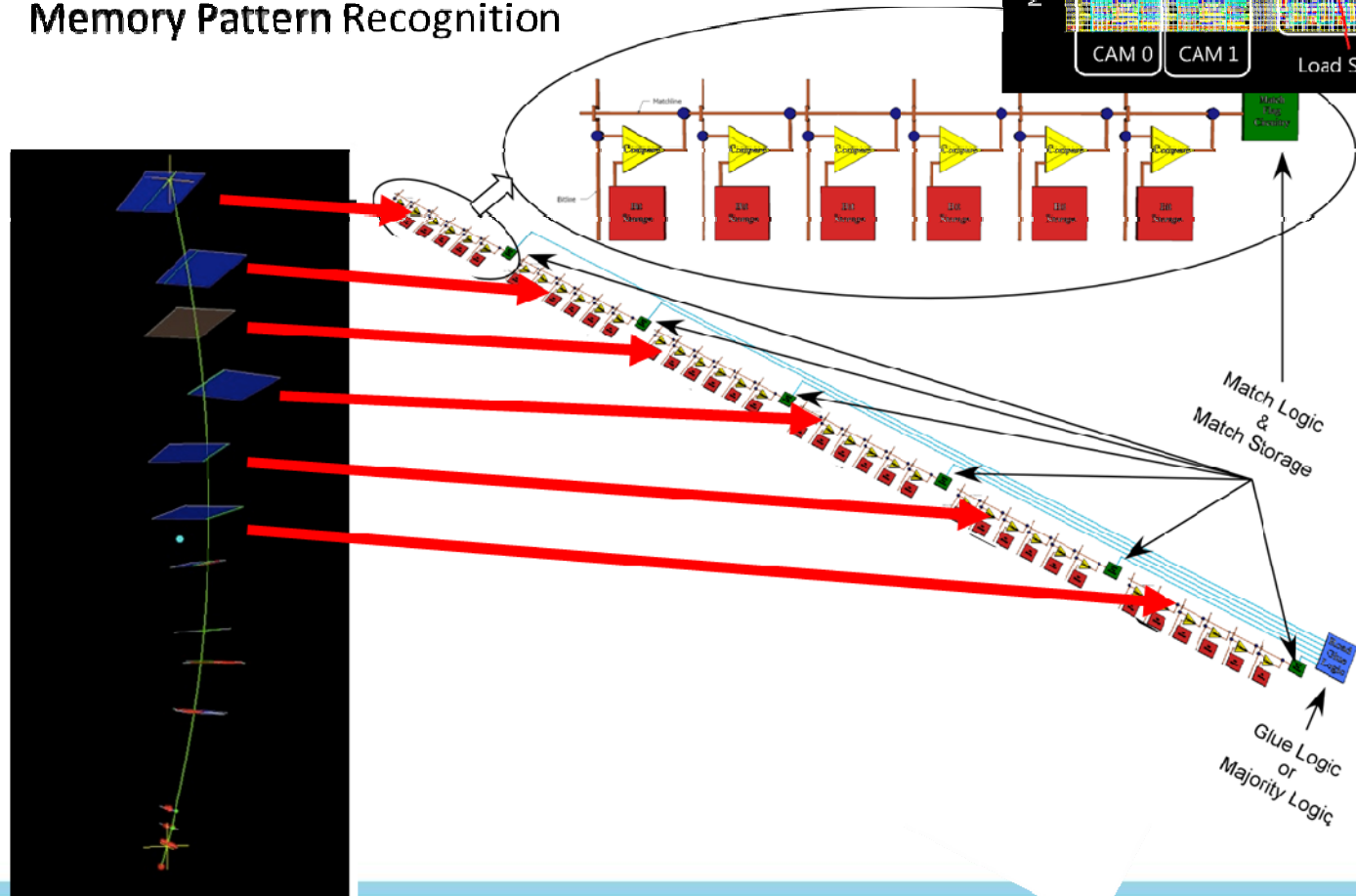
- Power efficient scheme
- One coarse DLL / entire chip with bin size tuning
- 320 MHz clock and 16x200ps spaced edges distributed to each pixel precise clock distribution
- Reuse of coarse bin for ToT ADC
- No tuning of in-pixel time bins
- Programming measurement window/pixel x200ps
- IC size slightly smaller than sensor pixel outline to allow module abutting of ICs



# Current Projects Highlights (VIPRAMs)

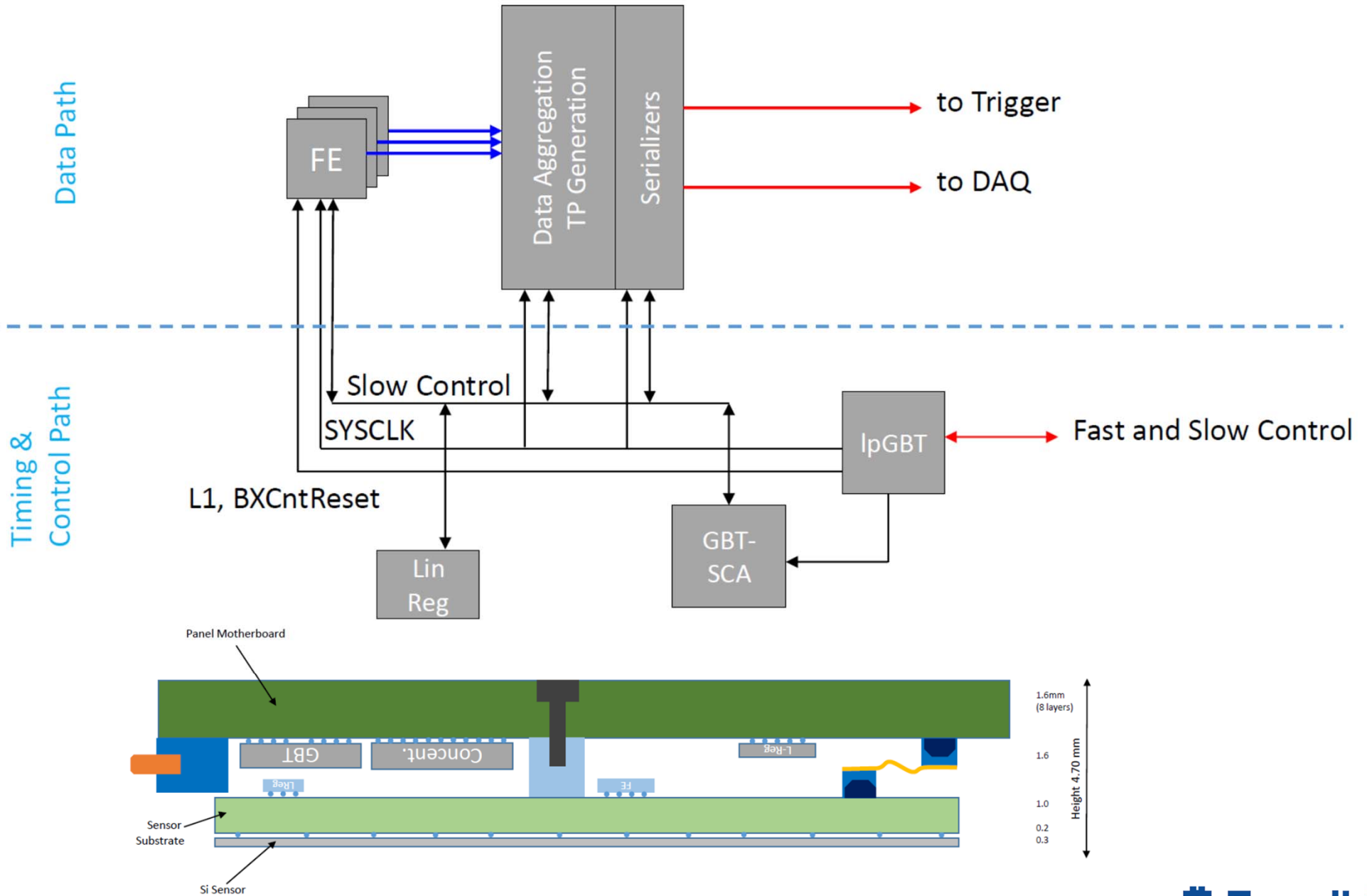
- **VIPRAM3D** – Generic R&D. Increased pattern density, increased speed, reduced power, reduced cost, reduced design effort through multi-tier 3D integration
- **VIPRAM L1CMS** – Specifically dedicated to CMS and the Level 1 Tracking Trigger. The architecture is enhanced by 3D and takes advantage of it.

## The PRAM Idea – Track Fitting through Associative Memory Pattern Recognition



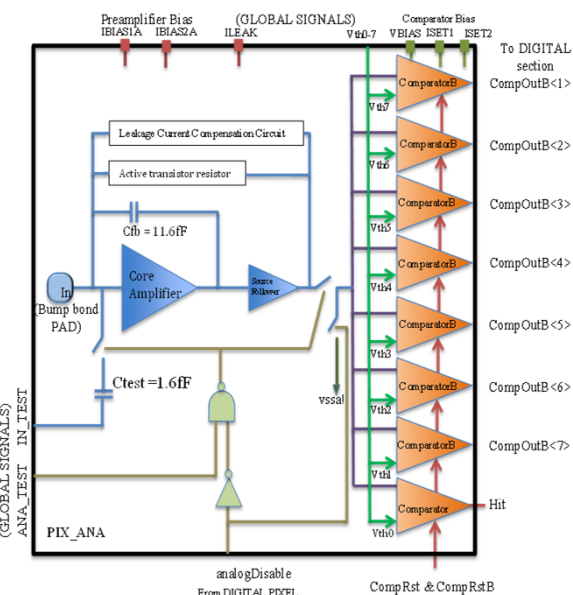
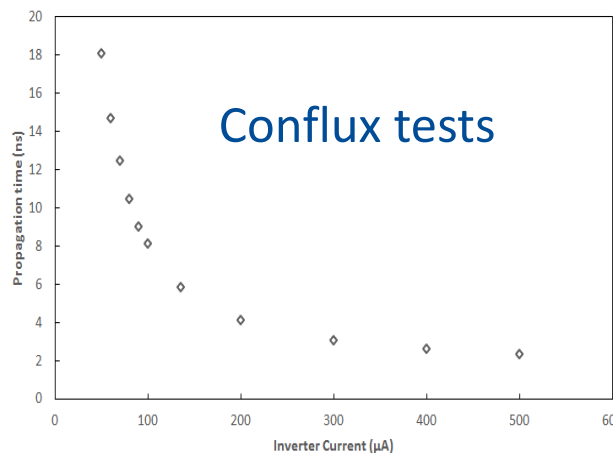
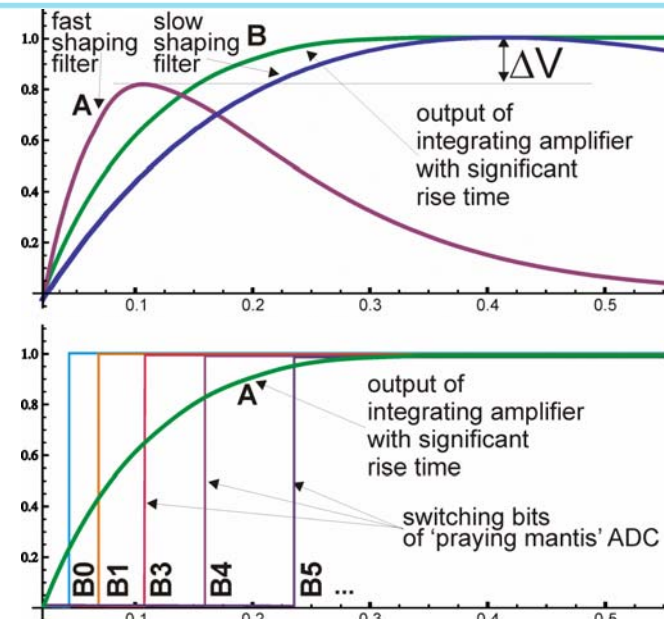
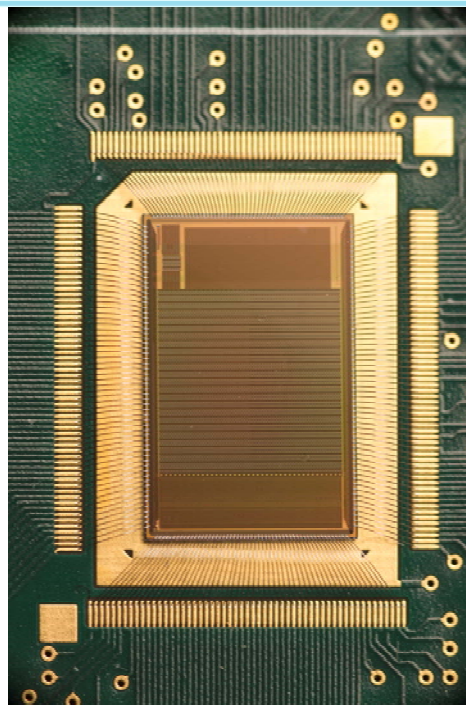
The VIPRAM Idea –  
Performance  
Improvement  
through Vertical  
Integration

# Current Projects Highlights (HGCaIConcentrator)



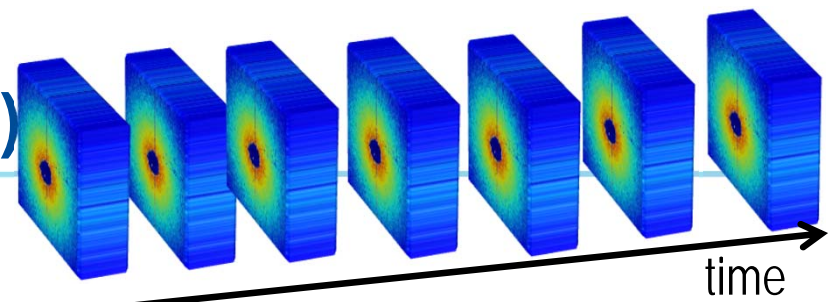
# Current Projects Highlights (FCP130 / IFCP65)

- Novel Synchronous front-end concept for CMS Phase II forward pixel
- Correlated double sampling for noise reduction
- $\frac{1}{2}$  BXClk cycle for reset &  $\frac{1}{2}$  for compare
- Version 1- Issues:
  - Unbiased and wrongly Biased Deep N Wells
  - Substrate contacts instead of Antenna Diodes
  - Thresholds are parasitically connected
- However: Successful Preliminary Qualitative analysis
  - Preamplifier response can be monitored; change of current is feedback loop changes the return to baseline.
  - All comparator response times are changing with change in threshold voltage
- Configuration register is able to correctly program the pixels
- The serial mode of transfer in FIFO 2 daisy can correctly send data Out
- The Spy signals for last superColumn ( Pixel Hit, ADC value and address can be correctly monitored)
- Conflux performance could be measured
- Version 2- Status
  - Change in Preamp and comparator
  - All other bugs fixed
  - Top Level changed for only 1 design
  - Submission on February 2017

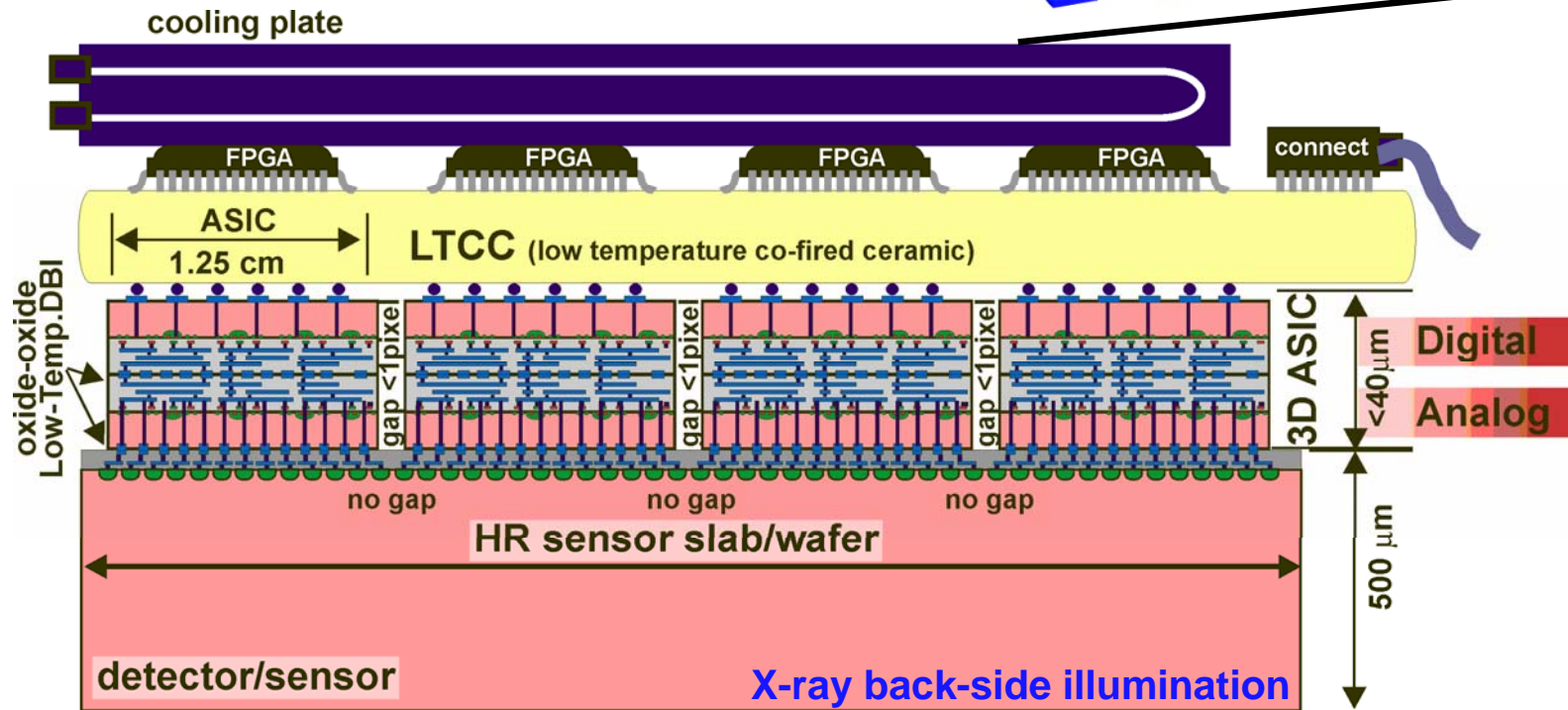




# Current Projects Highlights (VIPIC-L)



## Vertically-Integrated Photon Imaging Chip - Large



1.3M-pixel, single module camera for X-ray Photon Correlation Spectroscopy, 8-12 keV X-rays,

- VIPIC-L is a two tier 3D ASIC  $1.25 \times 1.25 \text{ cm}^2$  with  **$\sim 120\text{M}$  transistor** (largest ASIC built by any US National Laboratory) and  $65 \mu\text{m}$  pixel pitch
- 1 Mpixel = 3 slabs of  $2 \times 6$  VIPIC-L LTD-bonded directly to a Si sensor wafer
- configurable in sparsification or imaging mode (up to 78kfps of read everything)
- 1 FPGA per VIPIC-L (fitting in its footprint) for on the fly data processing (up to 0.72 Tbps of raw data produced)
- Multi-layer (>20 routing layer LTCC) supports b-bonded detector structure



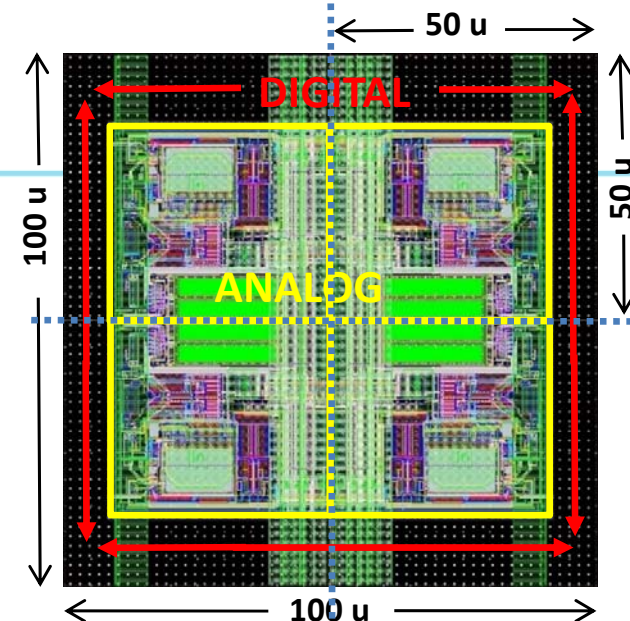
# Current Projects Highlights (FLORA)

## LCLS-II Soft X-ray Detector

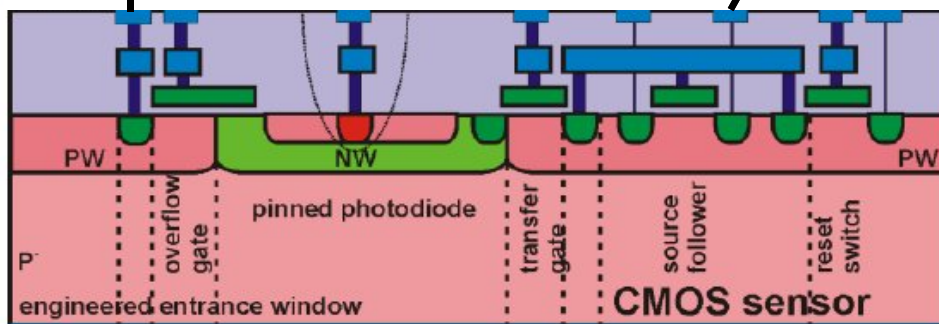
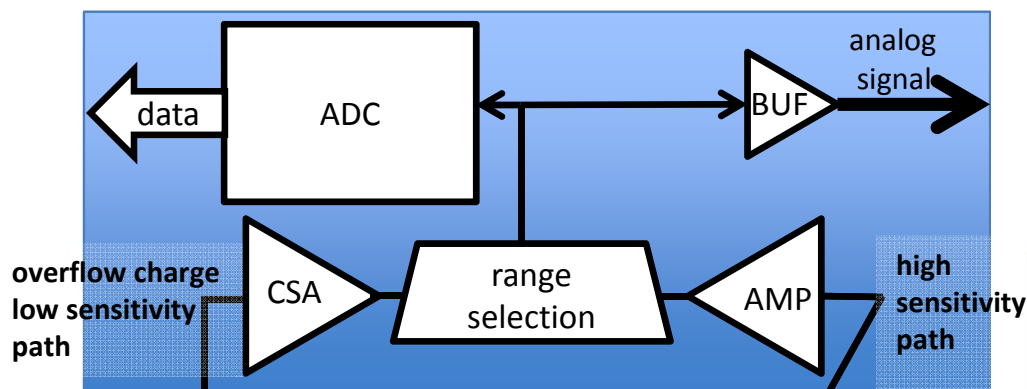
Coherent Imaging, Scattering and Diffraction; Inelastic Scattering Hybrid

FLORA: Fermilab-LCLS CMOS 3D-integrated detector with Autogain

CMOS detector with high dynamic and fast frame readout



4 pixels, mirrored vertically and horizontally forming 4 pixel island.



FLORA high level pixel schematics

### Soft X-ray: Low noise / high rate - Goals:

- noise 10 e<sup>-</sup> rms & high QE
- dynamic range ~10<sup>4</sup>: maximum signal ~500ke<sup>-</sup>/pixel/pulse
- 50 μm × 50 μm pixel size
- > 10,000 frame/s pixel detector

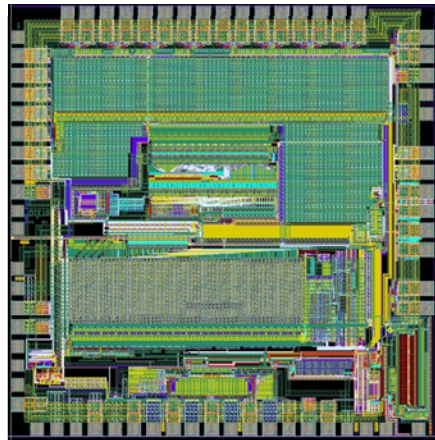
### Divide and conquer:

- CMOS Imager Sensor
  - high quantum efficiency and single photon resolution
- ROIC ASIC
  - Signal processing, dynamic range, fast readout

# Current Projects Highlights (QIE and FASPAX)

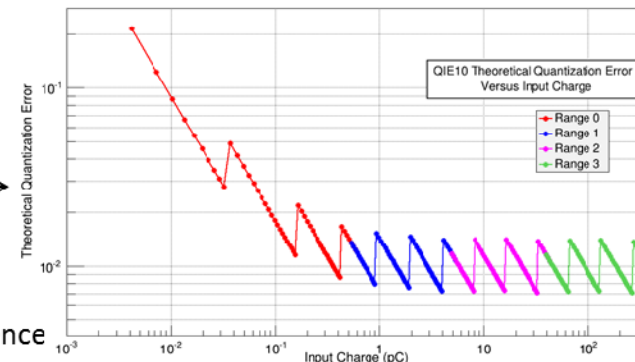
**QIE: a multi-decade development effort in high dynamic range floating-point readout chips for HEP**

**1989:** original idea (Bill Foster)   **1995:** QIE5 for KTeV   **1996:** QIE6 for CDF   **1997:** QIE6 for CDF   **2002:** QIE7 for MINOS  
**2003:** QIE8 for CMS   **2004:** QIE9 for BTeV   **2016:** QIE10 and QIE11 for CMS, QIE12 for ATLAS



**QIE10: a charge integrating, floating point digitizer for CMS**

- 40 MHz dead-timeless operation
- Very high dynamic range: 3 fC to 350 pC (~17 bits)
- Four ranges
- Pseudo-log ADC gives 4 sub-ranges in each range
- "Floating point" yields approx. constant resolution
- Programmable threshold TDC with 500 ps timing
- Many programmable parameters
- LVDS outputs
- Very successful development based on years of experience

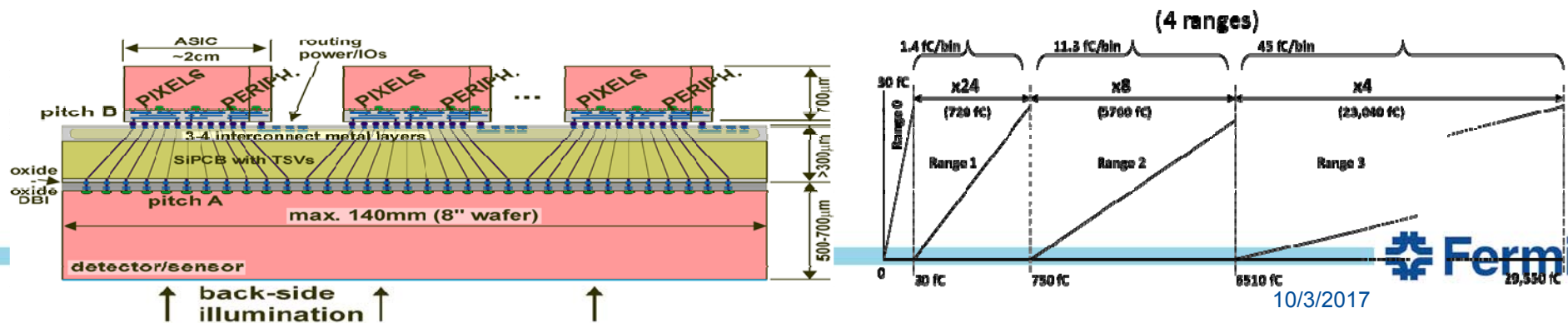


**2015 - 2017**

*Translate QIE experience to a dense pixel array application*

**FASPAX: a wafer scale X-ray camera of small pixels with unprecedented dynamic range**

Use QIE principles and experience to obtain a dynamic range of 10<sup>5</sup> in a 100u X 100u pixel



# Summary

---

- Demand for ASICs from DOE-HEP has varied from a local minimum a few years ago to high demand now,
- Aggregate demand for ASICs and projects flow have been steady keeping Fermilab ASIC Group occupied through the entire existence
- New projects on the plate are coming with new challenges:
  - Decanometric technologies,
  - High speed,
  - Complexity, multi-block designs, SoC (individual block = project for 1 FTE )
- Seen the list of projects, Fermilab ASIC Group:
  - Is open for Guest/Visitors also PhD students
  - Considers hiring ASIC designers
  - Works through collaborations

# Summary

---

- ASICs solve problems unsolvable otherwise and there is no experiment without at least one ASIC nowadays,
- Can DOE ASIC designs be contracted to industry? With a few exceptions NO, (market too small for industry, cost models based on industry have been explored and are expensive (too specialized for industry), some overlap with healthcare e.g. ADAS1256 Analog Devices' 256-Channel, 16-Bit Digital X-Ray Analog Front End Delivers Industry's Best Combination of Noise, Power and Image Quality)
- ASICs design is not cheap and it cannot be cheap, but what costs \$1M does not mean that it is expensive (absolute vs. relative scales) and be careful in making illusions:
  - CAD/EDA licenses cannot be free (Fermilab uses CAD/EDA support for an equivalent of 1FTE easily),
  - groups of 5-8 ASIC designers are not big, such group counts allow carrying one or two projects nowadays (decananometer technologies and many blocks on chip),

# Summary

---

- Attracting and retaining talented staff is a continuous challenge. Things, like:
  - access to professional development and to top professional experts around,
  - projects with scientific and design challenges not available elsewhere,
  - possibility of pursuing self-inspired research activities (Q: do you have budget code?),
  - conferences and workshops not always with a paper – e.g. ISSC+IEDM+ISCAS,
  - clear + well/established + unbureaucratized procedures for everyday needs,
  - proactiveness and facilitating approach in the laboratory structures (e.g. legal offices),
  - research platforms for PhD and post-docs with co-supervision,are very important in attracting ambitious and talented workforce.

- national laboratories have become not the first consideration for IC designers, (small number of applicants even in fellowships)
- Motivation, productivity and happiness come less with flexibility but more with quality infrastructure, low b-burden and systematicity

