1a

- Which parts of the ASIC design should be left to trained experts and which are important for keeping an innovative edge in the readout?
  - What are “trained experts”?
    - Very good experience with EE PhD students
      - During R&D phase evaluate both innovative & conservative options
      - Very good/fast at layout
      - Pull in supervisor’s expertise
    - Physicists (in many cases students and postdocs) make significant firmware contributions (especially in algorithmic parts)
      - Mixed experience
      - Not a big step to synthesizing this in a chip… but presumably only after have proven their skills
  - Experts become experts through training and experience…

1b

- How will we encourage collaborations to be formed between smaller institutions and national labs?
  - Phase-1 ATLAS upgrade ASICs:
    - LAr: ADC (Columbia), multiplexer-serializer (SMU)
    - Muon: VMM (BNL), TDS (Michigan)
  - No US national lab-university collaboration (some SBU EE students following GdG class contributed to VMM):
    - No shared blocks in VMM
    - But significant collaboration between university groups (Columbia-Michigan-SMU) and with CERN microelectronics group
      - » Value of having (national) labs build/coordinate common building blocks like I/O drivers, PLLs, serializers etc.
      - » Intrinsic benefit of centrally useful SoC like GBTx: many contributors coordinated by (national) lab
  - No outreach from national labs for DUNE ADC, even though significant university expertise

2

- How will we maintain the participation and meaningful review of the Experimental Physics community that drives the need for ASIC's?
  - ASICs where they have clear advantages
    - Functionality doesn't exist in COTS
    - Inhospitable environment precludes COTS (radiation, temperature, volume, power,…)
    - Cost (large number of channels)
    - Future similar application to which one of 3 above applies
      - Develop expertise
  - Don't do ASICs for the sake of doing ASICs
    - Bright future for FPGA-based systems in HEP (ATLAS upgrades have at least as many FPGA-based deliverables as ASIC-based)
      - More data to be processed off-detector fast (also true for DUNE, but not for ILC…)
    - FPGAs to dominate LHC improvements beyond 2024 (mainly trigger & DAQ)
    - Versatile designers: ASICs but also FPGA-based applications
      - Smaller groups have these, because they have to

3

- How will we invite and train new designers with a foot in both engineering and physics communities to become involved in future projects to renew our physics instrumentation ranks?
  - No home run solution
  - Build pipelines in groups strong in instrumentation
    - Hope some of the students passionate enough to stay
    - Can't compete with industry salary-wise
      - So compete by versatility of work (industry jobs have much narrower focus)
      - And our search for answers to big questions

4

- How should we document experience/lessons learned with new tools or PDK related DRC errors that require hours or even days to figure out to speed up design cycles and reduce labor costs.
  - Agree this is a BIG issue
  - If CERN can host a central page, that would be great
  - But:
    - "Easy" to say what didn't behave
    - Not always clear why
      - And therefore what else is at risk
      - Or if another issue has the same underlying cause