ASIC Developments at Columbia's Nevis Labs

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COLUMBIA UNIVERSITY
IN THE CITY OF NEW YORK

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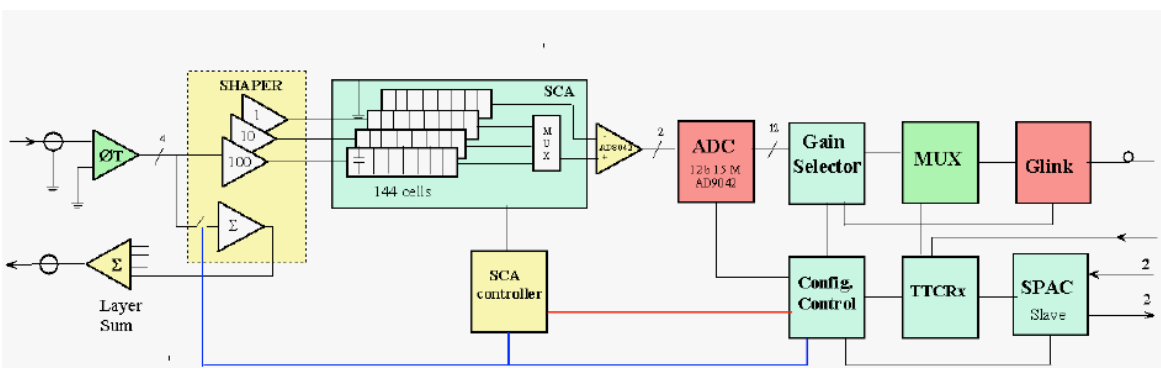
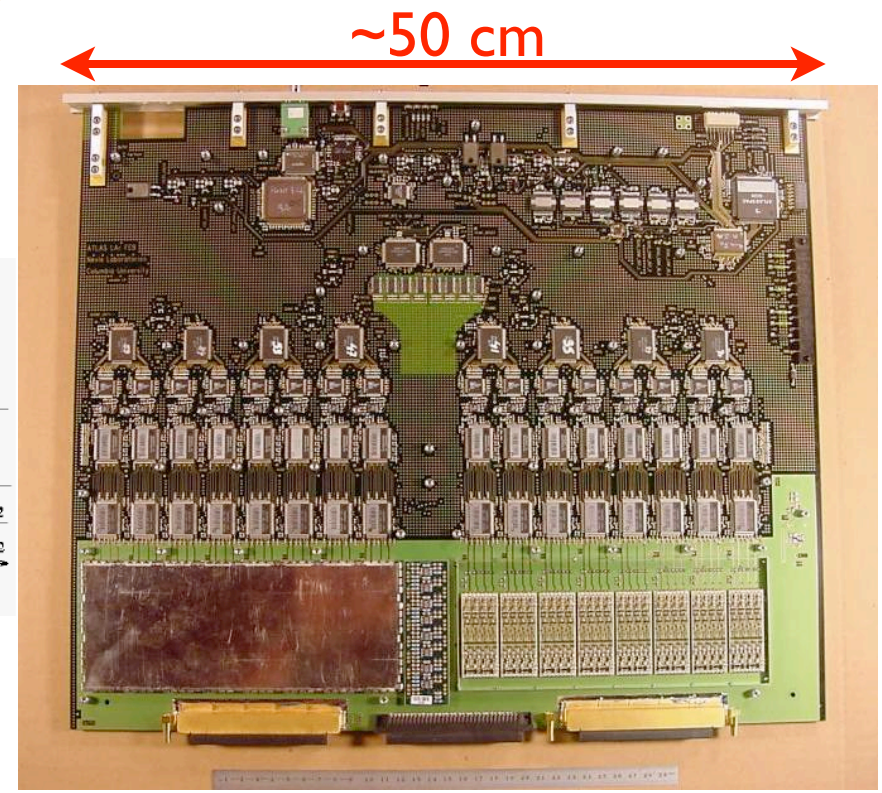
Outline

- LHC Original Construction
- Phase-I Upgrade
- HL-LHC Upgrade
- DUNE

LHC Construction

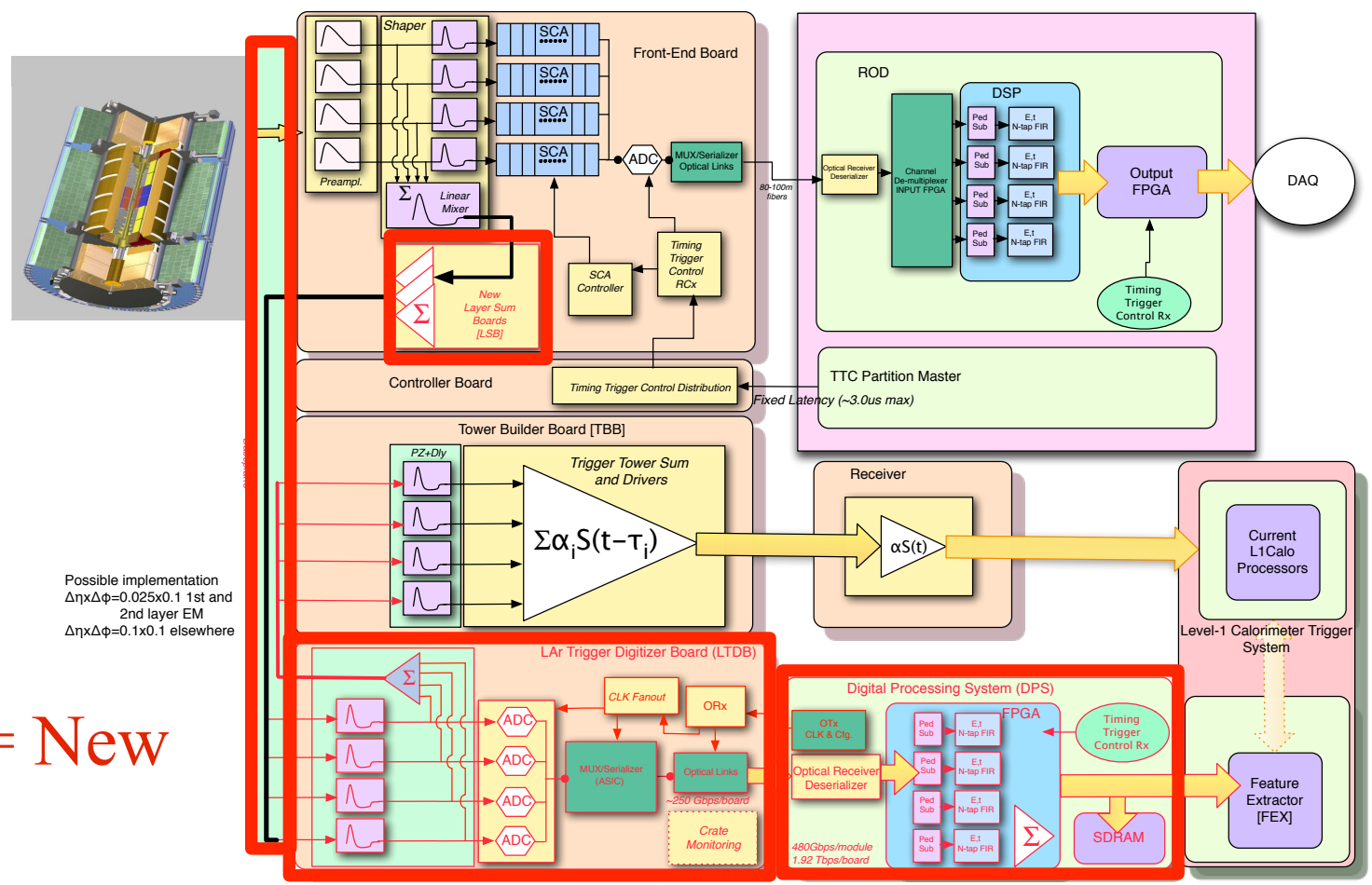
- Designed and built ~1600 LAr calorimeter front-end boards
  - Moderate radiation requirements ~100 kRad
  - Analog pipeline on-detector
  - 11 ASICs
    - Designed 5, including SCA pipeline





Phase-I Upgrade

- New trigger path readout for LAr calorimeter
  - Increase granularity
  - **Digitize at bunch-crossing rate and send all data off-detector**

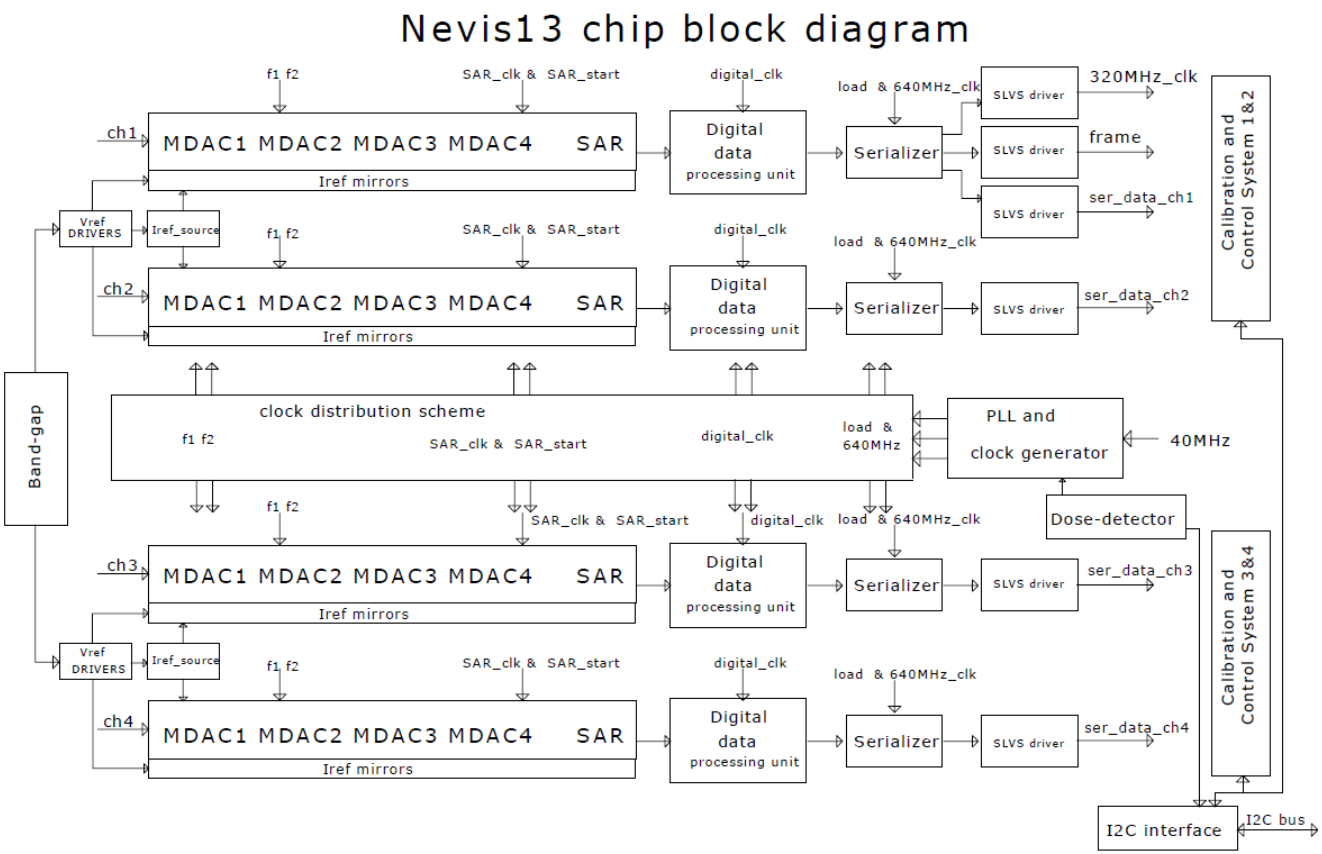


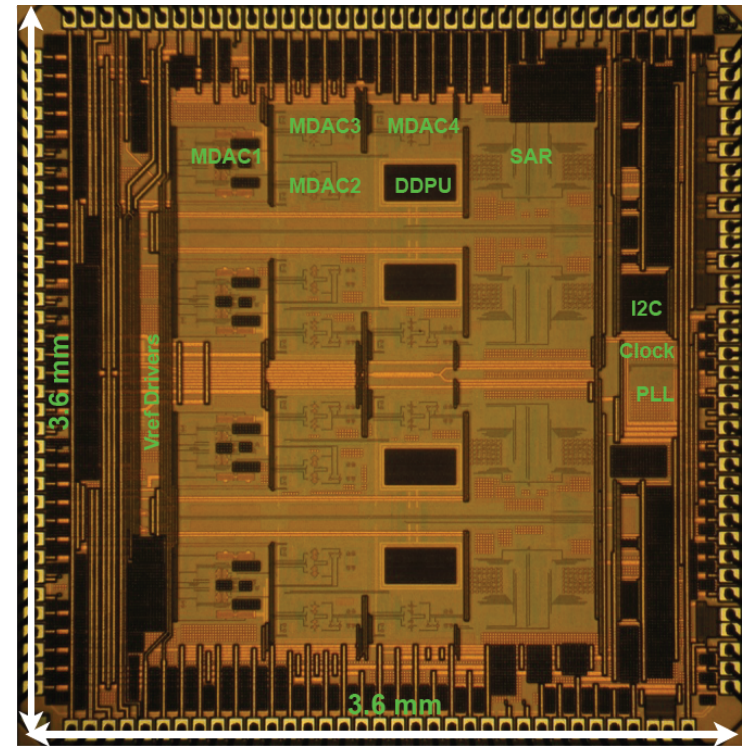
Red = New

Nevis ADC - Key Aspects

- Nevis ADC designed to fulfill Phase I upgrade requirements
  - Quad 12-bit ADC, 40 MSPS, ENOB ≥ 11, 50 mW/channel, ~100 ns latency
  - Semi-conservative design:
    - 4 most significant bits resolved using 4 x 1.5 bit pipeline
      - 12.5 ns/step
      - Digital error correction to compensate for technology's limited precision (cap matching)
      - Determining calibration takes ~1 s, correction applied on-chip
    - 8 least significant bits resolved by 8-bit SAR
      - All in 12.5 ns
      - Internal PLL generates 640 MHz clock from 40 MHz input clock (should work for input clock from ~20 to ~60 MHz, tested 20-42 MHz), SAR uses both edges, i.e. runs at 1.28 GHz
    - Outputs serialized over 320 MHz links (DDR)

Block Diagram

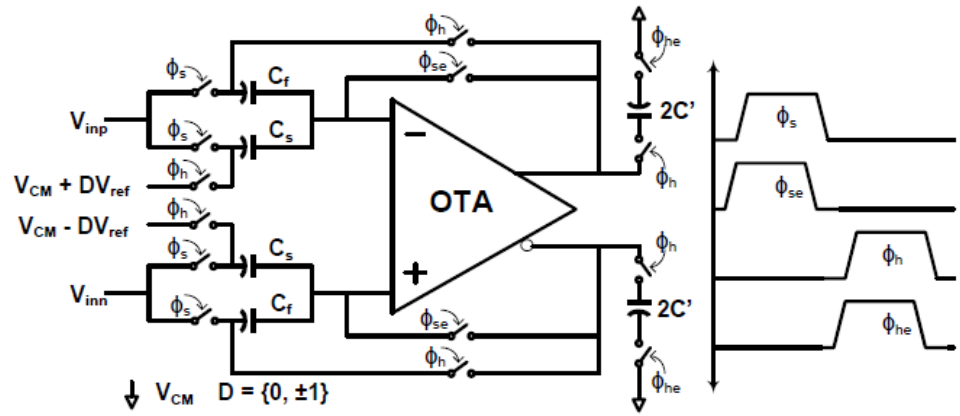


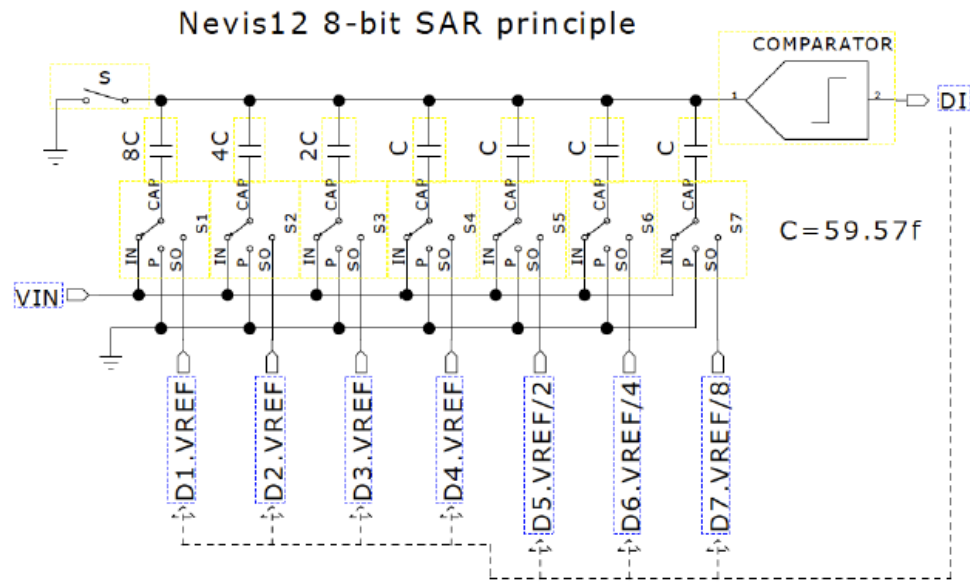


3.6 x 3.6 mm²
120 die pins
48 GND down-bonds
72 pin QFN package

Key Blocks

- MDAC
  - Developed over two test chips
  - Calibrate by forcing input voltage and decision
- SAR
- PLL
  - Adapted from CERN design (P. Moreira, K. Poltorak, A. Kluge)
- Clock generator
- V_{ref} driver
- DDPU
  - Sums results and applies calibration





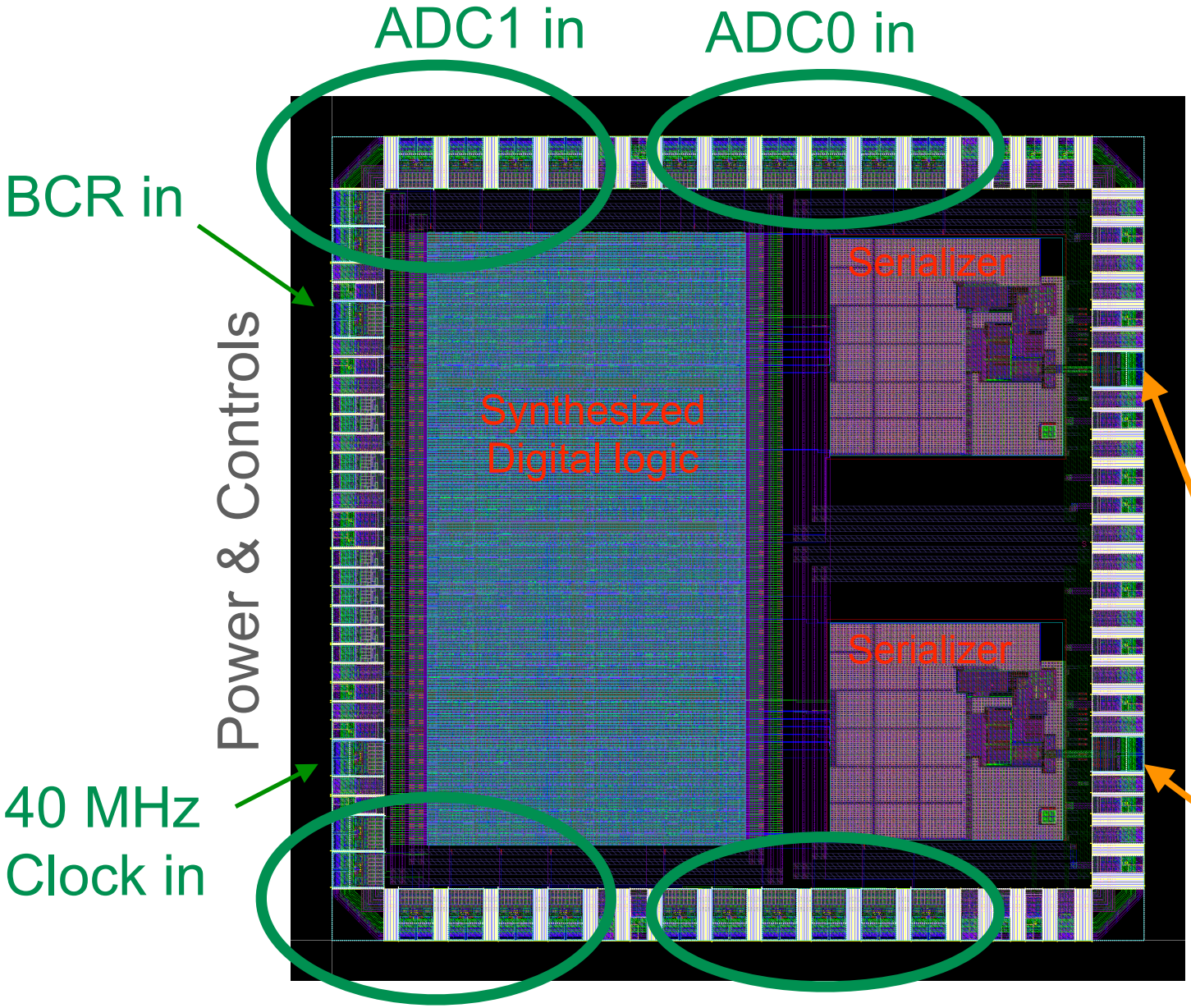
Current Status

- Achieved
  - 11.8-bit dynamic range (small loss to enable calibration)
  - 10.8 ENOB
  - 45 mW/channel
  - ~100 ns latency
- Production about to be launched
  - 10k chips needed

LArTDS

- Multiplexer/serializer chip (fall-back for LOCx2)
  - Take data from 4 ADC chips (16 channels), multiplex on 2 x 4.8 Gbps out
- Take high speed building blocks from TDS (serializer, PLL, output drivers); add digital front-end; add all the plumbing
  - Muon TDS chip
    - For TDS, Michigan converted GBTx serializer to 8RF-DM, and start at 160 MHz
      - Fewer multiplexer stages: reduced power and latency
  - Architecture
    - Receivers deserialize ADC data
    - Digital logic to build frame, incl. BCID, scramble, …
      - Synthesized
    - Feed into TDS serializer, output drivers

Chip



3460 x 3428 mm²

Digital logic block ~65% "full"

Synchronization

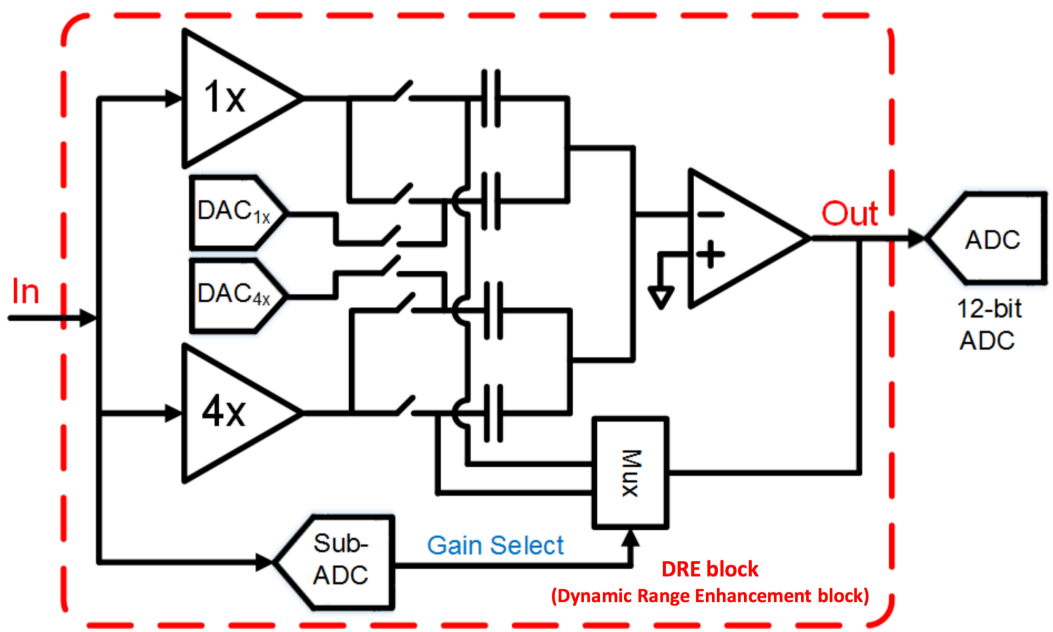
- Three clock domains:
  - 2 ADC 320 MHz clocks (derived from 40 MHz collision clock to ADC)
  - 1 serializer 160 MHz clock (derived from 40 MHz collision clock to LArTDS)
  - Fixed but unknown phases between each 320 MHz and 160 MHz
- Data from ADC into deserializer register (320 MHz DDR/640 Mbps)
- On frame, transfer (12 bits) to parallel register (320 MHz ADC clock)
  - There, data "safe" for 25 ns (but actually stay < 5 ns)
- Signal to transfer to transmitter input (160 MHz serializer clock)
  - 6.25 ns pulse derived from 160 MHz clock and BCR (through register flags)
  - Can shift that pulse to any of 4 places in 40 MHz clock (I2C setting)
  - Monitor outputs to check which setting is best (no metastability, lowest latency)
- Chip latency: [25 ns (deserialize - shouldn't double count with ADC!) +] ~3 ns (transfer) + 6.25 ns (encoding) + 6.25 ns (to serializer) + 25 ns (serialize 4 words - don't double count in FPGA) = ~40 ns

Current Status

- Prototype meets all specs
  - (Compiler dropped activation of termination resistors on one side, fixed for production)
- Production about to be launched
  - 2.5k chips needed

HL-LHC Upgrade

- Now need 14-bit dynamic range ADC, still 11 ENOB
  - Switch to 65 nm
    - Faster, can do 12-bit SAR (being developed by UT Austin, see Tim's talk)
  - In front of SAR, "dynamic range enhancer"



First test chip just back
Testing underway

DUNE

- DUNE needs an ADC
  - Located in LAr
  - Sample at 2 MSPS
- Baseline is new LBNL-BNL-FNAL development
  - Columbia designs could be good fallback
    - Plan to test both 65 and 130 nm designs in cryogenic environment

Summary

- Columbia ASIC developments mostly in ADC area in past decade
  - Challenging, but successful
- Benefitted extensively from work done on other chips
  - Often modified designs somewhat, but still a lot of effort gained
    - SLVS I/O
    - Bandgap
    - PLL
    - I2C slave
    - GBTx/TDS serializer
    - …
- Planning to continue in this direction in the next ~4 years at least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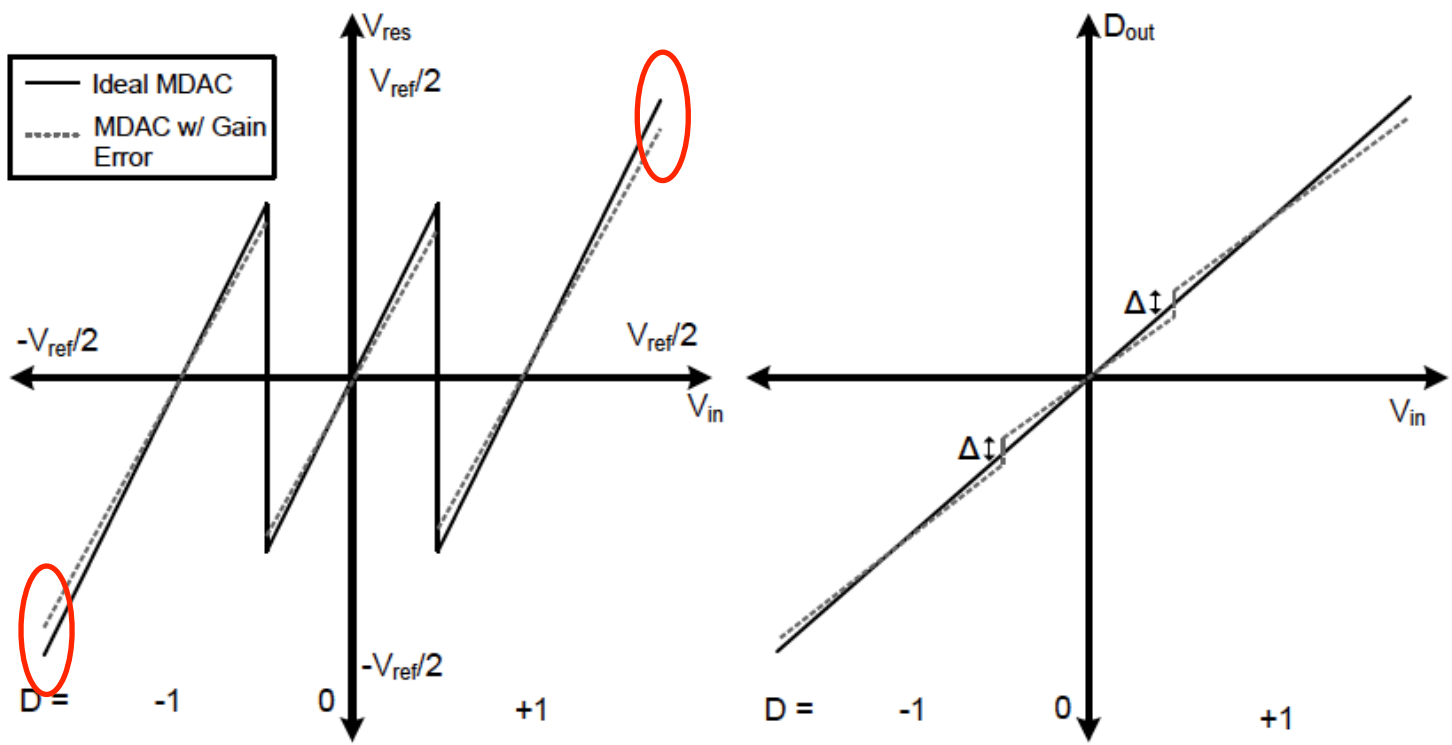
ATLAS

Dynamic Range

- Pipeline MDAC stages have gain < 2
  - Cannot correct for capacitor mismatch if > 2
    - So do not correct for parasitic capacitance
  - At the price of reduced dynamic range: 11.85 bits (3700 counts) instead of 12 bits (4096 counts)



LArTDS Frame

- TDS uses 120-bit frame (broken up in 4x30 bits “words”)
  - LArTDS frame:

header 1100	4 bit BC Flag	4 bit BCID ADC12	ADC 12 data 48 bits	4 bit BCID ADC34	ADC 34 data 48 bits	8 bit parity

- Header is unscrambled
- BC flag indicates whether first (1000), last (0100) or other BC (00xx)
- 2x4 bits of BCID: one for each ADC chip
- 8-bit parity (rather than CRC):
  - One bit per ADC channel, calculated while deserializing ADC data
    - Calculated immediately, so covers full time in chip
    - No latency penalty
    - Better than CRC as allows to flag which channel has bit flip