VLSI for Physics!

Stuart Kleinfelder
Electrical Engineering and Computer Science
University of California, Irvine

New Solid State Devices for HEP - 1985

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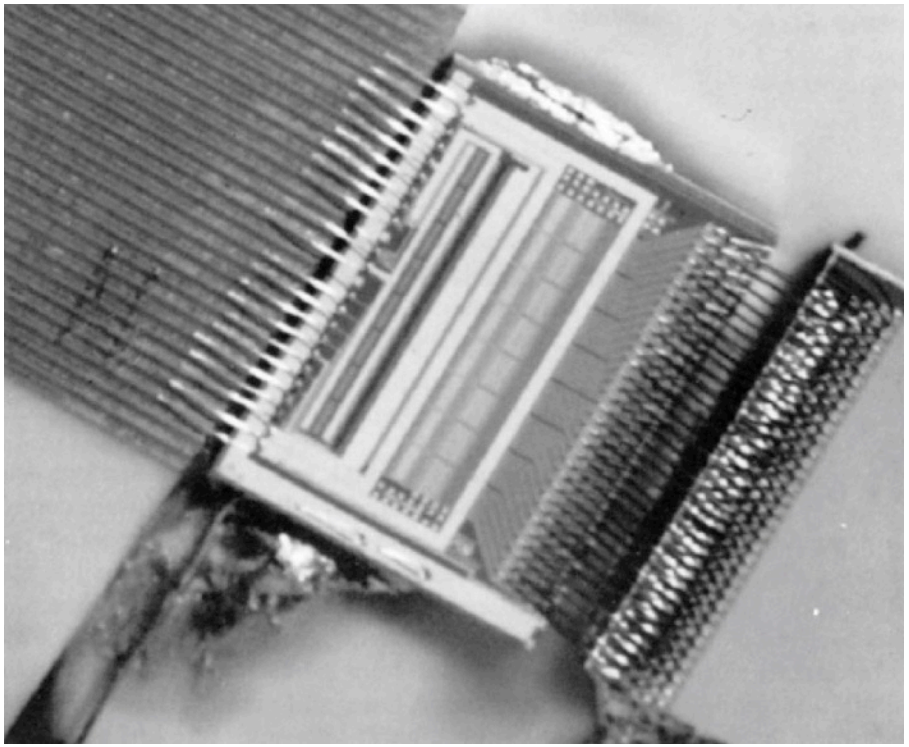
VLSI for Physics

Stuart A. Kleinfelder
Physics Division, Lawrence Berkeley Laboratory
Berkeley, CA. 94720 USA

From silicon detectors to super colliders, physicists need VLSI. Institutions and collaborations now recognize the feasibility and power of custom and semi-custom integration. Novel application specific architectures expressed in VLSI allow tremendous gains in speed and efficiency over systems of commercial components. An example of the flexibility of this medium is

The Beginnings: Stanford / SLAC ‘84-85

- ASIC technology was “accessible” but little experience evident.
- Stanford / SLAC’s NMOS Microplex (left) and Microstore (right) chips were two − perhaps the only two − examples at the time.
  - Walker, Parker, Hyams, Shapiro, “Development of High Density Readout for Silicon Strip Detectors,” NIM 226 (1984).
  - Walker, Chae, Shapiro, Larsen, “Microstore − the Stanford Analog Memory Unit,” IEEE TNS NS-32, No 1. Feb. 1985.



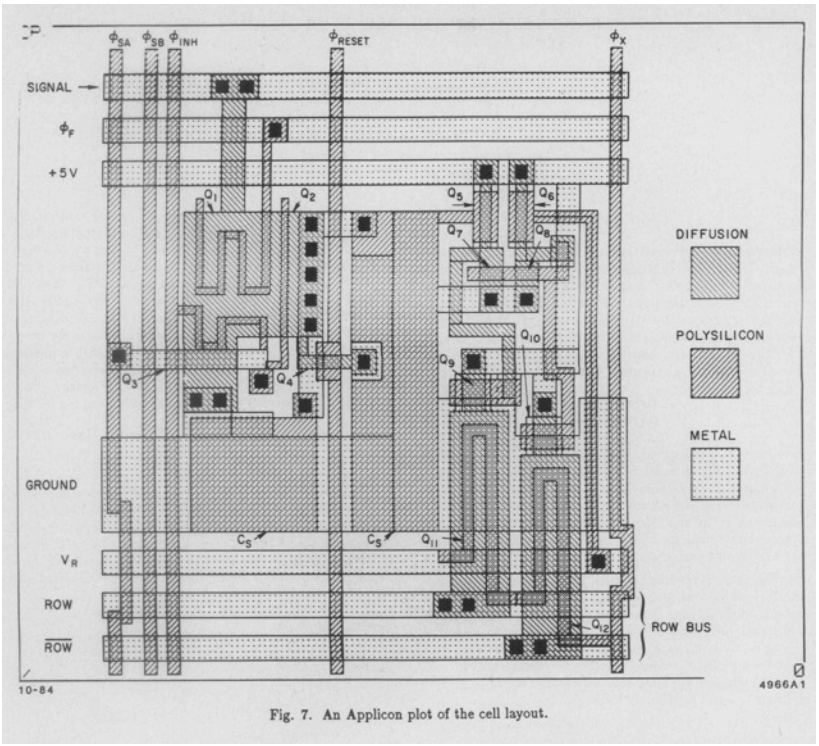
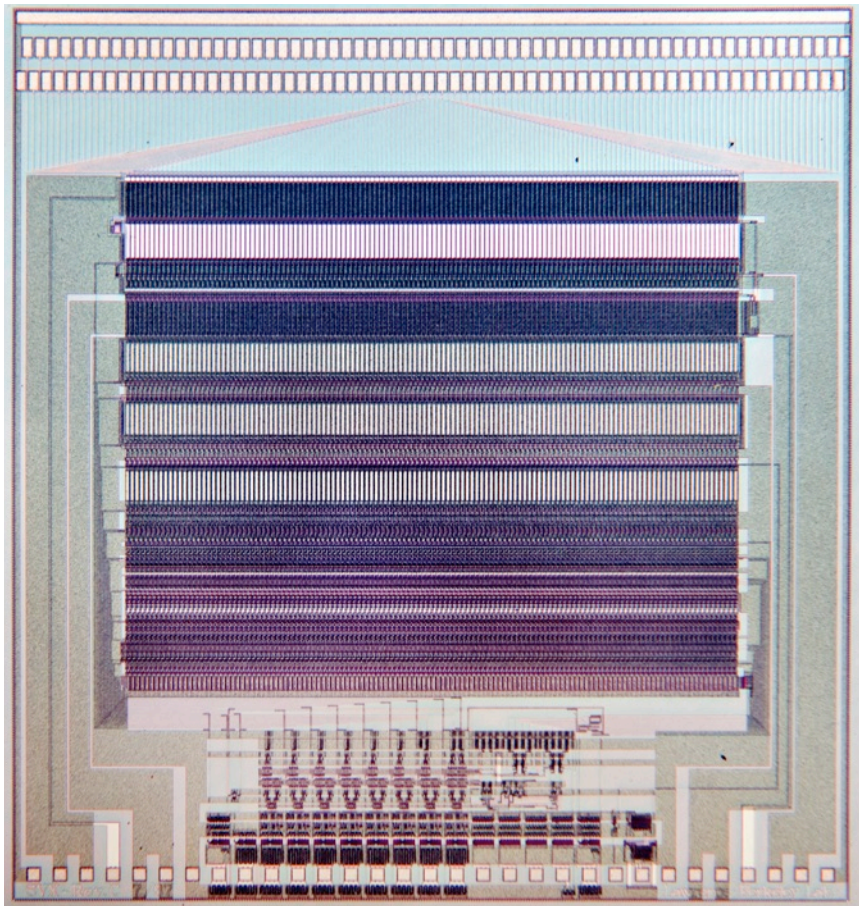
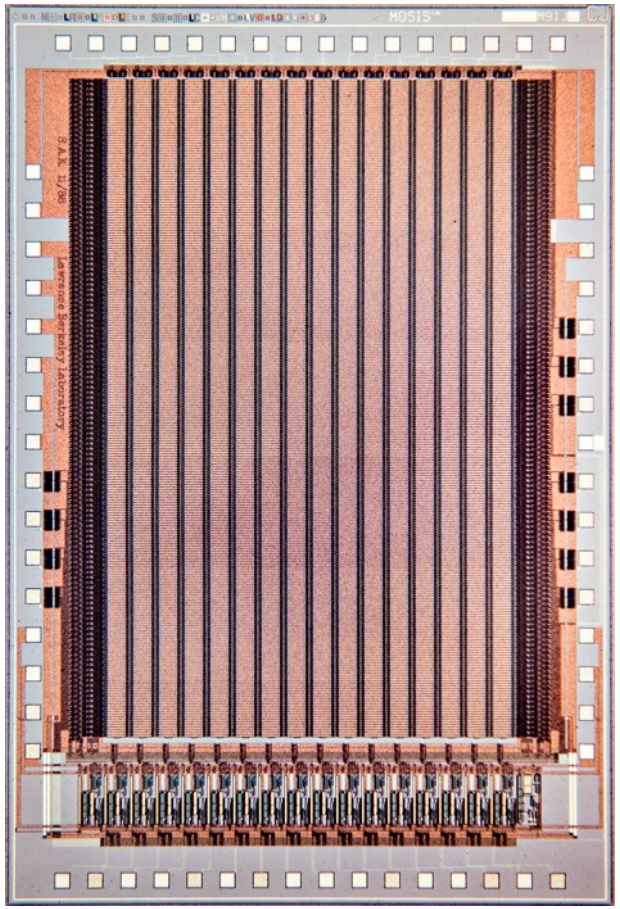


Fig. 7. An Applicon plot of the cell layout.

“Good artists copy, great artists steal.”

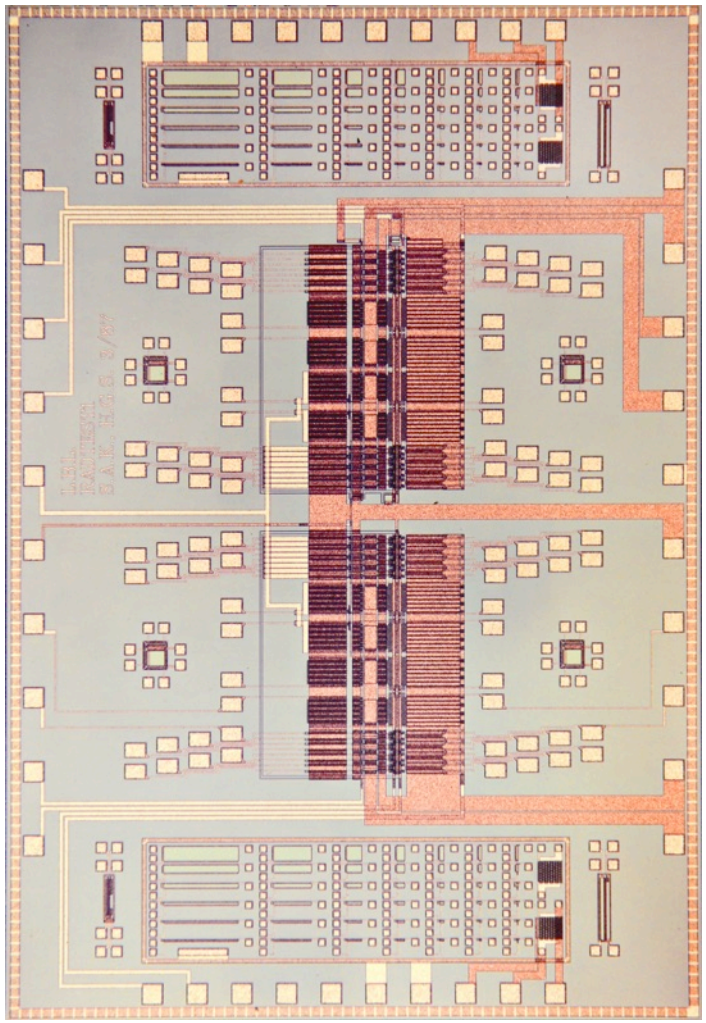
- The SVX chip was likely the first CMOS ASIC for physics. It offered improved amplification, auto-zeroed offset and leakage, sparse data scanning + nearest-neighbor logic, etc. (Kleinfelder, 1988).
- The SCA Switched Capacitor Array introduced a DRAM-like architecture for high density and low power, with rail-to-rail operation (Kleinfelder, 1988).

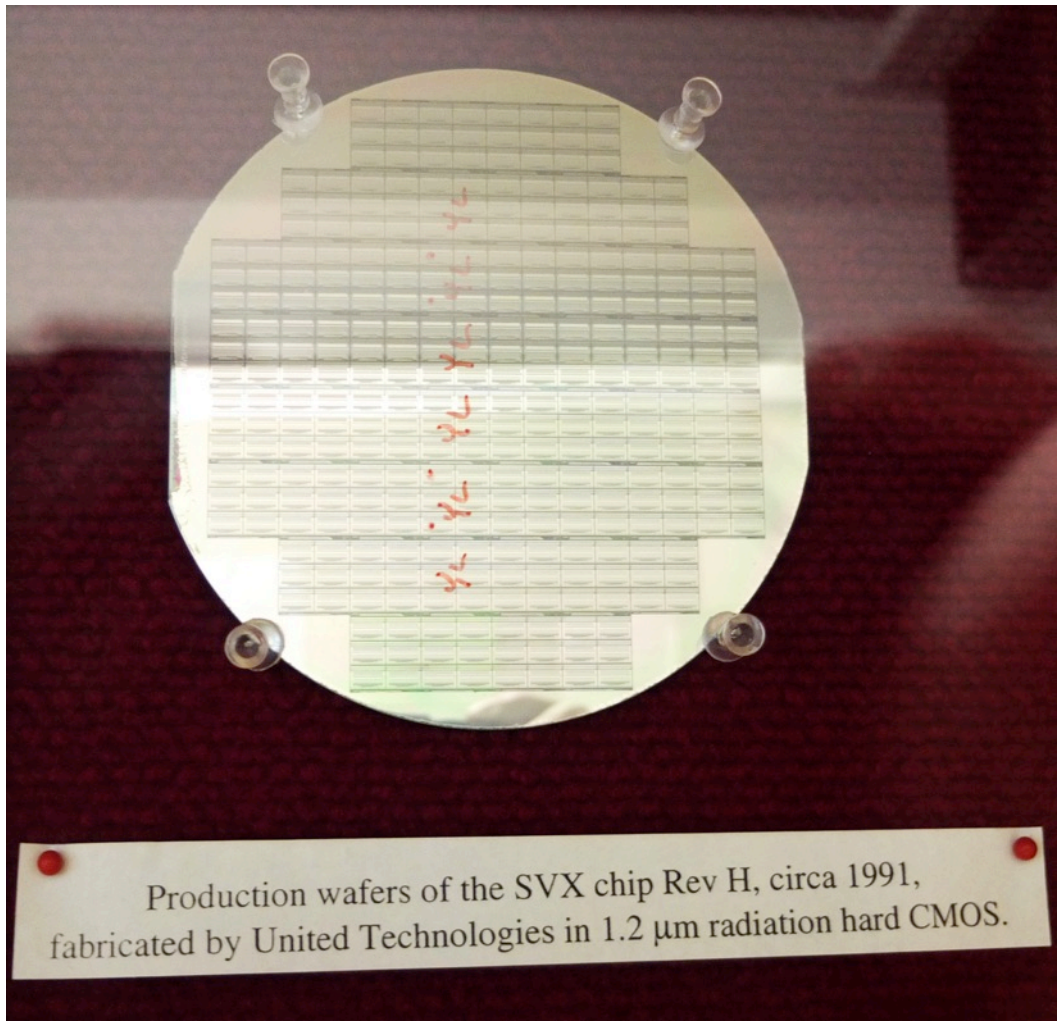




But is it Radiation-Hard?

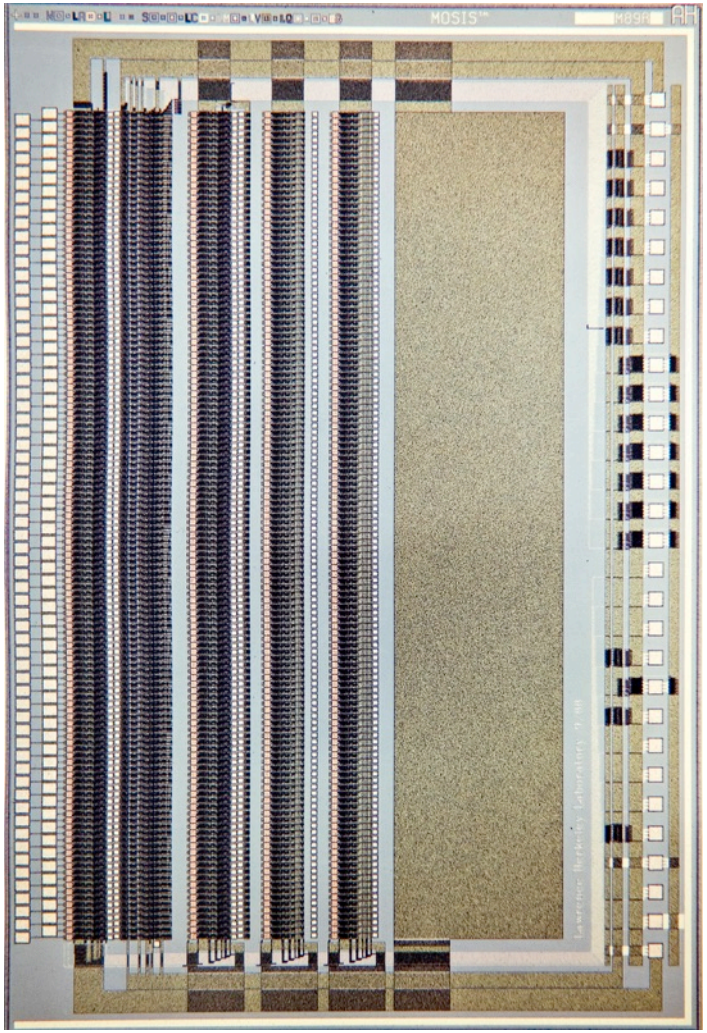
- Radiation hardness was recognized as a problem: SVX-based "Radtest1" chip (Kleinfelder, 1988), used in radiation studies.
- First rad-hard physics ASIC: SVX-h, right (Kleinfelder, 1991).

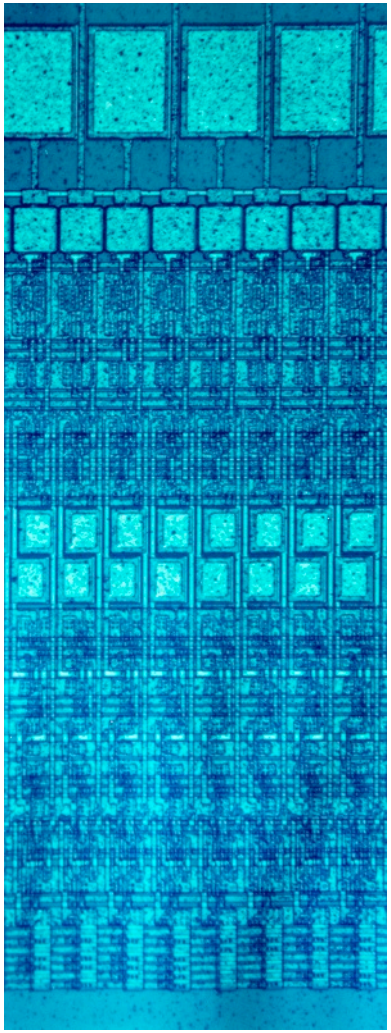


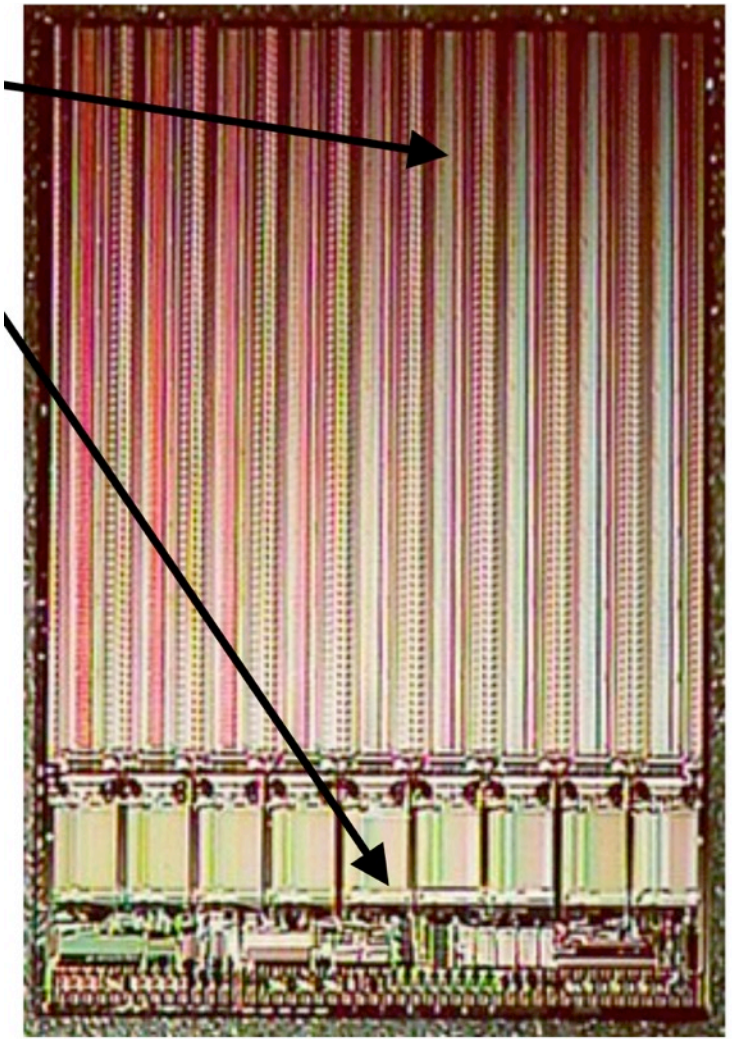


Strips to Pixels

- LBL's first pixel detector prototype chip, with column-oriented sparse-data readout and pixel array close-up (Kleinfelder, 1988).
- ATLAS pixel detector prototype, right.

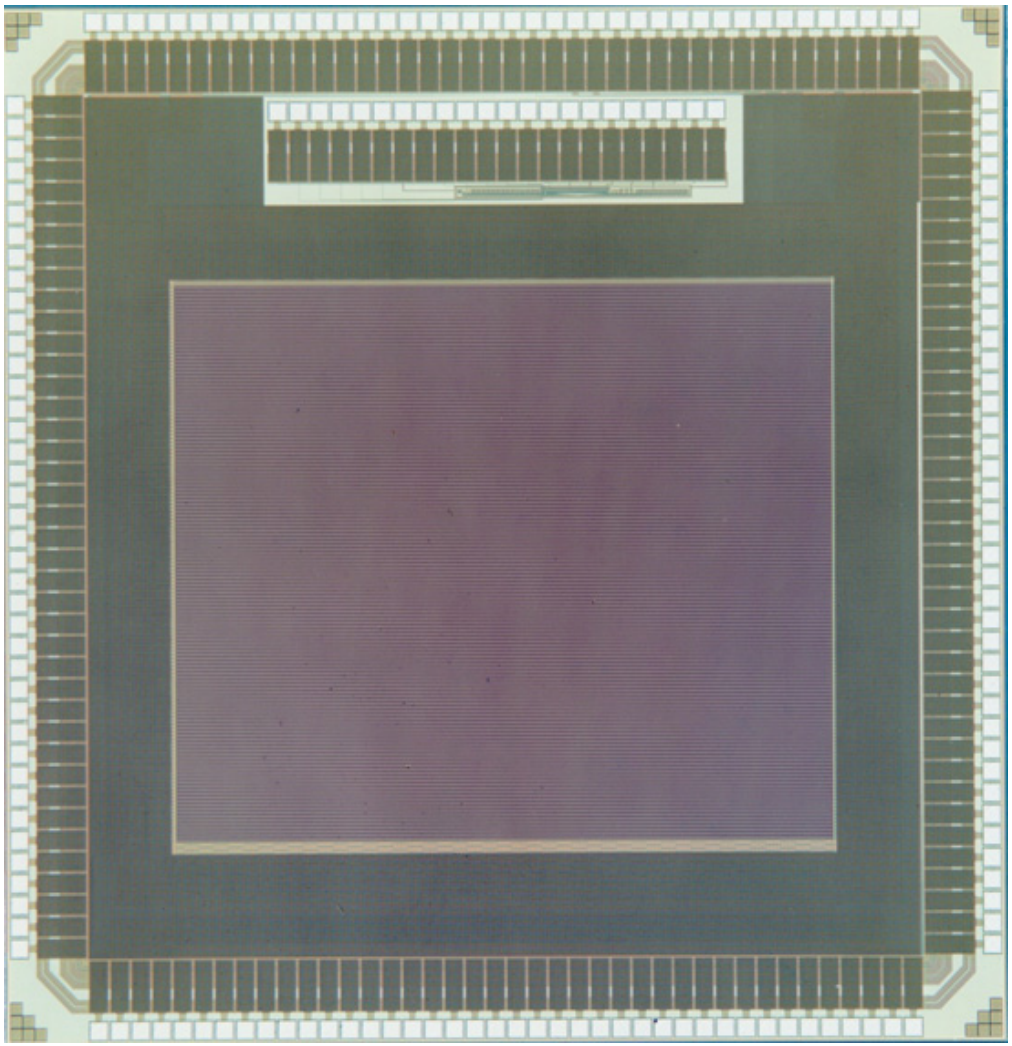


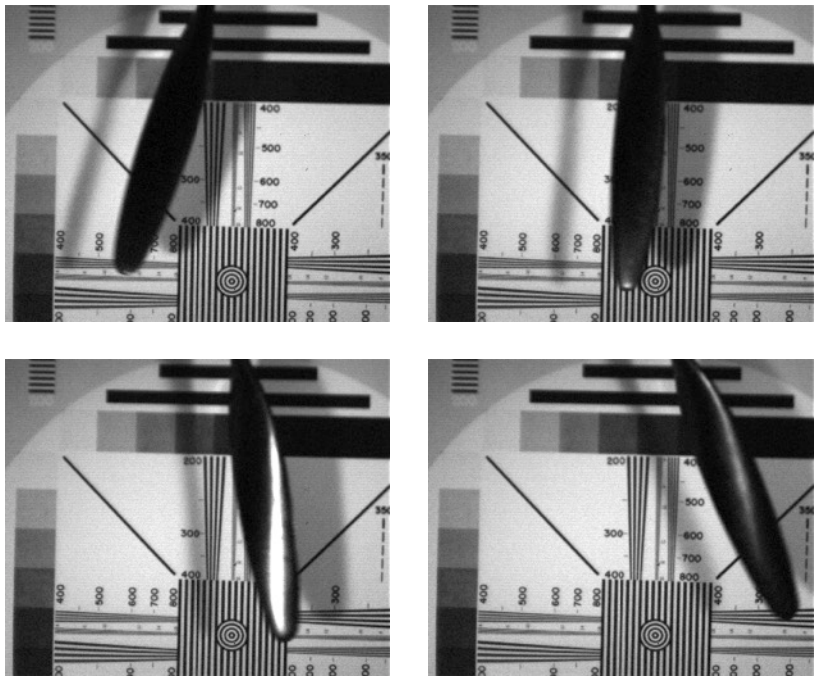




DPS: Pixels get Faster.

- The first full “Digital Pixel Sensor,” (Kleinfelder, et al., 2001).
- 10 times faster than prior reported digital cameras: 10,000 fps.

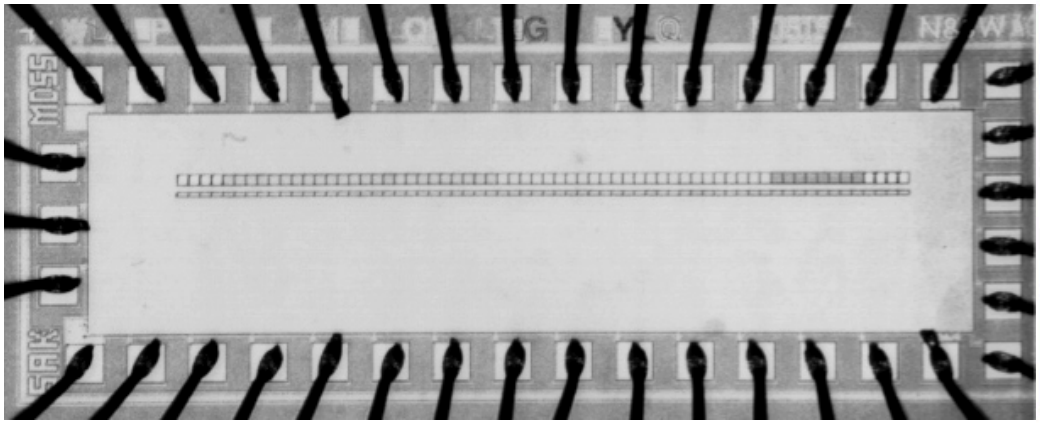




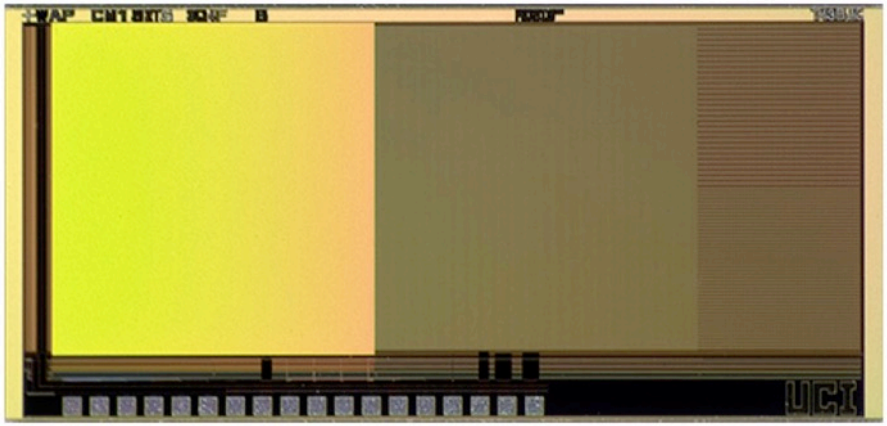
Every 10th frame at 10k fps

- Complete ADC/pixel.
- Parallel 64-bit readout.
- 9 μm pixels in 0.18 μm.

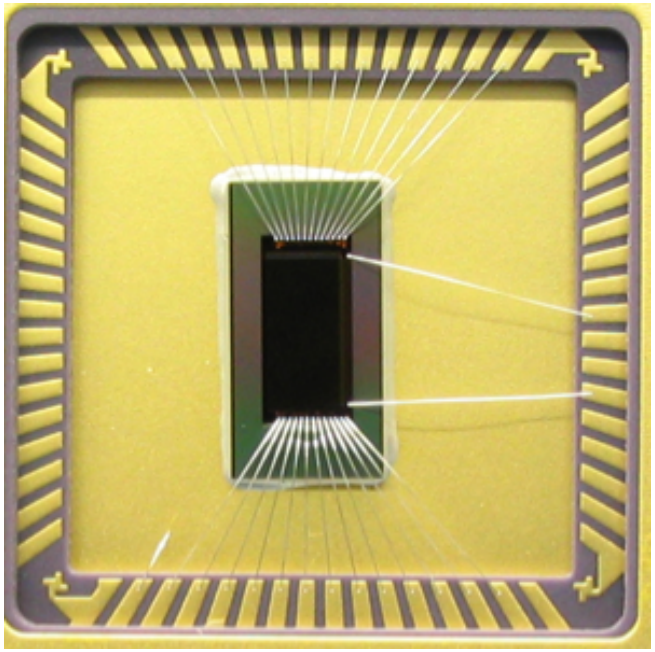
More and More Pixels

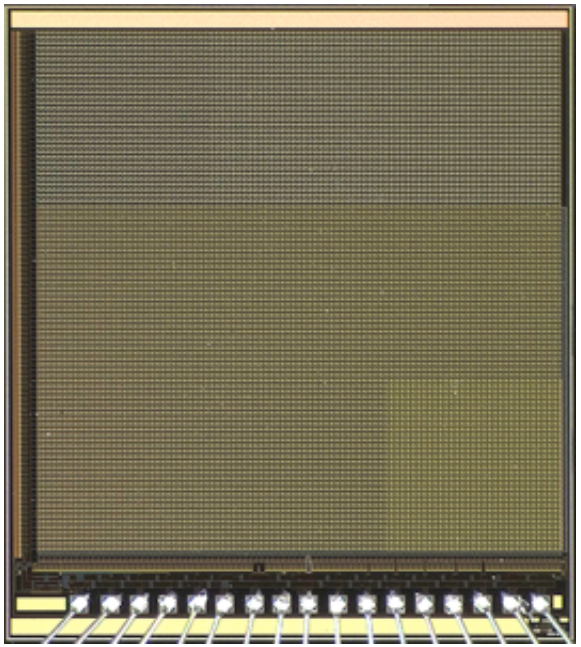


DPS for I.R. test chip.

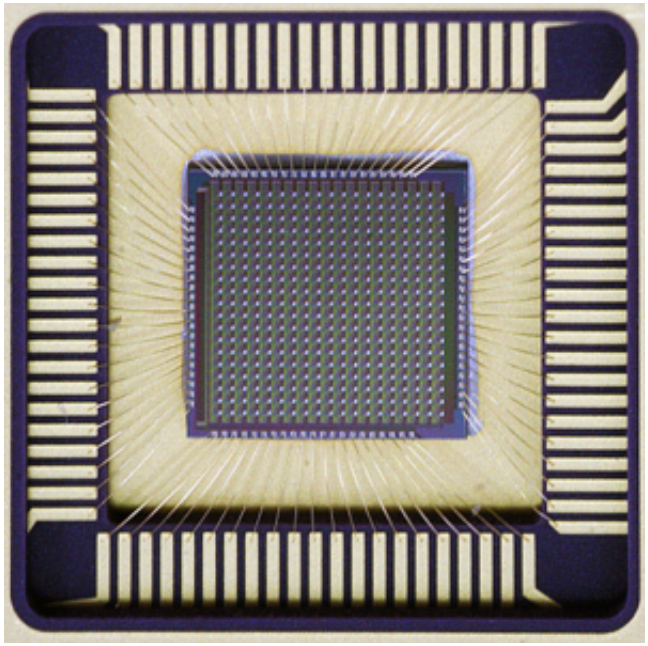


Monolithic APS test chip.



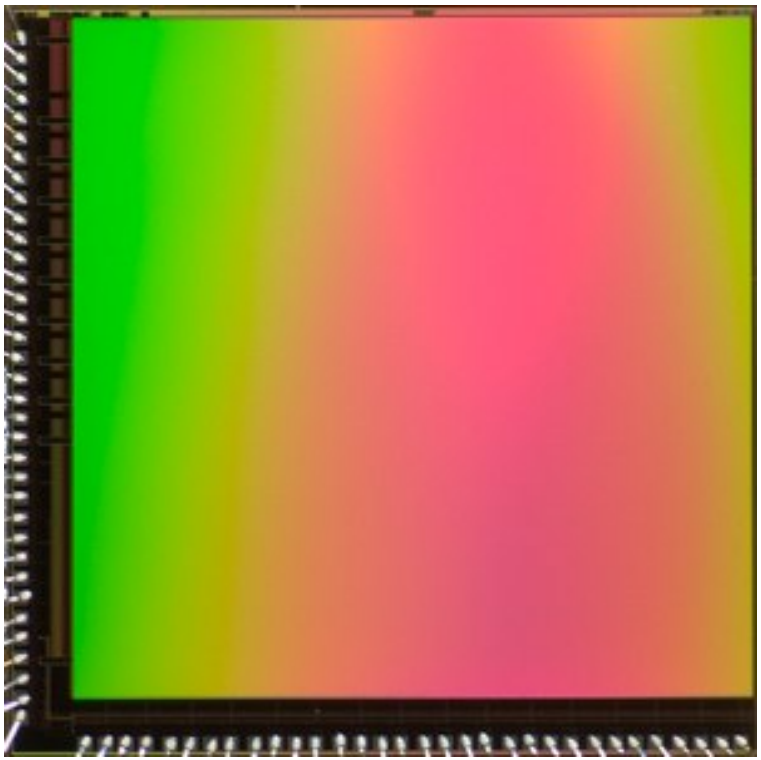


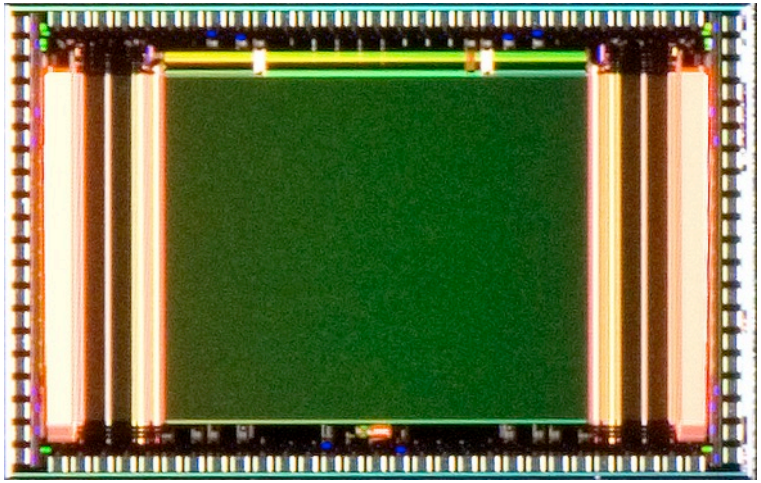
400 MHz “streak” (line sensor) camera.

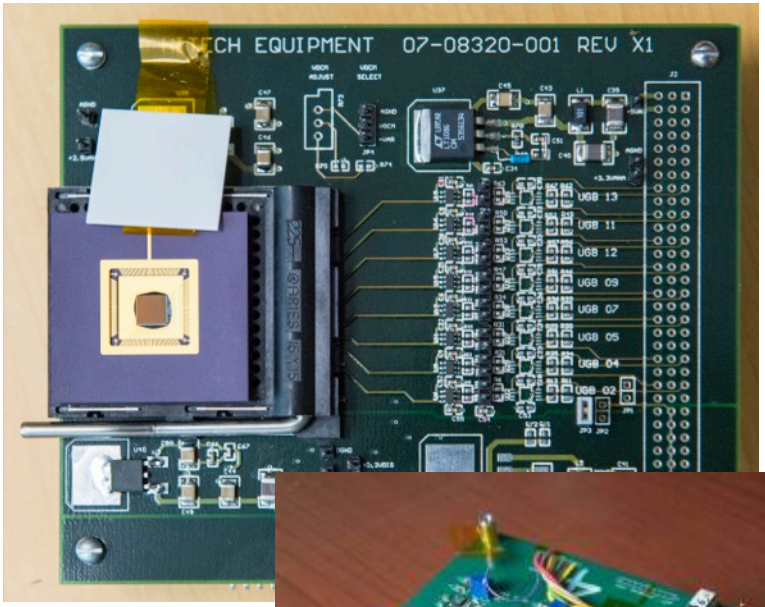


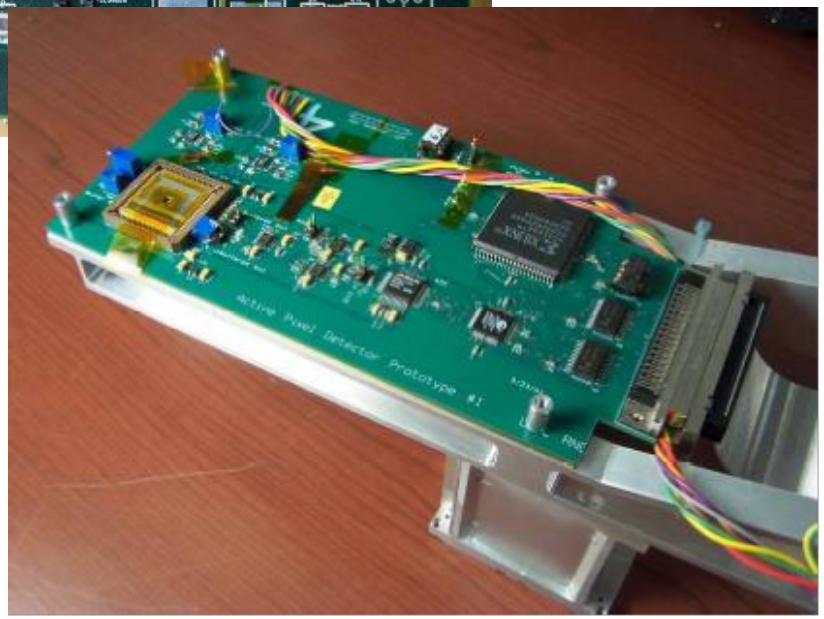
Ever more chips...

Direct Imaging for Electron Microscopes



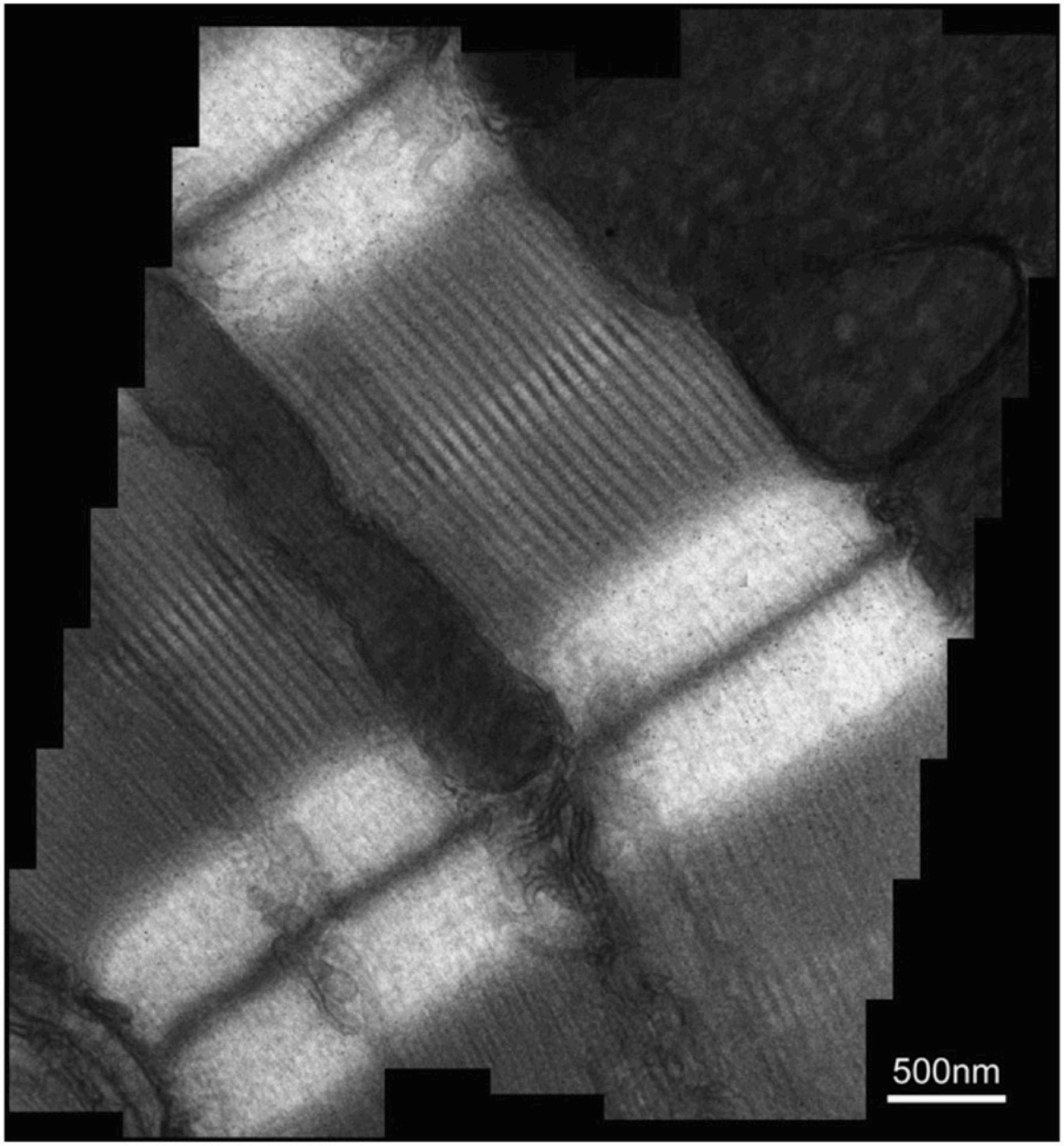


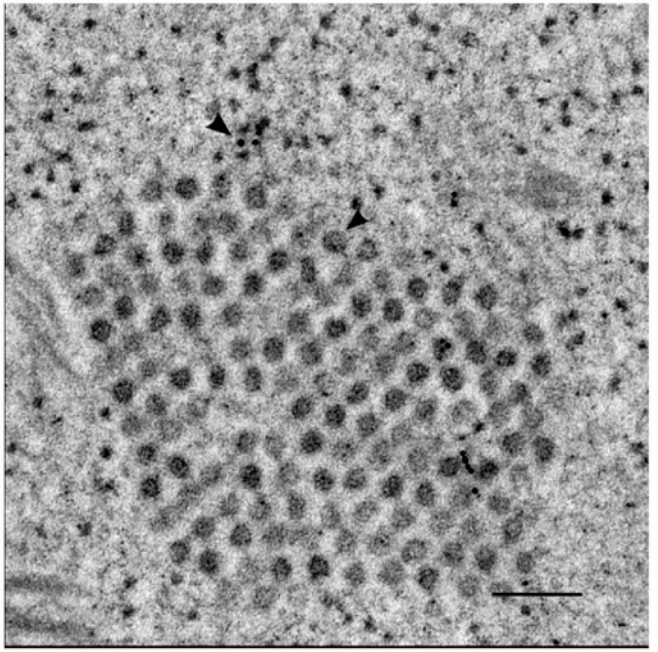


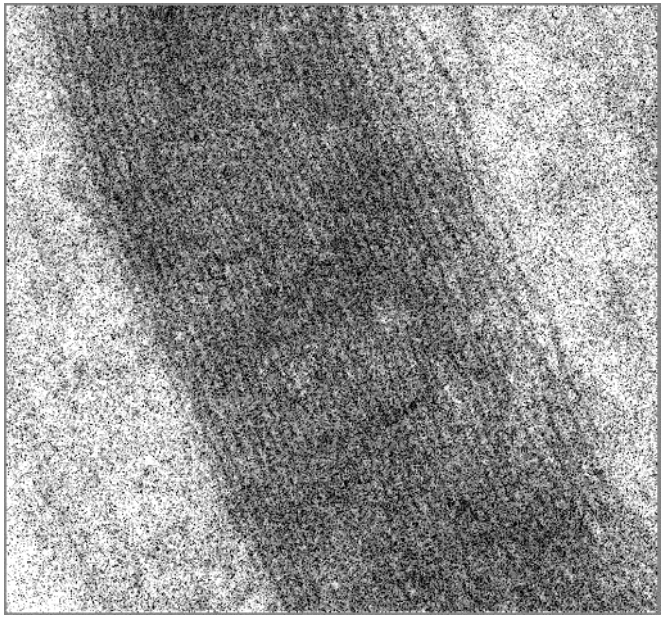


Upper left: 1 M-pixel APS, 5 μm pixels.
Left: APS with column-parallel ADCs.

Direct Imaging for Electron Microscopes



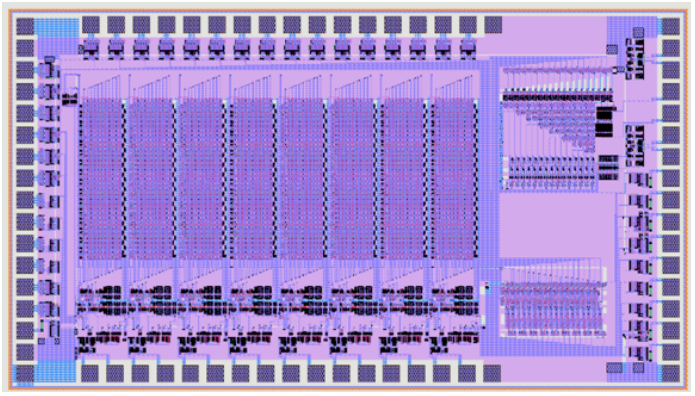




Stuart Kleinfelder, U.C. Irvine

First Complete Fast Timing ASIC

- R&D-100 award-winning “MTD-132” (Kleinfelder, et al., 1991).
- 8 channels, 16 hits/channel.
- 16-bit resolution with 0.5 ns LSB.
- Automatic stale data deletion.
- 1.2 micron CMOS
- But waveform recording came next



IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 38, NO. 2, APRIL 1991

MTD132 - A New Sub-Nanosecond Multi-hit CMOS Time-to-Digital Converter

Stuart Kleinfelder, T. J. Majors, K. A. Blumer, W. Farr, and Ben Manor
LeCroy Corporation, 700 Chestnut Ridge Rd., Chestnut Ridge, N. Y. 10977

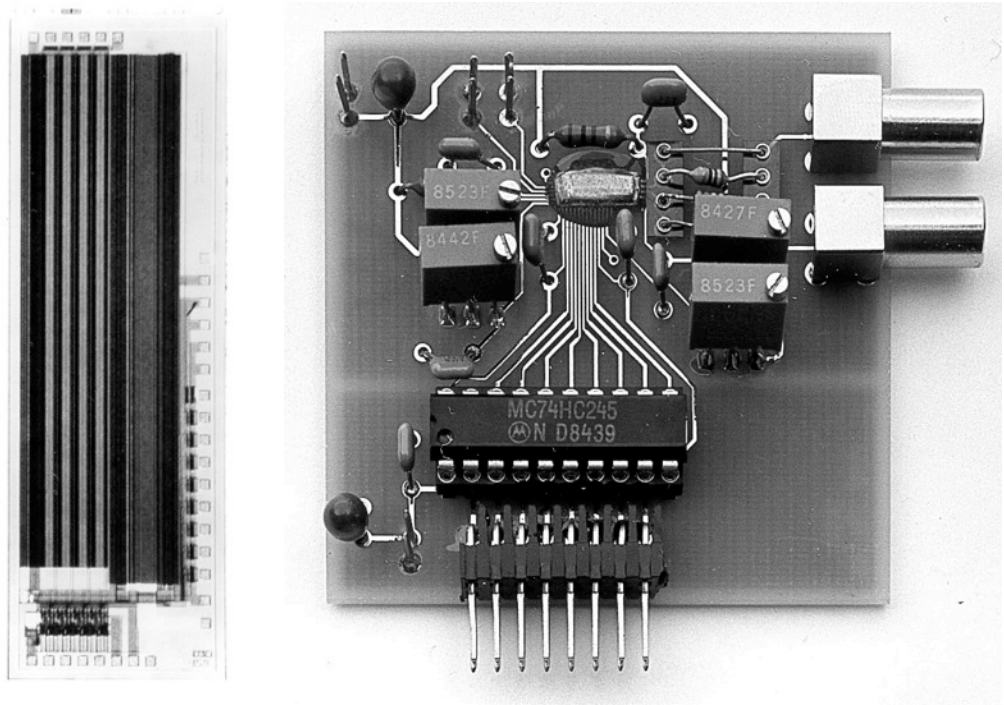
Abstract

A new 8 channel, 16 hit, sub-nanosecond resolution, 16 bit dynamic range time-to-digital VLSI CMOS circuit is described. It can operate in either common start or common stop mode and records either leading, trailing, or both input edges. Double pulse resolution is 15 ns. Readout is sparsified, and input signal levels are ECL while control and output levels are CMOS. Measured performance of prototype devices is presented. A CAMAC and a FASTBUS TDC board using this chip are under development.

difference between a common input, either common start or common stop, and individual inputs without adding pedestal.

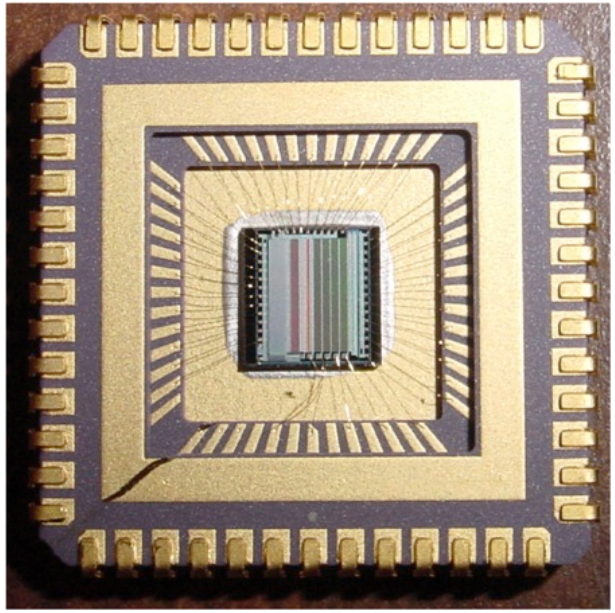
The MTD132 uses the idea of interpolating between the LSBs of a coarse digital counter to increase resolution [5], implemented in a full custom CMOS integrated circuit. The basic concept of the MTD132 is a continuously running coarse counter clocked by an external bi-phase clock in conjunction with an interpolator of two bits interpolating between coarse counter LSBs. The output of these is distributed to 8 channel memories which independently latch the count value at the time of an input pulse. Similarly their output value at the time of the common

SCA to ATWR to ATWD: IceCube, etc.



Advanced Transient Waveform Recorder (Kleinfelder, 1992)

- First multi-GHz Switched Capacitor Array.
- 5 G-samples/s acquisition speed,
- 4 Channels of 512 samples/channel.
- 1.2 μm 2-metal CMOS.
- 350+ MHz B.W.
- 11+ bits RMS dynamic range.



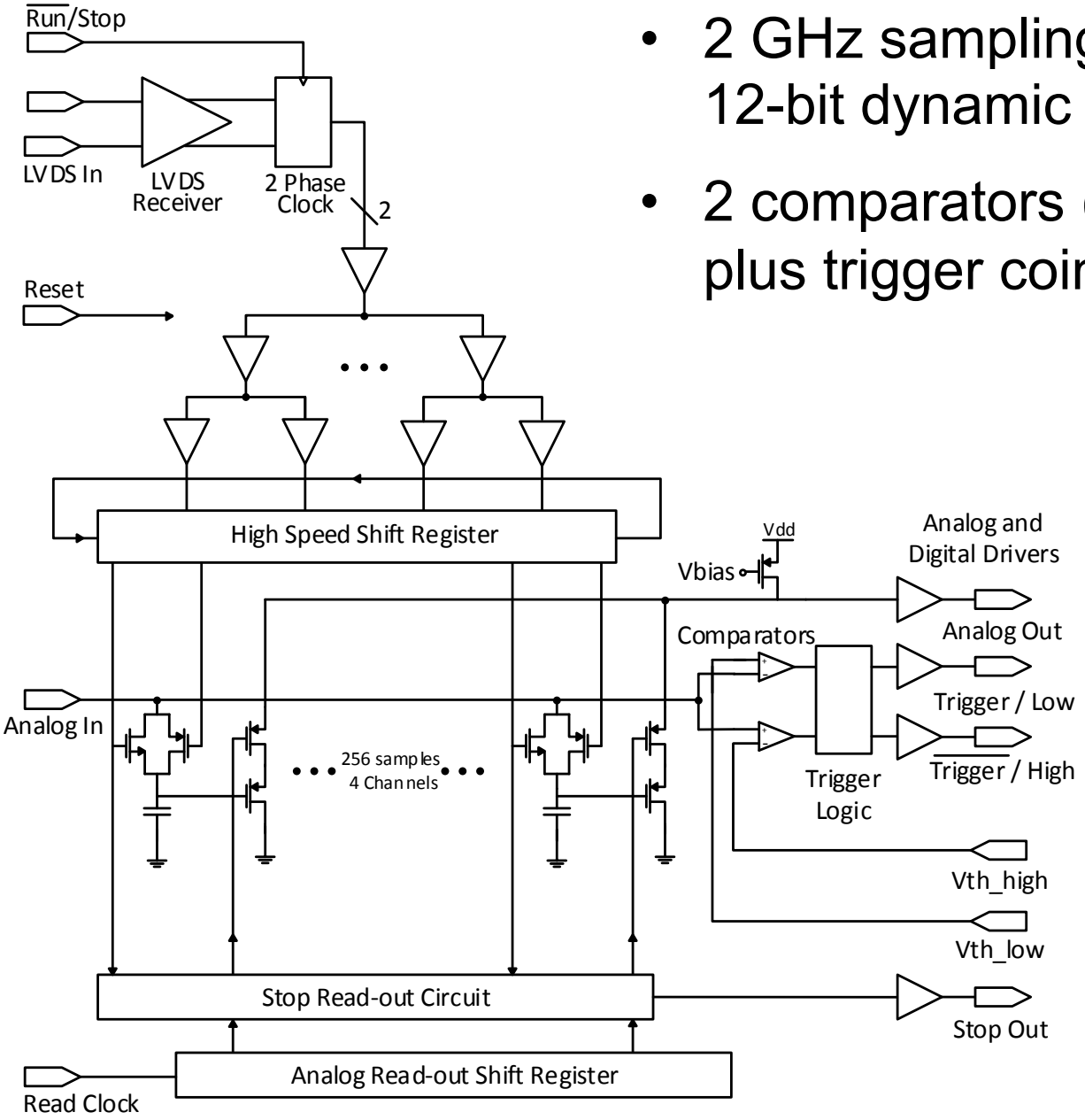
Advanced Transient Waveform Digitizer with on-chip channel-parallel digitization.

Used in AMANDA, IceCube, KamLAND

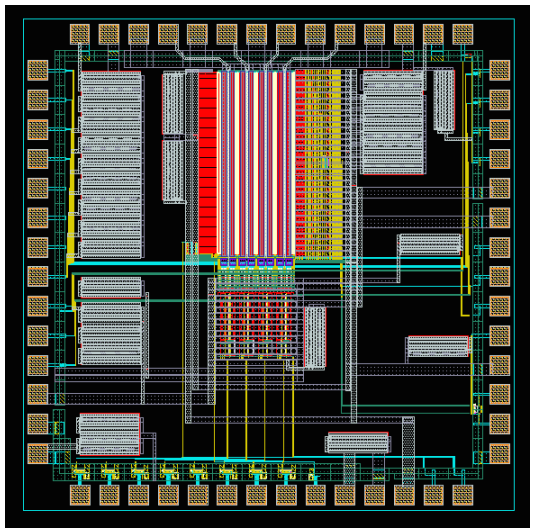
In IceCube:

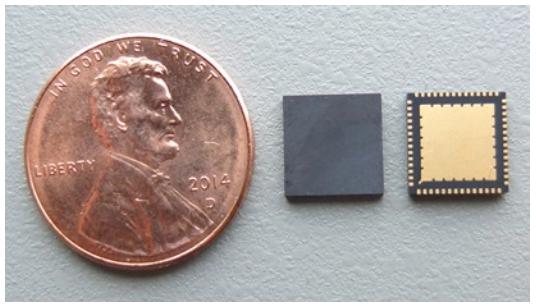
- Four channels combined to create equivalent of 14-bit ADC.
- Two chips used per photomultiplier tube for dead-time reduction.

SST: Multi-GHz Sampling + sub-ns Trigger

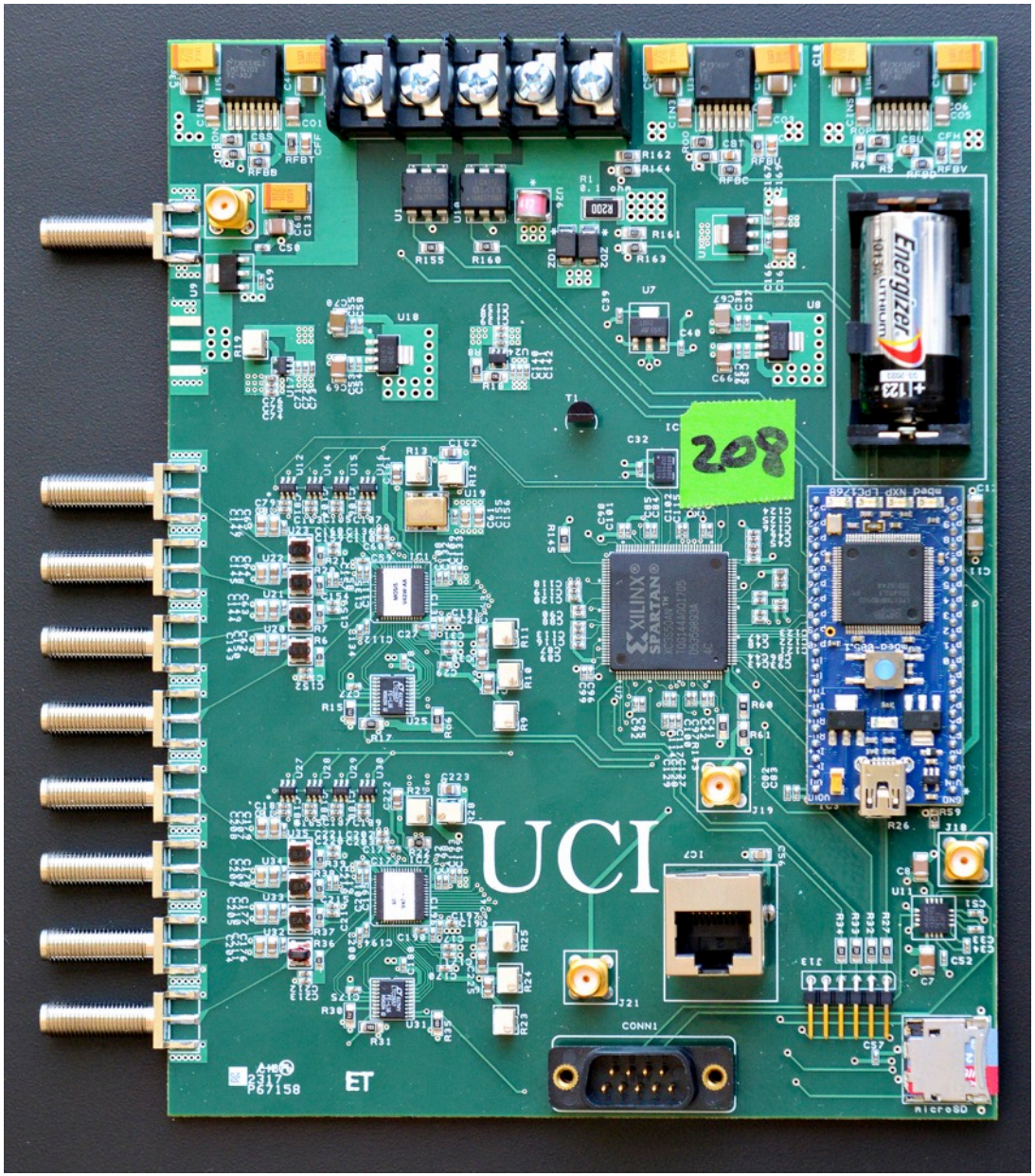


- 2 GHz sampling, 1.5 GHz bandwidth, 12-bit dynamic range, ps-level timing.
- 2 comparators (<500 ps) per channel plus trigger coincidence logic.



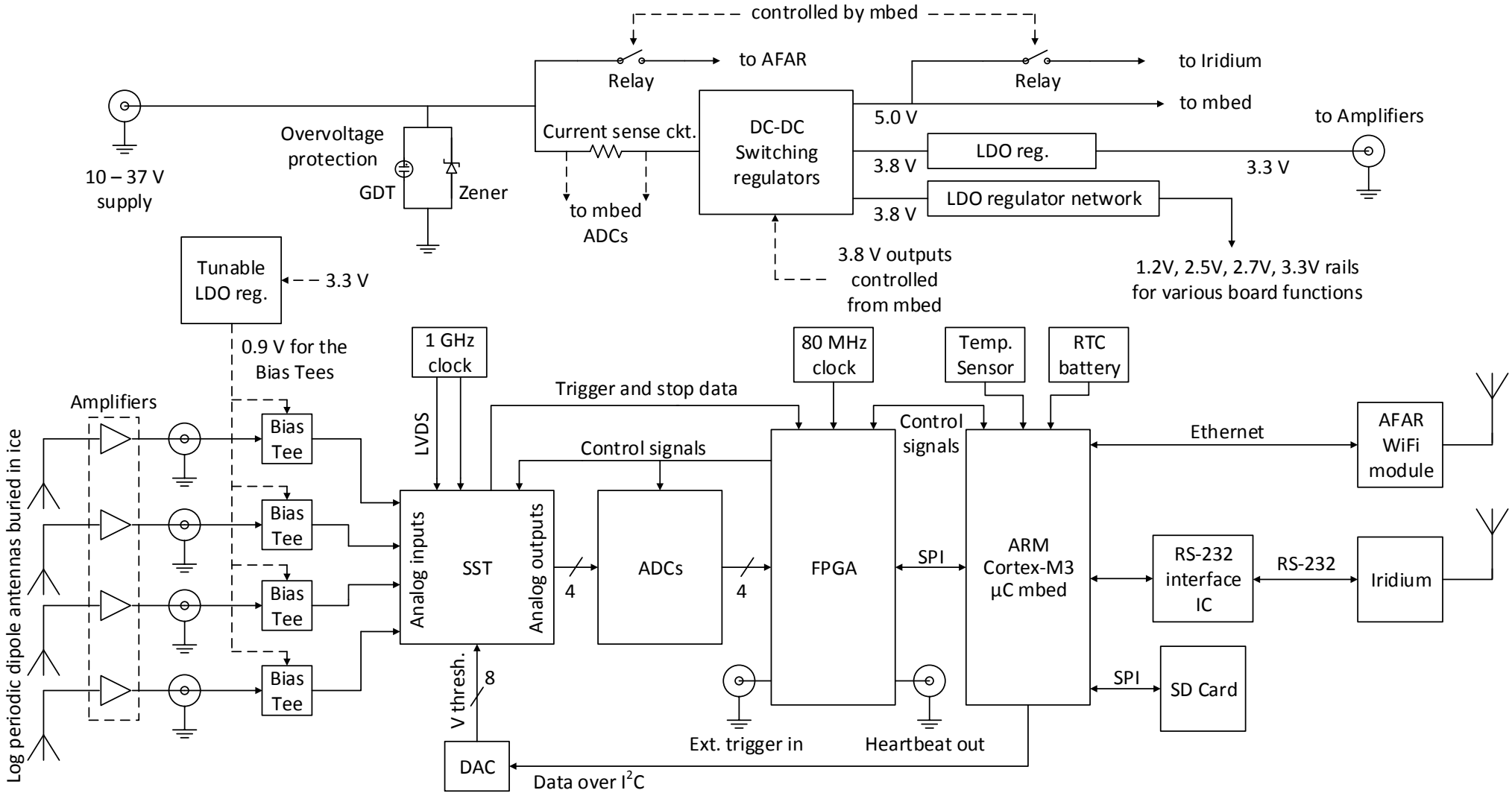


SST System Board: Radio Detection of Neutrinos



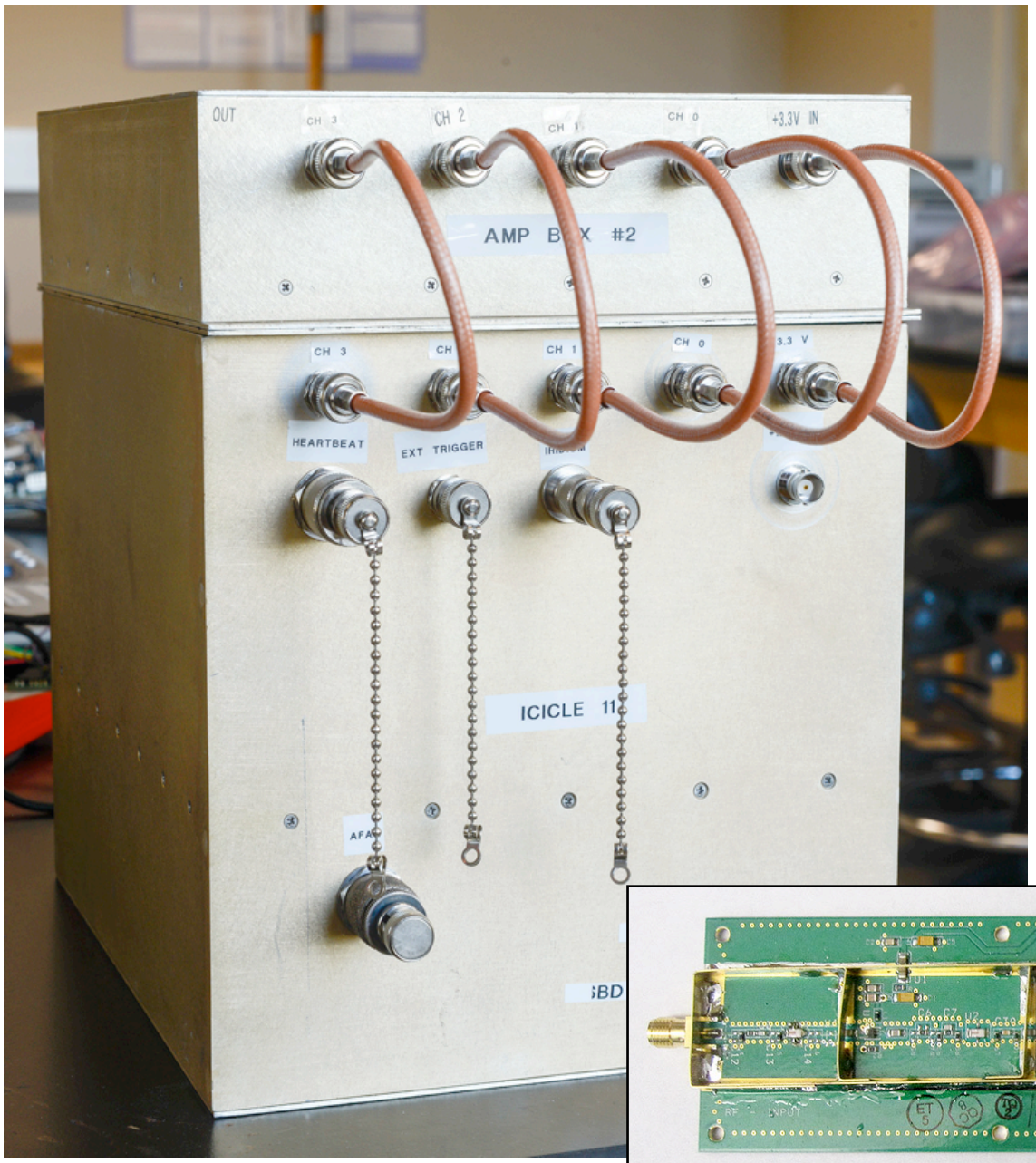
- 8 channels at 2 GHz
- Includes 32-bit μP
- A/D and D/A
- Power control
- Ethernet (WiFi)
- RS-232 (Iridium)
- 32 GB flash card
- Temperature monitoring
- Fast reference pulse out
- Trigger in and out
- Consumes ~1.7W

Gen. 2 System Board with SST

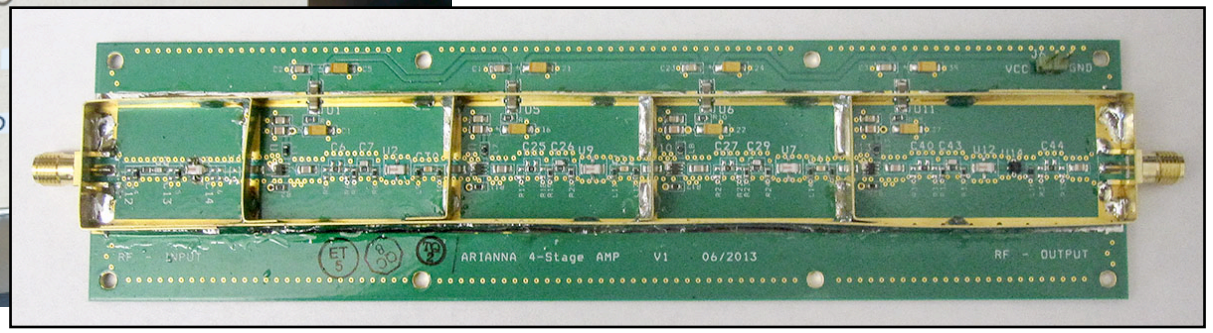


- Includes 32-bit µP, A/D and D/A, Ethernet (WiFi), RS-232 (Iridium), 32 GB S.D. card slot, power conditioning, control and monitoring, temperature monitoring, real-time clock backup…

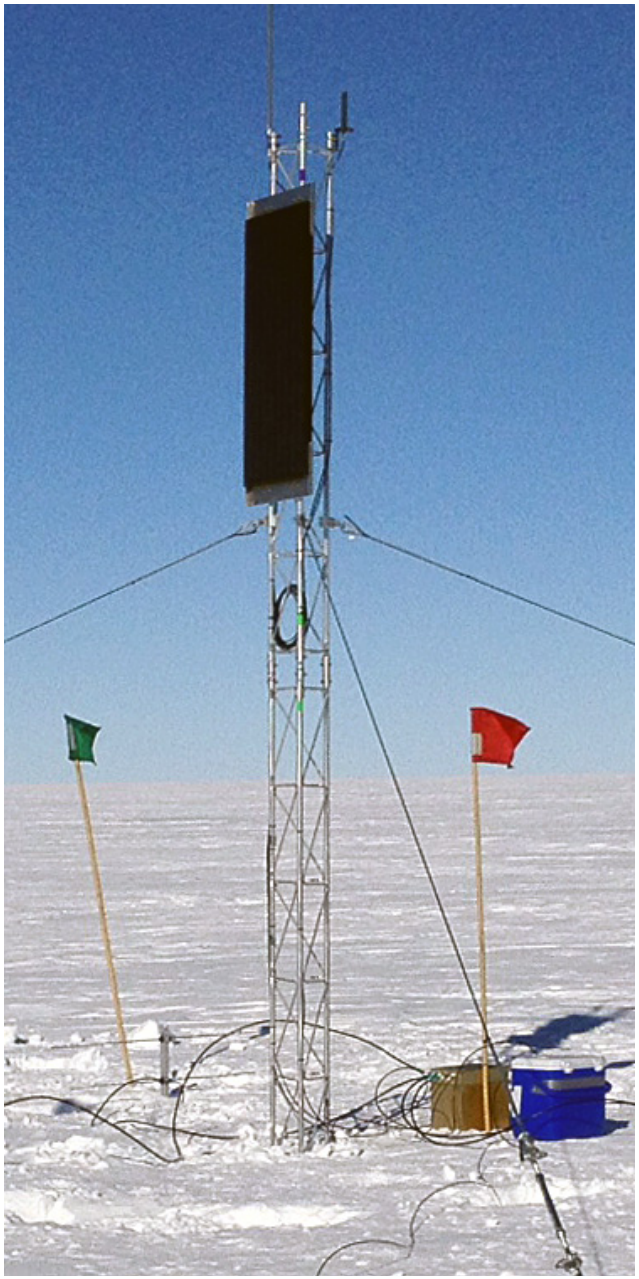
Amplification and System Boxes

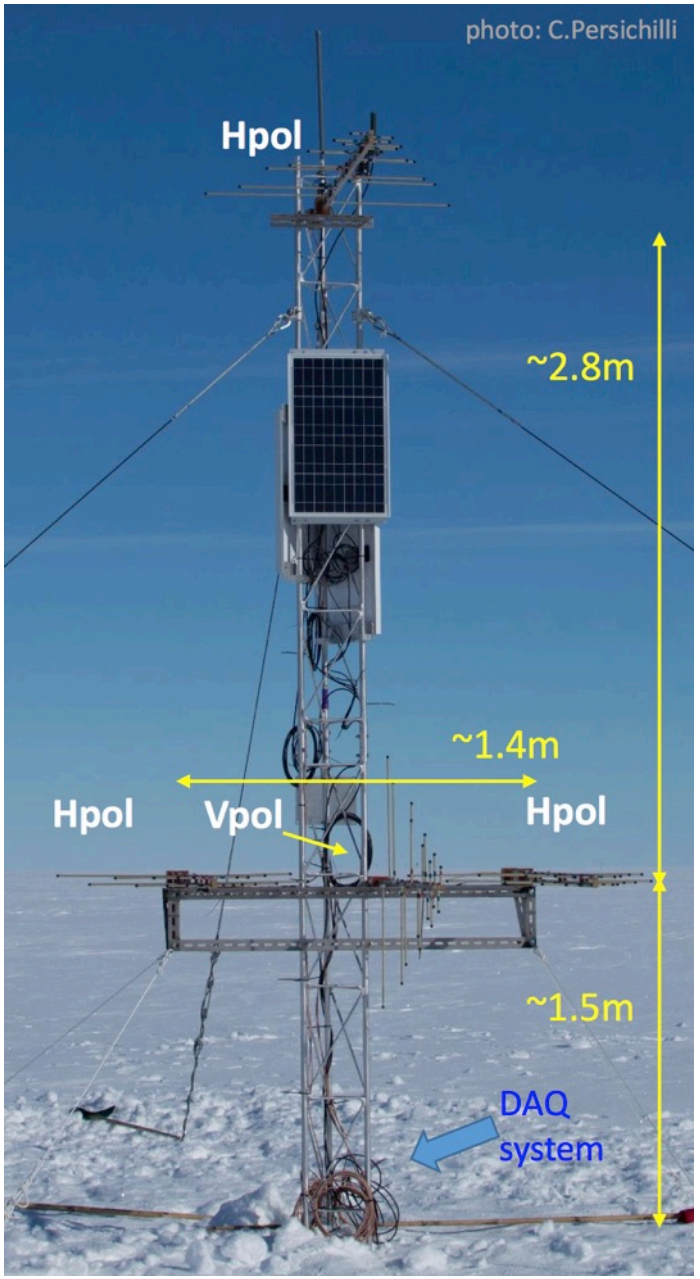


- Amplifier box contains 4 channels with 3.3V power supplied via coax.
- System box encloses all other electronics, including power conditioning and control, data acquisition, WiFi and Iridium modules, 20 Ah LiFePO4 battery.
- Heartbeat pulse out.
- External trigger in.
- Can be bolted together.
- Approx. 9x11x12 inches.

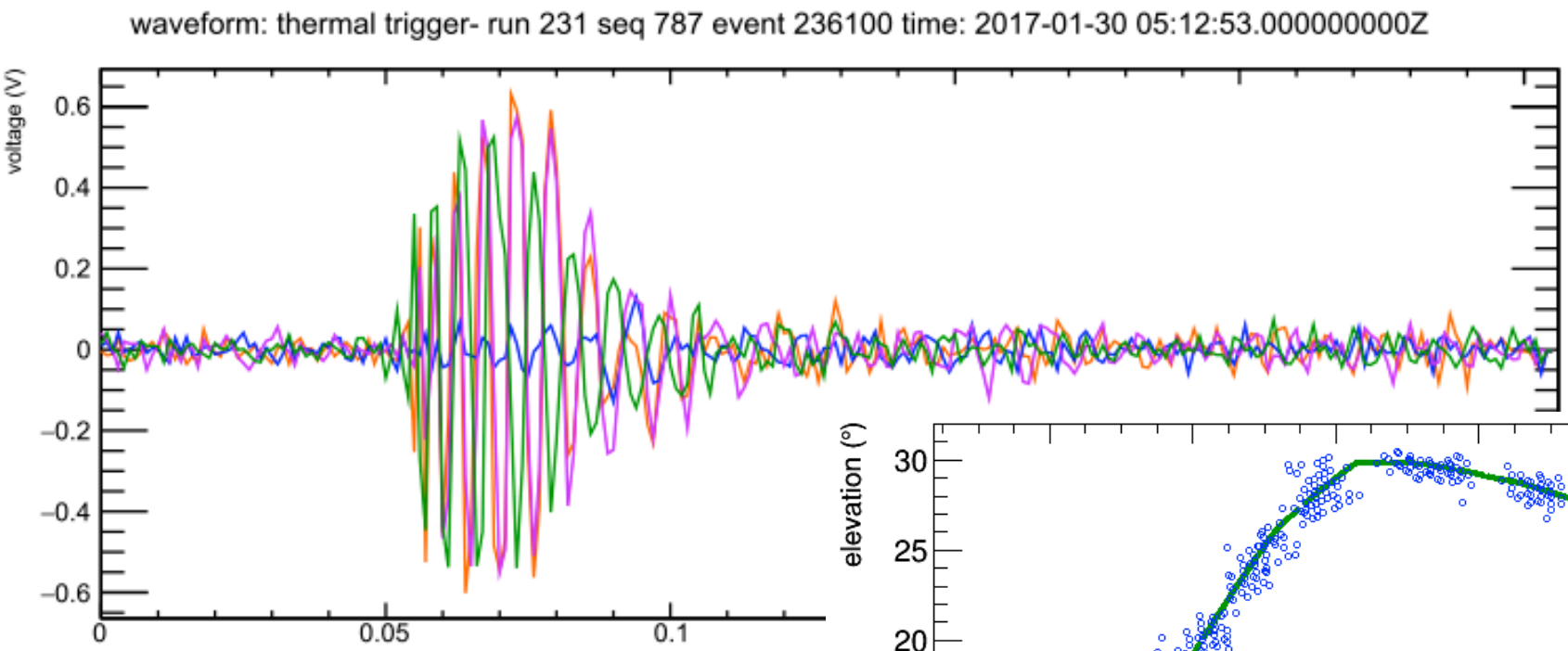


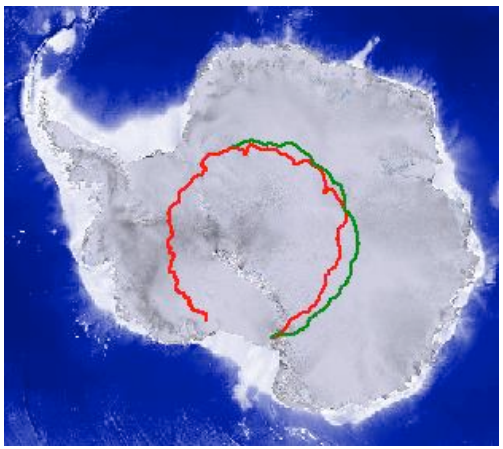
ARIANNA / HCR, Ross Ice Shelf

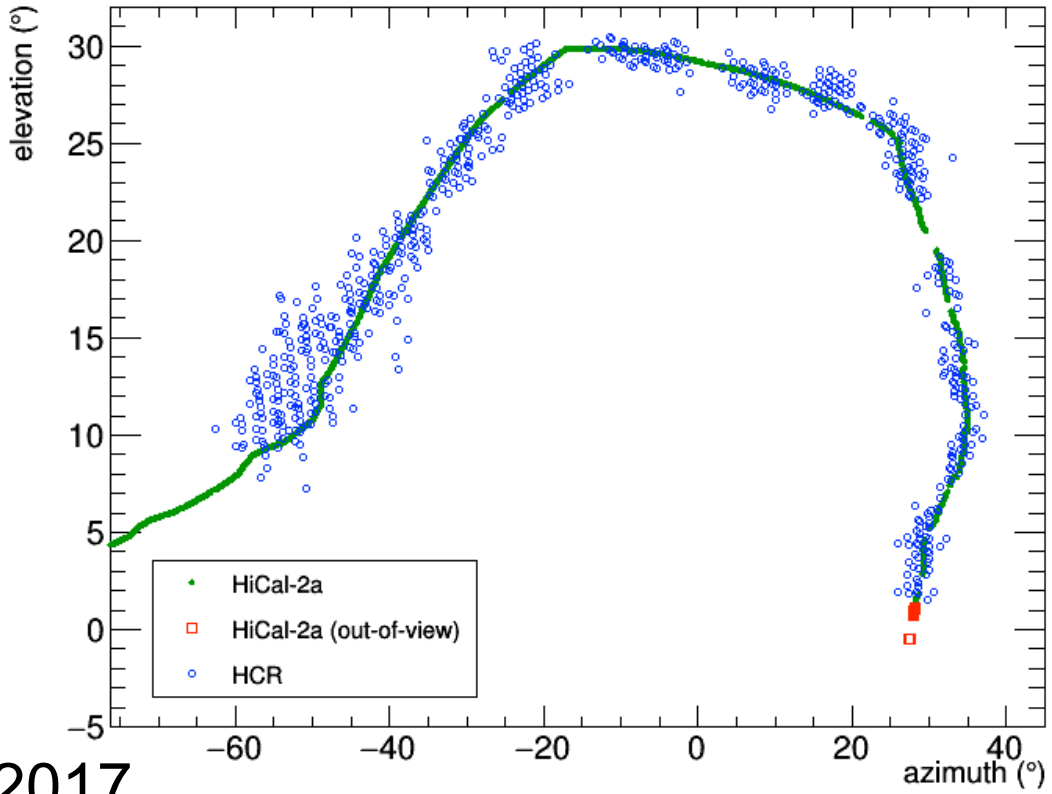




Candidate Cosmic Ray, HiCal2 Tracking

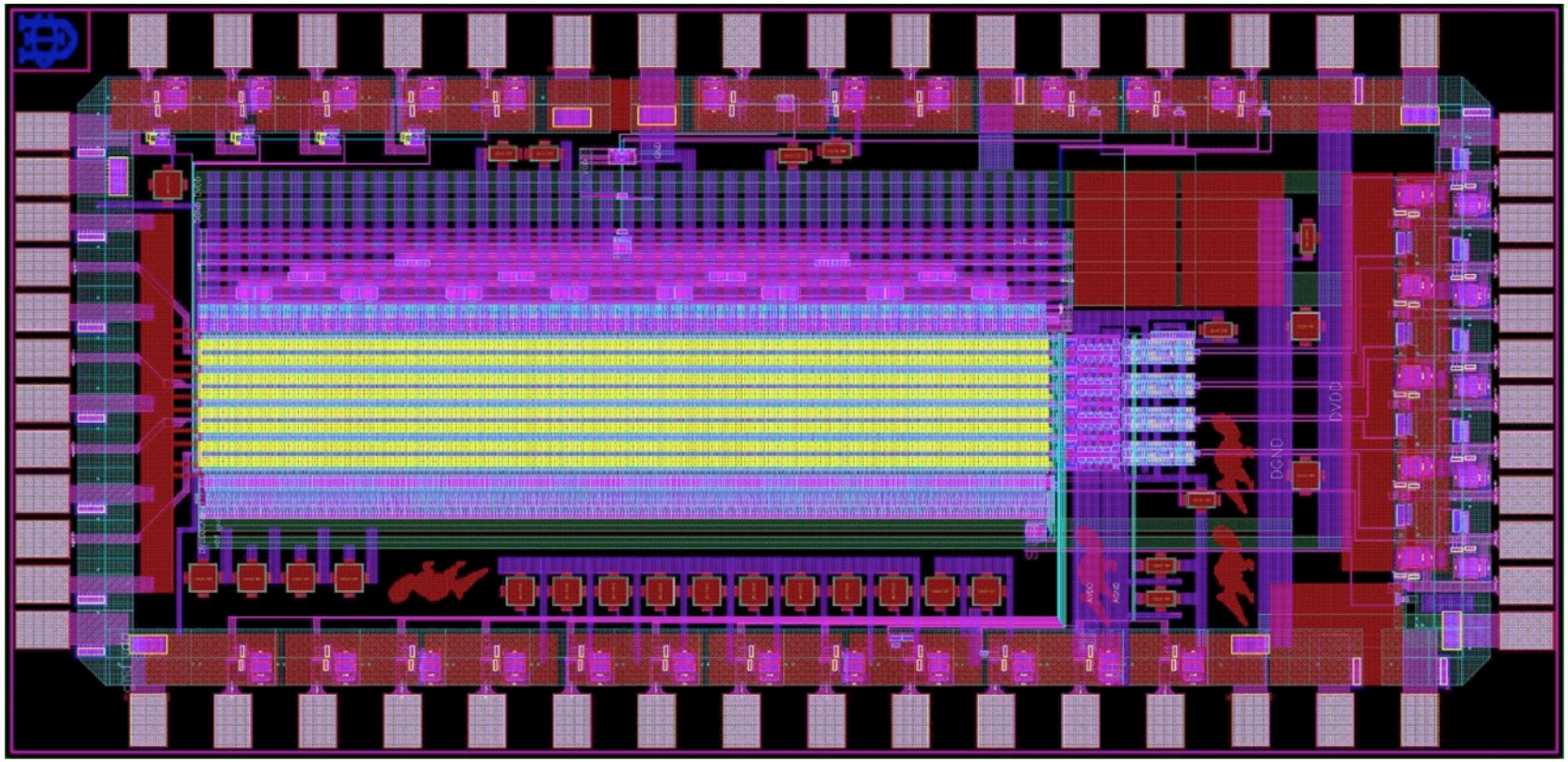






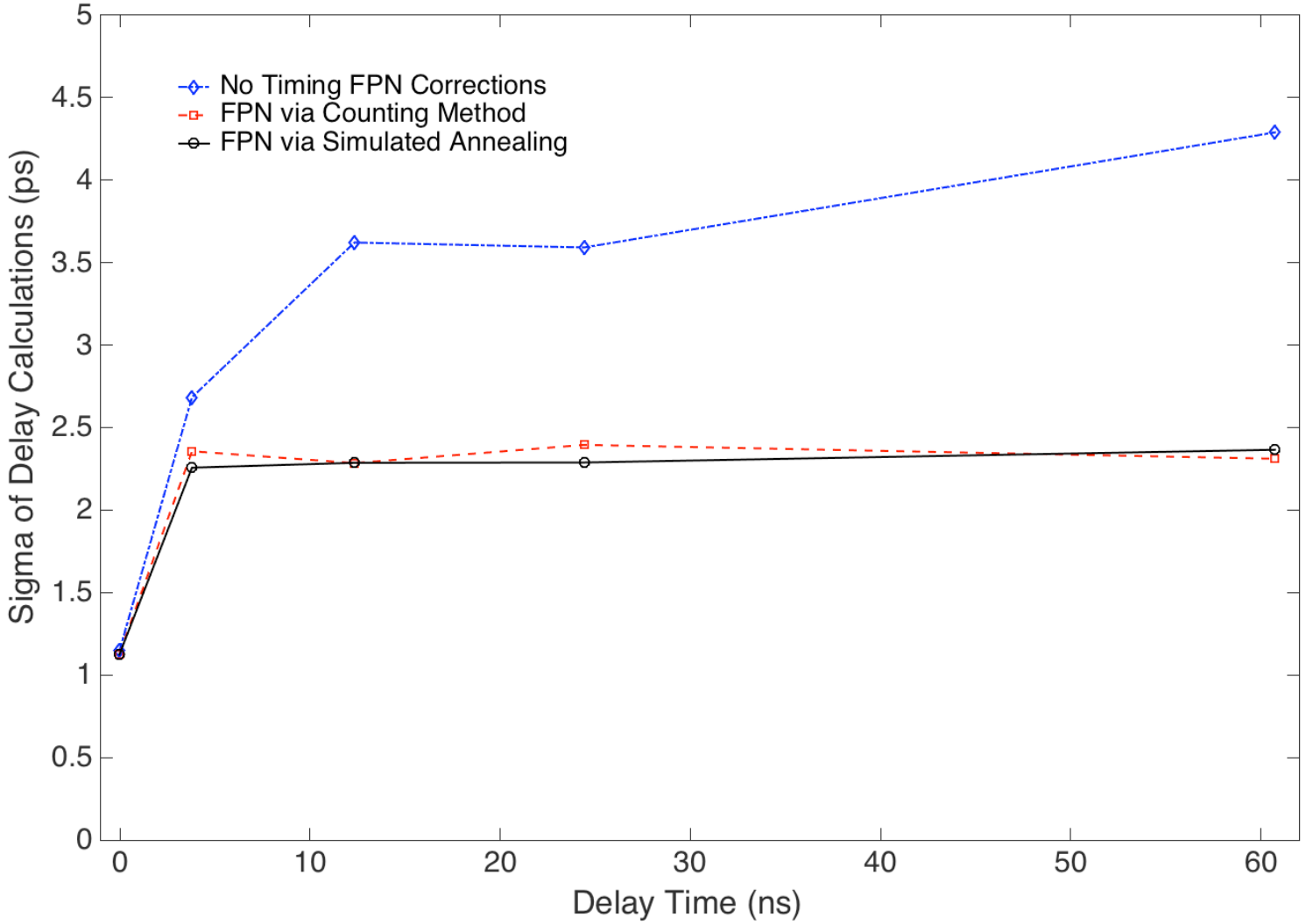
Wang, et al., ARIANNA-HCR, 2017

Deeper SST with Improved Timing FPN



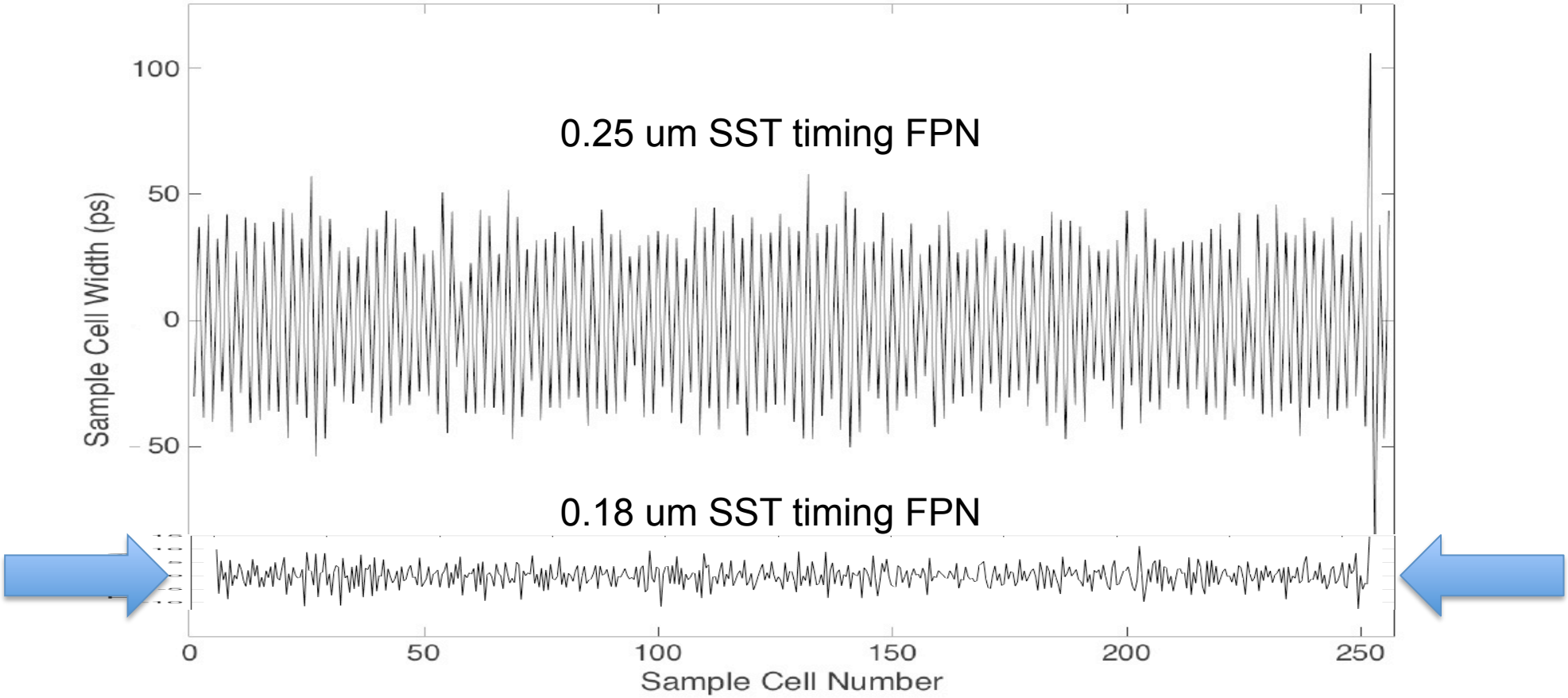
- Goal is to substantially reduce timing FPN errors, to reduce or eliminate the need for FPN corrections.
- 4 channels of 512 samples per channel in 0.18 μm CMOS.
- Synchronous 3 GHz sampling, common-start or common stop with 1 ns start/stop time. Fast (<500 ps) trigger + trigger logic.

Inter-Channel Accuracy vs. Calibration



- Cross-correlation result.
- Uncorrected sigma is under 4.3 ps. Corrected is < 2.4 ps.

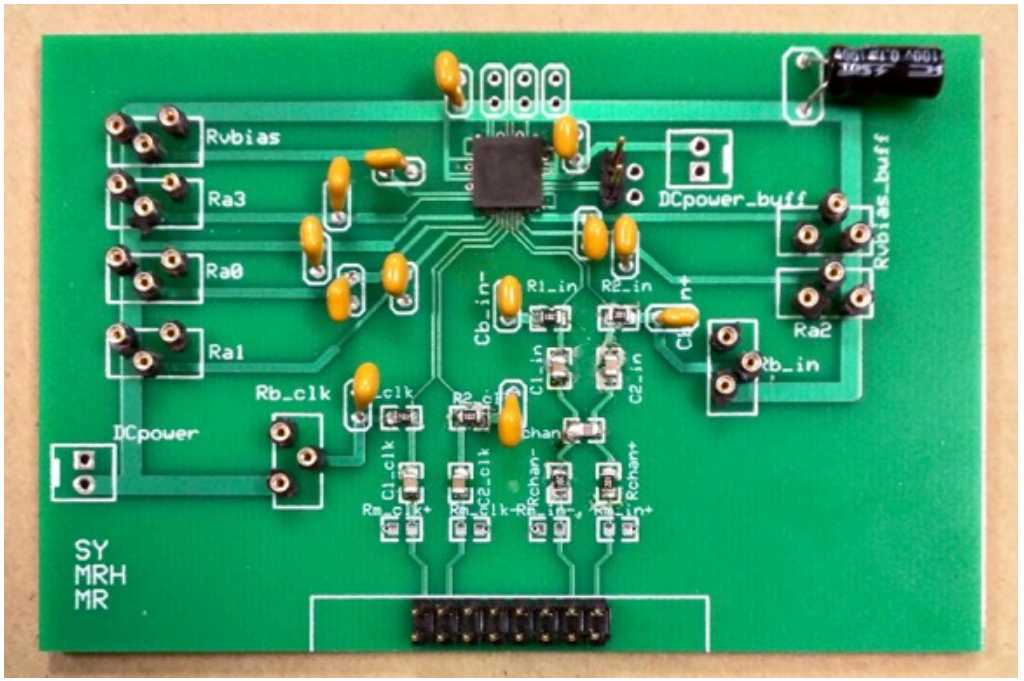
SST (0.25) vs. SST (0.18) Timing FPN



- Uncorrected timing FPN reduced by a factor of 10, to 4 ps RMS.
- Worst-case integral and differential non-linearity (generally the same, i.e. the “wrap around”) reduced from ~200 ps to <20 ps.

EECS 275: VLSI Design and Test Sequence

- Nearly 400 students have designed and tested their own chips via Kleinfelder's sequence.
- About 90 student projects have been fabricated.
- Example projects have included data-paths, finite-impulse-response filters, neural networks, game-playing chips, digital cameras, fast ADCs, RAM-DAC's, CAMs, transmitters / receivers, PLLs, clock recovery, and even SCA's.



Student team's 8 GHz SCA

- But the march towards smaller nodes is challenging for students, e.g. increasing the time and effort required to complete a design in 10 weeks.

Thank you!

Look! His brain is still 3 micron CMOS!