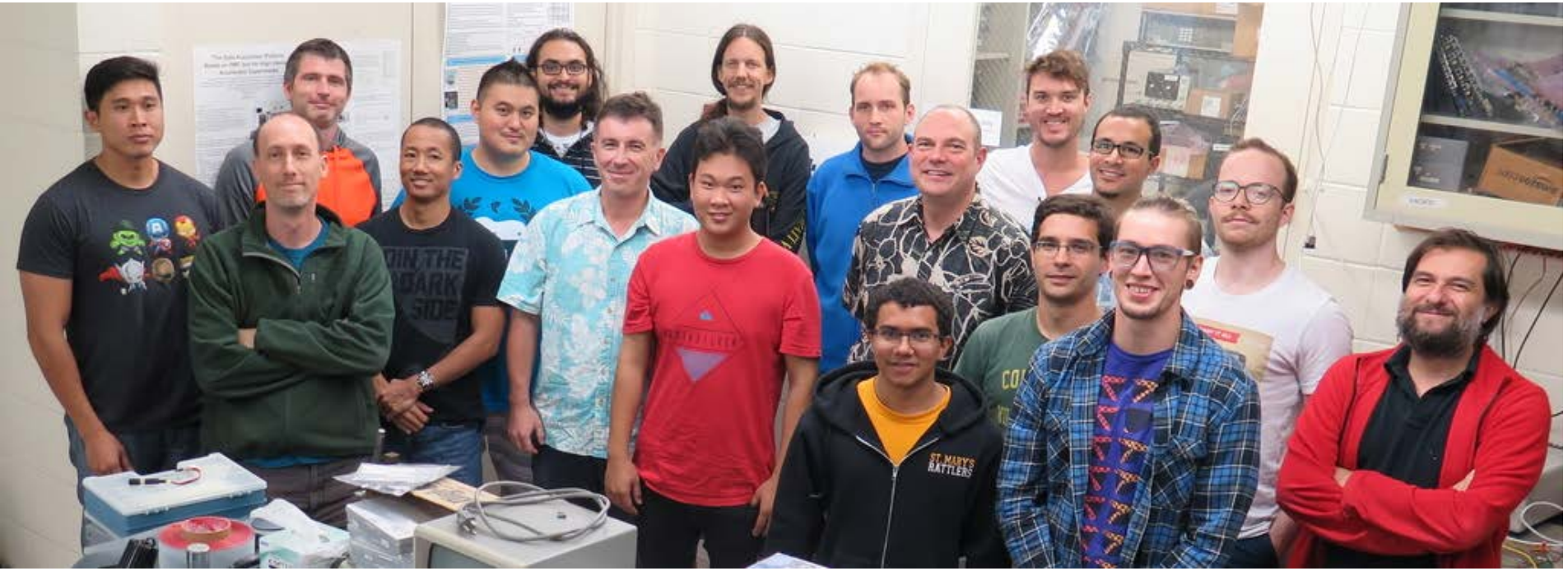
Hawaii Group Activities



Nalu Scientific
Data Acquisition Systems

Univ. of HAWAI'I SiPix LAB

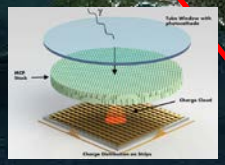
Gary S. Varner
University of Hawai'i

HEPiC 2017

UNIVERSITY of HAWAI'I® MĀNOA

Supporting the Discovery Frontier

High intensity MCP-PMT Charge Sensitive Amp +WFS

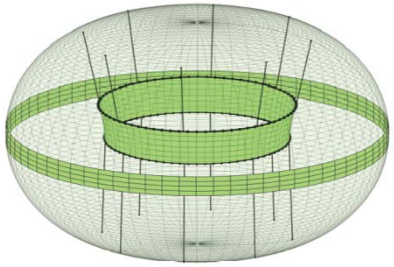


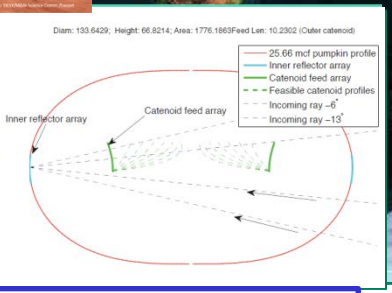
EIC PID Readout

Belle II Construction & Commissioning (pixel, Silicon Upgrades)

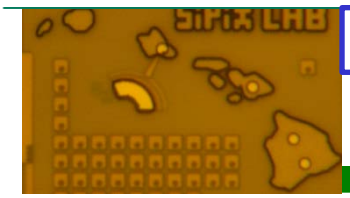
Belle II

Cherenkov Telescope Array (CTA)

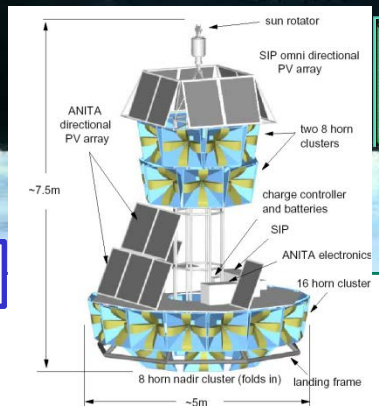


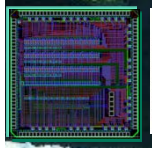


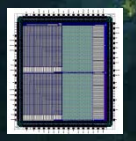
ExaVolt Antenna (EVA)



ANITA4/5





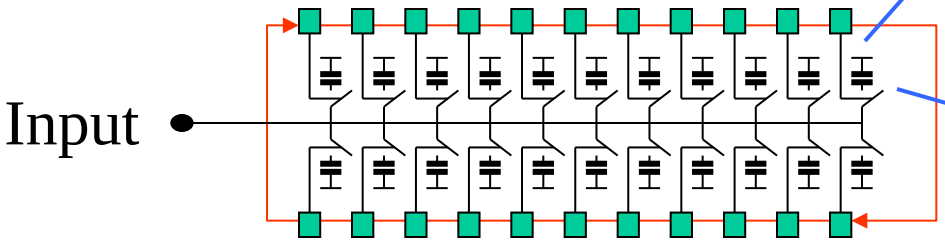


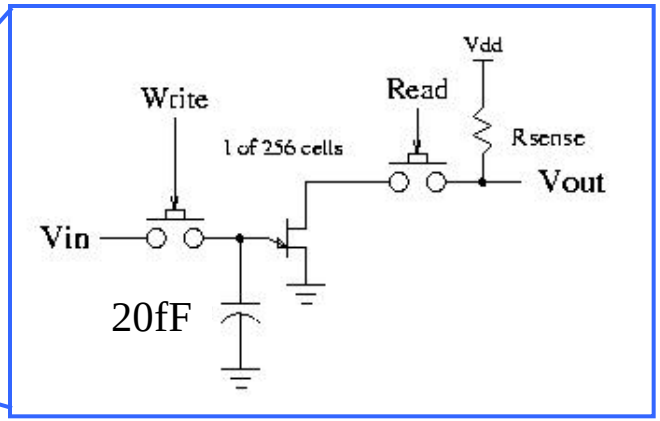
Development Overview (SCA/WFS centric)

- Current Deployments
  - LABRADOR (UHE ν searches)
  - IRS (ARA and Belle II TOP)
  - TARGET (Belle II KLM, CTA)
- Completing development
  - GRAPH for space applications (low-noise CSA+WFS)
  - CTA production versions (CT5TEA + CTAC)
- Evolving Directions (commercialization):
  1. On-chip Feature extraction: ASoC (System on Chip)
  2. High density: Si-READ (64 channels, low-cost)
  3. Precision timing: RFpix (details tomorrow)

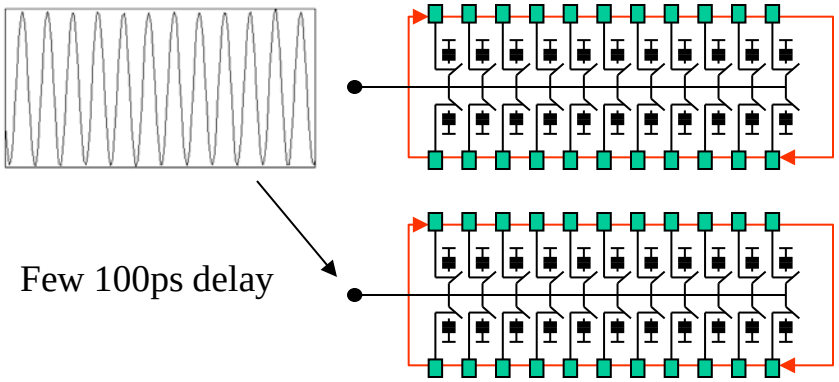
Switched Capacitor Array Sampling

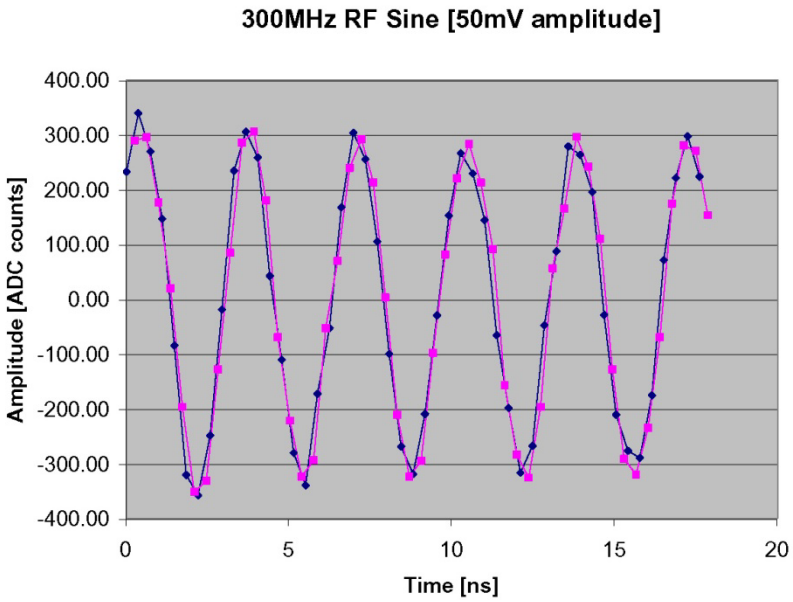
- Write pointer is ~few switches closed @ once



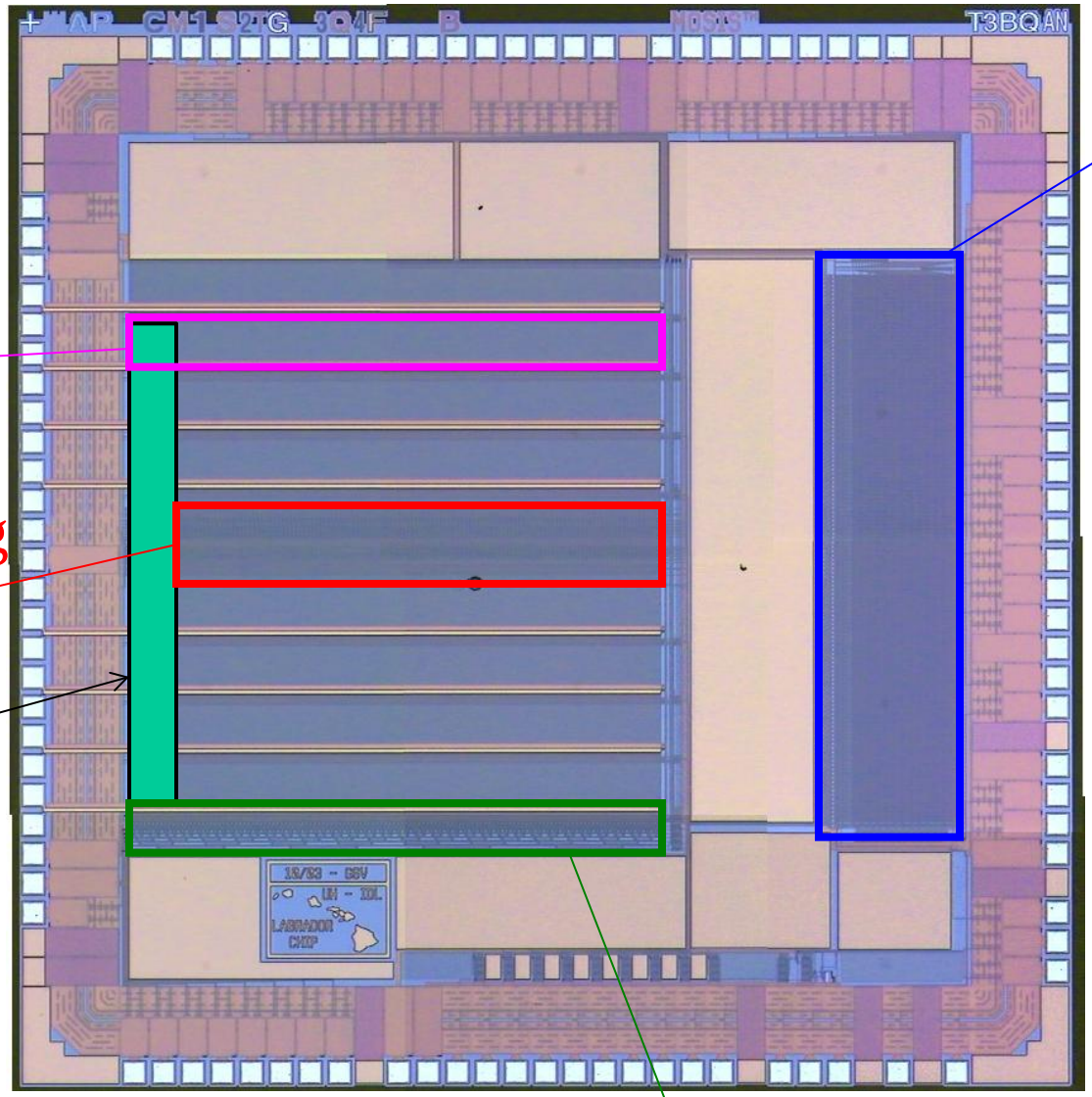


Tiny charge: 1mV ~ 100e$^-$



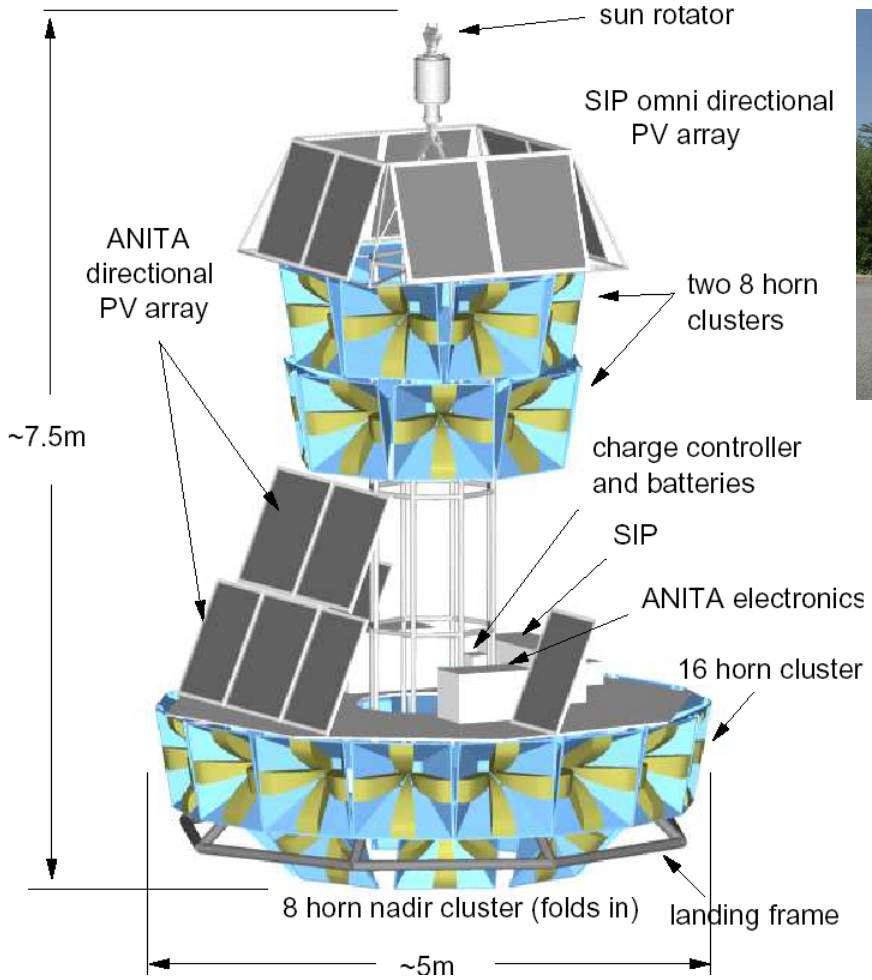


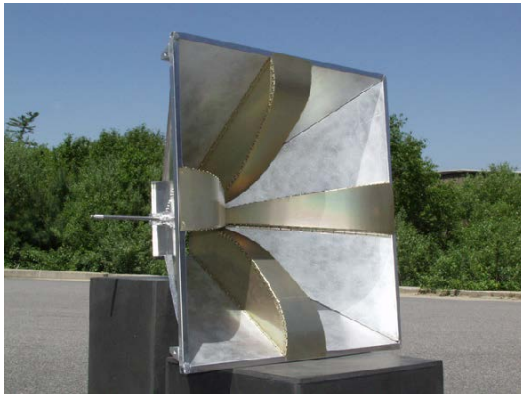
Basic Functional components

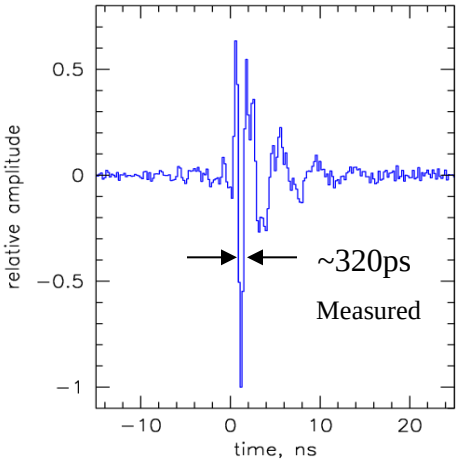


A Very Challenging Design

A radio "feedhorn array" for the Antarctica Continent



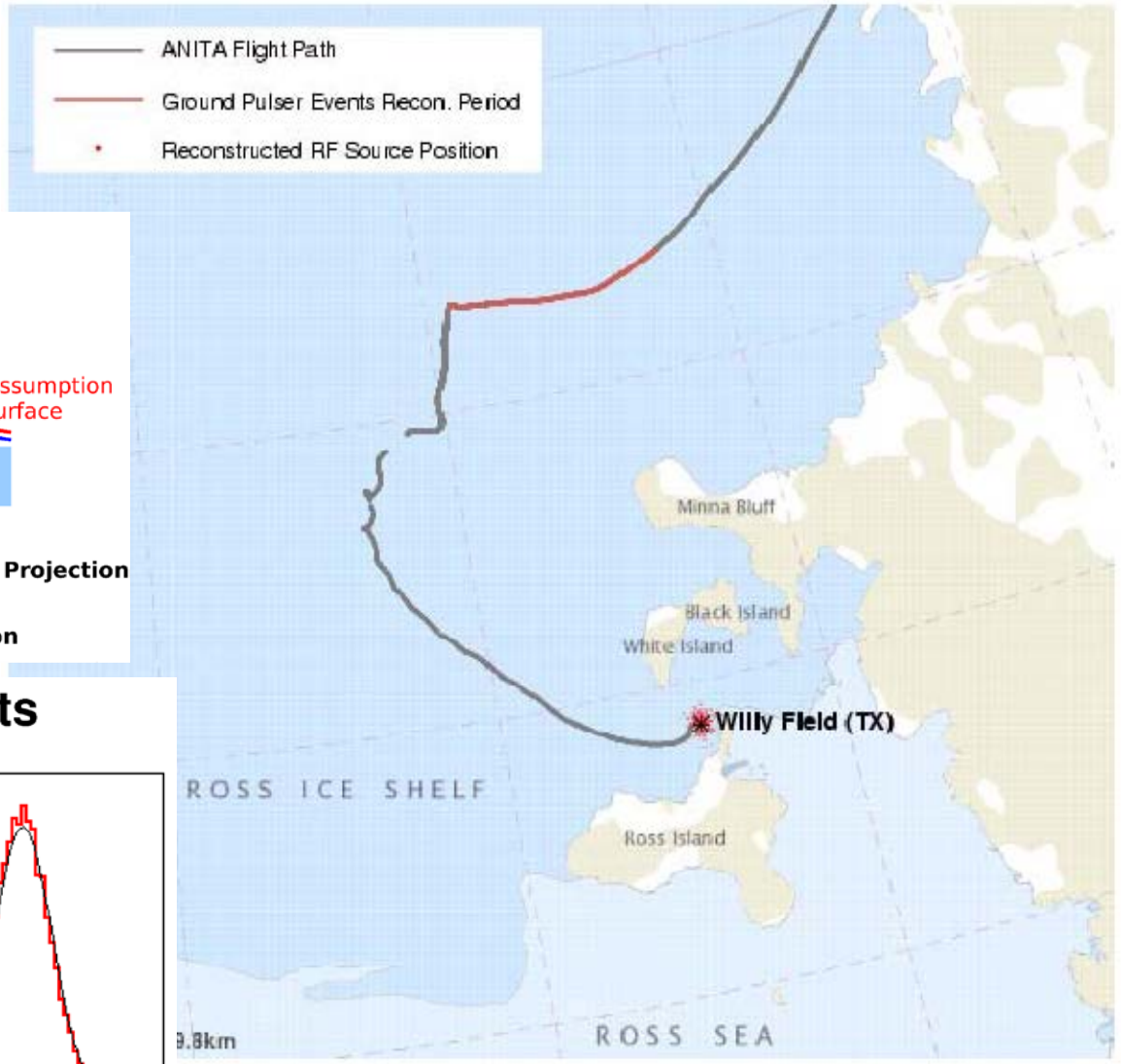




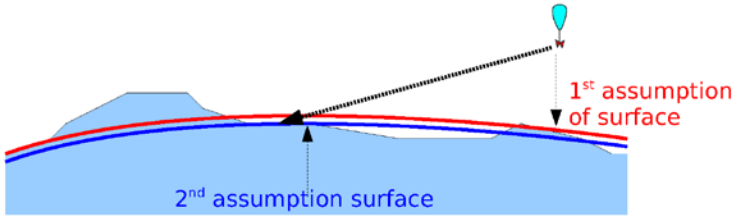
- Quad-ridged horn antennas provide superb impulse response & bandwidth (200-1200 MHz)
- Interferometry & beam gradiometry from multiple overlapped antenna measurements

Demonstrated performance -- Not just in the lab

<30ps timing



RF Projection onto the surface



Fast Algorithm: Line Sphere intersection

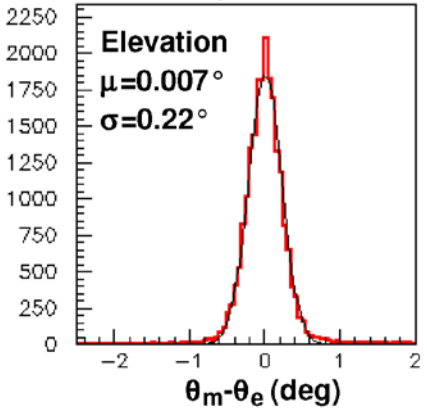
1st R_{earth} =Geoid + Surface @ Ballon position -> Rough Projection

2nd R_{earth} = Geoid + Surface @ (position from 1st)

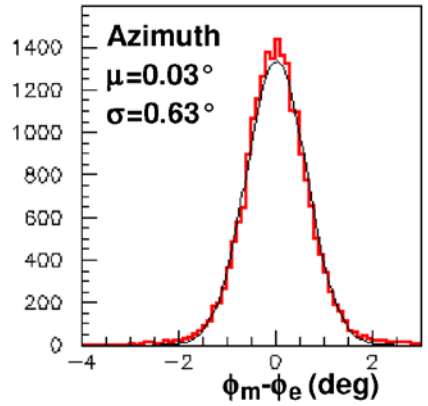
3rd: one more iteration -> converged after 2nd iteration

V-pol results

Borehole Data (used for calibrations)



3.8 mrad



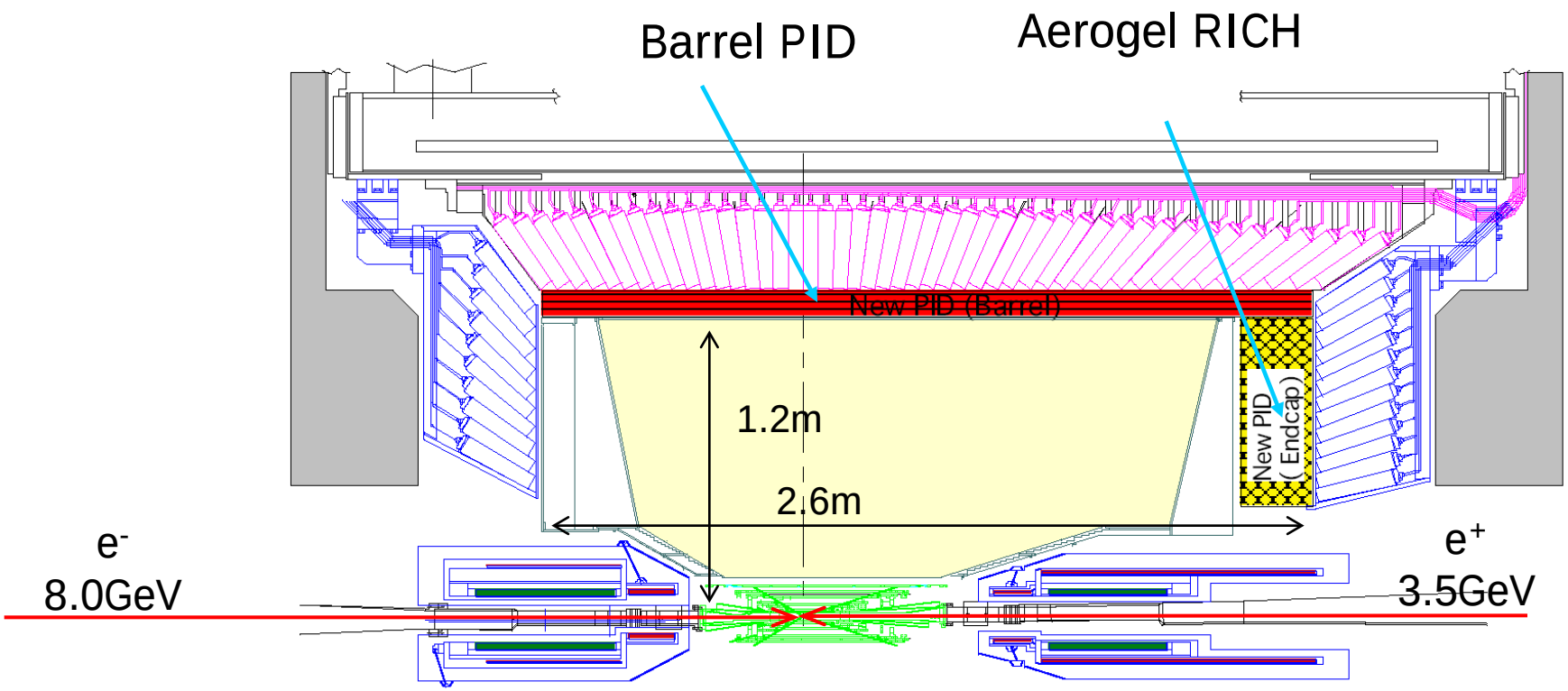
11.2 mrad

Upgraded Belle detector

- PID (π/K) detectors
- Inside current calorimeter
- Use less material and allow more tracking volume

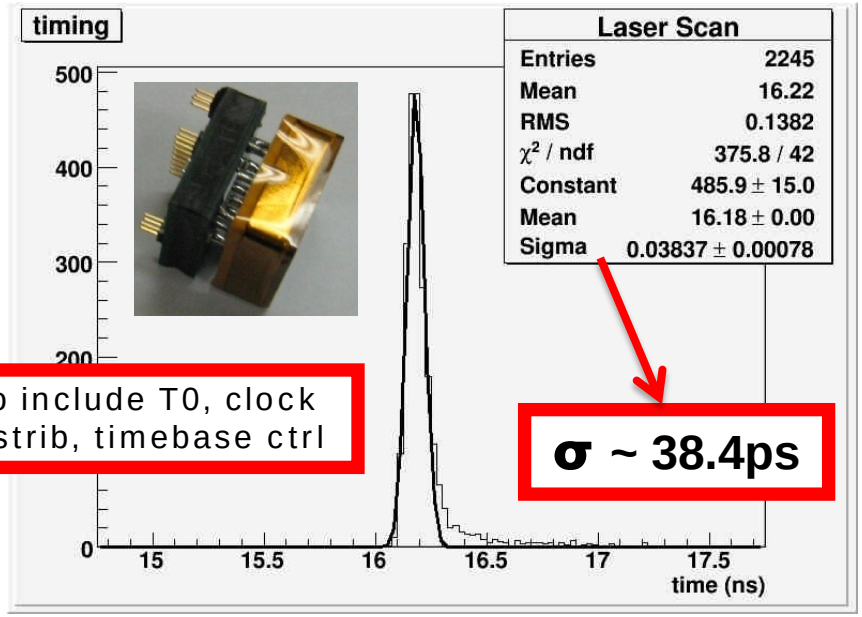
→ Available geometry defines form factor

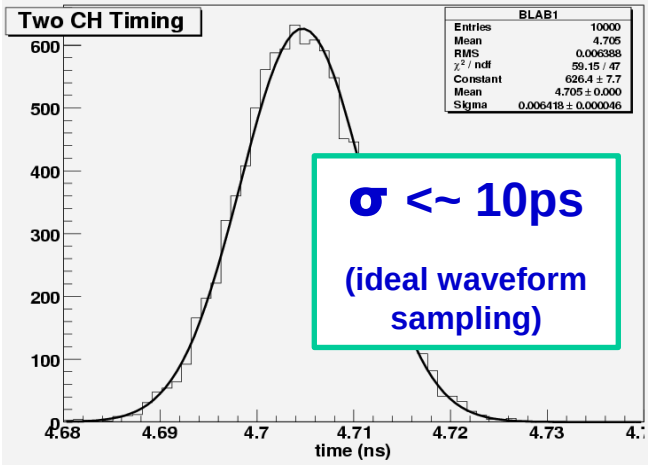
-



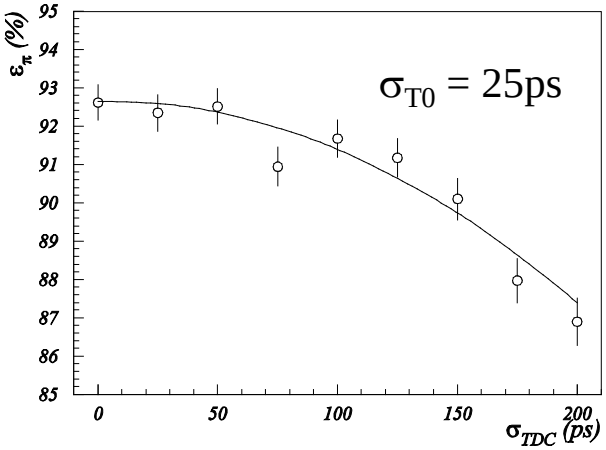
Single photon detection for TOP

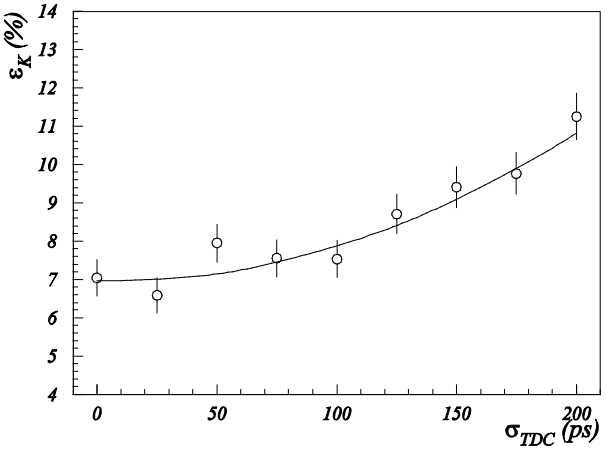
- Single photon timing for MCP-PMTs





NIM **A602** (2009) 438

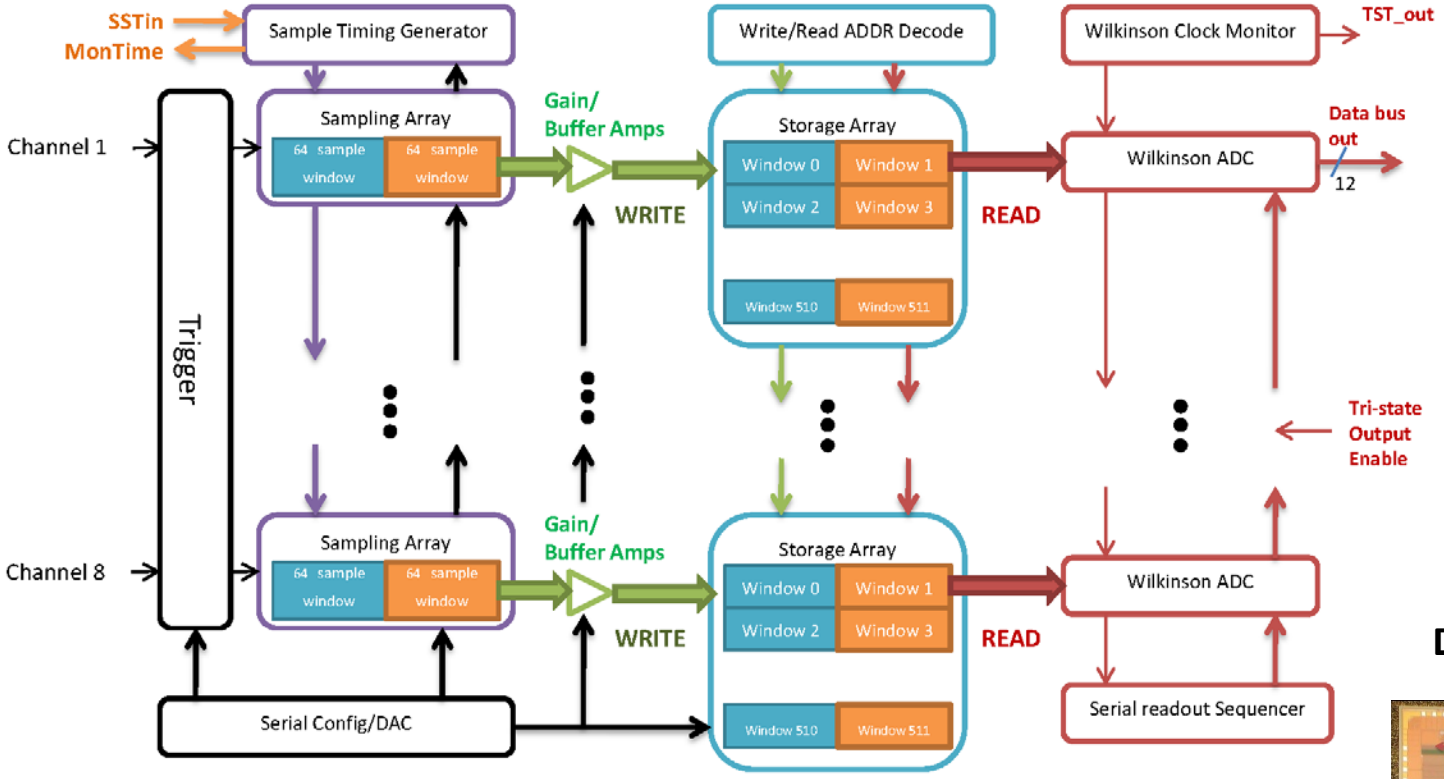




σ <~ 50ps target

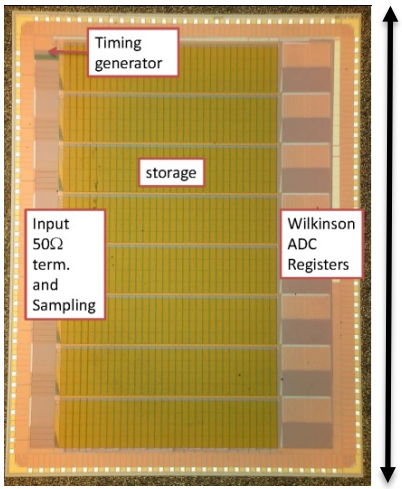
NOTE: this is single-photon timing, **not** event start-time "T_0"

IRS family ASIC Overview



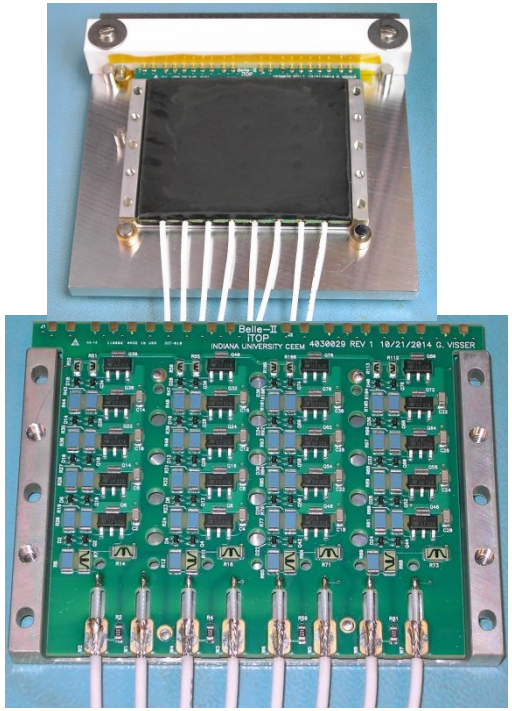
- 8 channels per chip @ 2.8 GSa/s
- Samples stored, 12-bit digitized in groups of 64
- 32k samples per channel (11.6us at 2.8GSa/s)
- Compact ASICs implementation:
  - Trigger comparator and thresholding on chip
  - On chip ADC
  - Multi-hit buffering

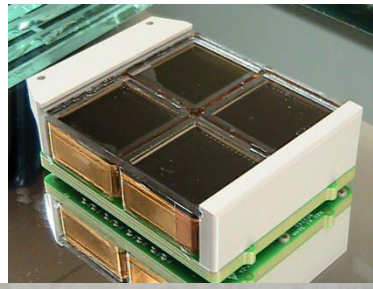
Die Photograph

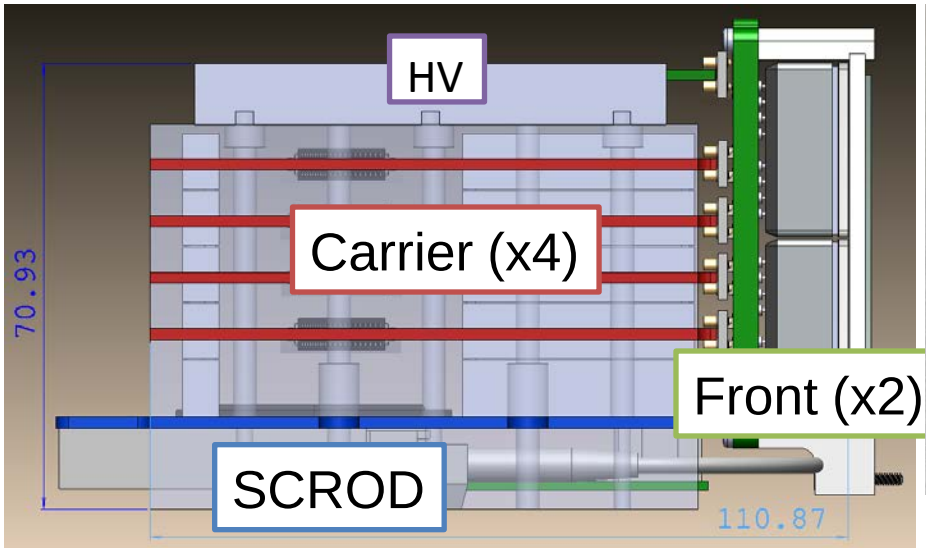


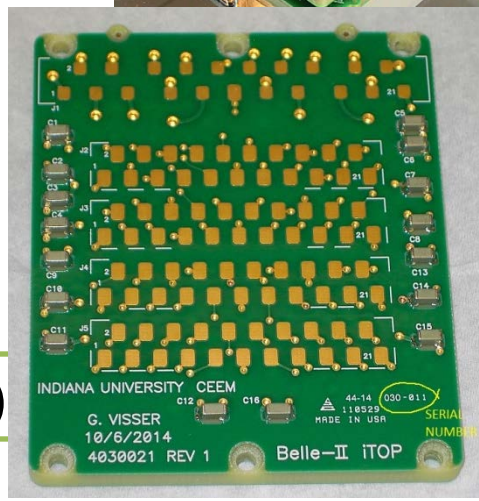
iTOP Readout “boardstack”

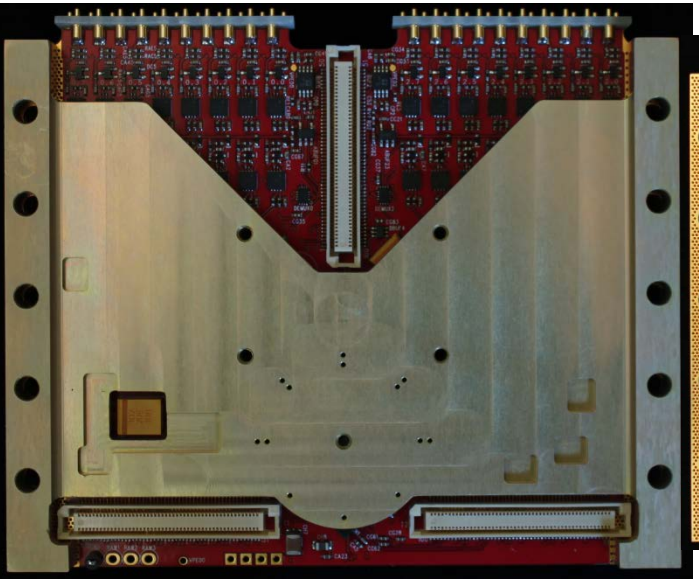
(1 of 4 per TOP Module)

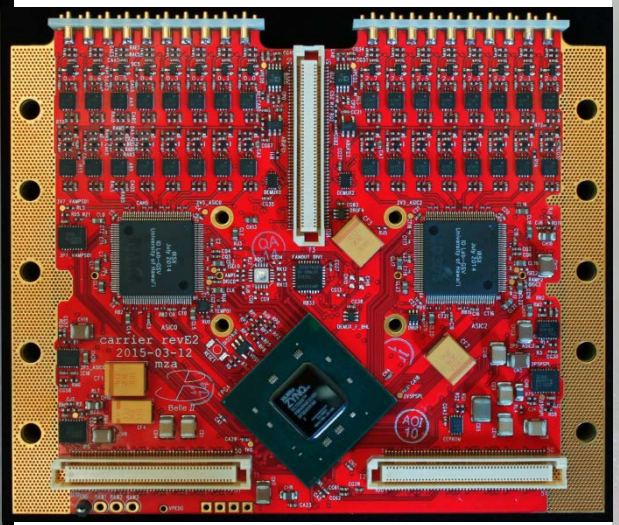




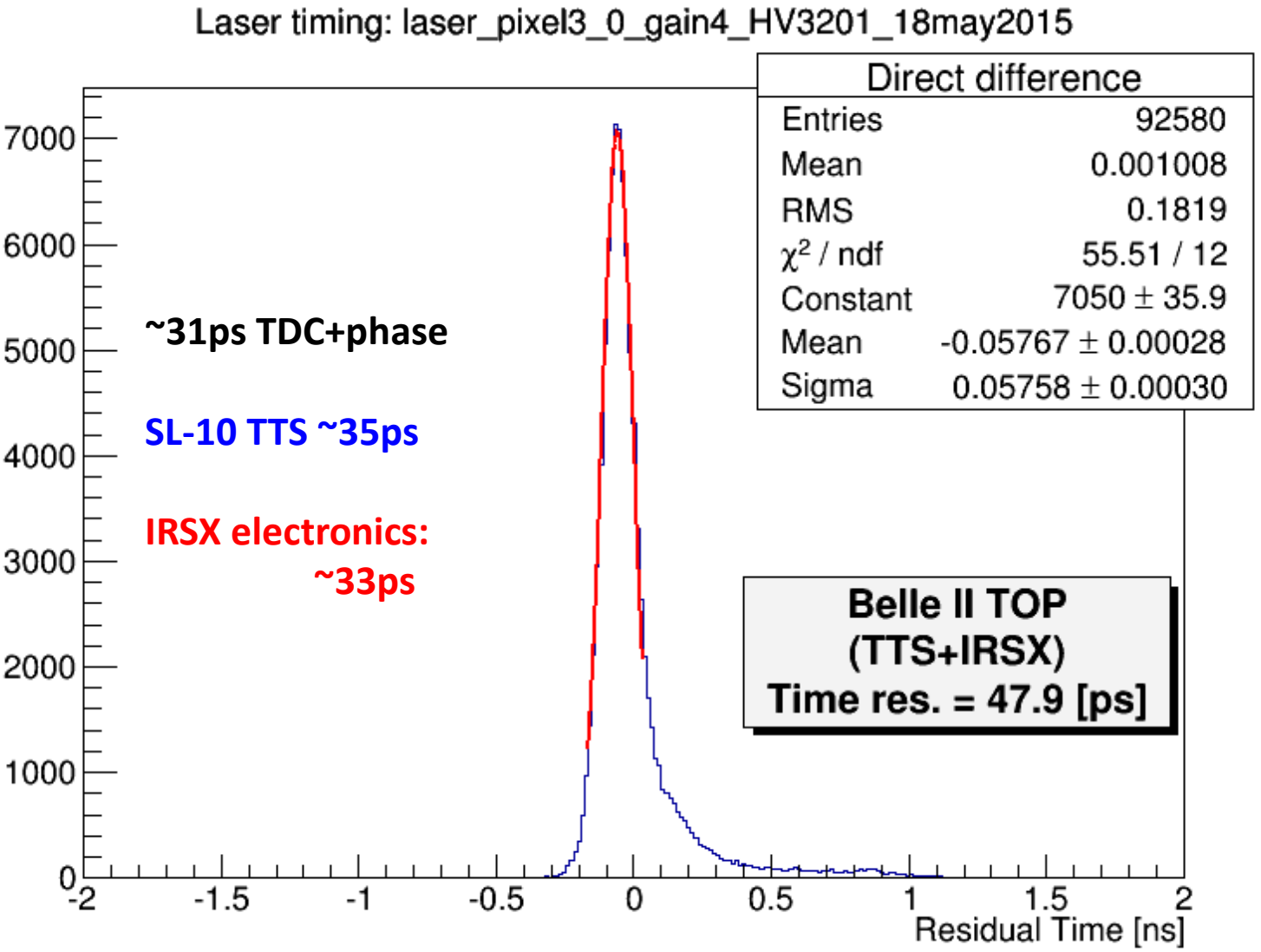






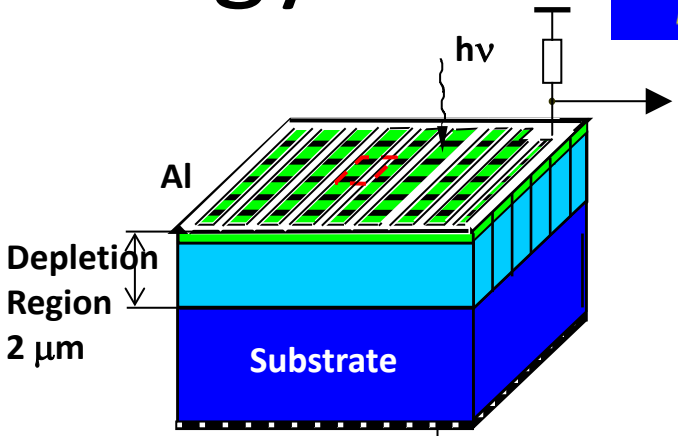


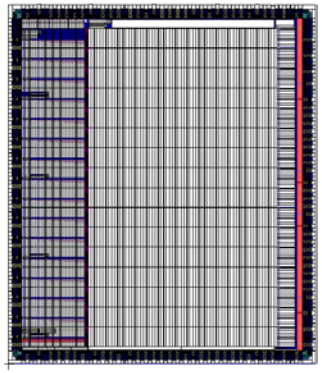
Production single photon testing

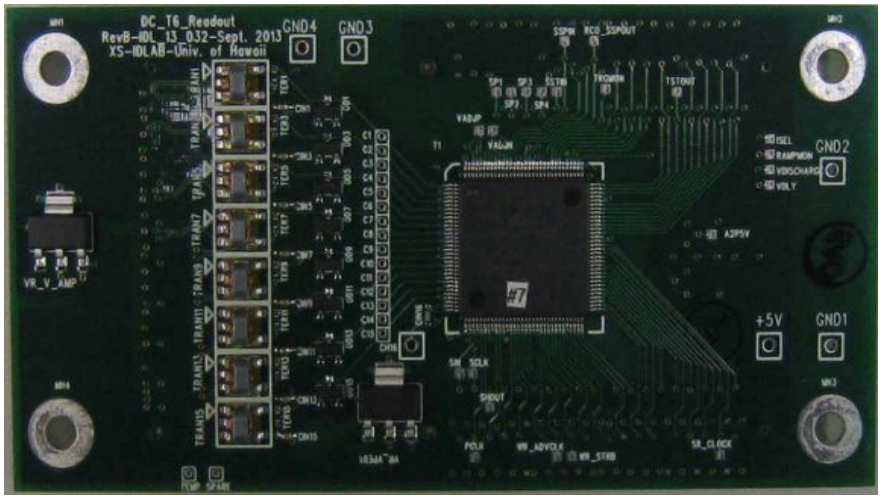


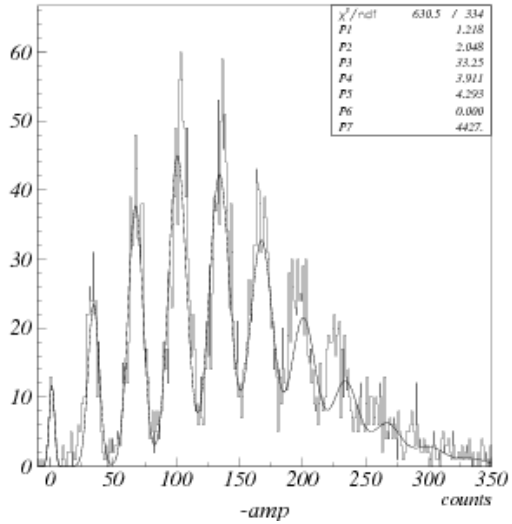
TARGET technology

- Highly pixelated readout
- *20,000 channels Belle II Muon system readout*





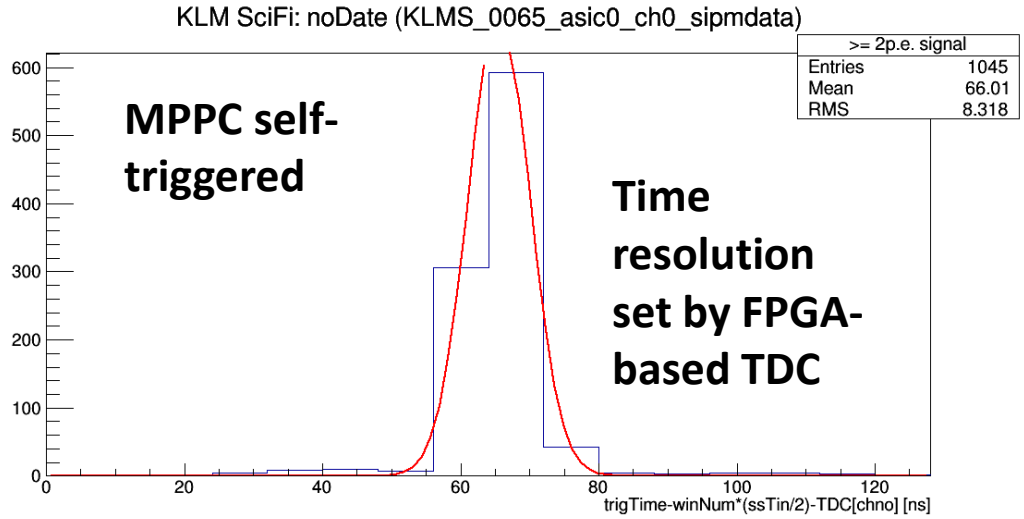


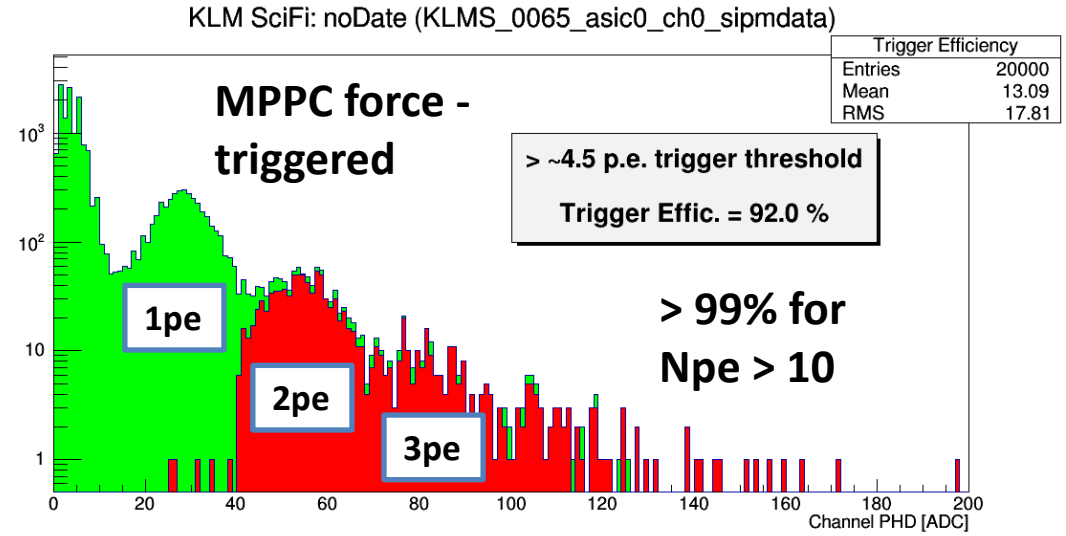


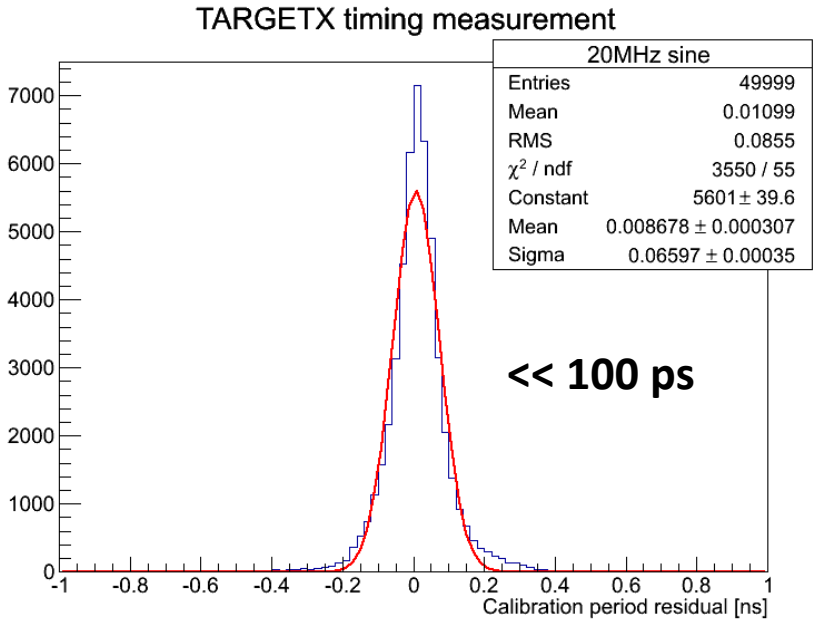
- **16 channels**
- **0.5-1.2 GSa/s**
- **10-12-bit digitization**
- **Samples stored, digitized in groups of 32**
- **16k samples per channel (16us at 1GSa/s)**
- **Integrated triggering capability**

500kHz – 2MHz dark rate not a problem:
5 p.e. threshold reduces rate to < 1kHz
while maintaining > 99% MIP efficiency

Performance Reference







Sine scan data (zero crossing)

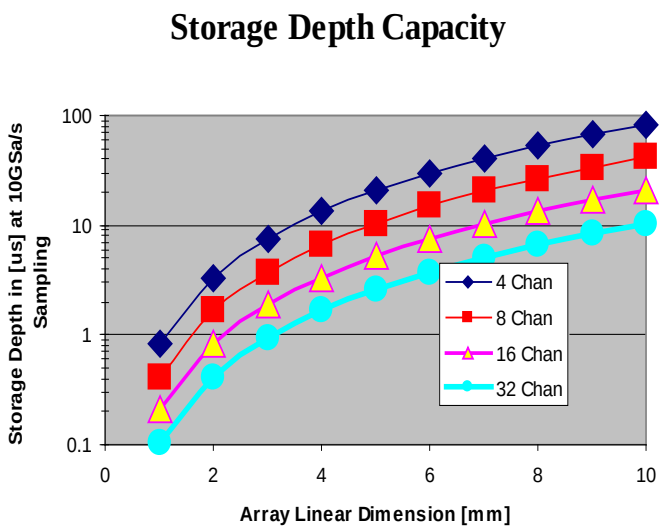
TARGET family Synopsis

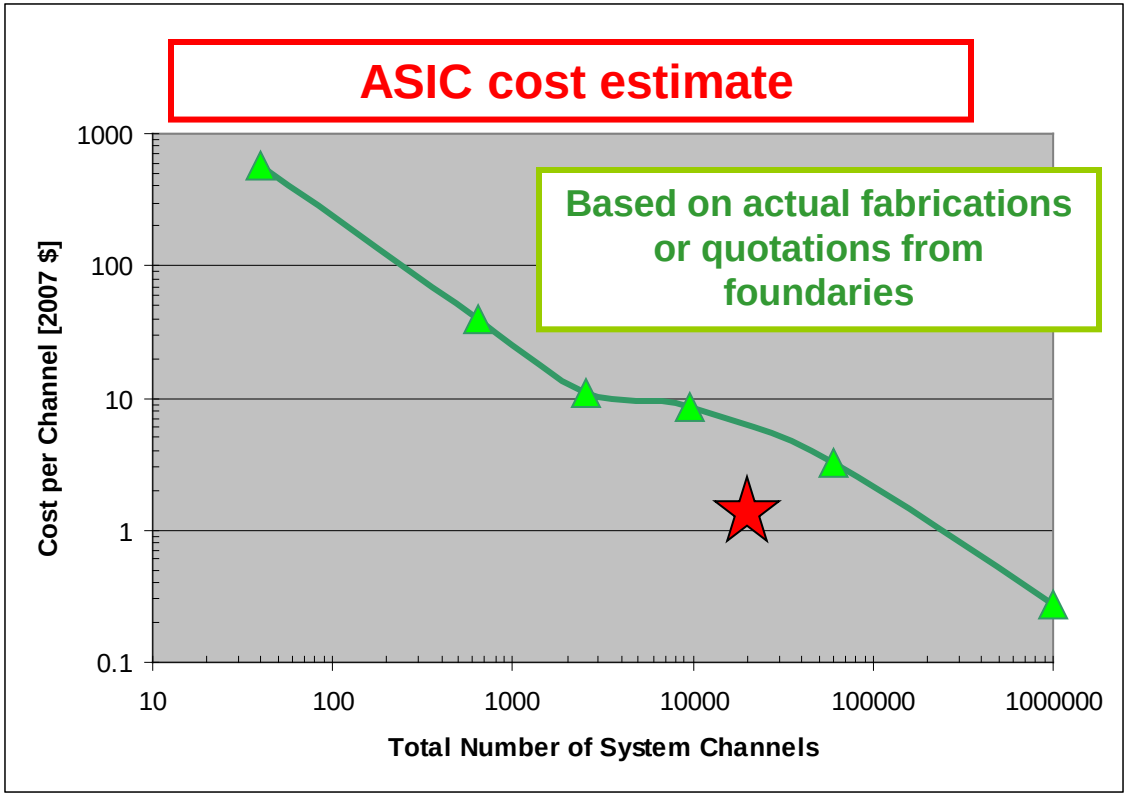
- ~21000 channels of TARGETX deployed for Belle II K-long and Muon system scintillator upgrade
- Each CTA camera 2048 channels
- 256k storage cells per ASIC (>300 million tested)
- 16 channel density attractive for compact sensor arrays (e.g. high-density DIRC …)
- **64 channel version** (SiREAD) in design
- Engineering run quantities: **$1.40/channel** (ADC and trigger on-chip)
- While not for precision timing, **< 100ps**

Looking back on >10 year development

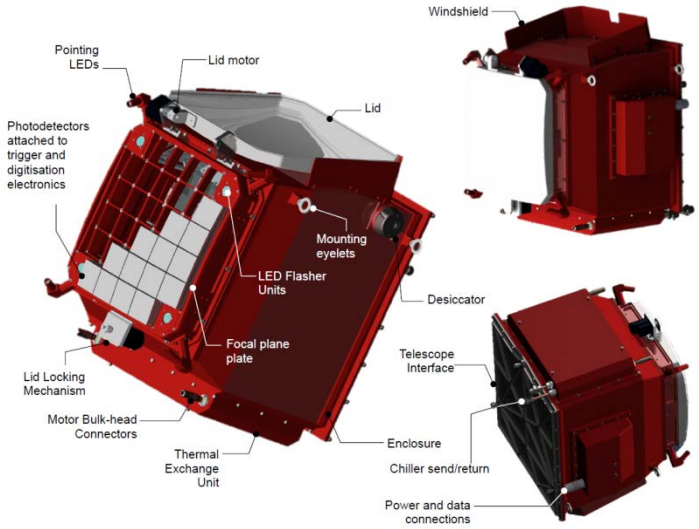
- ASIC costing well understood, very competitive!

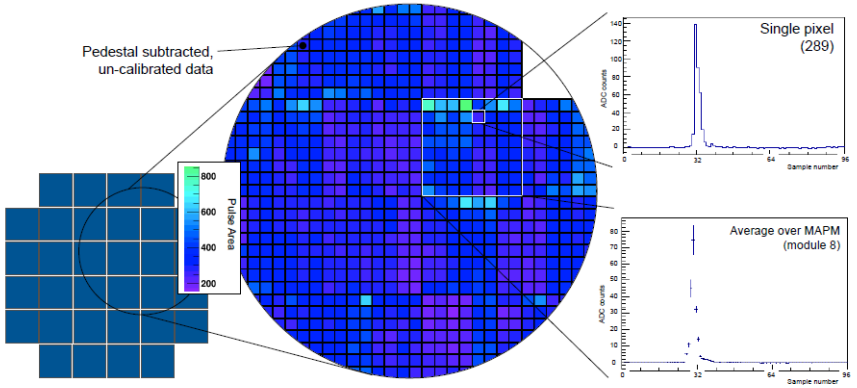
NIM A591 (2008) 534-345.

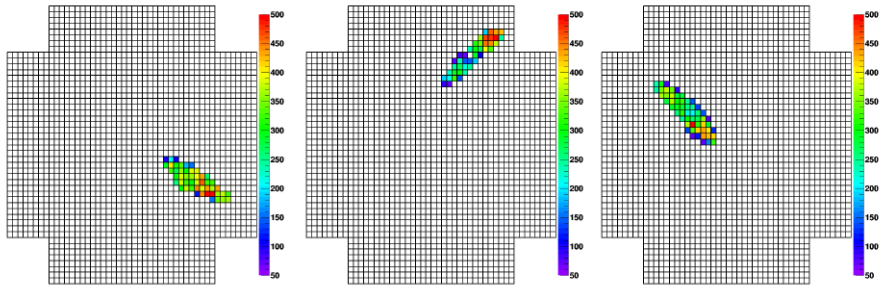


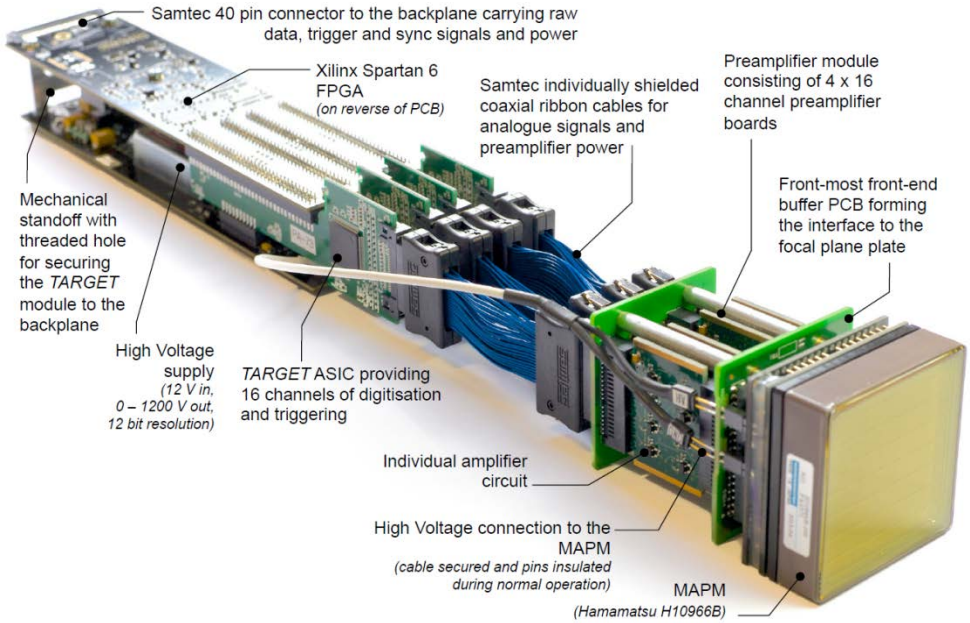


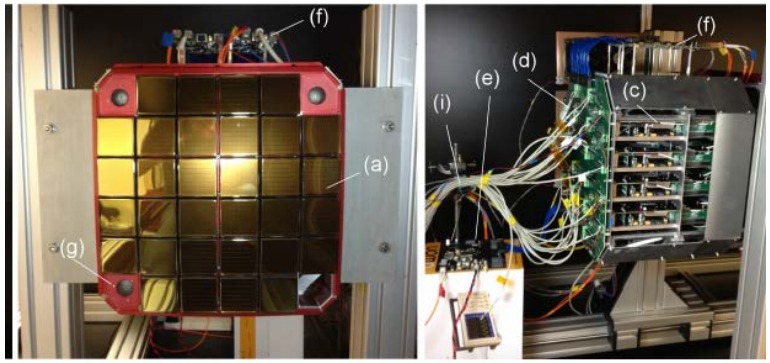
GCT Camera (CTA) – TARGET ASIC



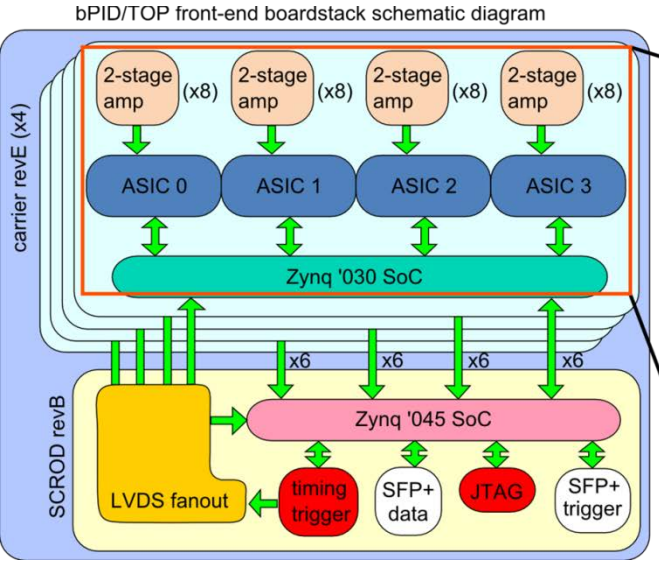


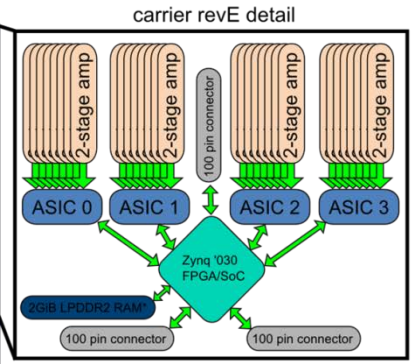




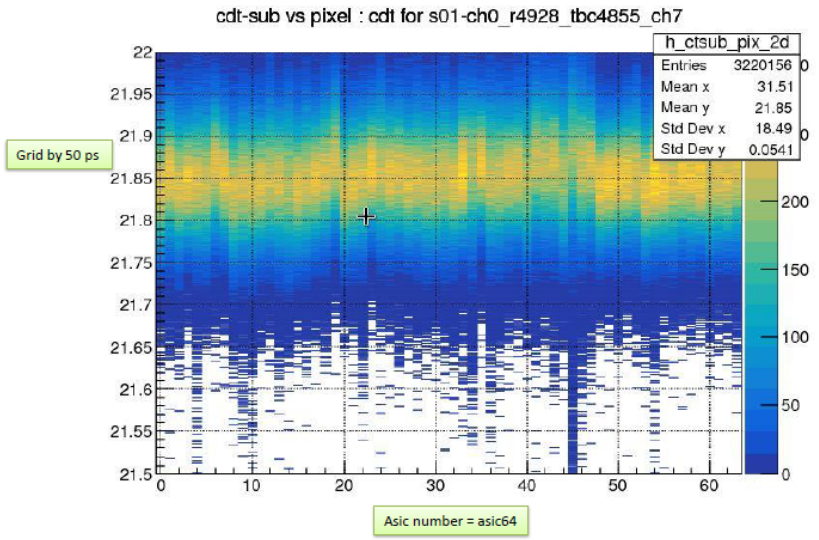


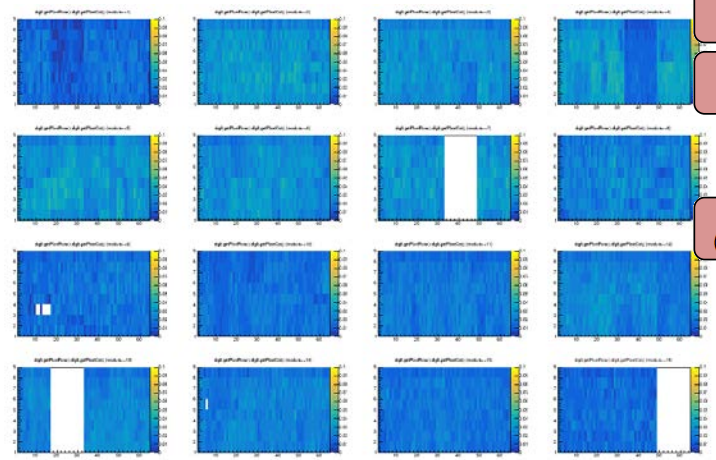
Biggest challenge: Firmware complexity

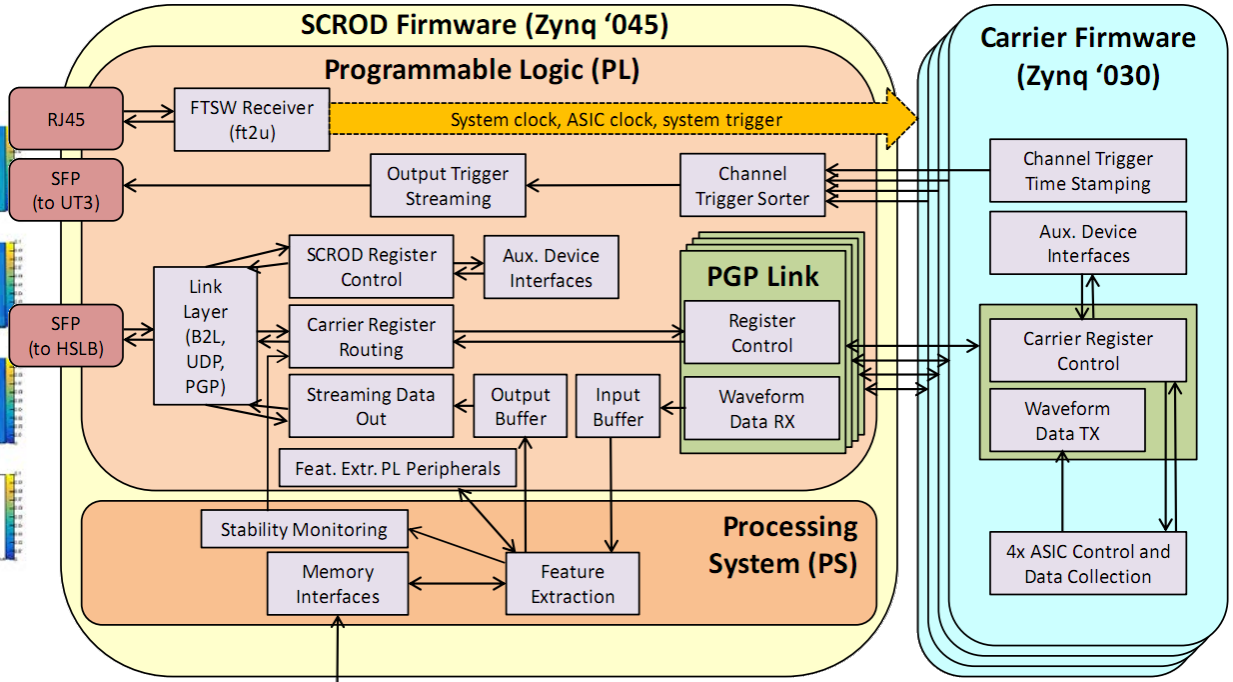




in addition, on the board, there are:
11 voltage regulators
voltage and current monitoring for all regulators
power supply sequencing logic
calibration signal amplification and fanout
automatic fallover wiring to close JTAG chain
temperature sensor (i2c)
EEPROM (i2c)







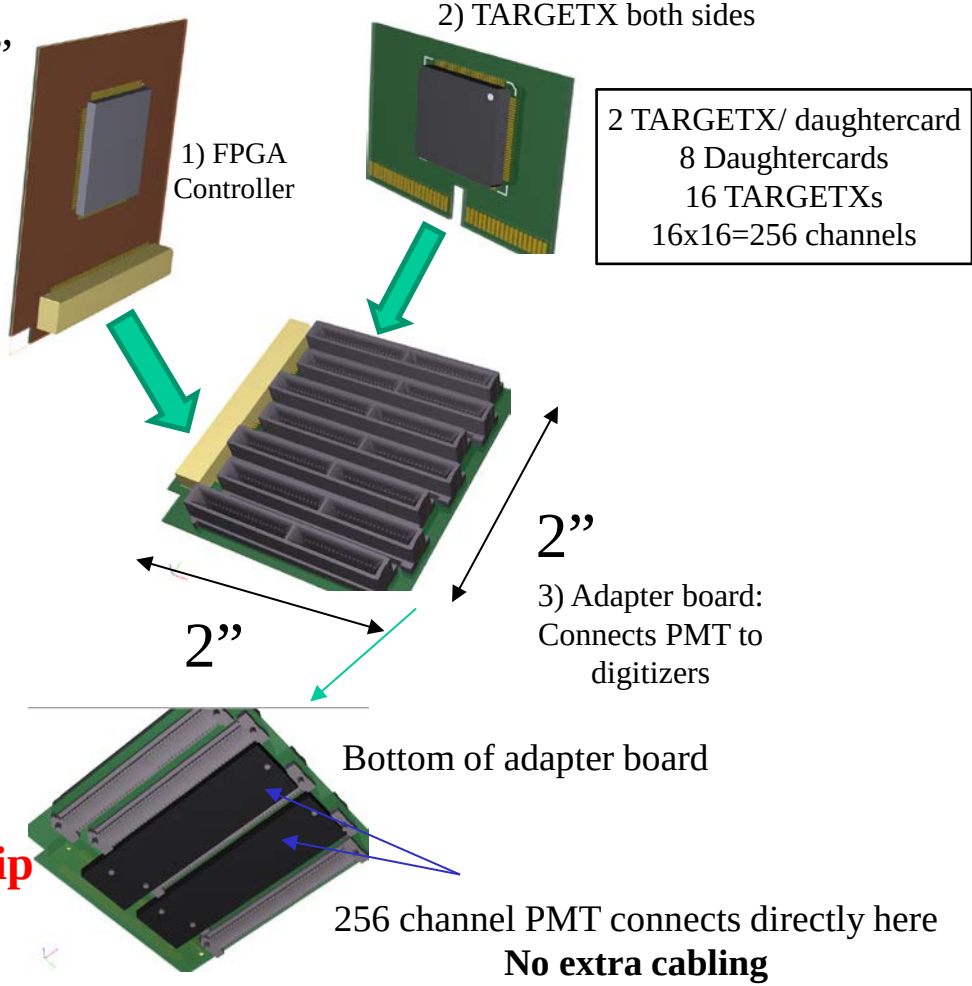
One example: modular RICH readout

Challenge:

- Readout of compact H13700 MCP-PMT
- Compact and dense: 256 channels in 2”x2”
- Timing resolution: ~100ps
- Long buffer
- Abutted Photosensors
- Likely convert to SiPM array later
- Minimize analog cabling

Solution:

- 1st gen prototype based on existing TARGETX ASIC:
  - 1GSa/s full waveform sampling
  - 16 us trigger buffer
  - 16 channels
  - Self triggering capability
  - Low cost 250nm CMOS
  - **Upgrade to 64-channel SiREAD chip**



Nalu Scientific
Data Acquisition Systems

University of Hawai‘i Mānoa

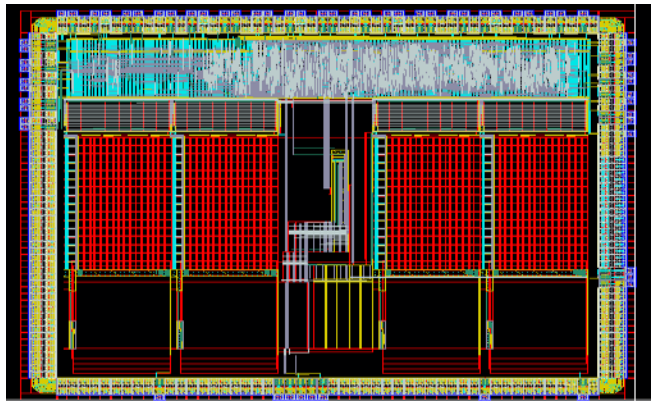
SiREAD in more detail

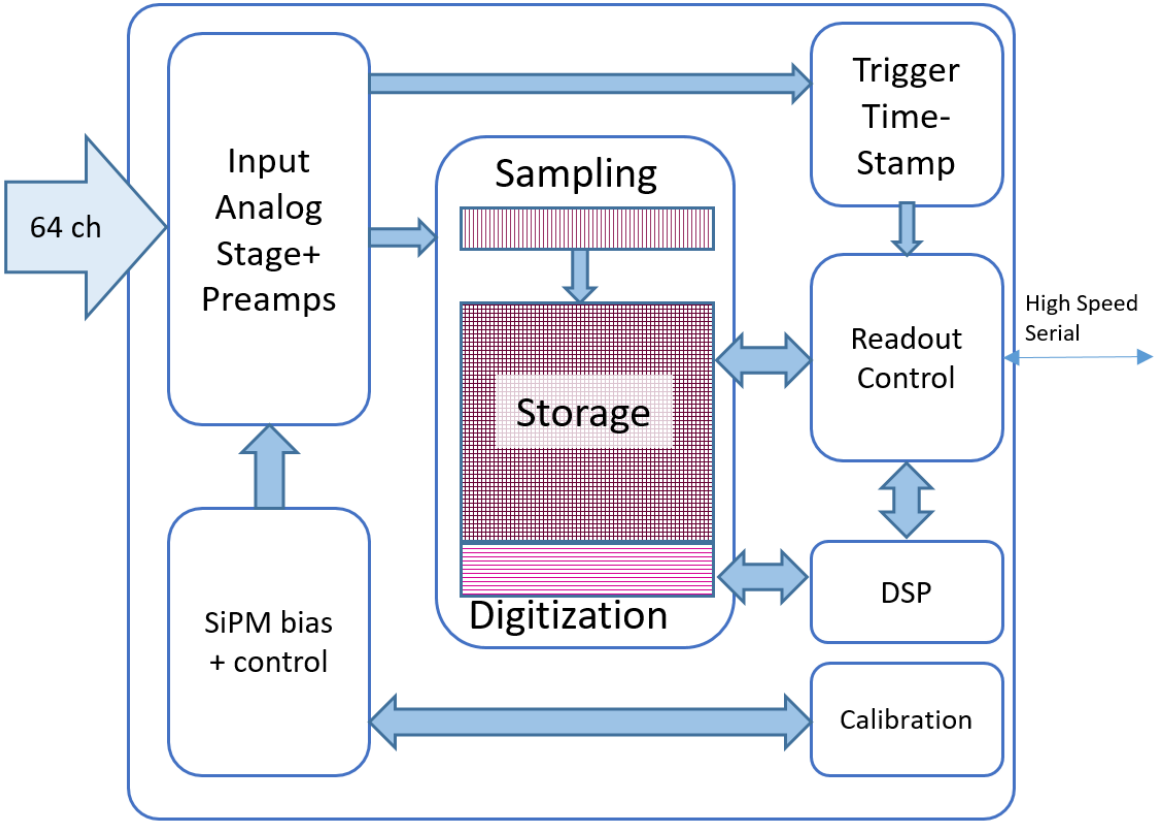
SiREAD

Silicon photomultiplier REadout, Automated calibration and Detection

Nalu Scientific, LLC.
2800 Woodlawn Dr. Ste 298
Honolulu, HI 96822
info@naluscientific.com
Nalu Scientific
Data Acquisition Systems

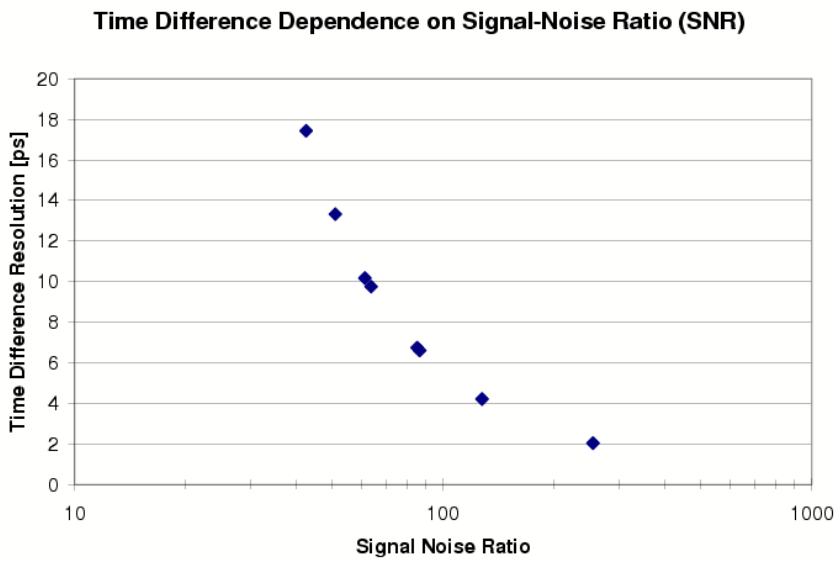
SiREAD Parameter	Specifications
Channels	64
Sampling rate	1-4 GSa/s
Storage samples/ch	4096
Analog bandwidth	0.7-1.1 GHz
RMS voltage noise	<1mV
Dynamic range	10-11 bits
Signal voltage range	2.1 V
ADC on chip	12 bits
Readout	Serial LVDS
Power consumption	20-40 mW/ch





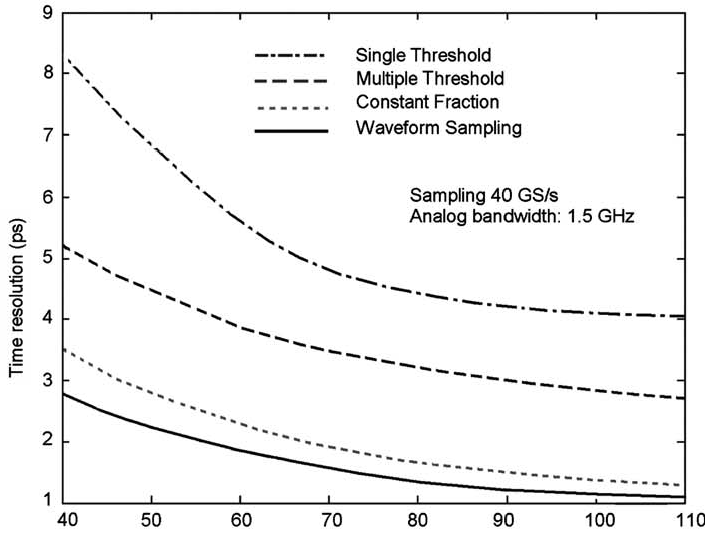
Technology has room to improve

1GHz analog bandwidth, 5GSa/s



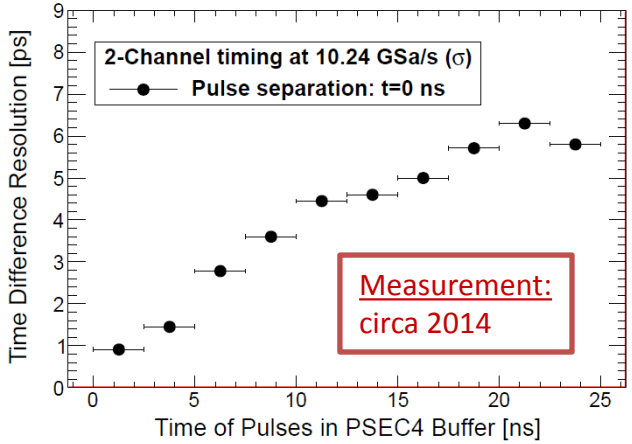
G. Varner and L. Ruckman
NIM A**602 (2009) 438-445**.

Simulation includes detector response



J-F Genat, G. Varner, F. Tang, H. Frisch
NIM A**607 (2009) 387-393**.

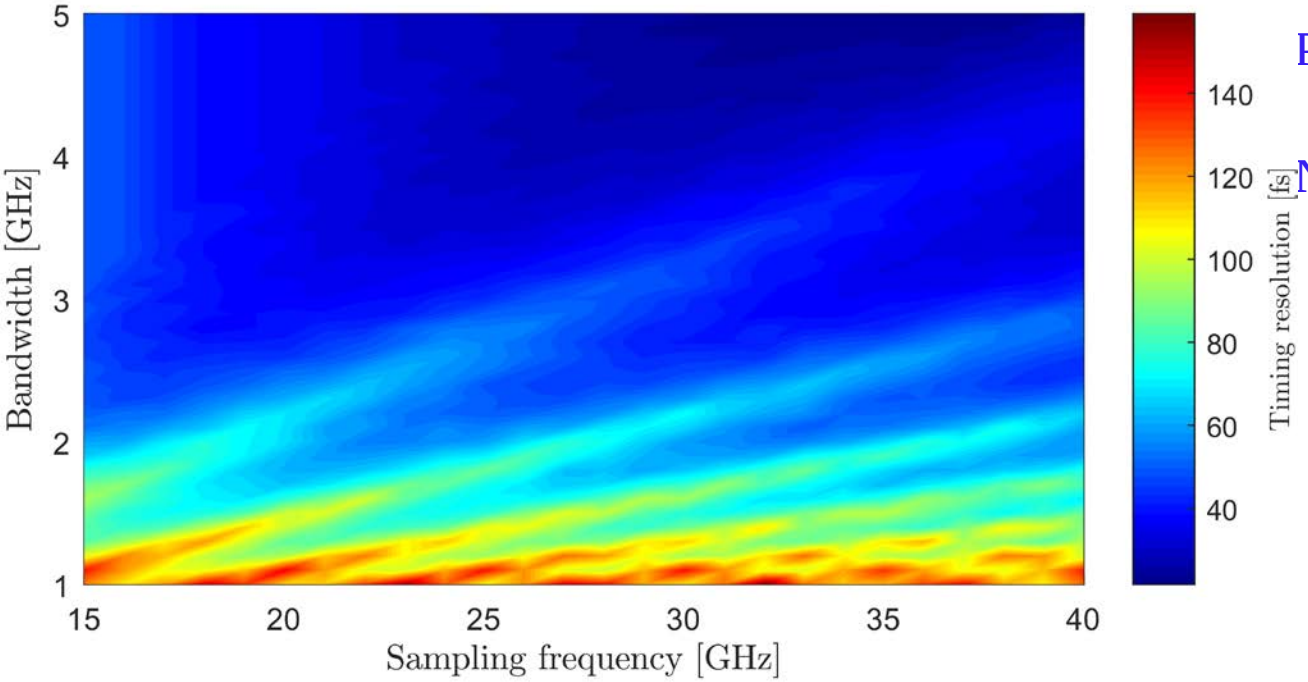
E. Oberla, J-F Genat,
H. Grabas, H. Frisch,
K. Nishimura, G. Varner
NIM A**735 (2014) 452-461**.



Extending to 1ps and lower, with advanced calibration techniques

Now pushing to the femtosecond regime

Pushing sampling speed and analog bandwidth



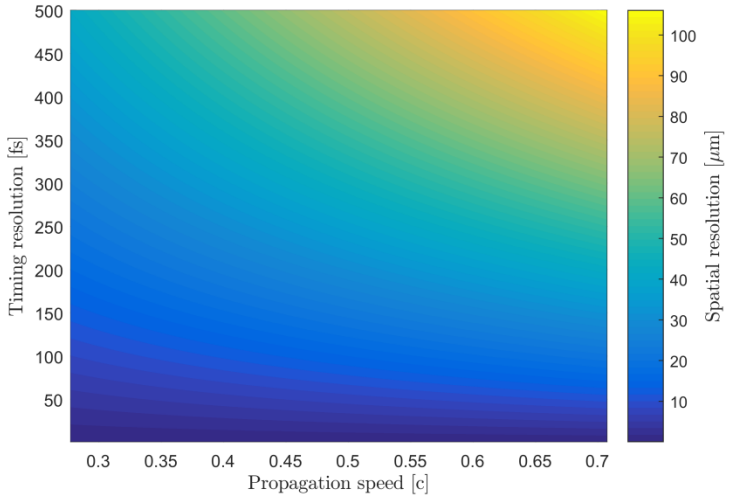
P. Orel, G. Varner and P. Niknejadi

NIM A**857 (2017) 31-41**.

And pushing the **space-time limit**
(new type of PID or DIRC devices?)

P. Orel and G. Varner

IEEE Trans. Nucl. Sci. **64 (2017) 1950-1962**.

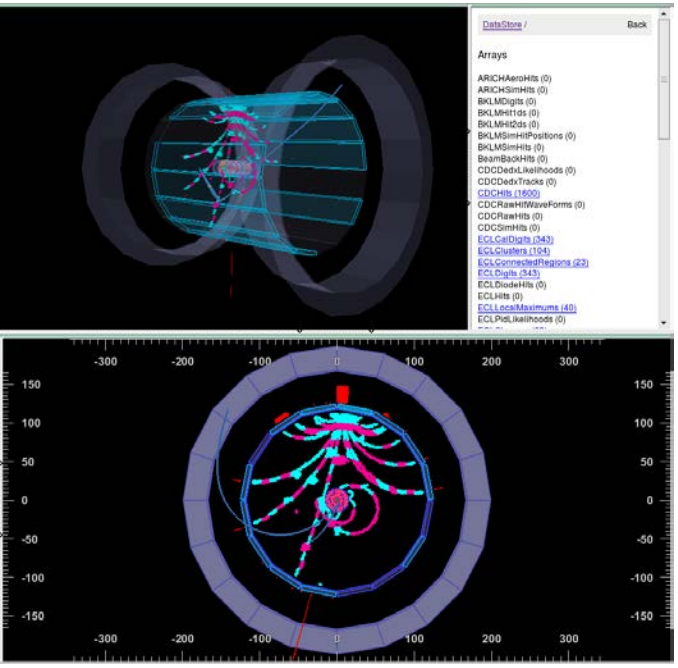


Summary

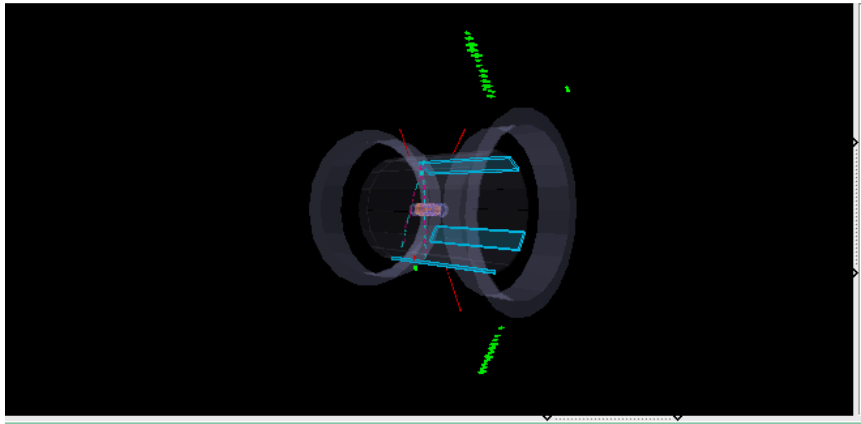
Waveform-sampling readout, directly married to fast detectors has been a Hawaii focus

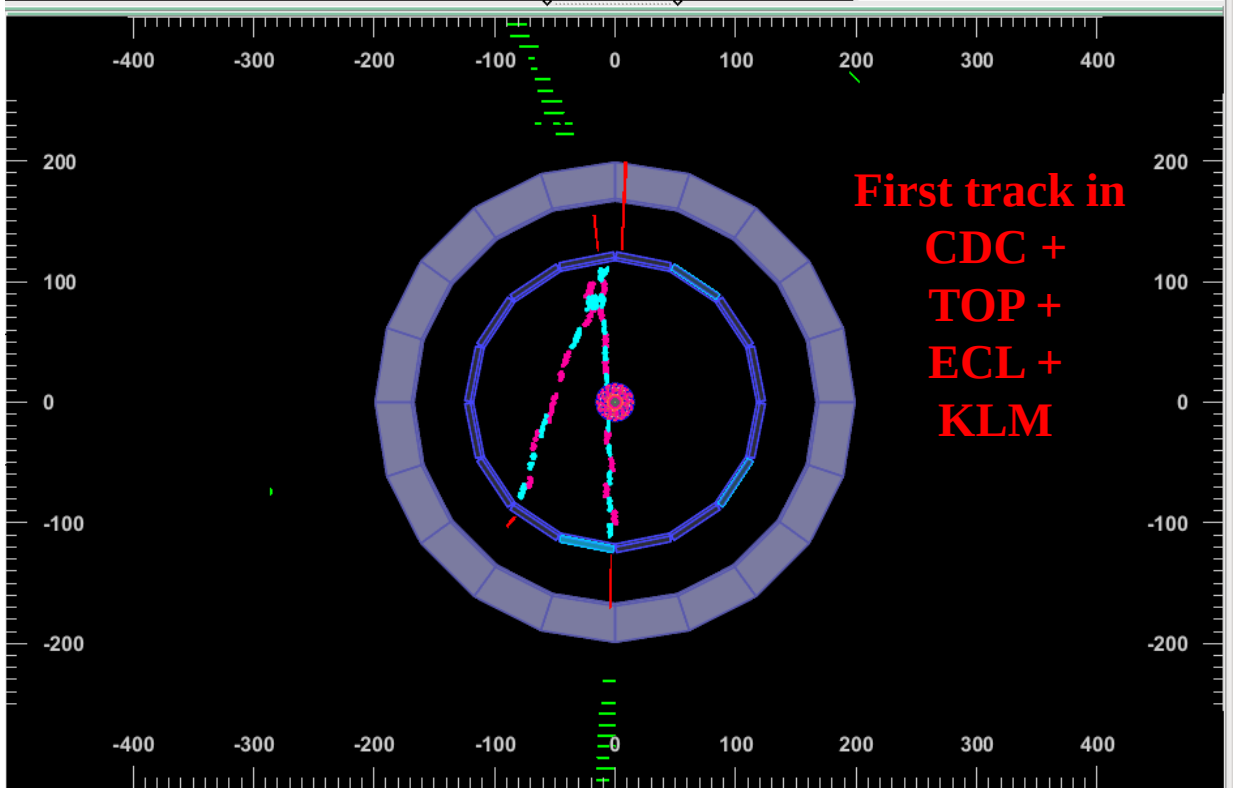
- **Cost for large experiments:**
  - **Reduce cabling, power requirements**
  - **Underlying technology inexpensive, powerful**
- **Performance:**
  - **Space-time photon resolution PD determined**
  - **High rate, pile-up robustness**
- **Maturity:**
  - **Complex firmware biggest headache**
  - **In-ASIC functionality, commercial support**

Backup



First showering Event: CDC + TOP + ECL



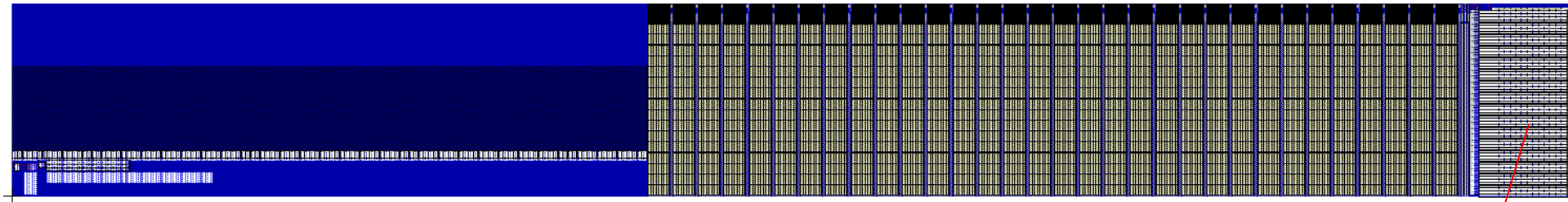


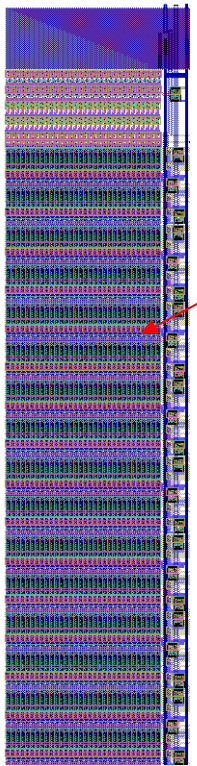
First track in CDC + TOP + ECL + KLM

IRSX Single Channel

- Sampling: 128 (2x 64) separate transfer lanes

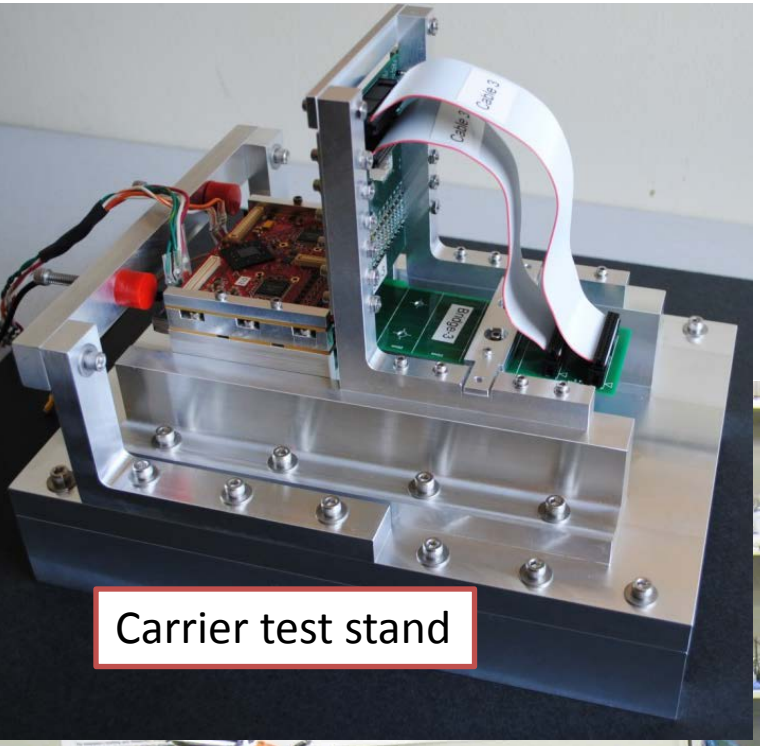
Recording in one set 64, transferring other (“ping-pong”)



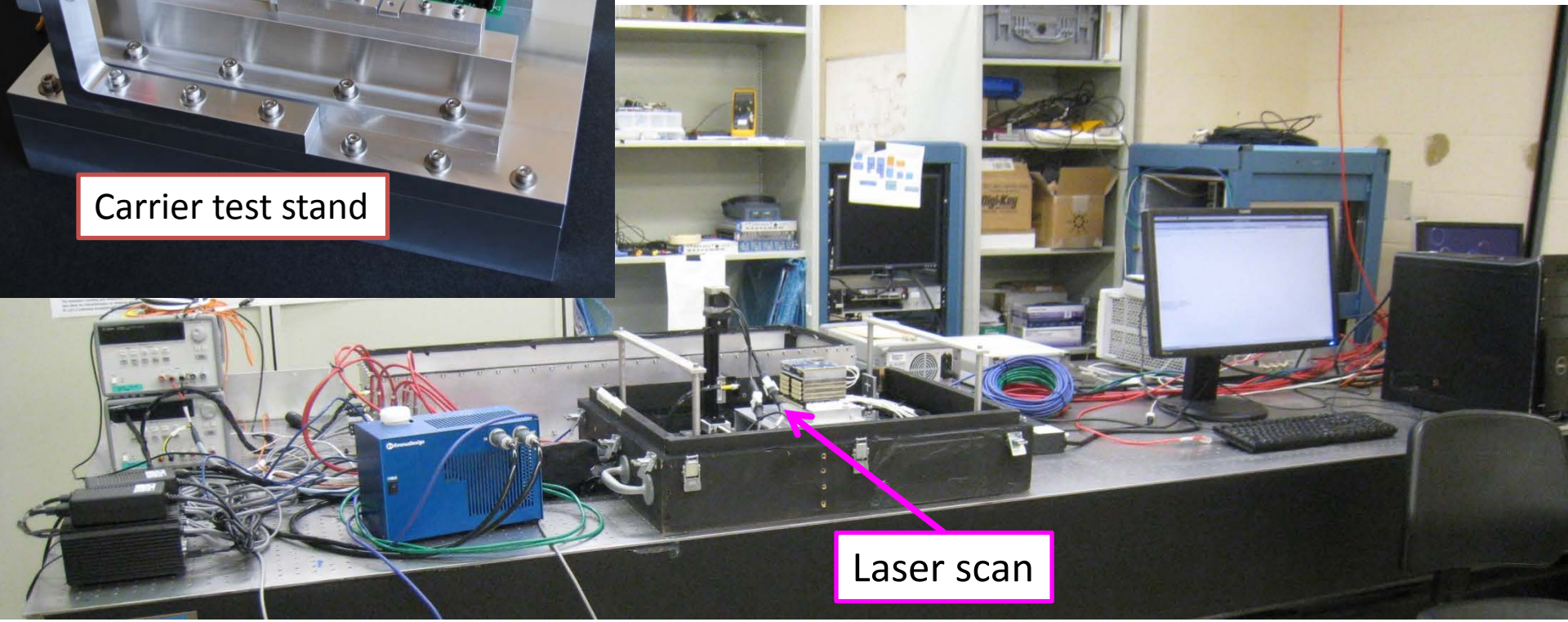


- Concurrent Writing/Reading
- Only 128 timing constants
- Storage: 64 x 512 (512 = 8 * 64)
- Wilkinson (64x1): was (32x2)
- 64 conv/channel

iTOP Readout Production Testing



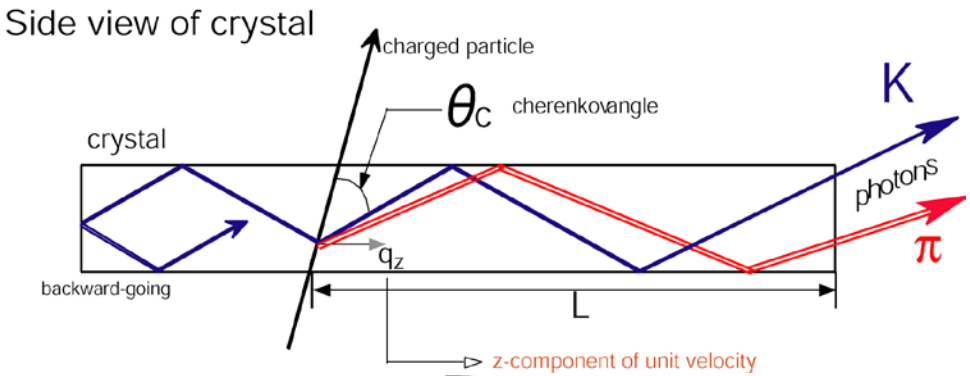
- **2x Carrier test stations at South Carolina, 1x backup in Hawaii**
- **Laser test stand Hawaii**
- **SCROD test stand in Pittsburgh**
- **Firmware test at PNNL**

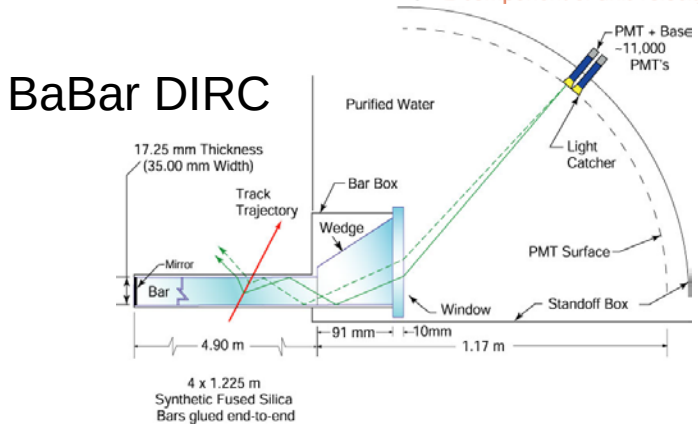


imaging TOP (iTOP)

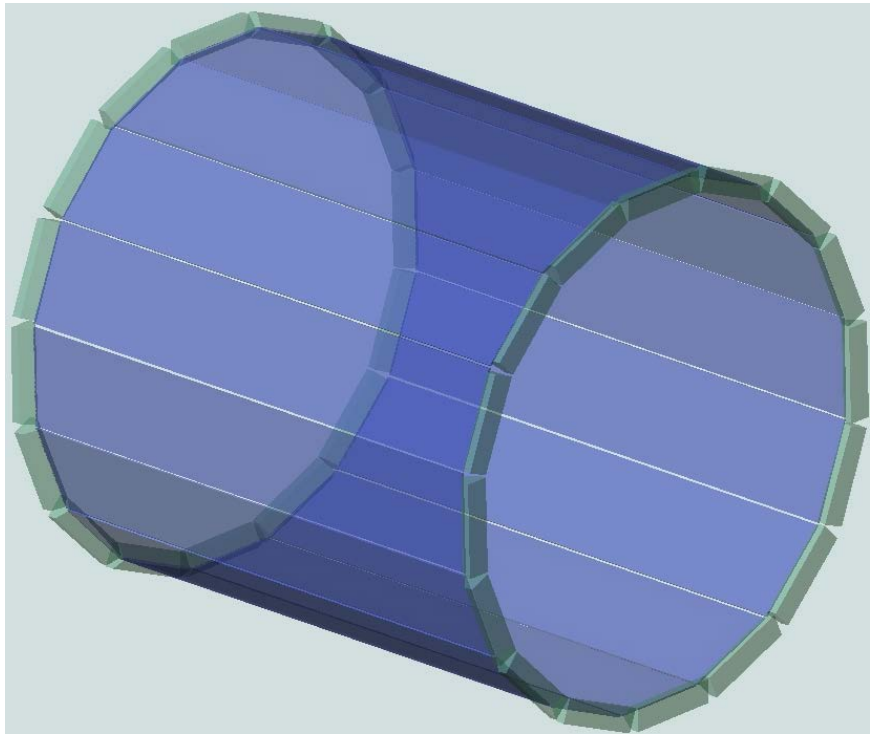
Concept: Use best of both TOP (timing) and DIRC while fit in Belle PID envelope

NIM A623 (2010) 297-299.





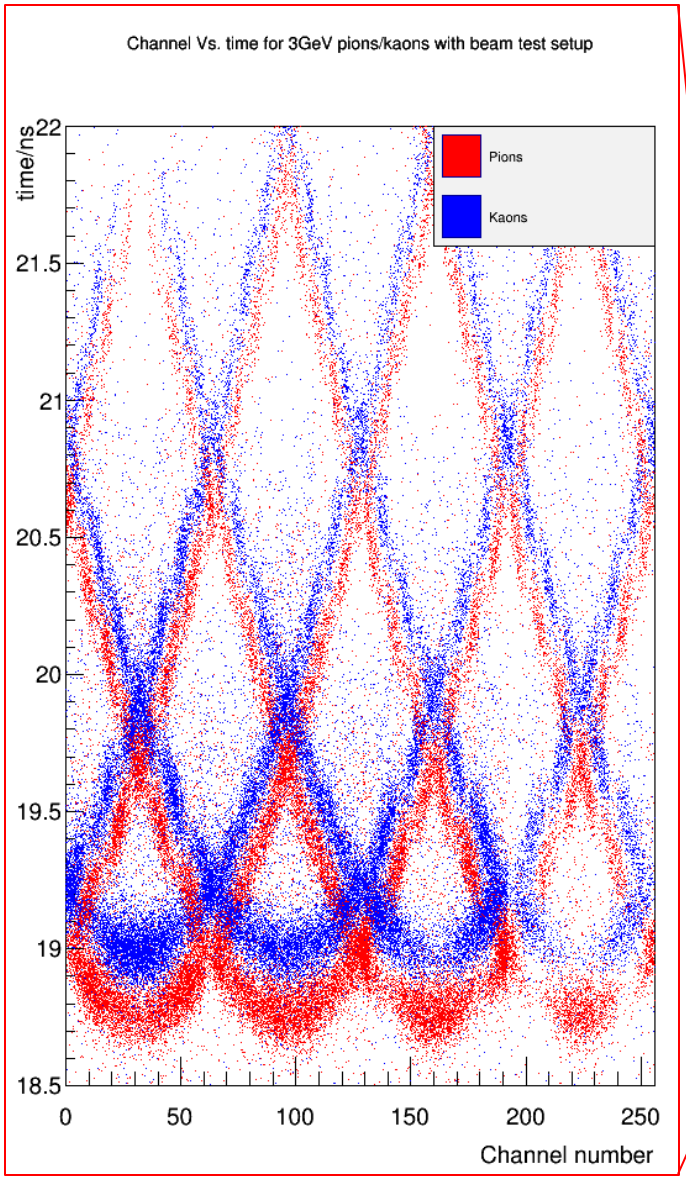
Use wide bars like proposed TOP counter

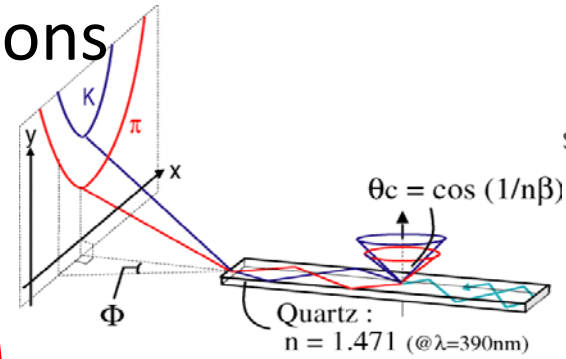


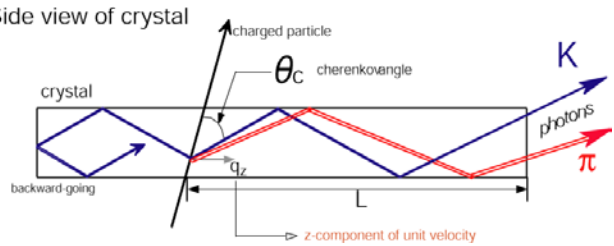
- Use new, high-performance MCP-PMTs for sub-50ps single p.e. TTS
- Use simultaneous T, θc [measured-predicted] for maximum K/π separation
- Optimize pixel size

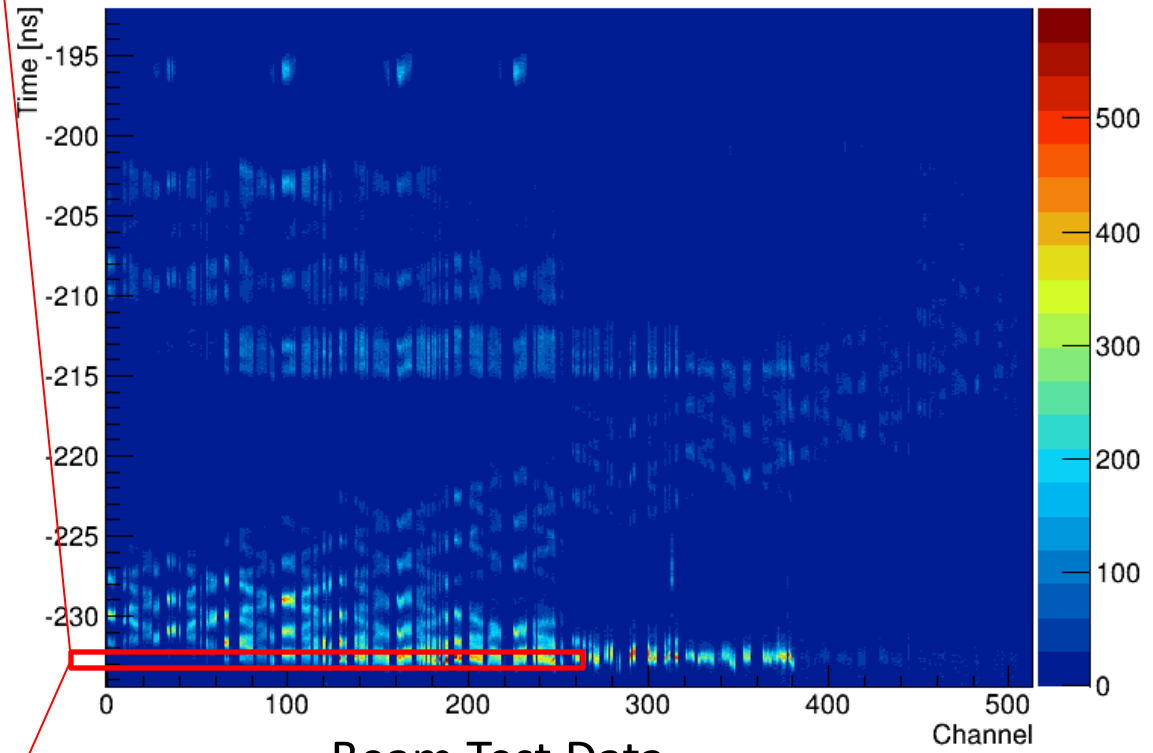
iTOP relativistic velocity

- Space-time correlations







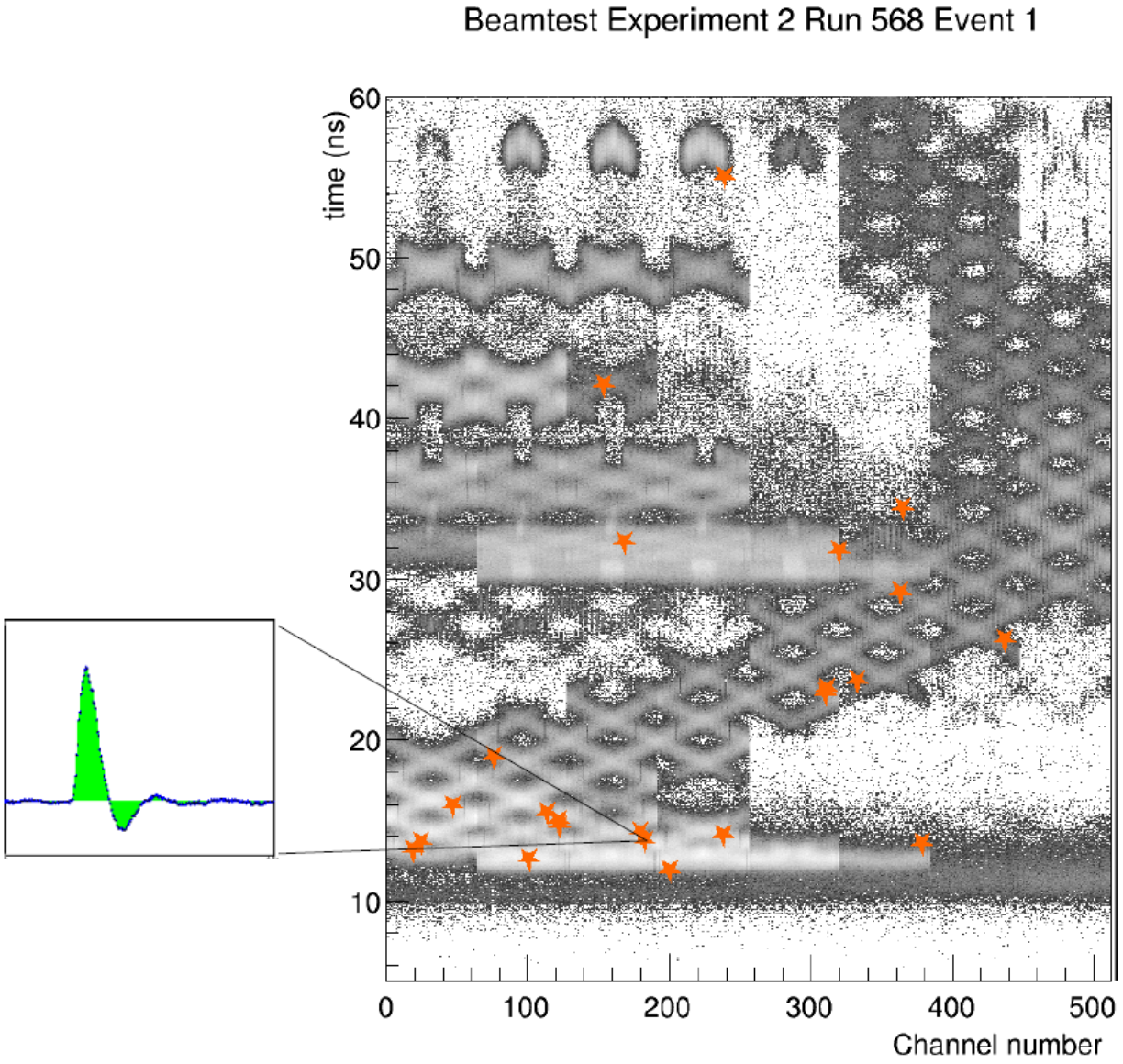


Beam Test Data

These are cumulative distributions

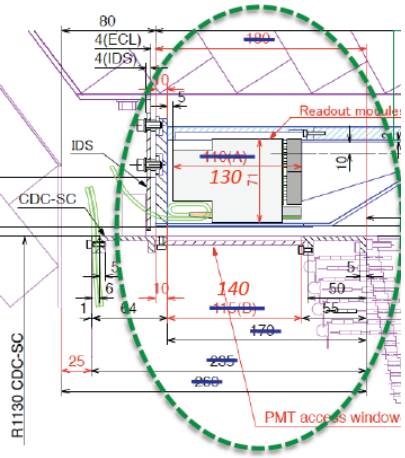
Actual PID is event-by-event

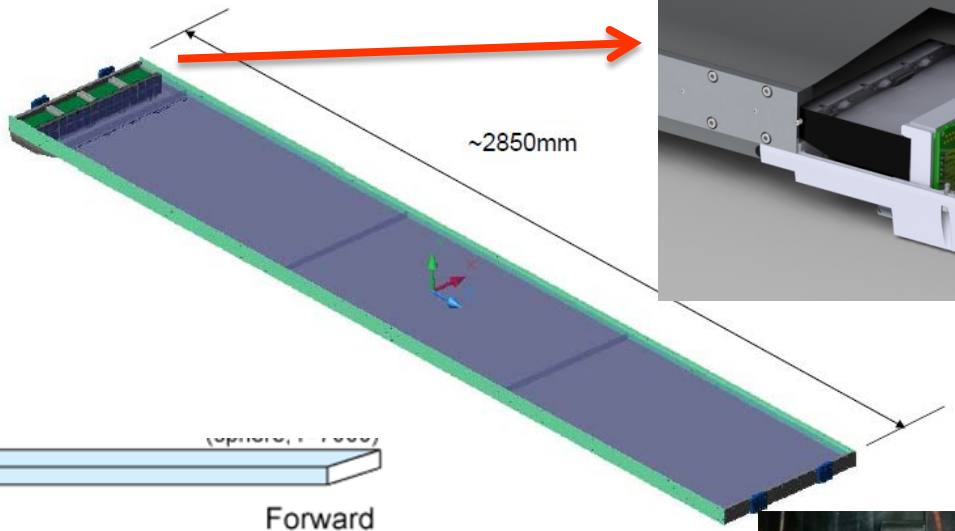
- Test most probable distribution

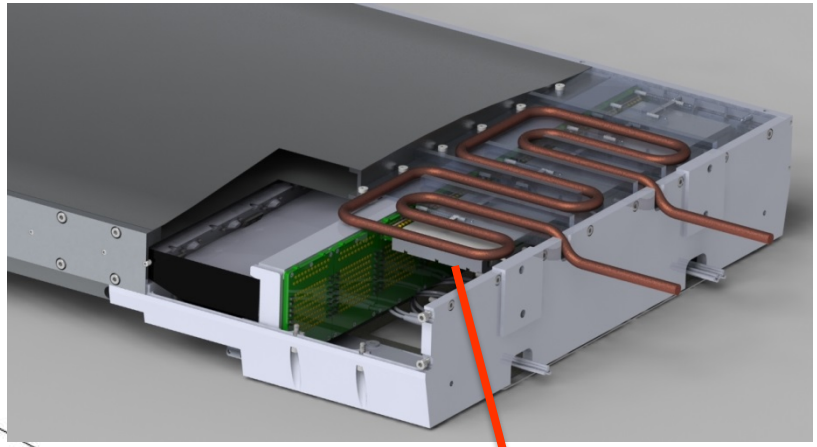


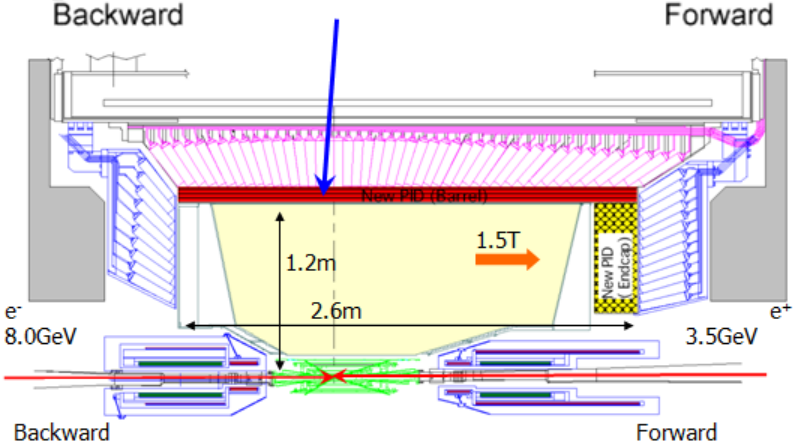
Highly integrated services

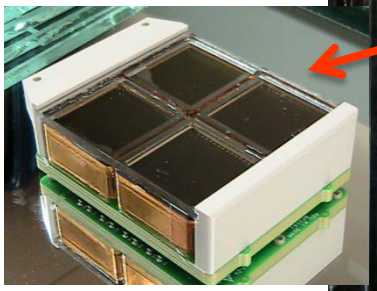
- A severely constrained space

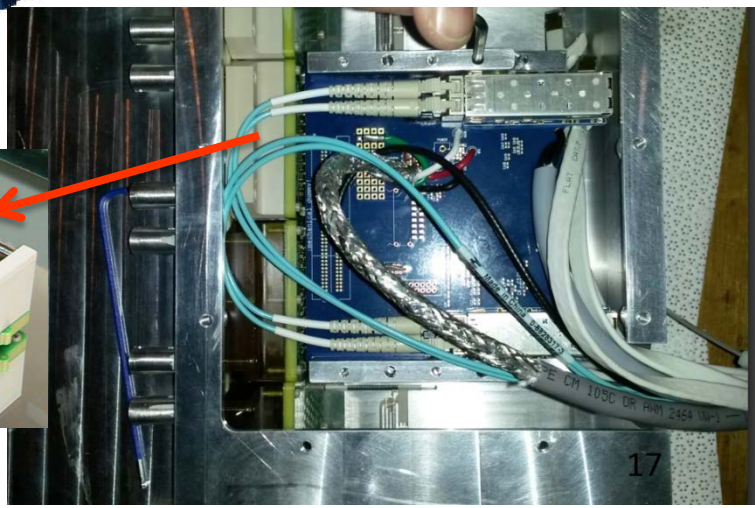








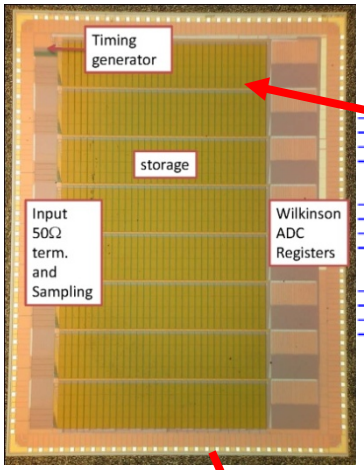


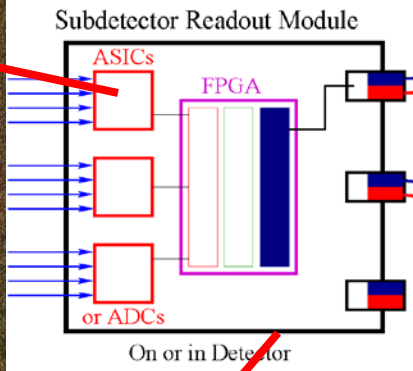


imaging TOP Readout (FDIRC proto)

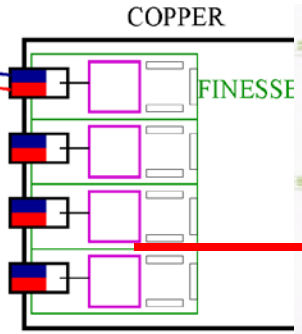
Waveform sampling ASIC

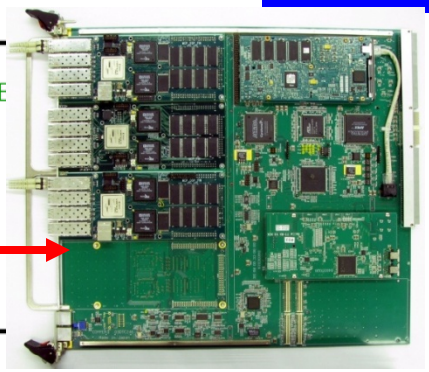
64 DAQ fiber transceivers



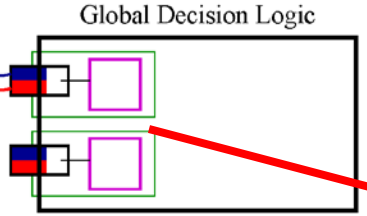


Giga-bit Fiber Transceiver Links





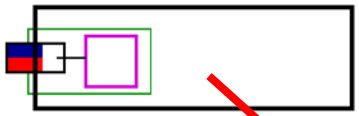
64 FINESSE
16 COPPER



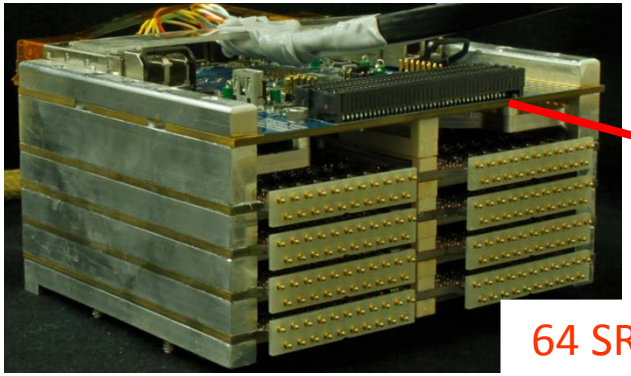
2x UT3 Trigger modules

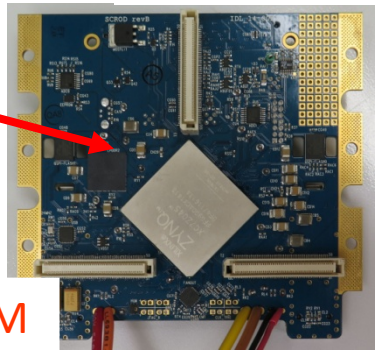
FPGA firmware consists of 3 parts:
1) ASIC/ADC driver (common)
2) Trigger feature extract (subdet. specific)
3) Unified DAQ transport protocol

8k channels
1k 8-ch. ASICs
64 "board stacks"



Low-jitter clock



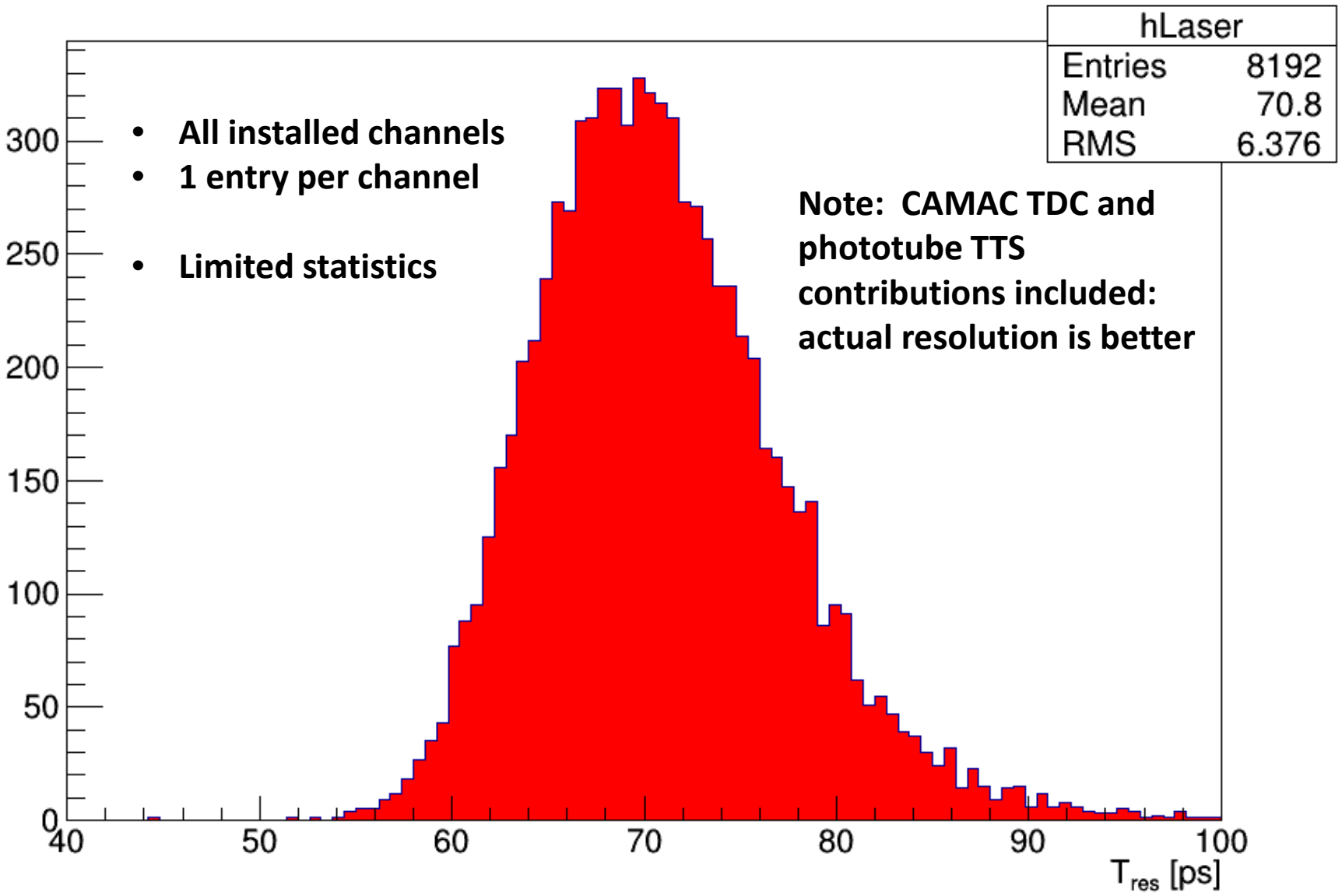


64 SRM

Clock, trigger, programming module (FTSW)

8 FTSW

Production – initial single photon timing



Incubated at the Manoa Innovation Center Near University of Hawaii

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Photo: http://www.myhawaiirealestateonline.com/manoa-real-estate/

UV Imager

IEEE/NSS 2016

A prototype 32 channel front end electronic readout system for an UV imaging detector

poster N08-16

A. Seljak [1], G. S. Varner [1], H. S. Cumming [1*], J. Vallerga [2] and R. Raffanti [3]

[1]Department of Physics, University of Hawai'i at Manoa, Honolulu, Hawaii, USA
[2]Space Sciences Laboratory, University of California, Berkeley, California, USA
[3]Techne Instruments, Oakland, California, USA
* Former member

1. Motivation:

2. Readout principle:

3. ASICs design:

CSAv3 – Programmable charge sensitive amplifier

Specifications:

- 16 input channels
- 10mv/fC gain (nominal)
- ~50ns FWHM pulses (without baseline under/over shoot)
- 5mW/channel
- Programmable settings
- Test pulse injection
- 130nm TSMC Technology
- QFN 68 package

Amplifier schematic

Amplifier output as a function of time for different settings

Amplifier output as a function of input charge

Channel layout

ASIC layout

Noise as a function of detector capacitance

Gain distribution for 16 channels

HalfGraph- 1 GS/S sampler and digitizer

Features:

- 16 input channels
- 1 GS/s
- 8us memory / channel
- 12bit Wilkinson converter
- Threshold programmable triggers (4 signal over threshold groups)
- Allows conversion and transmission simultaneously

Architecture:

- Serial shift register for slow control
- Programmable trigger logic
- Sampling windows
- Storage windows
- Routing multiplexer for data output streams.
- 8 ch LVDS serial data output
- TSMC 250nm technology
- LQFP 144 pin package

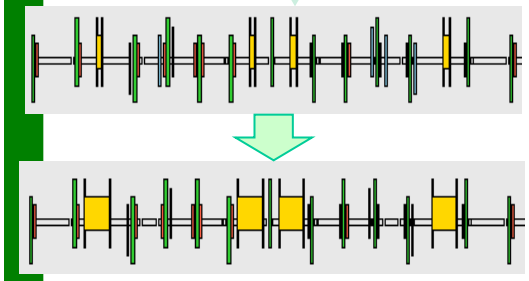
Schematic of the sampling base

Schematic of the HalfGraphV2 chip

5. Future prospect

KEKB to SuperKEKB

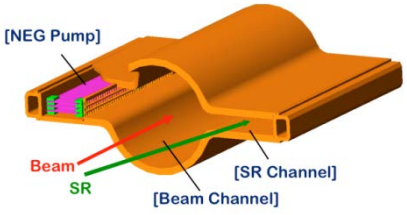
Replace short dipoles with longer ones (LER)

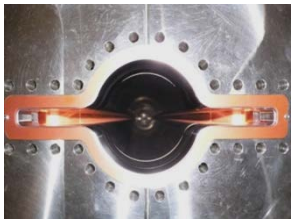


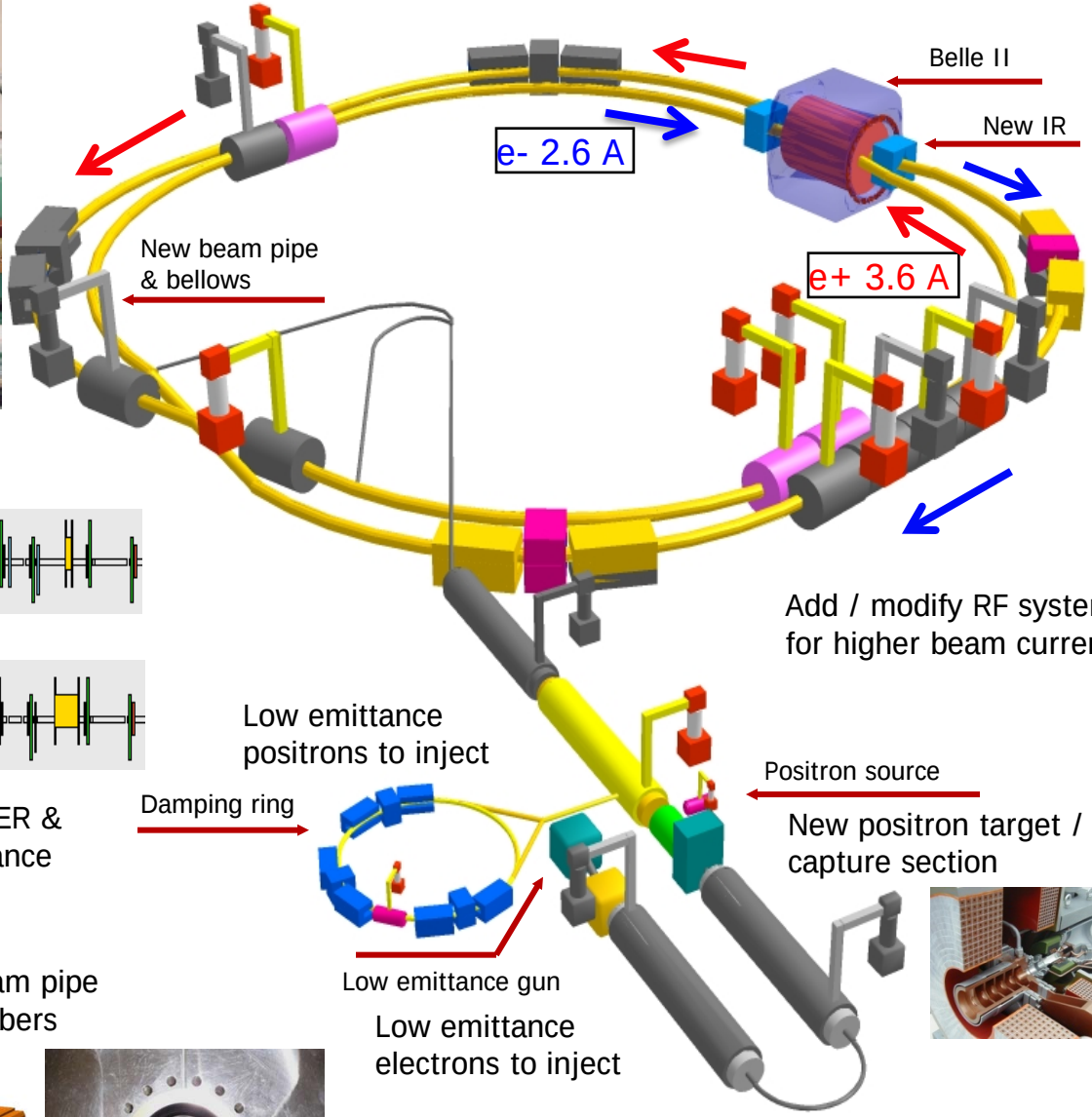
Redesign the lattices of HER & LER to squeeze the emittance

Nano-beams!

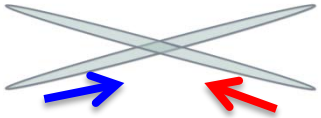
TiN-coated beam pipe with antechambers



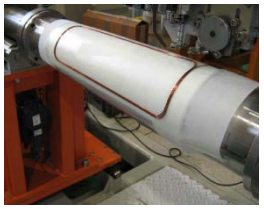




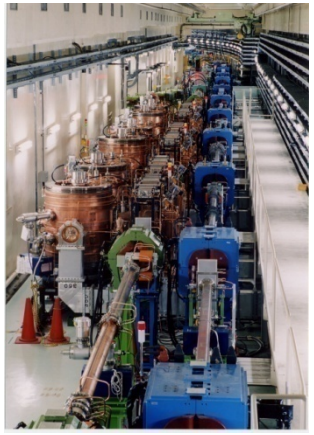
Colliding bunches



New superconducting /permanent final focusing quads near the IP



Add / modify RF systems for higher beam current

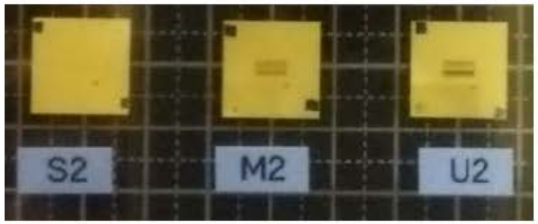


New positron target / capture section

To get x40 higher luminosity

XRM: Hardware

X-ray beam line under construction at LER

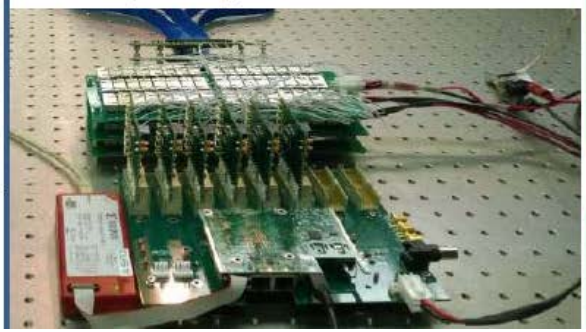


Masks: ~20 μm Au on 600 μm CVD diamond substrate

Water-cooled mask holder

US-Japan Collaboration (U. Hawaii, SLAC, Cornell U.)

High-speed readout electronics for the X-ray monitor, being developed by U of Hawaii.



Deep Si pixel detector and spectrometer chips for the X-ray monitor, being developed at SLAC.