UNIVERSITY OF MICHIGAN

HEP ASIC Projects @ University of Michigan

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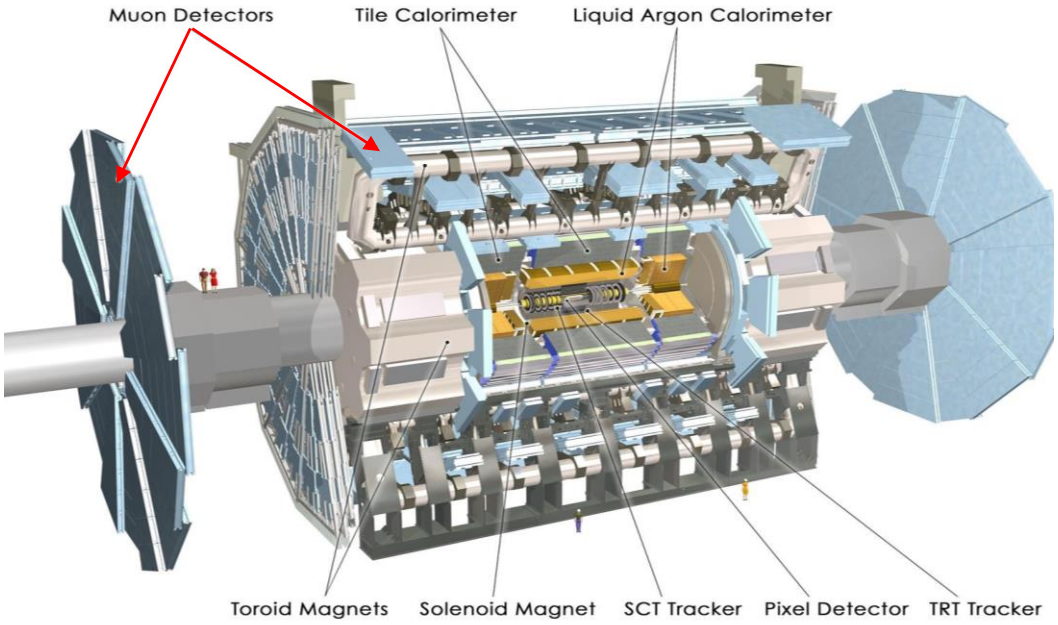
On behalf of the UM ATLAS Group

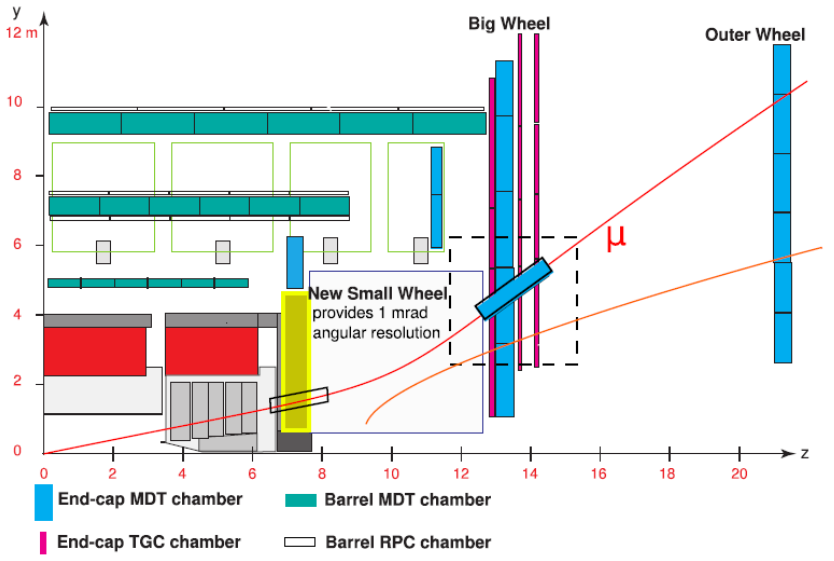
Oct. 4th, 2017

Two ASIC Projects at UM

❖ **Two ASIC projects on the upgrade of the ATLAS Muon Spectrometer**

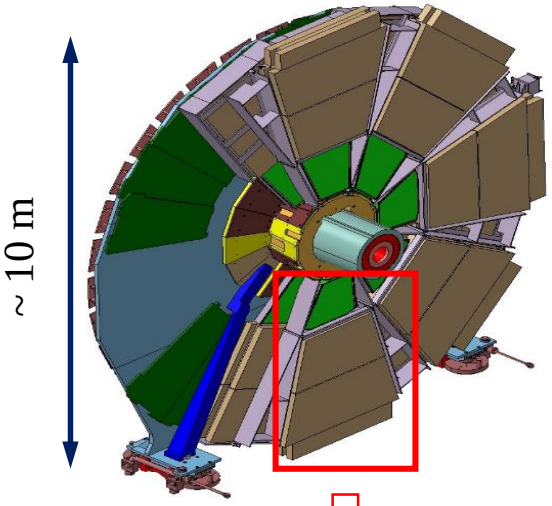
- **Phase-1 Upgrade (2019~2020): New Small Wheel**
  - **Design of a Trigger Data Serializer for the sTGC detector**
- **Phase-2 Upgrade (2024 ~ 2026): Replace Trigger and Readout Electronics**
  - **Design of a Time to Digital Converter for the upgrade of the MDT electronics**



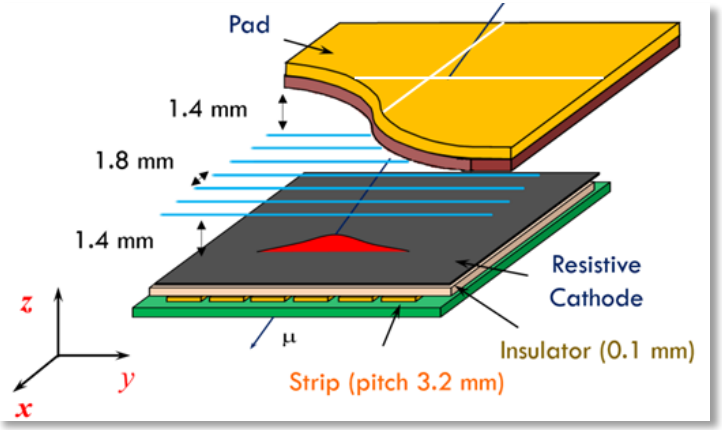


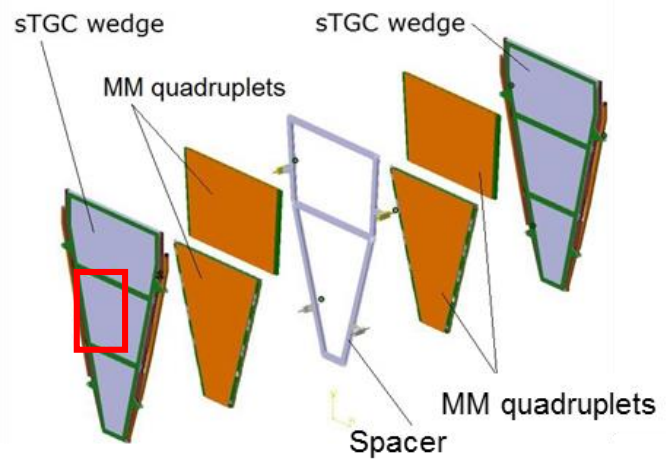
NSW in the ATLAS Phase-1 upgrade

- **Micromesh Gaseous Detector, Micromegas (MM)**
  - Primary precision tracker
  - Strips (~0.5mm pitch)
  - Position resolution <100 μm
  - Redundant triggering
- **Small-strip Thin Gap Chamber**
  - Primary trigger detector (pads/strips)
  - Region of interest determination (pads)
  - Angular resolution < 1 mrad (strips)
  - Phi position measurement (wires)



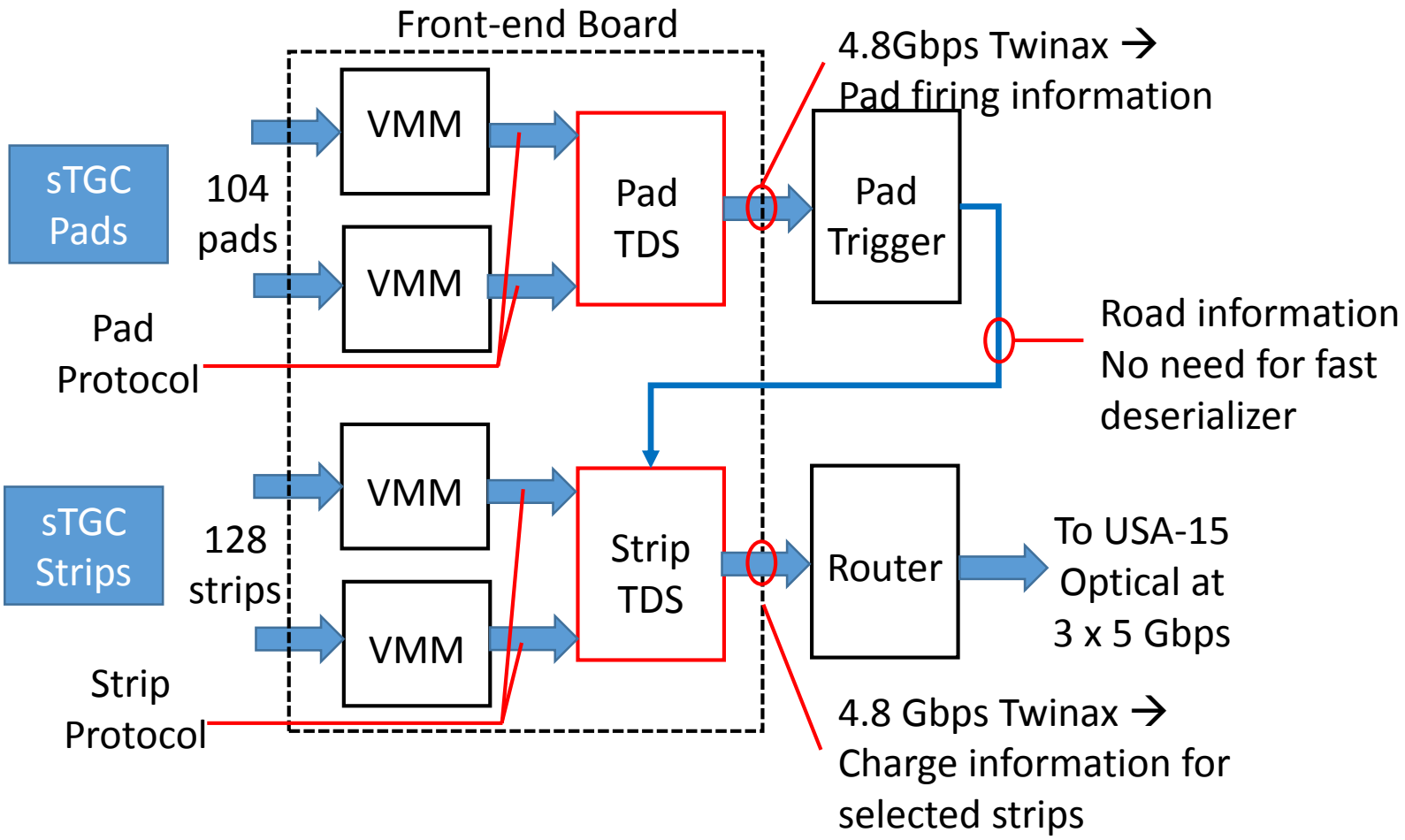
- **Trigger**
  - PAD signal selects strip region
  - Selected strips sent for triggering
- **Tracker**
  - Combine strips and wires



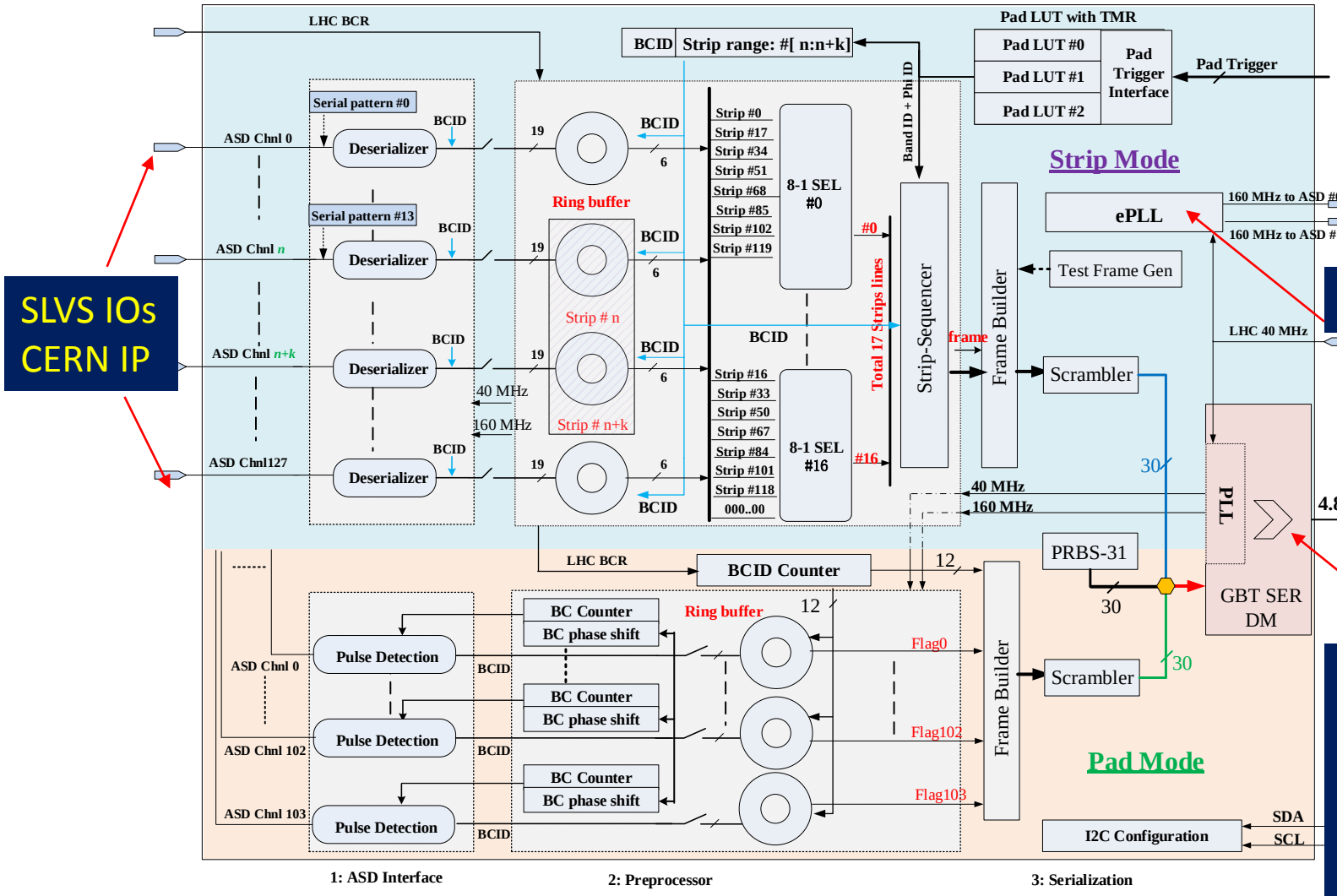


Design of a Trigger Data Serializer

- **Function**:
  - Prepare trigger data for both sTGC pads and strips, perform pad-strip matching, serialize trigger data to FPGA processing circuits on the rim of the NSW.
  - One chip with two modes: pad-TDS, strip-TDS



Design of the Trigger Data Serializer



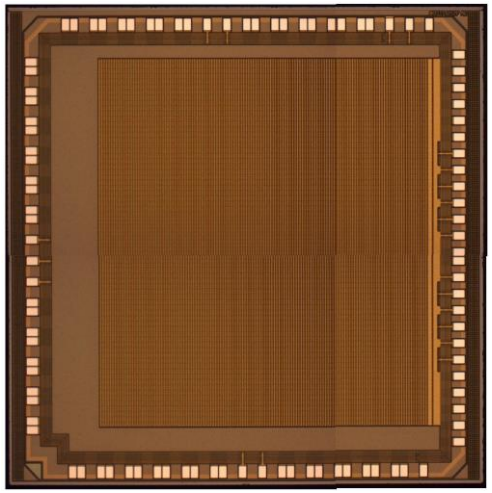
SLVS IOs CERN IP

ePLL, CERN IP

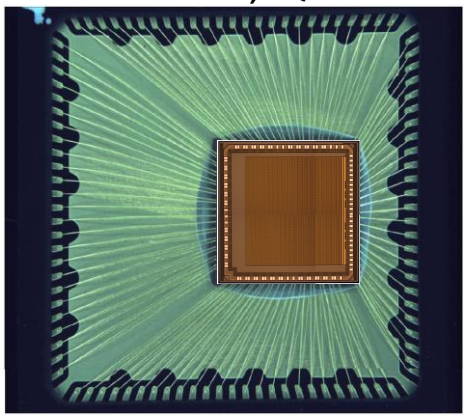
Serializer with significant modifications from the original CERN design

- IBM 8RF-DM 323, 130 nm CMOS; 1.5 Volt supply, < 1 W ; BGA 400 package
- 128 channels in strip mode; 104 channels in pad mode
- 4.8 Gbps serial output; 640 Mbps trigger info. inputs

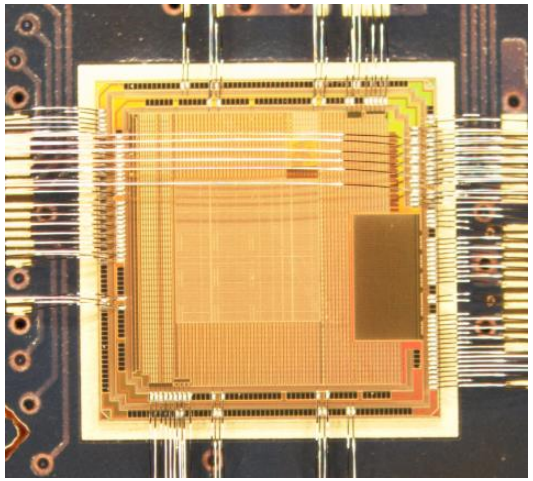
Prototypes of TDS



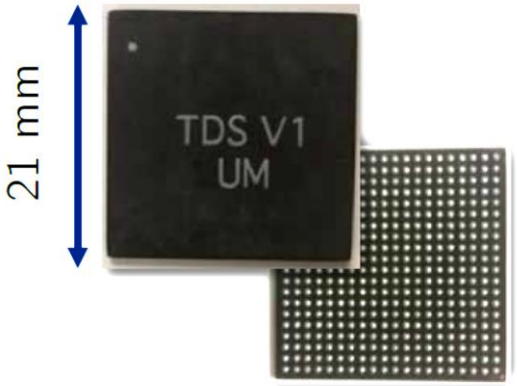
the GBT Serializer
@ Feb. 1st, 2014
~4X4 mm², QFN100



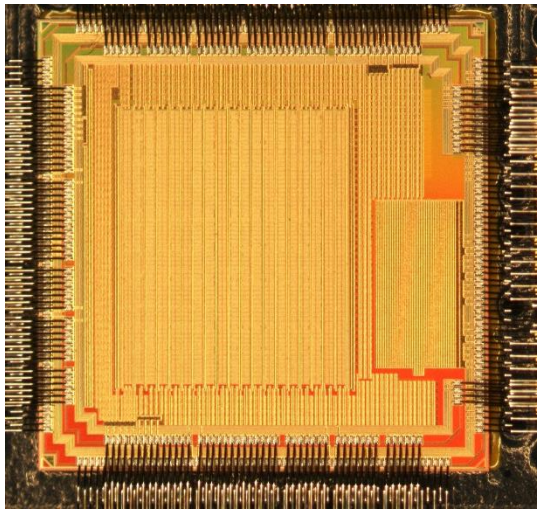
Originated from the CERN design
*architecture + metallization change



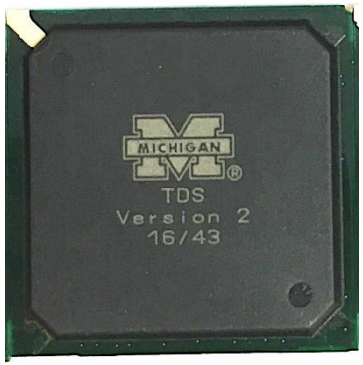
TDS V I
@ August. 19th, 2014
~5.2 x 5.2 mm², BGA 400



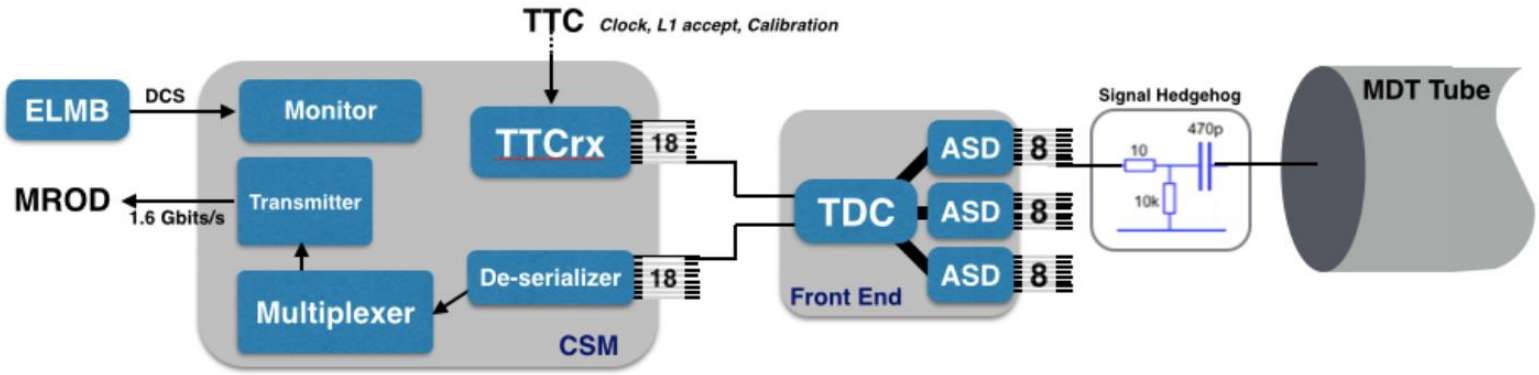
*major specification changes



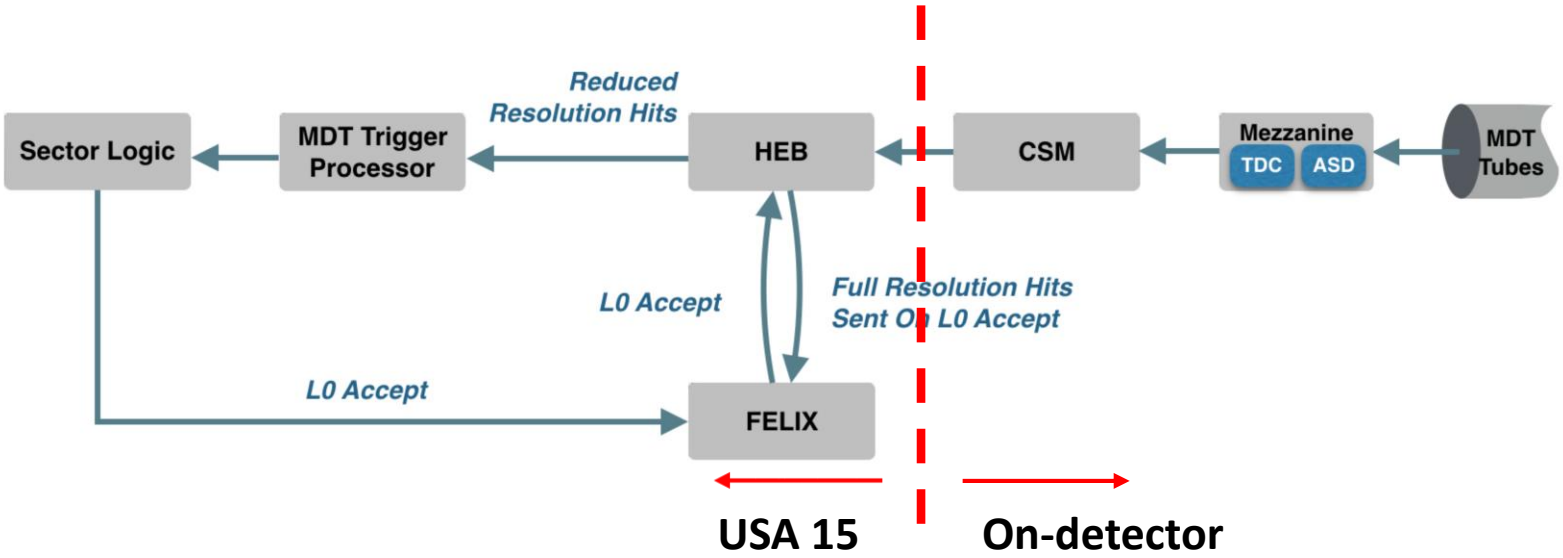
TDS V II
@ May 1st, 2015
~5.2 x 5.2 mm², BGA 400



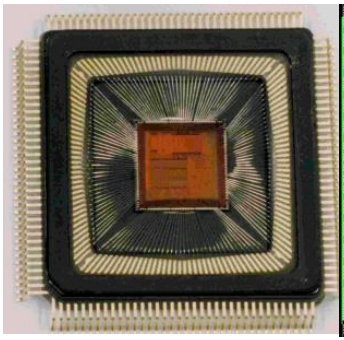
MDT Frontend Electronics Upgrade in Phase-2



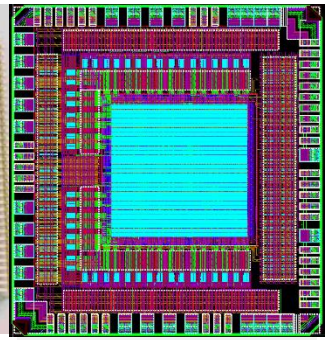
- MDT electronics needs to cope with new proposed ATLAS TDAQ scheme (1 MHz L0 trigger rate with a latency of 10 μs)
- In addition, MDT will be used at the first trigger level (only used as a tracker so far) to further sharpen the trigger turn-on curve



Design of a new TDC



AMT3



UM-TDC v1.0

Why a new TDC IS NEEDED?

- ❖ Previous AMT is no longer available for production
- ❖ Issues found with the AMT chip

  Ref: https://indico.cern.ch/event/504237/contributions/2138705/

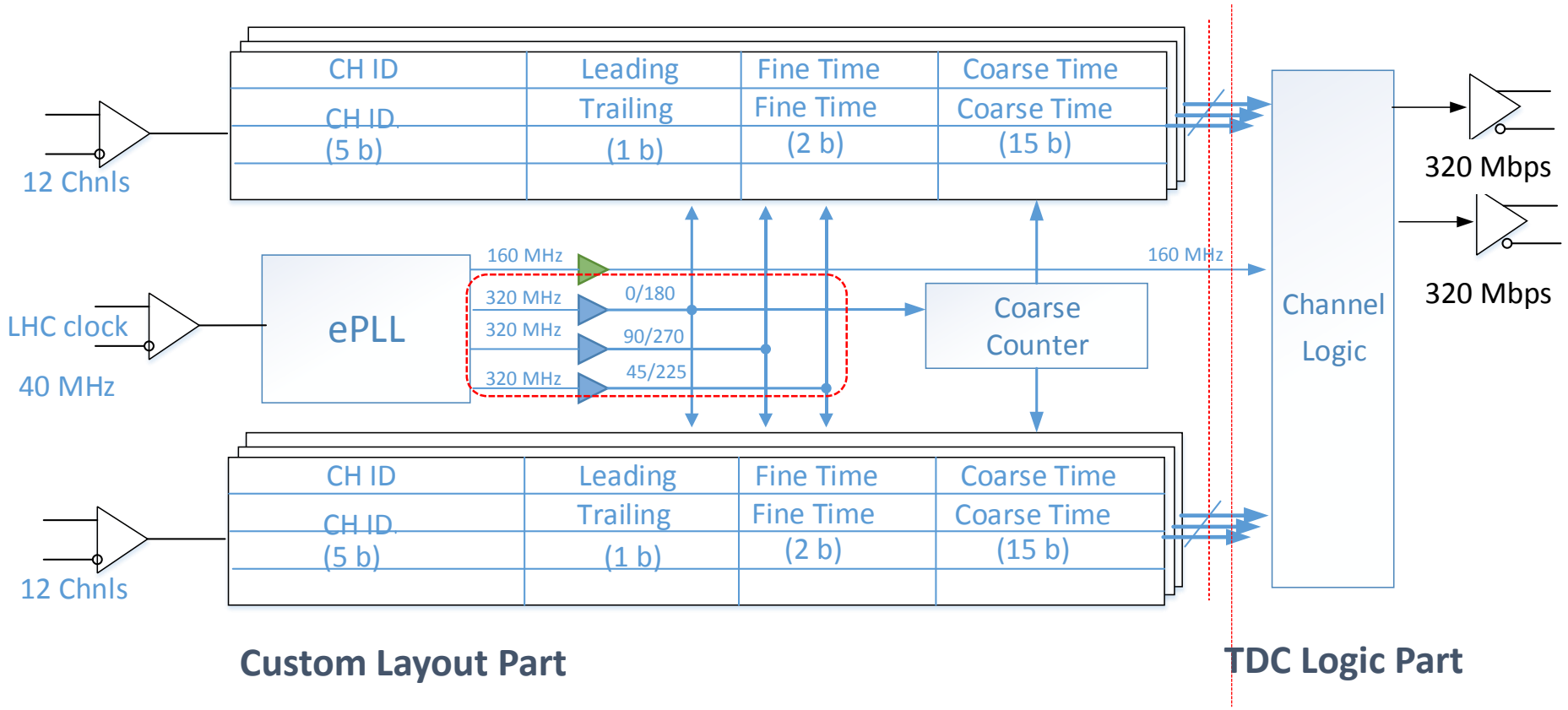
Develop a new TDC ASIC for the MDT phase-2 upgrade

- ➢ Comparable timing performance (Tubes unchanged)
- ➢ Additional features:

  Trigger-less mode => faster serial output interface; Latency Reduction; Radiation Tolerance…

Comparison	AMT	MDT-TDC UM
Technology	0.3 µm CMOS Toshbia	0.13 µm CMOS GF
# of channels	24	24
Resolution	0.78 ns	0.78 ns (~200 ps)
Dynamic Range	102.4 us	102.4 us
Measurement	Rising/falling/TOT	Rising/falling/TOT
Double-hit Resolution	<10 ns	~10 ns
Trigger Mode	Trigger buffer	Triggerless mode Trigger buffer (if needed)

Architecture of MDT TDC ASIC



- Timing resolution determines optimal architecture:

  Multiple clock phases interpolator @ 320 MHz: ***4*** phases of 320 MHz => 3.125 ns /4 = 0.78 ns LSB

- Main components:

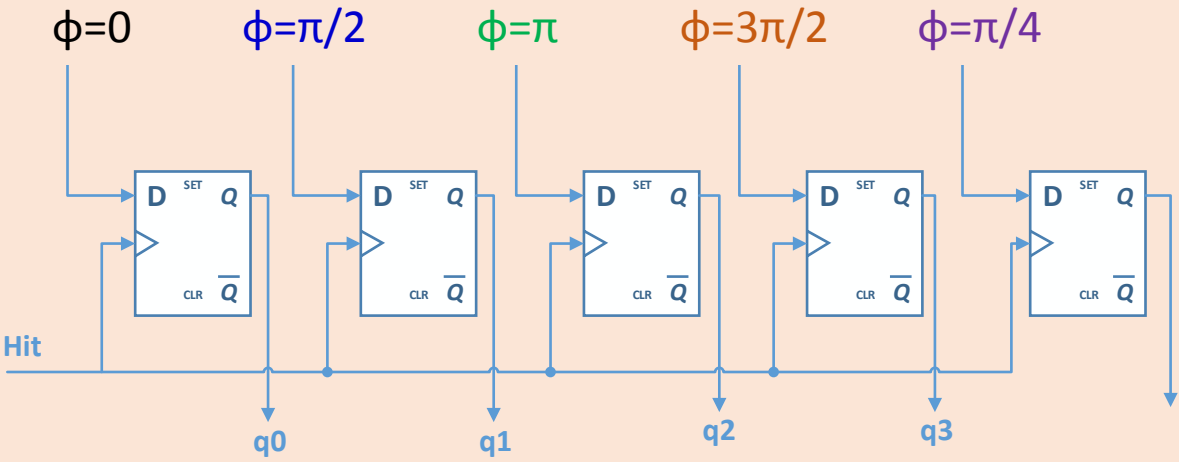
  => Generation of multiple clock phases: ePLL (CERN)

  => Time Digitization: TDC channels (x24)

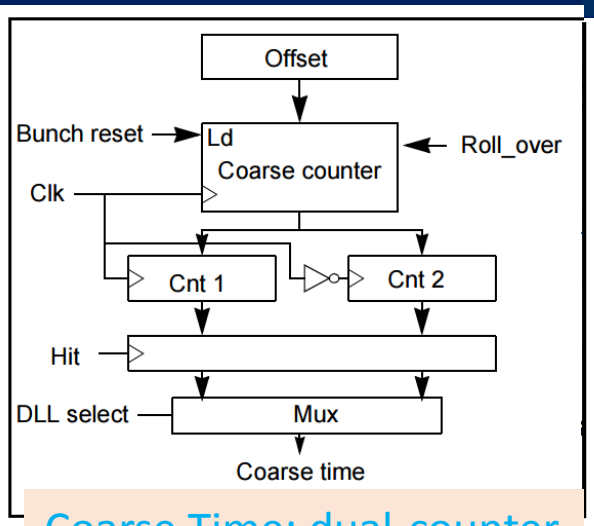
  => Time processing/calibration, output serial interface (TDC logic part)

  } Custom Layout

Channel Time Interpolator (single TDC channel)

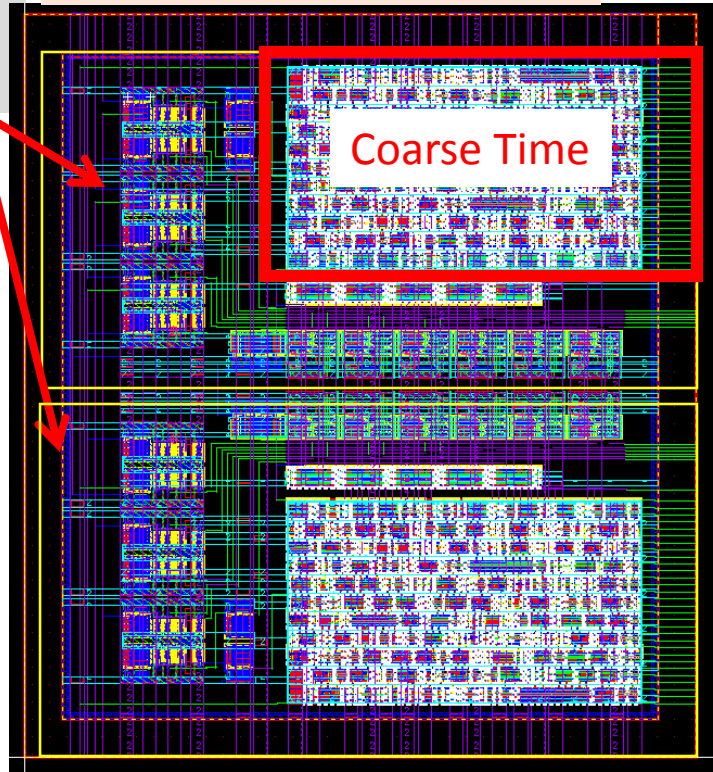


Fine time Interpolator
Hit samples clocks!



Coarse Time: dual-counter

A single channel with
Dual edges



- ❑ Time digitization for each edge in a channel
  => Range :102.4 us + 0.78 ns bin

Coarse time + Fine time

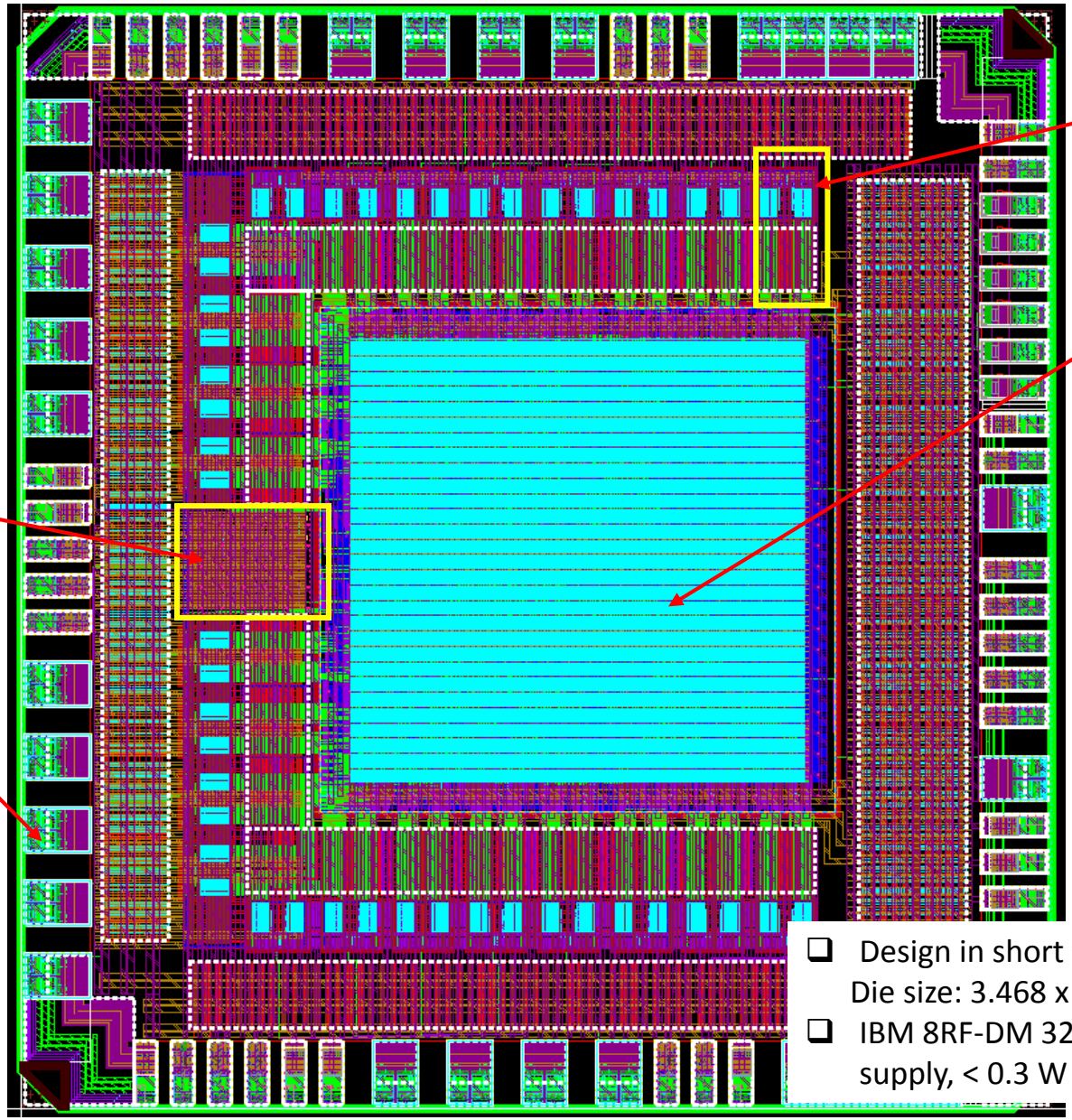
Total time: 17 bits

- Dual counters
- Each works @320 MHz
- 15 bits to cover 102.4 us

- 4 phase of 320 MHz
- One additional Phase
- 2 bits covering 3.125 ns

- ❑ A single Channel: dual edges processed independently
  Combined in Logic in pair mode.

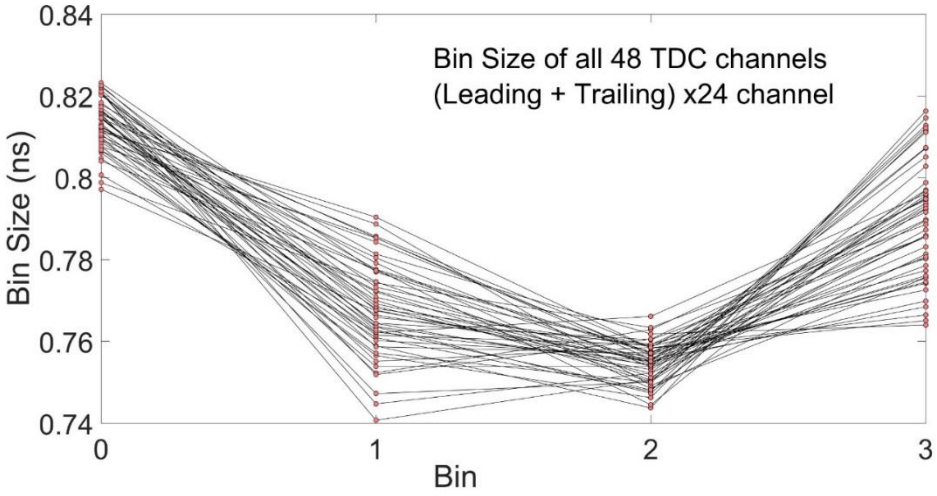
Architecture of MDT TDC ASIC

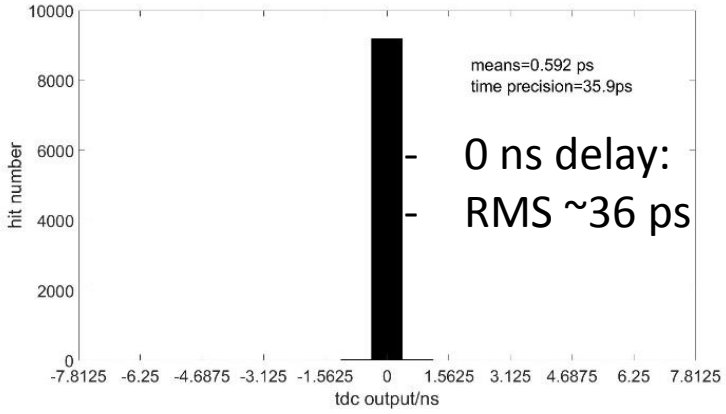


- Design in short time: May-August, 2018
  Die size: 3.468 x 4.812 mm^2
- IBM 8RF-DM 323, 130 nm CMOS; 1.5 Volt supply, < 0.3 W ; QFN 100 package

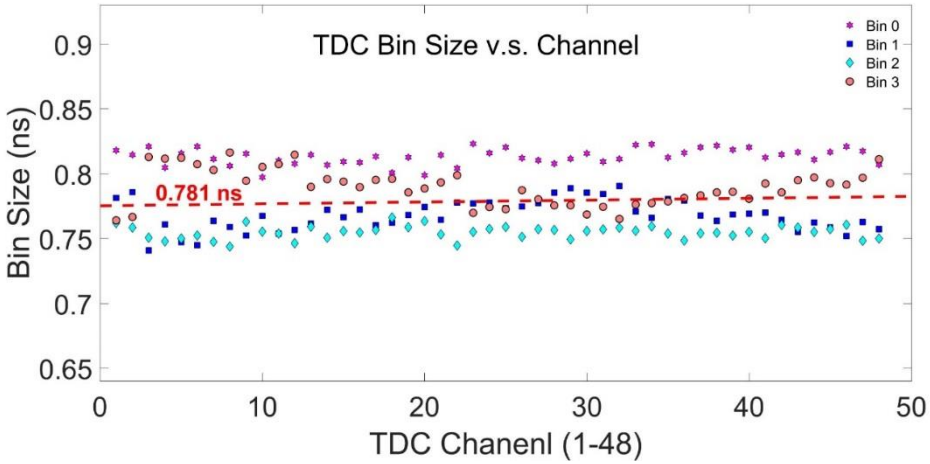
Performance of the TDC

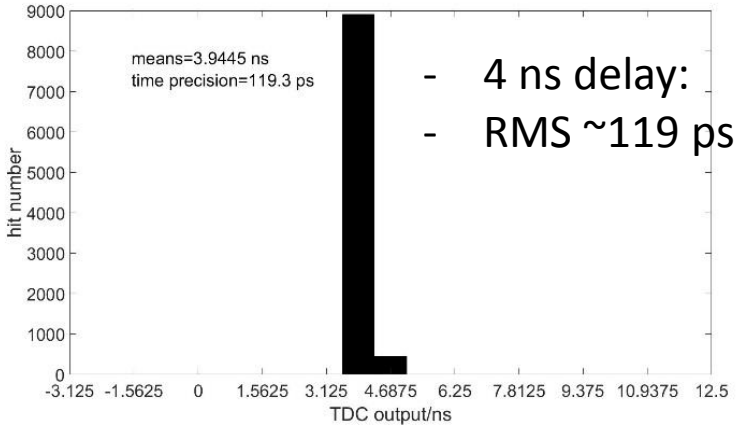
- Bin sizes for all 24×2=48 channels is within +/- 40 ps
- Integrated and differential non-linearity are less than 5% of the bin size
- Time precision: 0 ns delay, RMS ~36 ps;
- Power consumption: ~310 mW (TDC fully working, 48 TDC slices).





- 0 ns delay:
- RMS ~36 ps





- 4 ns delay:
- RMS ~119 ps

Summary

- Two ASIC projects at UM, both are for the ATLAS muon spectrometer upgrades
  - Phase I: A Trigger Data Serialzier for the NSW detector
  - Phase 2: A Time to Digital Converter for the MDT electronics
- We have been benefited a lot from the support and reuse of IPs from CERN
  - Differential IO driver/receiver: SLVS
  - Clock block: ePLL, with programmable clock phases
  - Serializer: 4.8 Gbps even though with significant modifications from us
- We also received a lot of help from US HEP colleagues, e.g. SMU, BNL.