IC Design Activities at LBNL

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Key Application Areas

The LBNL IC Group currently works primarily in three areas:

1. High-Energy Physics : supported by HEP we have developed integrated detector instrumentation since the late 1980s. Member of ATLAS and RD53 collaborations. Beginning work with DUNE (collaboration with BNL and FNAL).

2. Scientific Imaging:

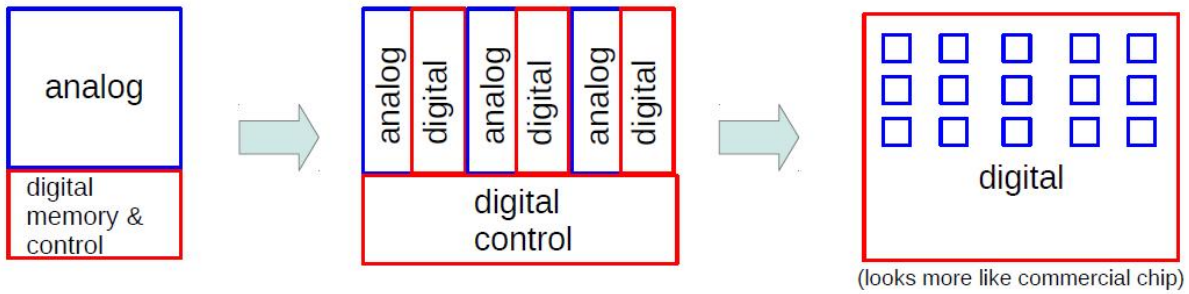
    - Active Pixel Sensors and peripheral chips primarily for electron microscopy.

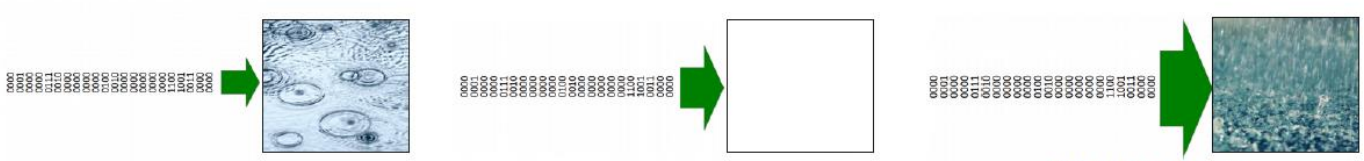
    - Leveraging the high-resistivity CCD developments at LBNL for astronomy, we develop sensors and readout ICs for high-speed CCD cameras (soft X-ray application).

1. Neuroscience : We develop high-channel count readout ICs for electrocorticography (ECoG) and penetrating extracellular readout. In addition, we develop specialized neural circuits (e.g. localized heaters and neural temperature sensors).

HEP Pixel Technology Development

Readout Chip Evolution





Another way to say memory per unit area: Logic Density.
We follow Moore's Law.

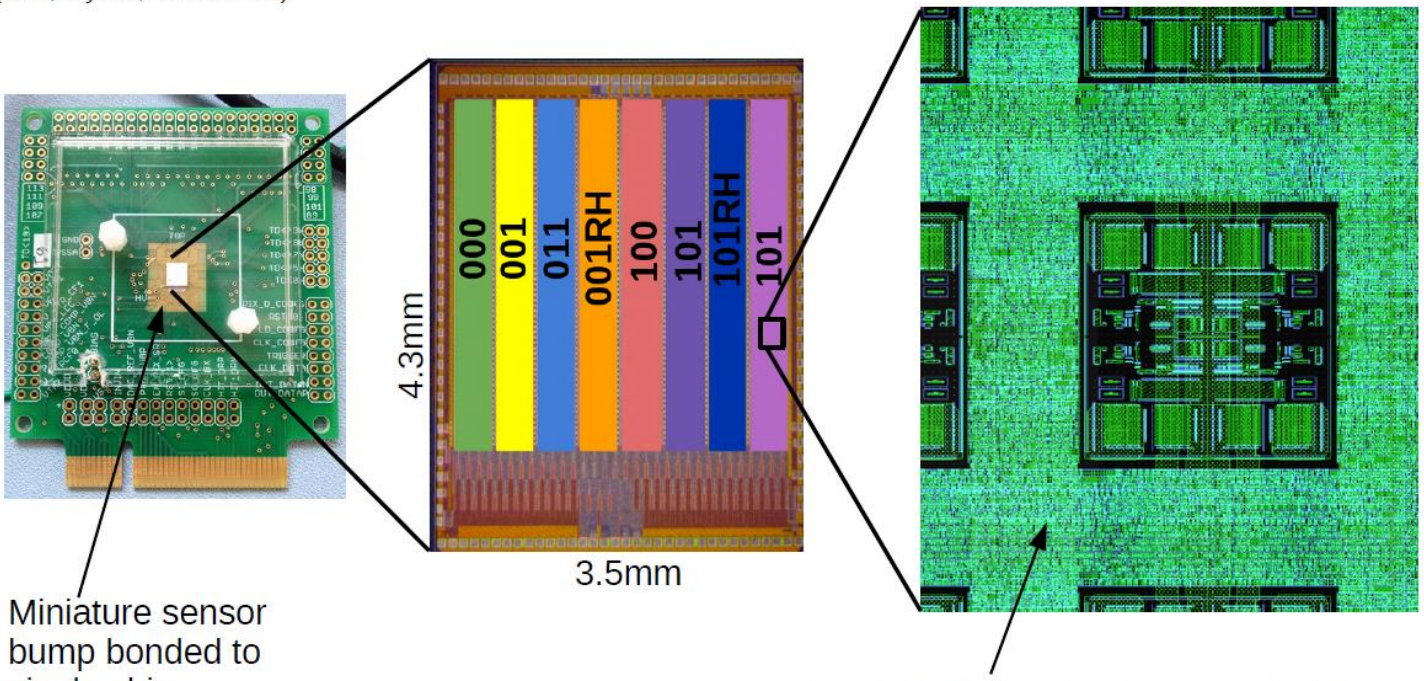
From ICHEP2016

FE65-P2 – Precursor to RD53A

FE65-P2 test chip

* Stepping stone to RD53A
  (flow, layout, isolation…)

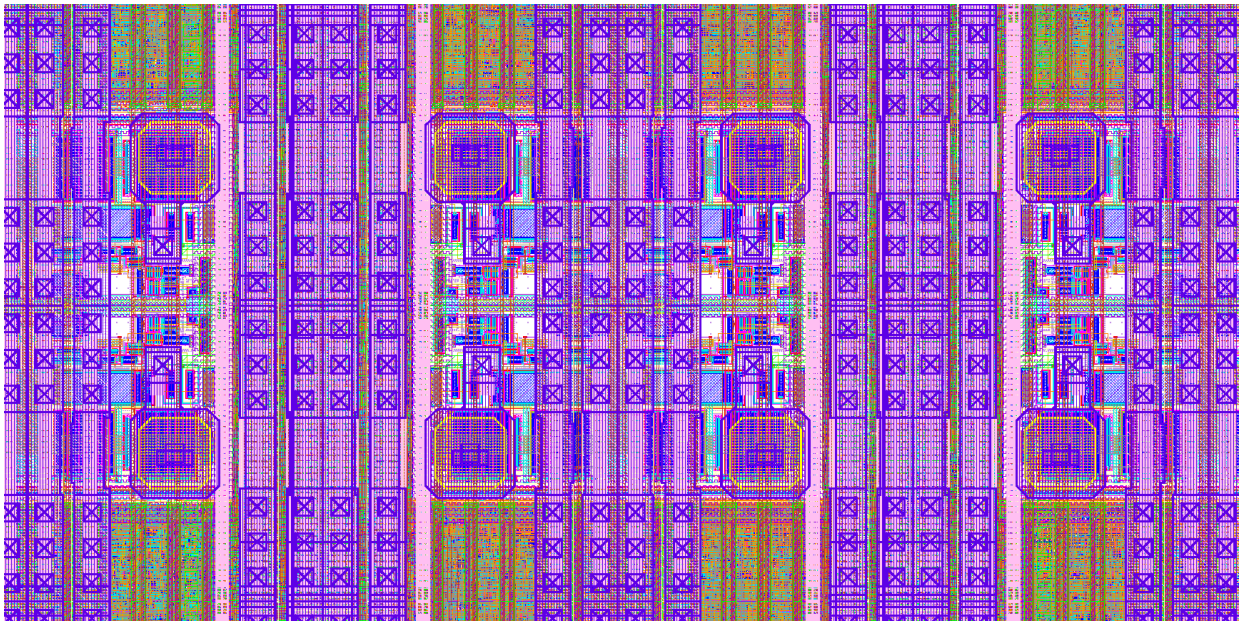
* 64x64 pixels on 50µm grid



From ICHEP2016

High-Energy Physics

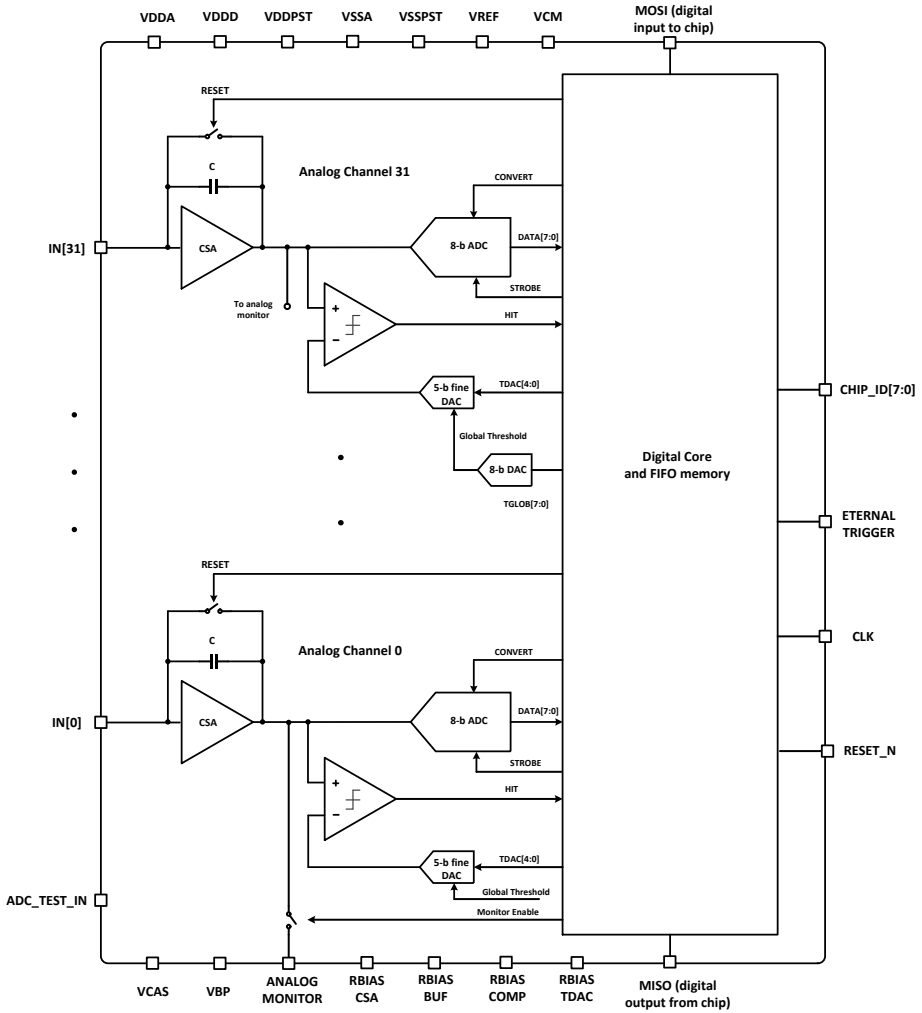
RD53a -- Developed one of three analog front ends to be evaluated in RD53 and also contributed to radiation hardening of digital logic (DRAD chip)



Zoom of 8 AFEs for RD53A

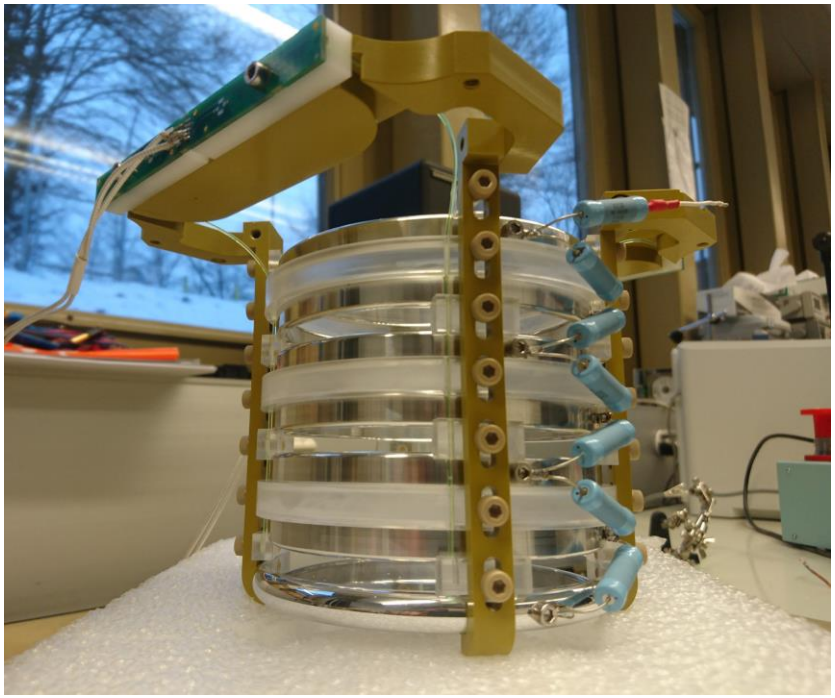
Cold readout -- Developed a prototype readout IC (LArPix) for interfacing to a pixelated liquid-argon detector developed at Bern. Beginning contribution to new cold ADC for DUNE far detector.

Cold Readout – LArPix

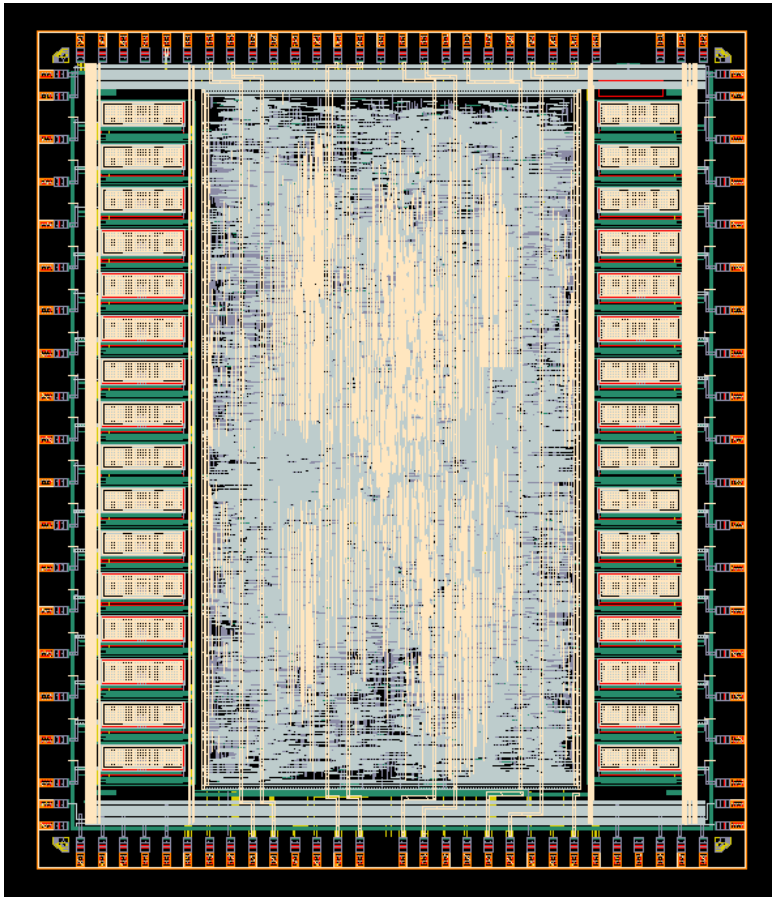


- 32 analog channels
- Pixel readout IC intended for LAr operation
- Single digital input and output per chip (reduce cryostat penetrations)
- 300 e- ENC noise @ 88 K (4 pF detector capacitance)
- 8-bit per-channel ADC
- 100 µW/channel
- 180 nm CMOS
- Parts due back from fab October 2017

Cold Readout – LArPix

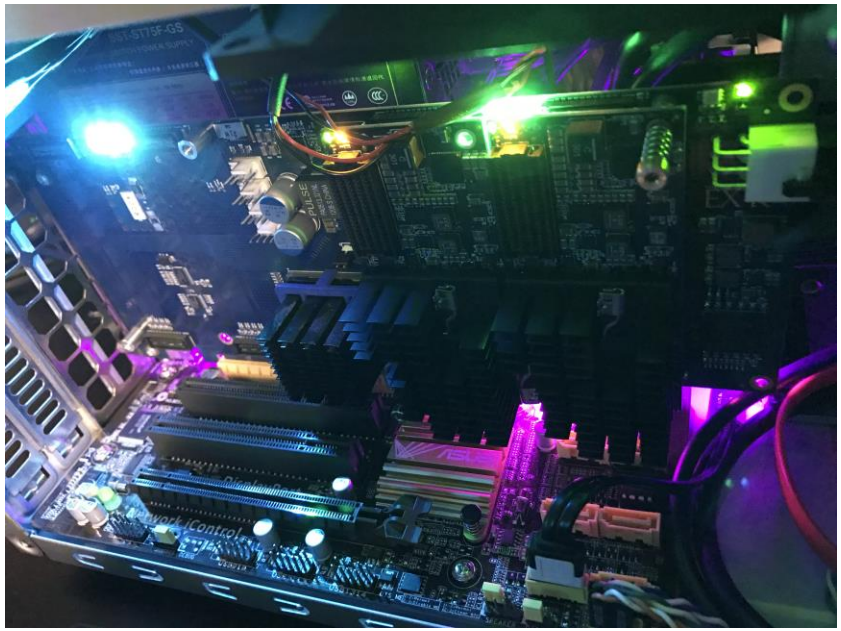


LArPix



To be tested by U Bern in mini ArgonCUBE demonstrator

Custom Processor for HEP (RISC-V)



- Custom processor configured using SoC-Architect and described in Chisel, a high-level hardware description language that outputs synthesizable Verilog
- Addition of custom instructions allows vastly improved performance/power
- Based on RISC-V open-source instruction set
- Design functional in FPGA, currently implementing in ASIC (65 nm)
- Collaboration with LBNL Computational Research Division

Scientific Imaging

In the last year LBNL has done development work for two imaging modalities

1. Electron Microscopy

    - Detectors for Cryo-EM (Nobel Prize in Chemistry, 2017)
    - Ultra-high-speed imagers for 4D-STEM and RIXS
    - High-Speed Readout IC
    - Single-to-Differential Buffer (to reduce camera size and BOM)
    - Collaboration with National Center for Electron Microscopy (LBNL) and Advanced Light Source (LBNL)

2. Soft X-ray detector (LCLS-II/ALS)

    - Very-Fast CCD (VFCCD) fully column parallel CCD with charge domain output for LCLS-II upgrade
    - VASE – 256-channel front end for VFCCD
    - Collaboration with SLAC (previously also collaborated with Argonne)

Cryo-Electron Microscopy

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google.com

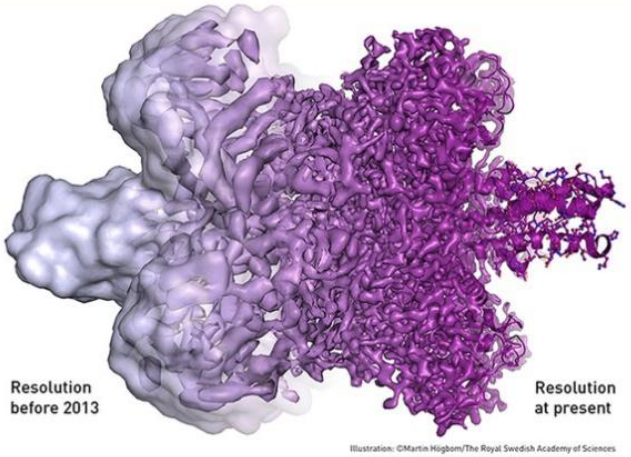
washingtonpost.com

Speaking of Science

Three biophysicists win 2017 Nobel Prize in chemistry for imaging molecules of life

By **Ben Guarino**

October 4, 2017 at 7:43 AM



The Nobel Prize @NobelPrize

The final technical hurdle was overcome in 2013, when a new type of electron detector came into use.

2:56 AM - Oct 4, 2017 · Stockholm, Sweden

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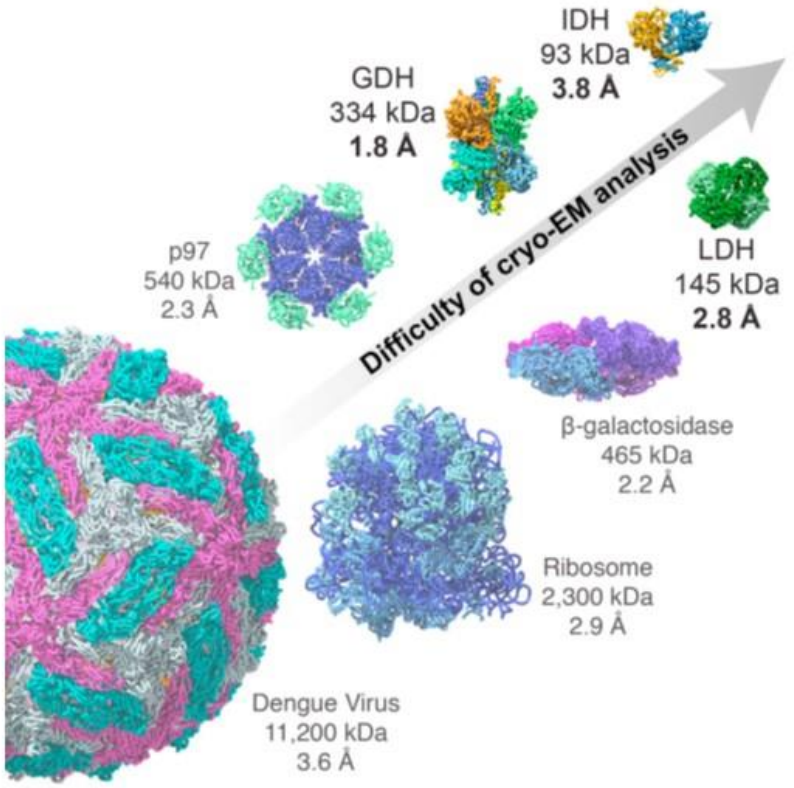
LBNL IC Group has worked with Gatan, Inc. on electron detectors for Cryo-EM for many years

K2 – Cryo-Electron Microscopy



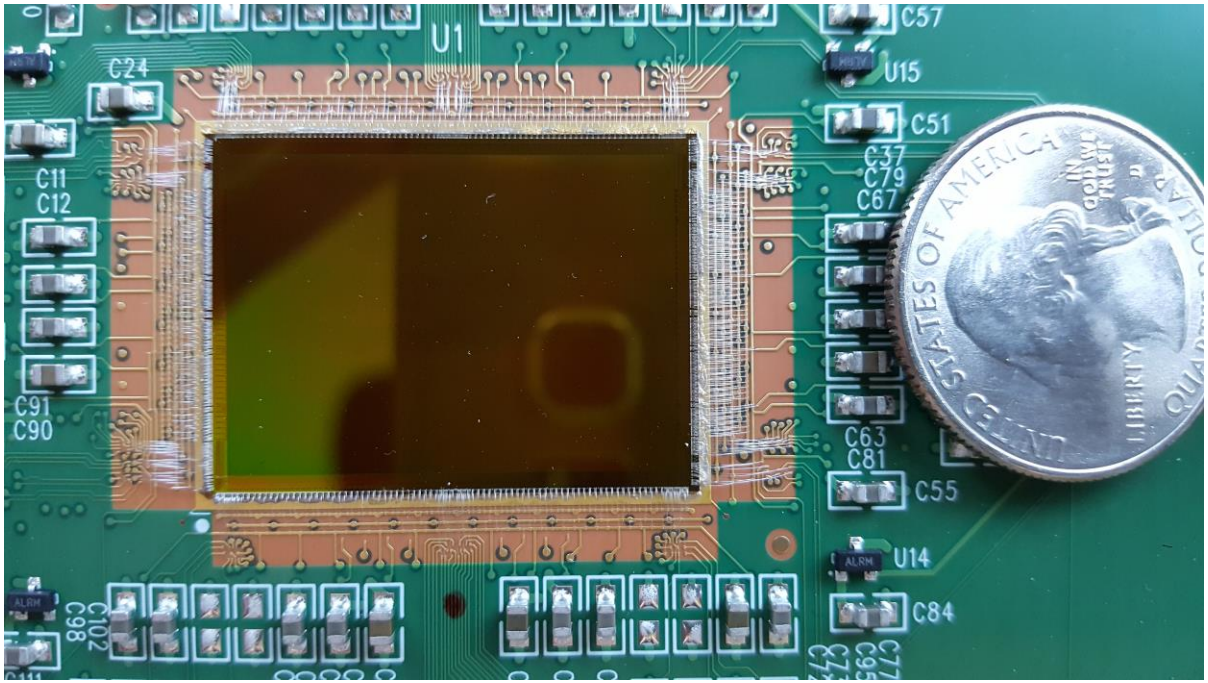
K2, Berkeley Lab's first reticle-scale CMOS imager, has been providing unprecedented insights into protein structures for 5 years. The K2 sensor, designed for Gatan by Berkeley Lab's IC Design Group, is the heart of the industry-leading K2 Summit electron microscope direct detection camera. Left, the 2.3 cm., 50 million transistor K2 sensor. Right, a K2 protein structure enabling new drug discovery at 1.8 angstroms resolution.

K2 has proven to be a ground-breaking, sensor in the field of cryogenic electron microscopy.

K3 – Cryo-Electron Microscopy

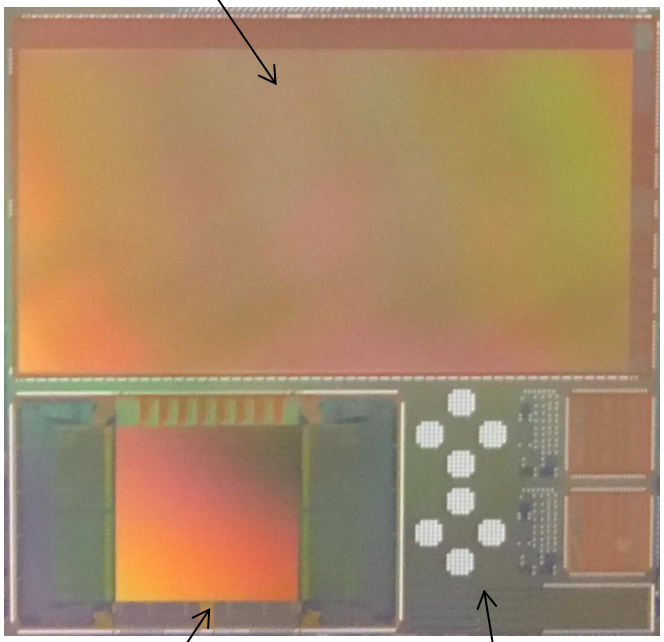
K3 is a 24 Mpixel CMOS thinned sensor for Cryo-EM, operating at 1.5 kFrames/s
It is implemented in a 180nm Imaging CMOS process with approx. 75 M transistors. It is currently undergoing productization by our industrial partner.

Pre-development work has begun on K4, a much larger, stitched version, first 100 M+ device from LBNL.



Specialized CMOS Image Sensors

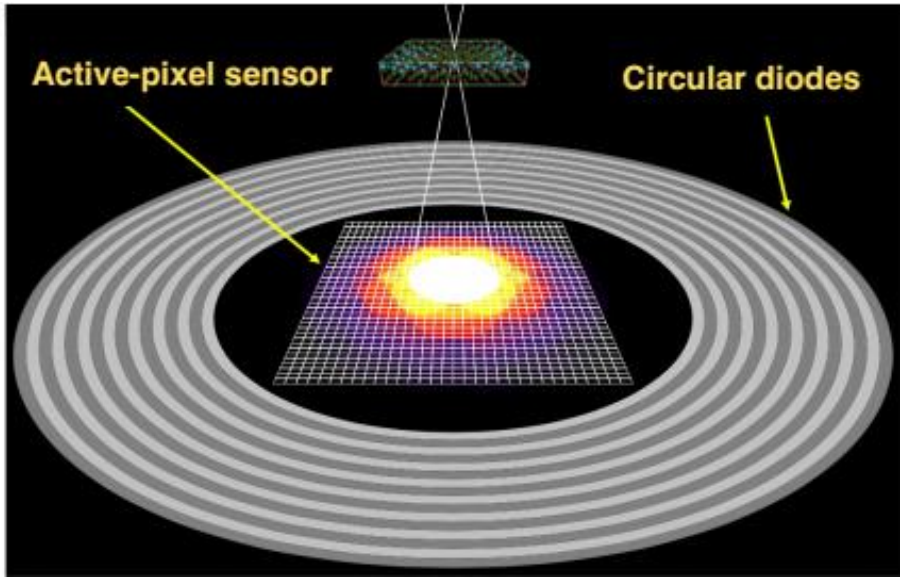
QERLIN – Soft X-ray
"2D RIXS" detector



4D-STEM – ultra high-speed electron imager

HCHIP – temp controller for testing neural thermal effects

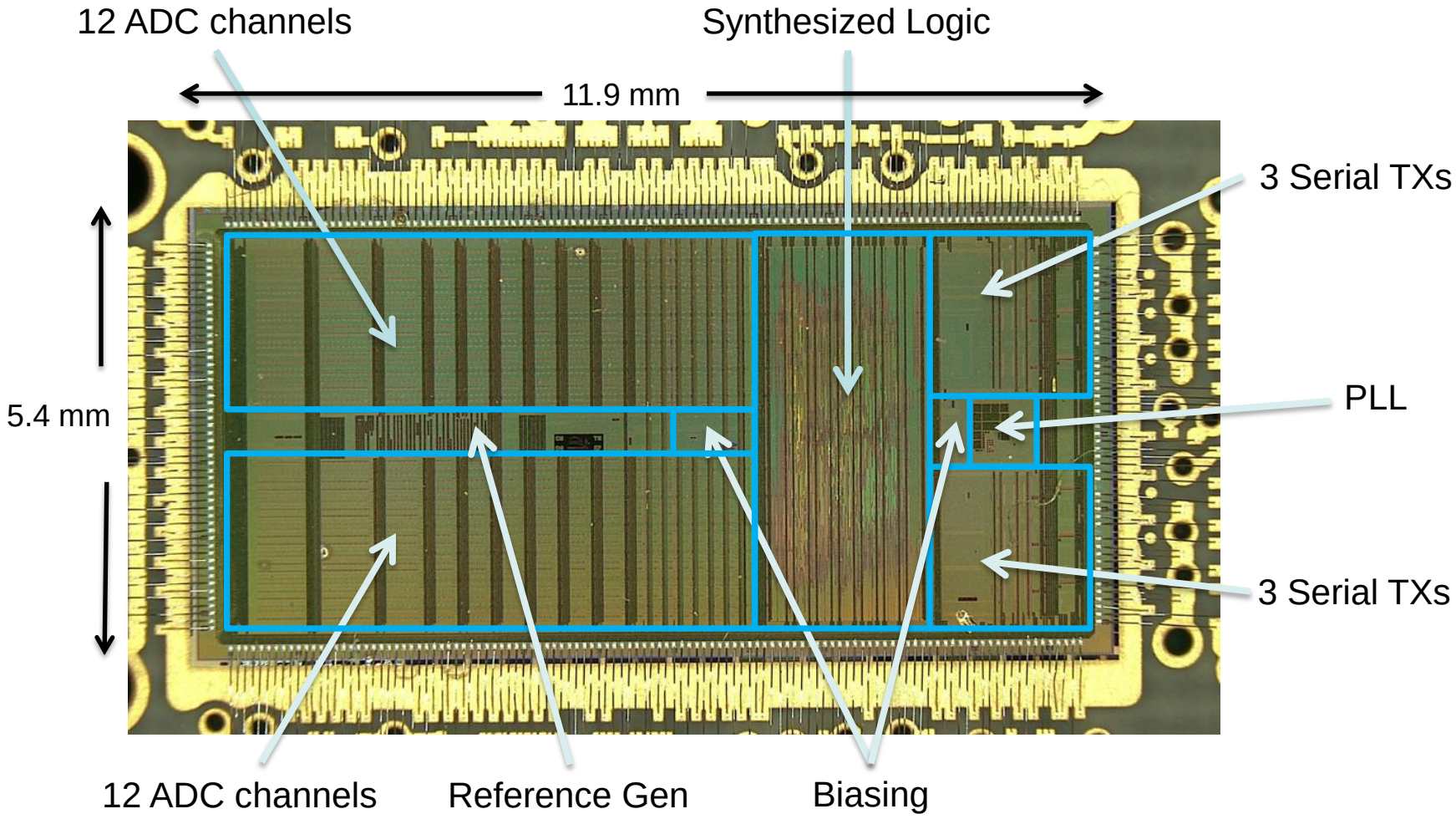
4D-STEM concept



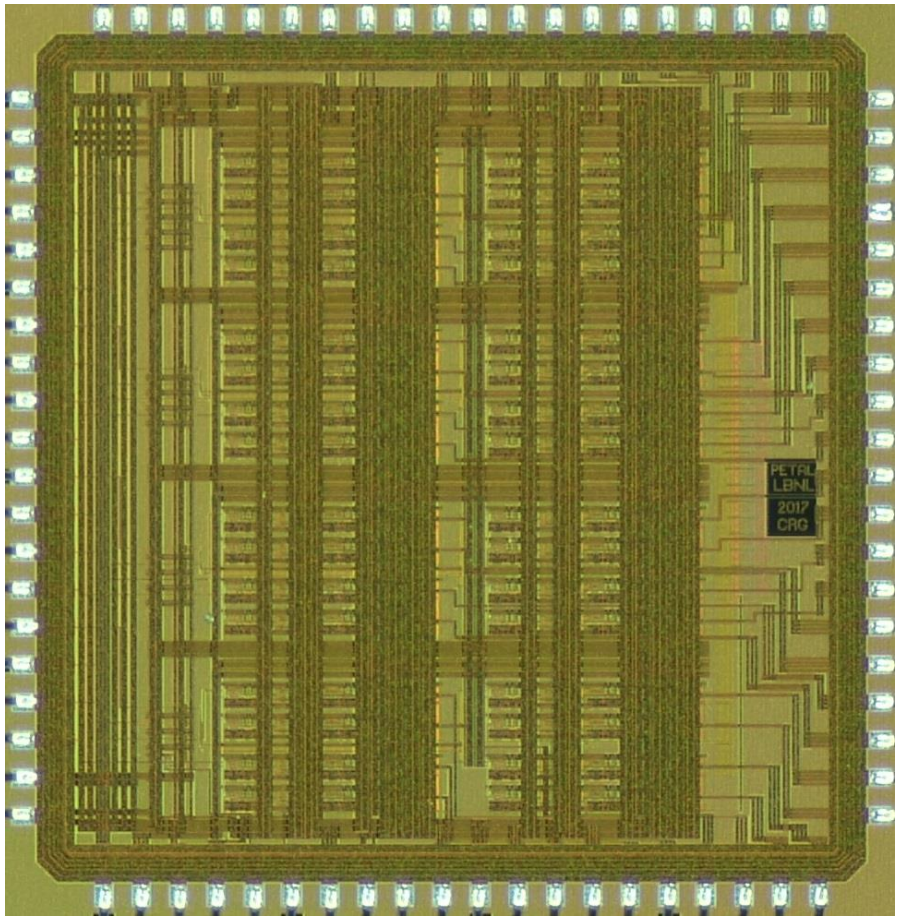
All chips undergoing lab characterization.

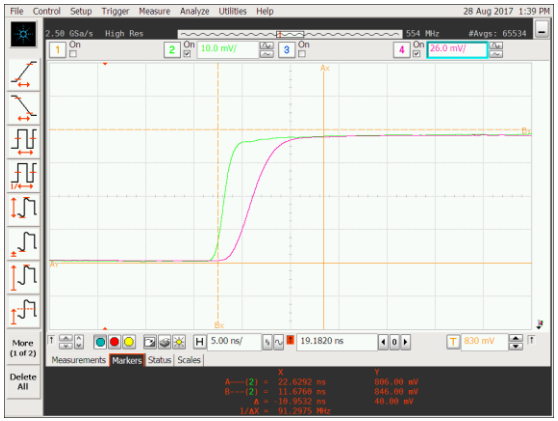
HIPSTER

24 channels of 12-bit, 25 MS/s ADCs, 4.5 Gbps JESD 204b serial links for electron imager readout

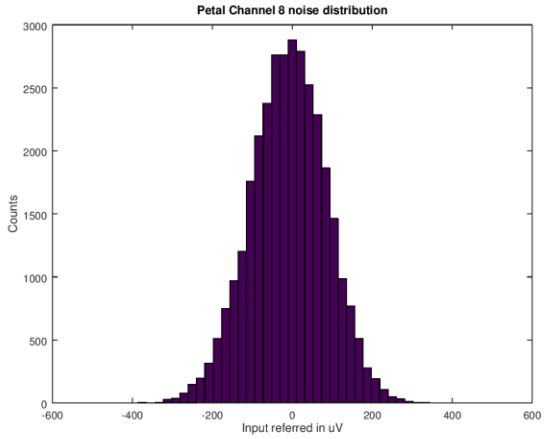


PETAL





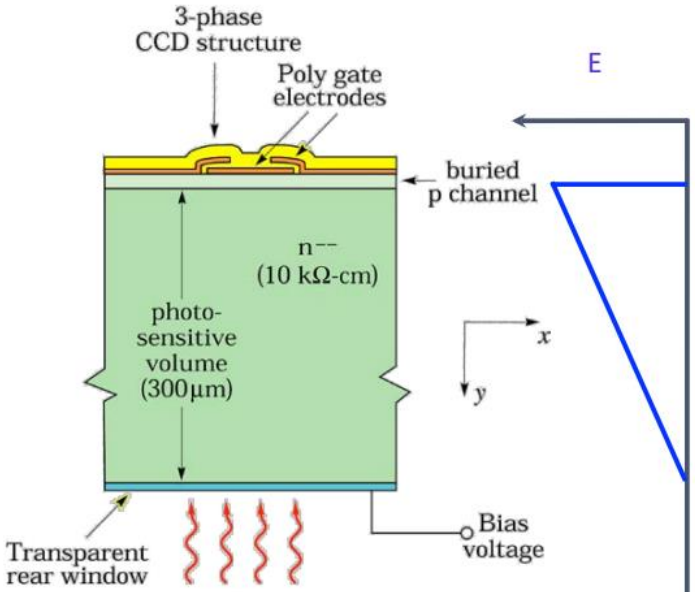
Settles to 0.5% in < 10 ns

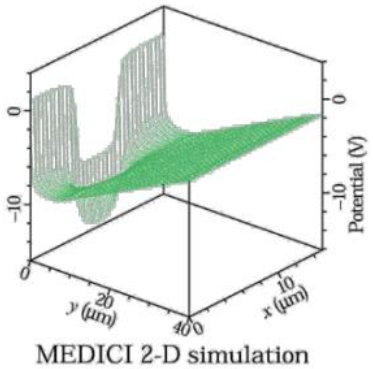


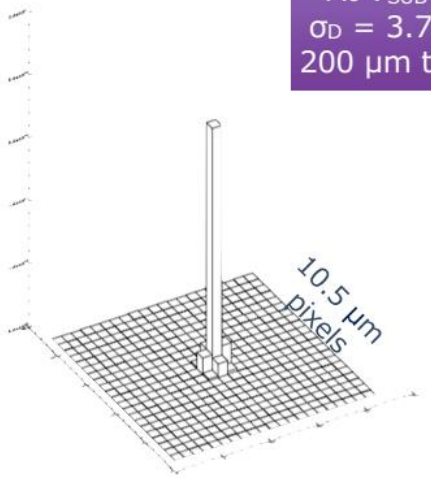
Measured Noise ≈ 90 µV-rms

Low-power single-ended-to-differential buffer for QERLIN

LBNL CCD (structure on high-ρ Si)







At V_{SUB} = 115 V,
σ_D = 3.7 ± 0.2 μm
200 μm thick device

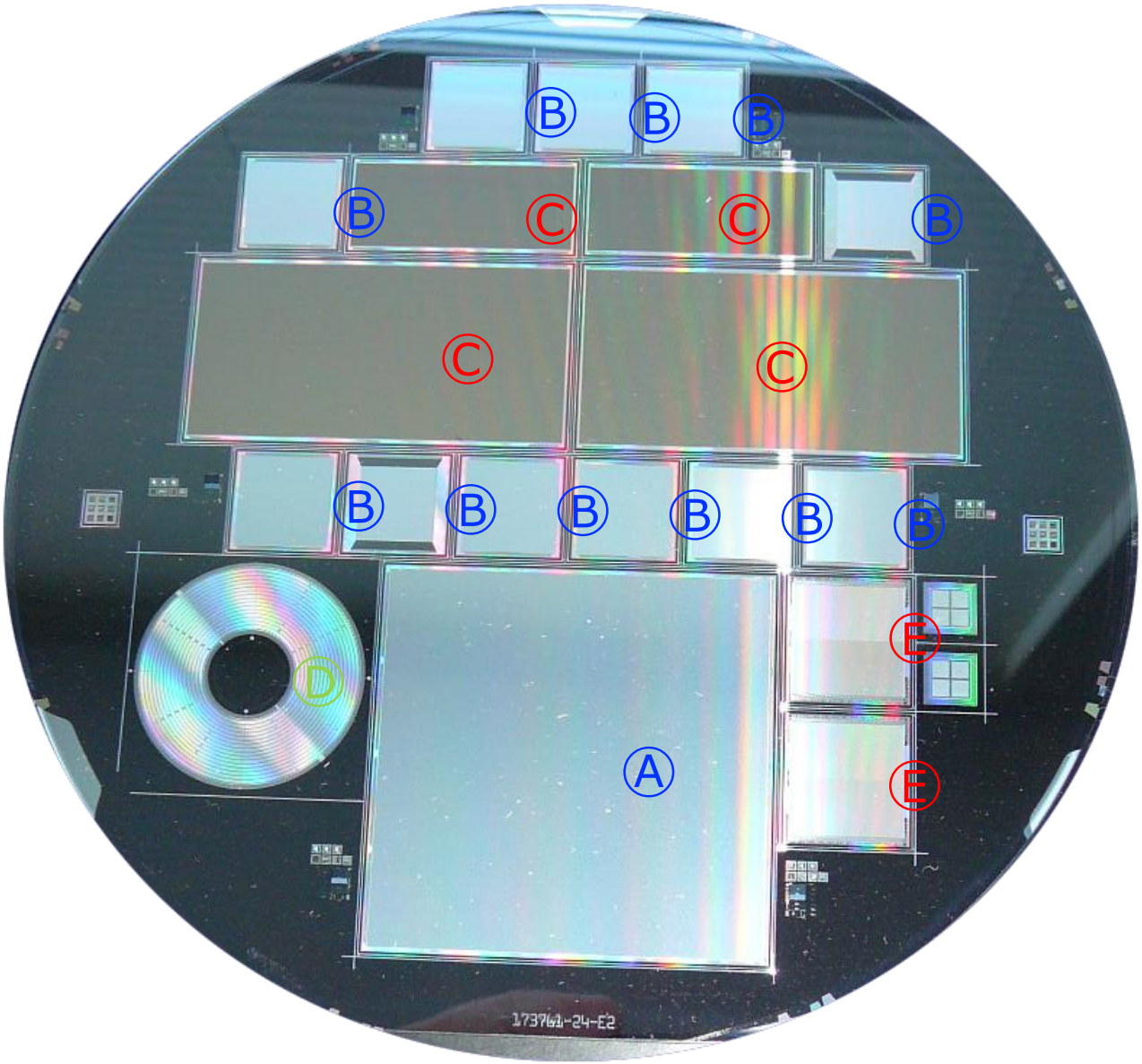
- Originally developed for astronomy
- Thick (up to 650 μm) high-resistivity Si
  - Fully depleted
  - Thick for good red QE
  - Thin window for good blue QE
- n-type (p-channel) for enhanced radiation resistance (space application)

LBNL CCDs

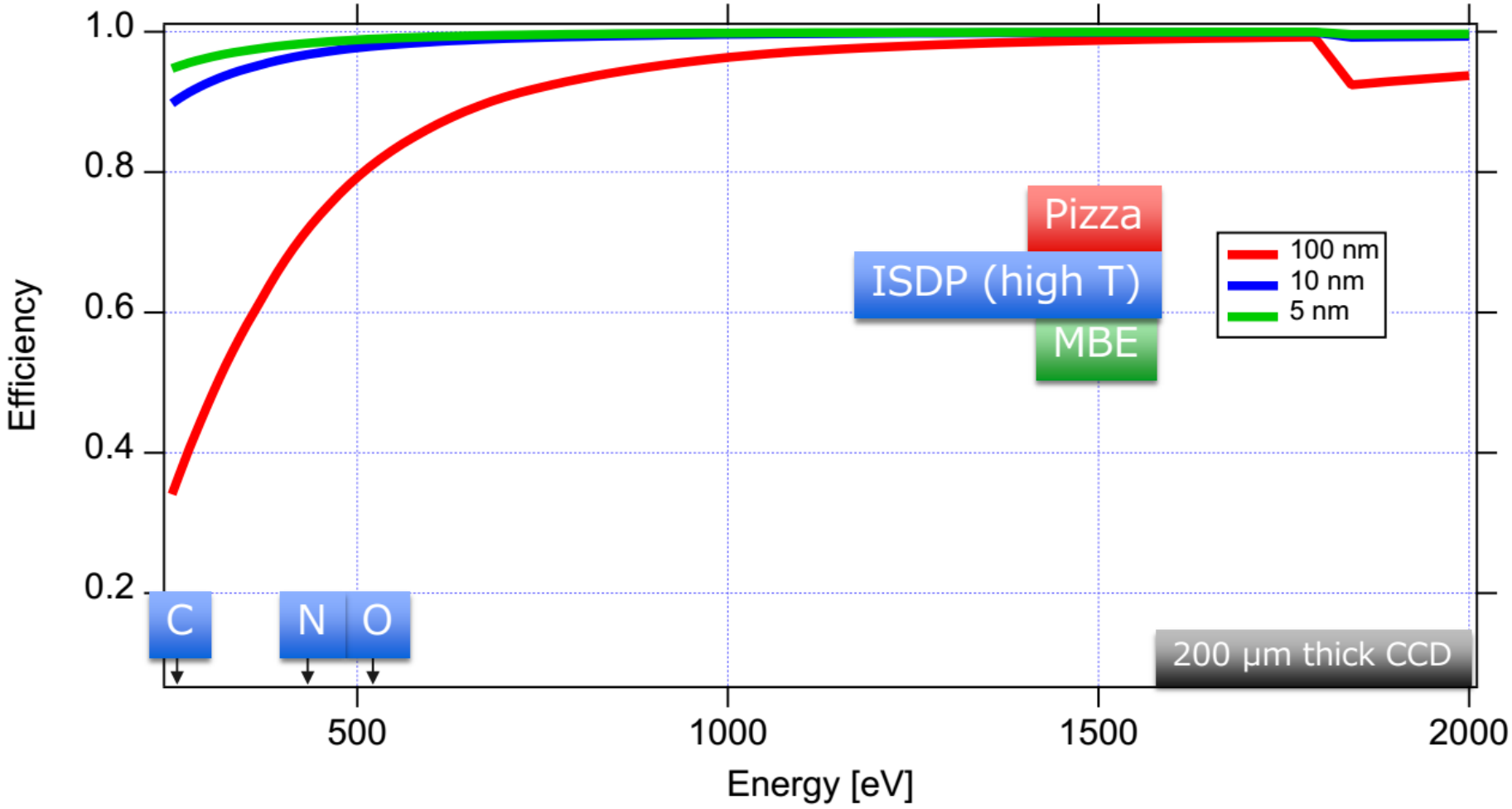
Ⓐ 1,204 VFCCD
3 phase, 48 µm pixels
Ⓑ 256 VFCCDs
3 phase, 39, 48 µm pixels
4 phase, 48 µm pixels
Ⓒ Ⓓ Other BES
Ⓔ FCCD
(process monitor)

High-ρ CCD process developed at LBNL (Microsystems Lab)

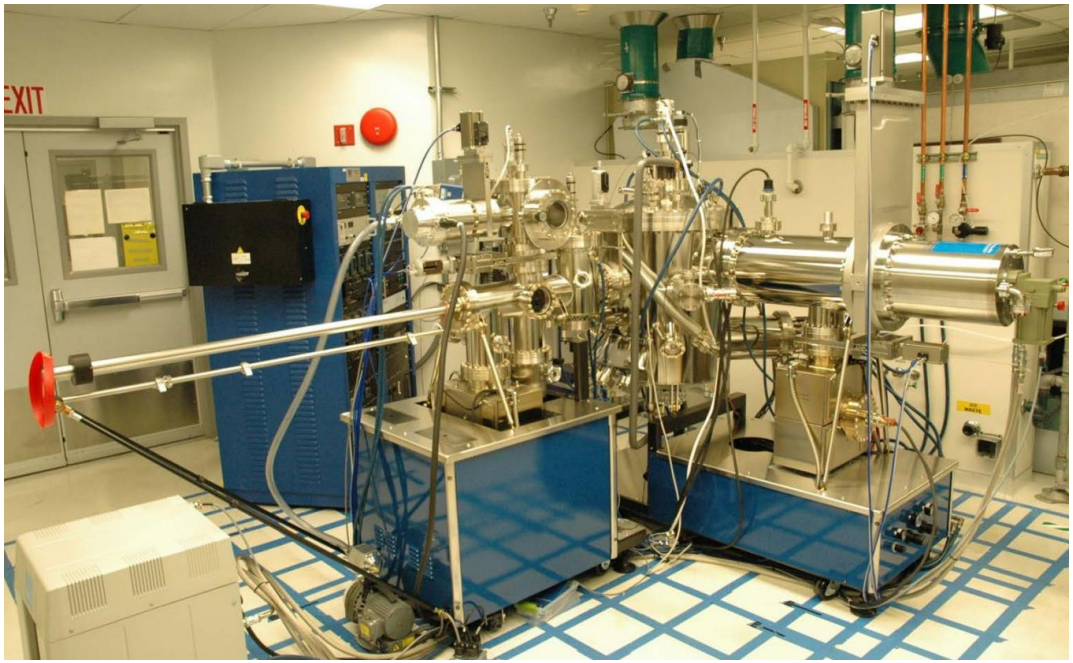
Process transferred to Dalsa Semiconductor for high-volume production

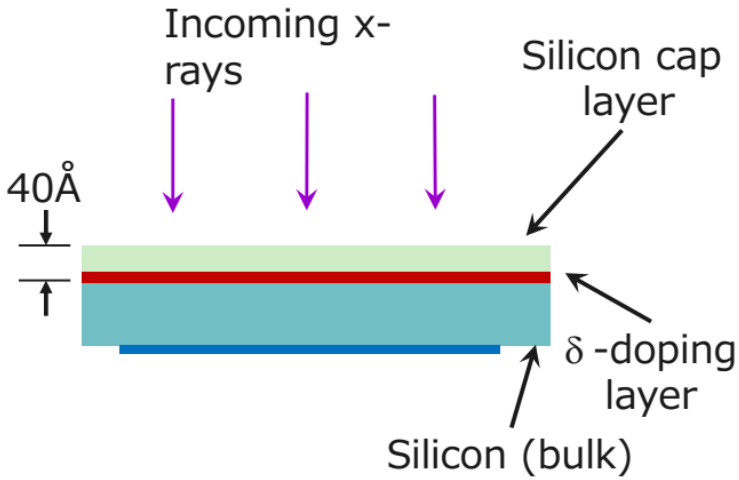


LBNL entrance window processing



LBNL Silicon Molecular Beam Epitaxy Facility



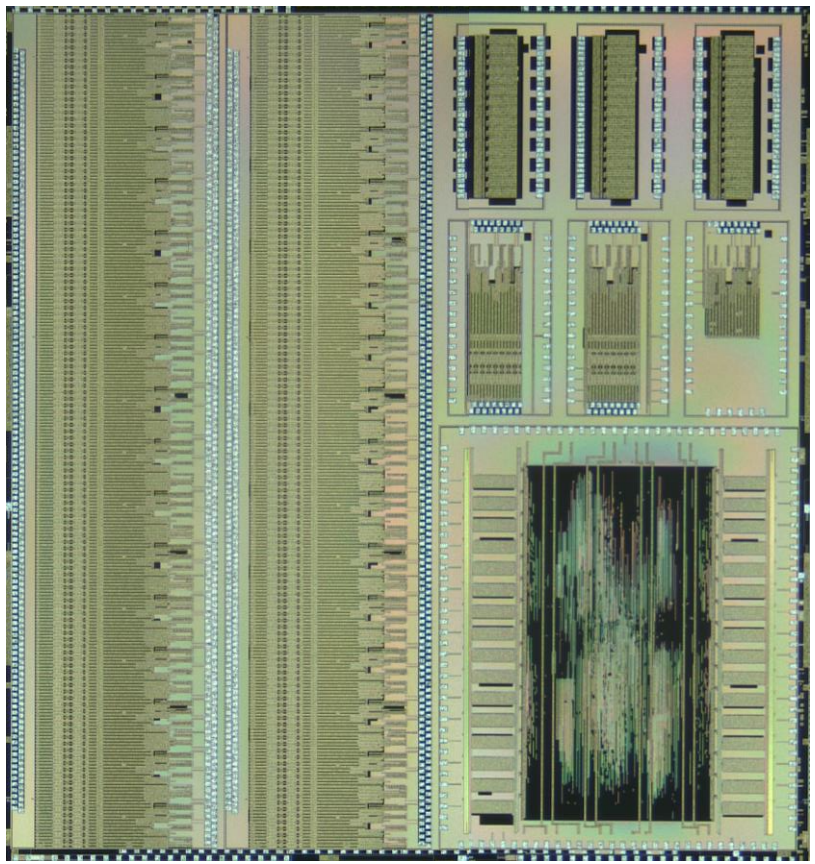


Pioneering work on δ -doped contacts was done by Nikzad's group at JPL.

One of three Silicon MBE Facilities in US (along with JPL & Lincoln Labs)

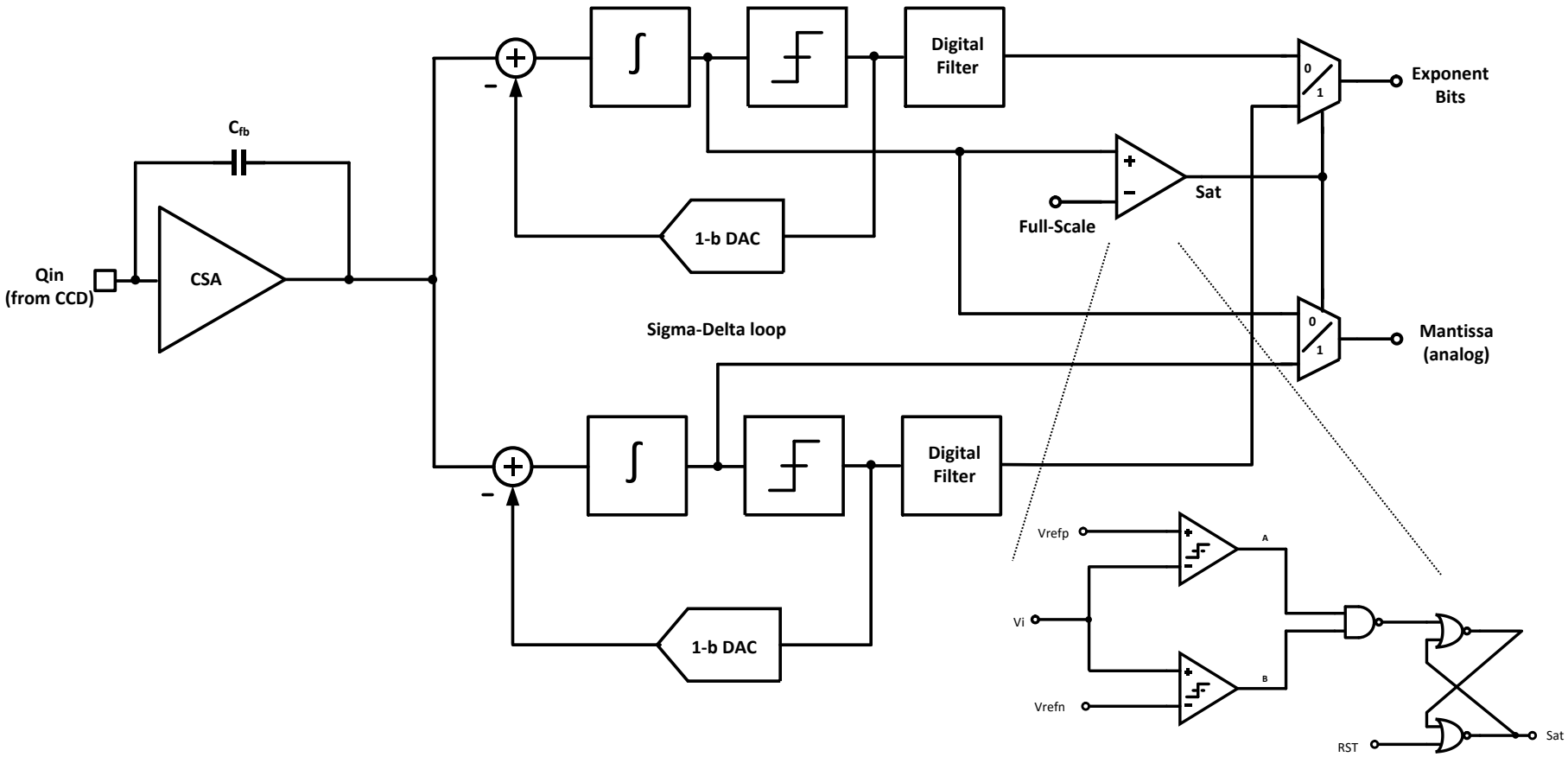
Capable of providing 5 nm entrance windows

VASE – charge-sensitive CCD readout



- CCD readout for LCLS-II upgrade
- 256 channels per chip
- Charge-amp and dual sigma-delta modulators per channel
- 5 MHz column rate
- ~ 10 e- ENC (100 fF input cap)
- ~ 1.5 mW/channel
- 180 nm CMOS
- Parts due back from fab October 2017

VASE Channel



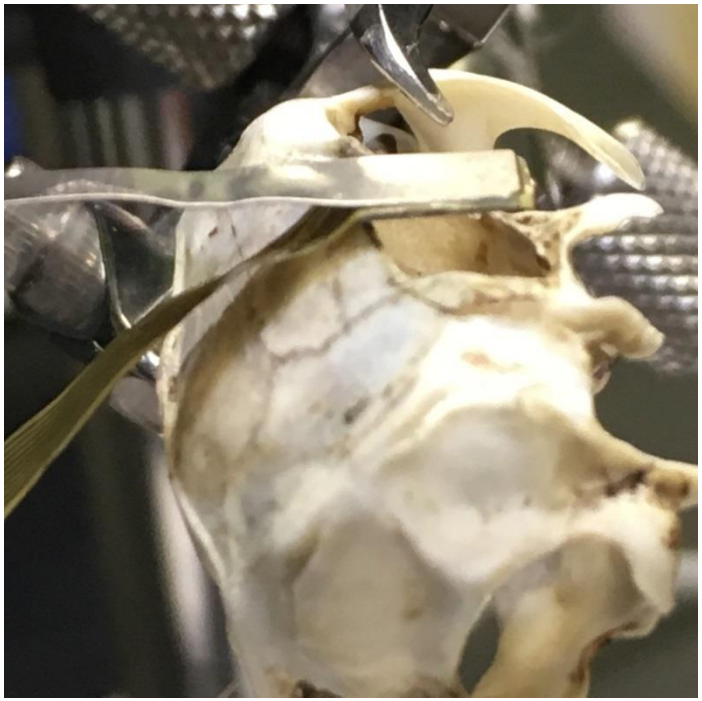
Dual sigma-delta modulators for increased dynamic range

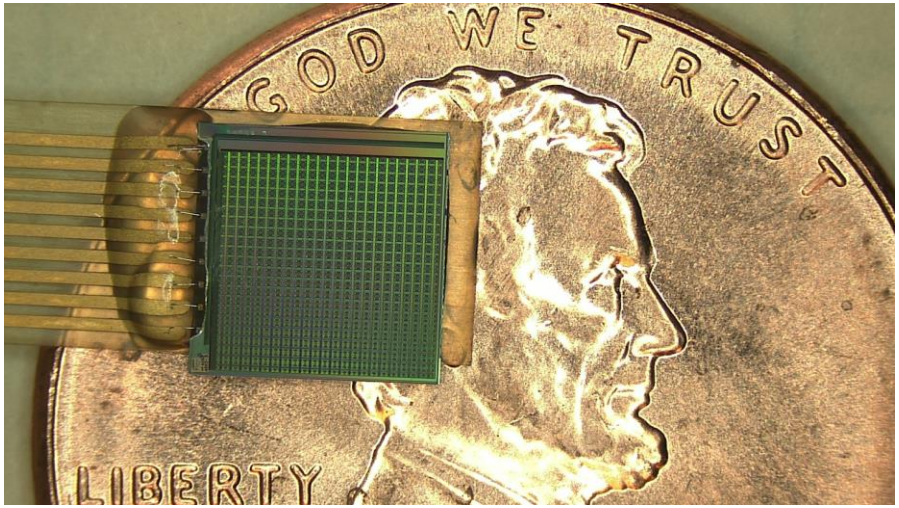
Residue digitized by commercial ADC

Neuroscience

Electrocorticography (ECoG) sensor with high density readout (1936 channels at 100 µm pitch). Taped out additional chips for neural thermal studies.

ECoG is a high-resolution electrophysiological recording technique that places electrodes directly on exposed surface of brain for high bandwidth recording.





Collaboration with
UCSF and LLNL

Contributors

- Peter Denes
- Erin Fong
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- Craig Tindall