UCSB R&D Efforts for HEP

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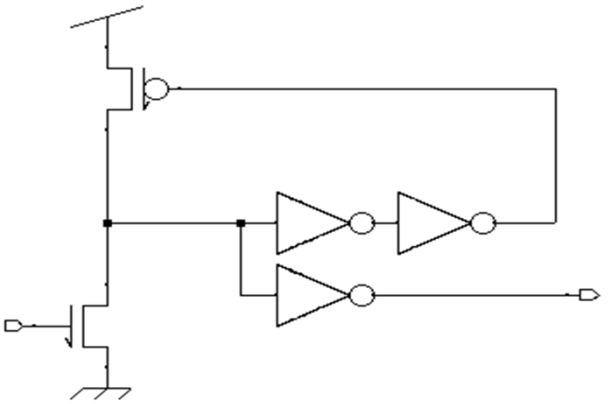
Our IP

- Pulse-gate cell library
  - High-speed accurate timing cells
- Used to make
  - Clocks
  - SERDES
  - Parallel PRBS sources/checker
  - Pads
    - HSTL 2.5GHz single ended
    - Differential edge (7+Gb/s)
    - Trinary pulse (4Gb/s)

Vast majority of IP is specific to 8rf (130nm CMOS), also pad and some cell designs in TSMC 65nm, Recent forays into 22nm FDSOI

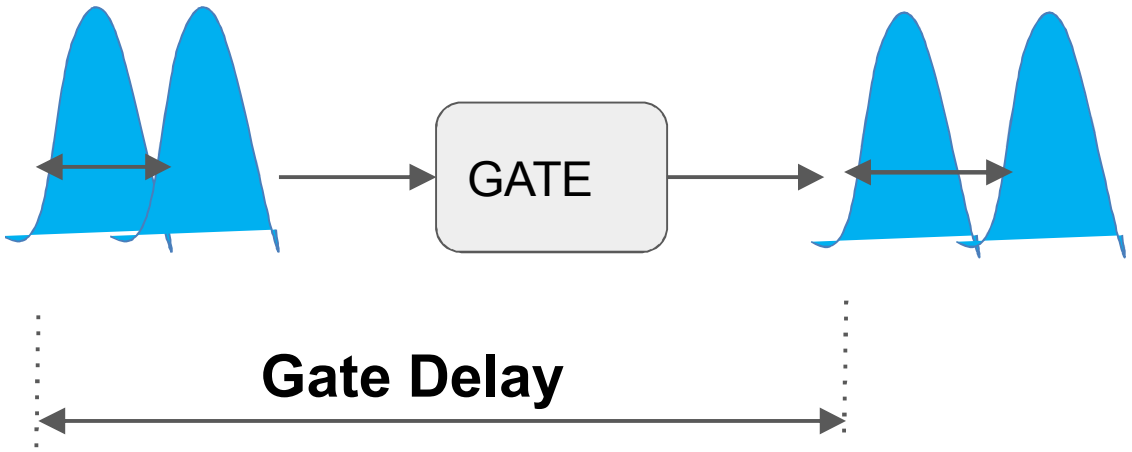
Pulse Gate Library

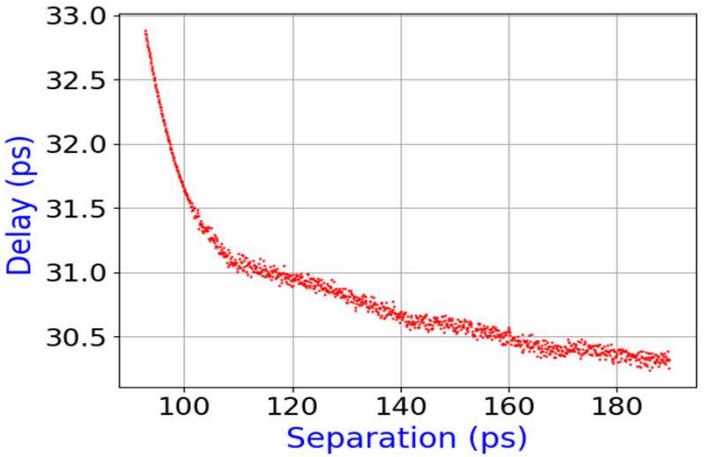


- Rad-Hard Design
  - Latch-up Surround Implants/TID Model
- 6.4ux10u+4ux pitch
- NMOS Pull-down guarded fire, self reset, output taps
  - And/Or/AOI/OAI/XOR/RS-latch/Arb/Delay
  - 30pS delay; 2-5pS variance; 130pS rapidity
- Verilog-A models
- Timing insensitive to pulse amplitude or width; regenerated pulse width from internal timing.
- Gates similar to Intel P4, composition rules differ
  - Low-order complexity timing verify

Pulse Dynamics

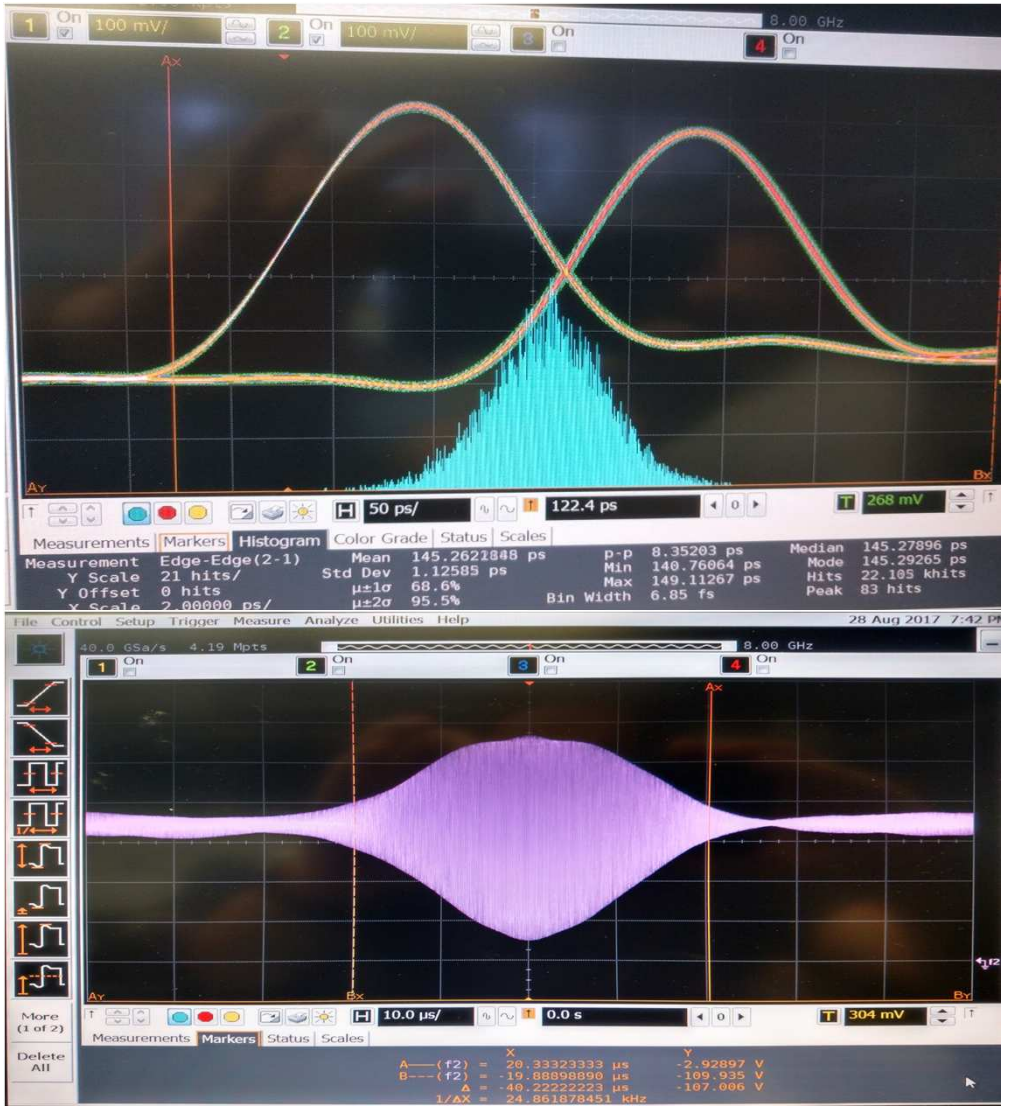
- Pulses interact by repulsion
  - Weak attraction for large time separation
- Exploit to ‘nudge’ timing away from critical events
- Forces uniform timing around loops
  - Can couple loops to create Vernier timing
  - Injection Locking/DLL/PLL



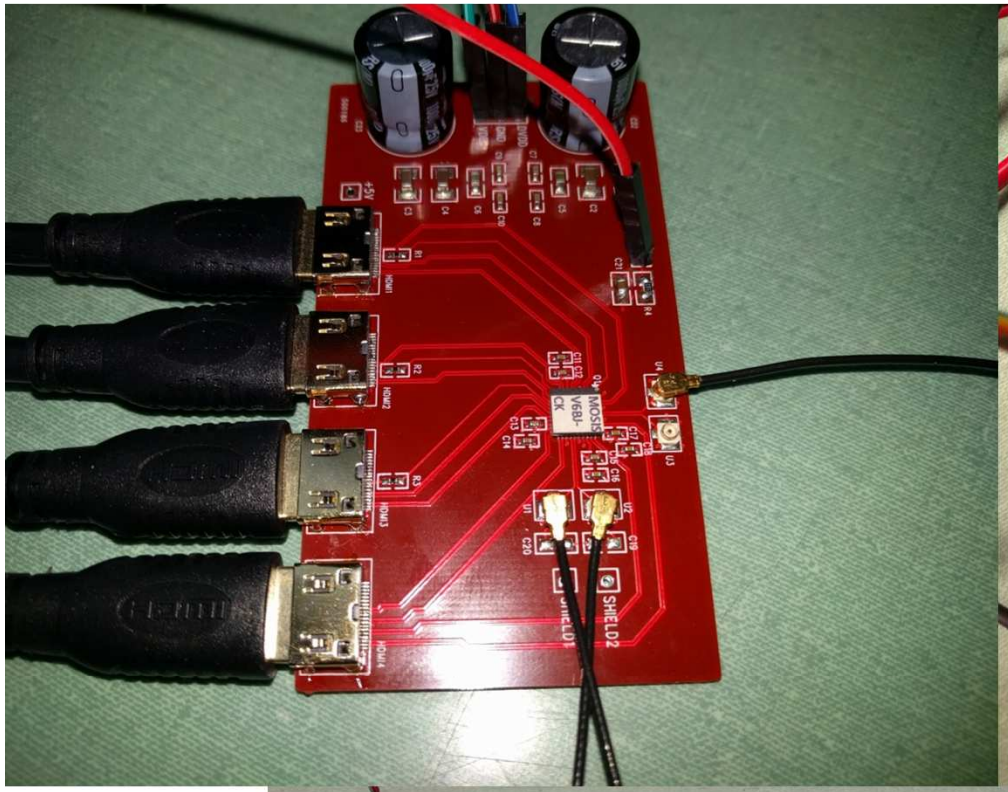


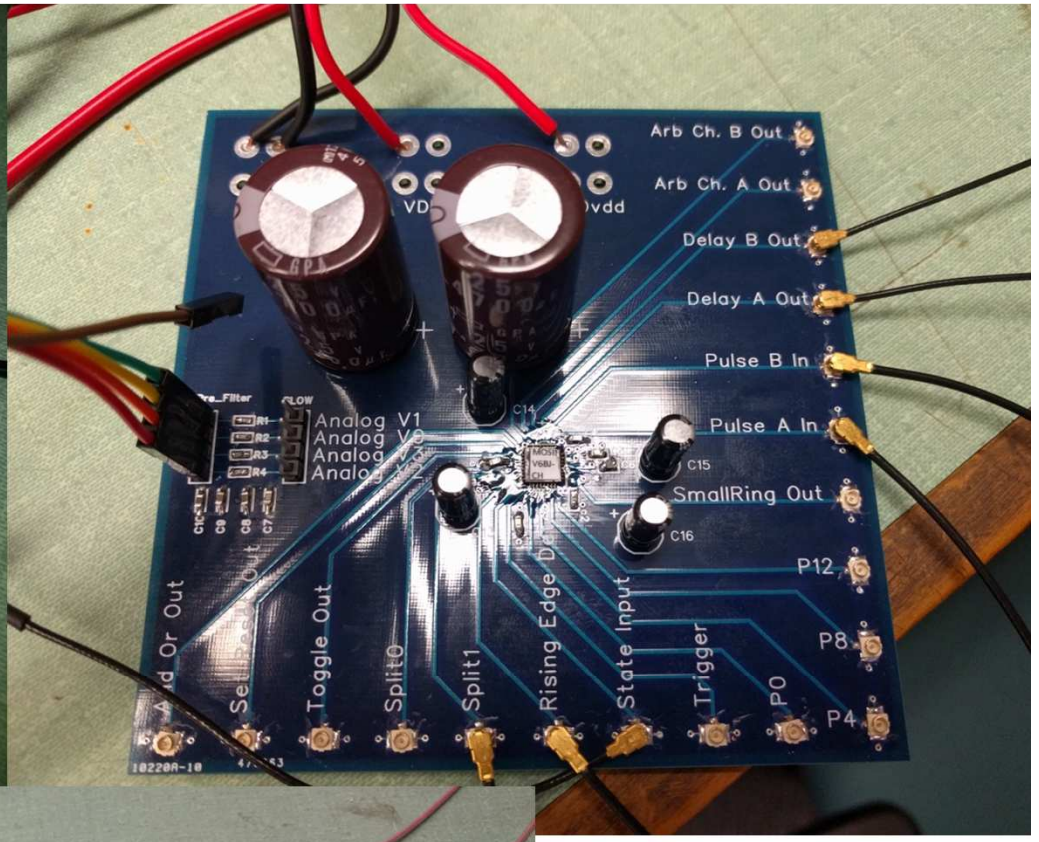
Timing

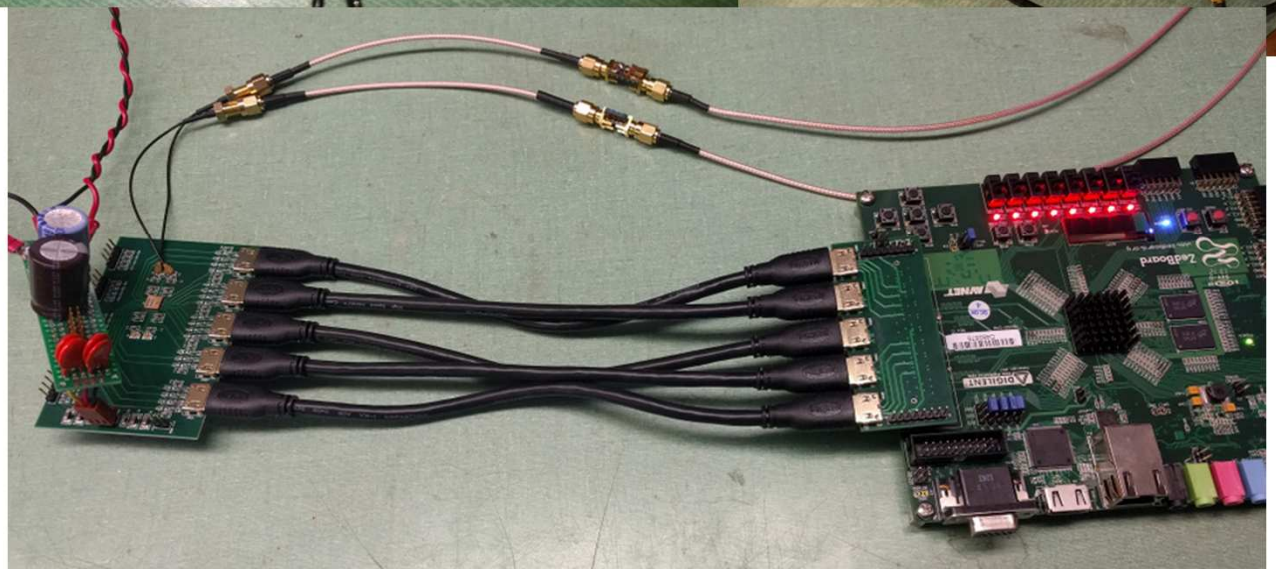
- Cells use pulse-encoding
  - Asynchronous (local timed)
  - Can be used synchronously
  - Timing Accuracy ~1ps
  - Upper:
    - 145ps delay (analog tuned)
    - External source
    - 4 internal logic stages in chain, not counting I/O
  - Lower:
    - 3GHz Oscillators accumulate ~150ps total jitter over 20us




University of California, Santa Barbara

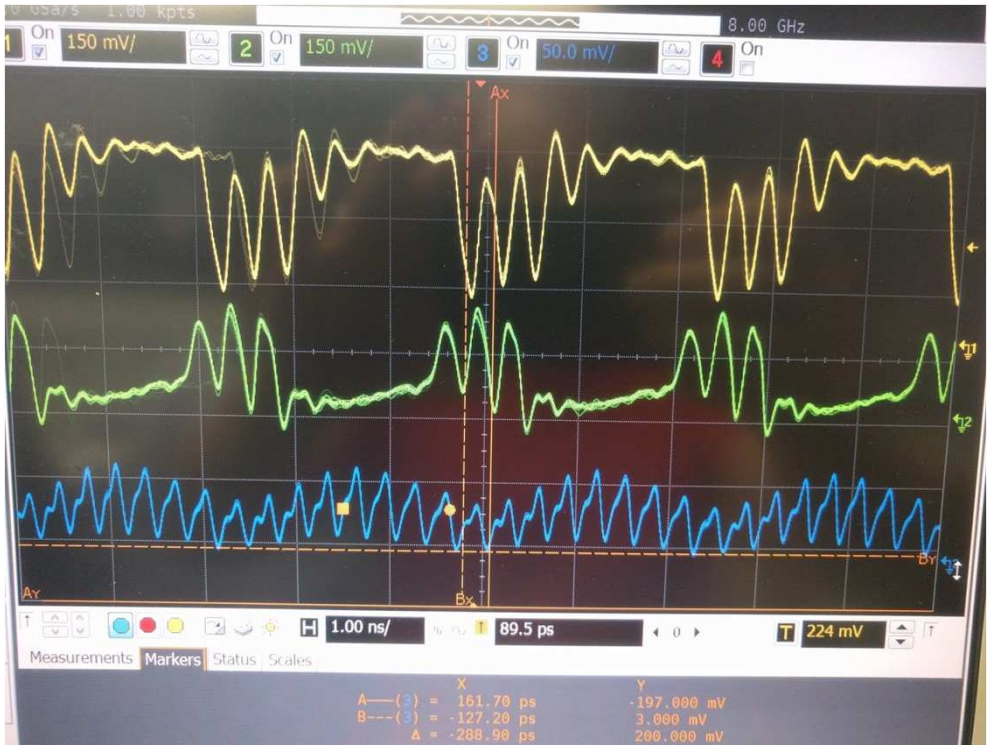



Arb Ch. B Out
Arb Ch. A Out
Delay B Out
Delay A Out
Pulse B In
Pulse A In
SmallRing Out
P12
P8
P4
P0
Trigger
State Input
Rising Edge D
Split1
Split0
Toggle Out
Analog V1
C14
C15
C16



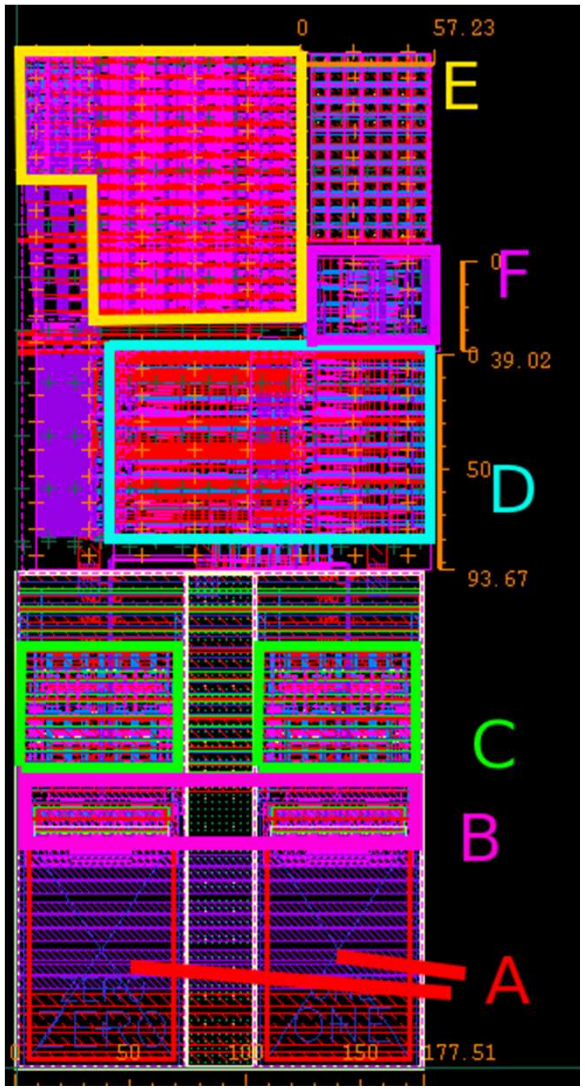
Serial Links & I/O

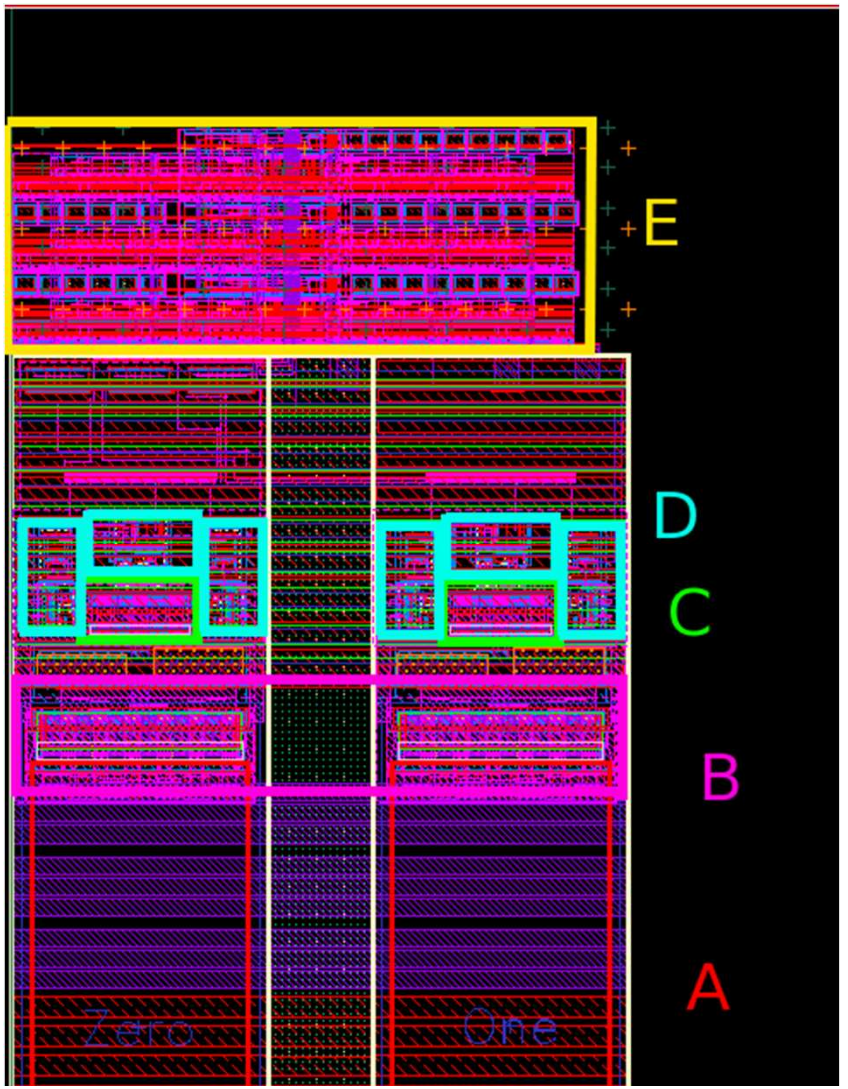
- High-speed serial operates at the upper limits of a logic family
- Pulse-based implementations of I/O have operated at > 5Gbps
  - Implementation of a traditional-style binary link operates at speeds of 6.5+ GBPS in 130nm



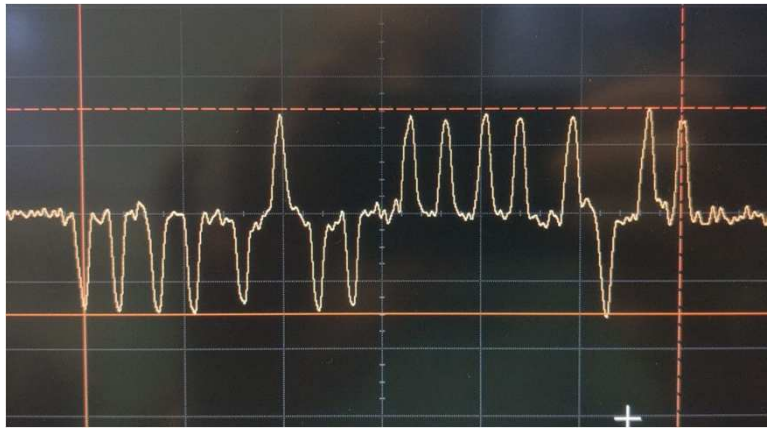
6.6Gbps operation @1.15v

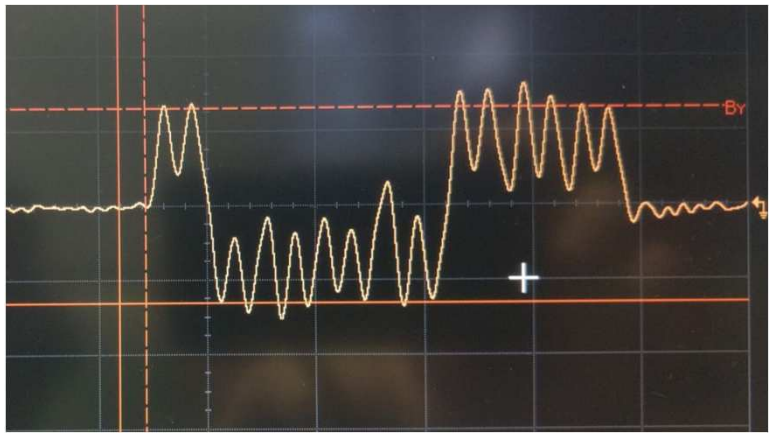
Layout


0
57.23
E
F
0
0
39.02
50
D
93.67
C
B
A
Zero
One
50
100
150
177.51

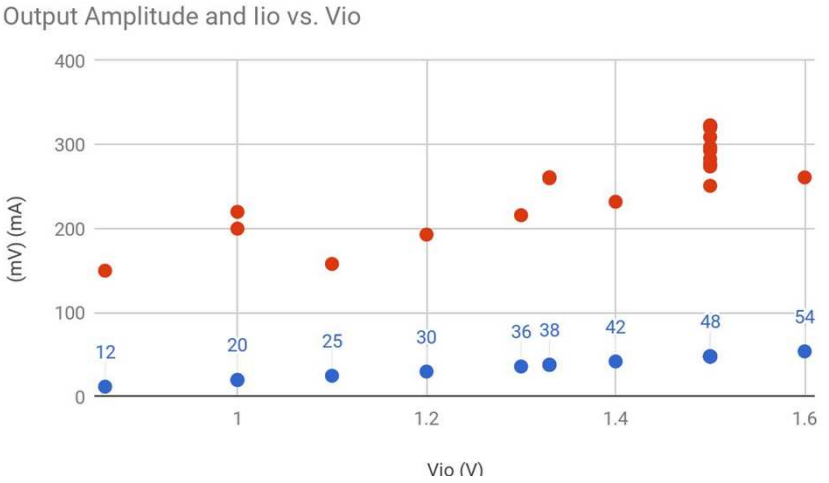

E
D
C
B
A
Zero
One

Asynchronous Low Power Links



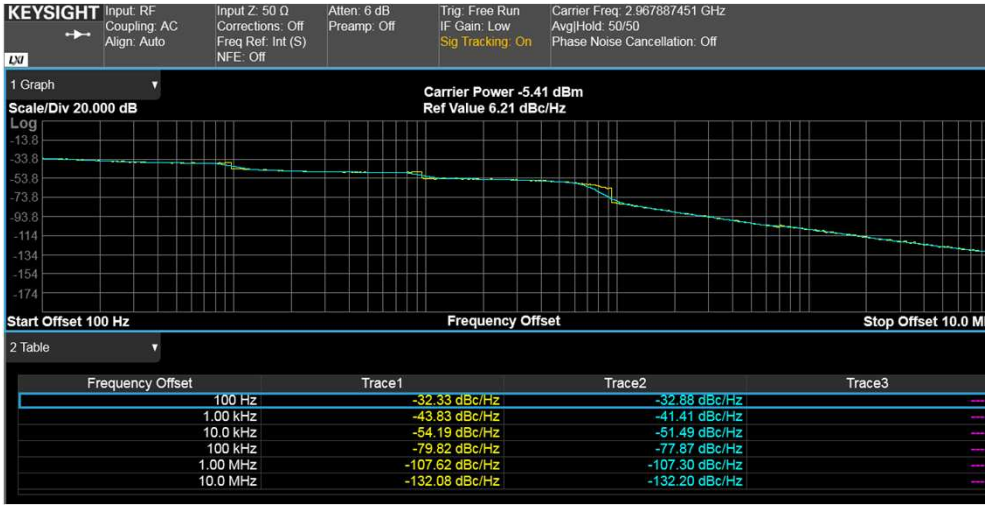


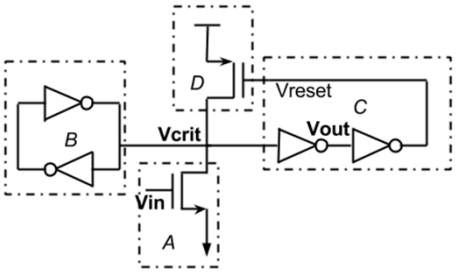
- 3-level Differential Pulse
- 130nm results:
  - 1.35GBPS @0.75V (8.9pJ/bit)
  - 4.3GBPS @1.6V (12.6pJ/bit)
- Useful for chip-chip

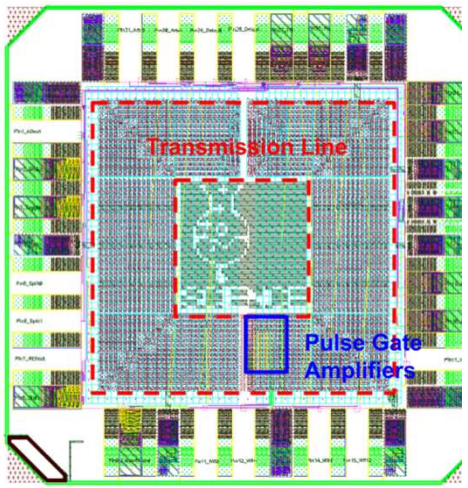


Oscillators/Clocks

- Take advantage of pulse-pulse interactions
  - Soft coupling cycle to cycle averages out noise
- Pulse Ring
  - Very small area
  - More stable than current starved inverter, Low Flicker Noise, Cheap
    - <-100dBc phase noise @10MHz
- Transmission-Line Stabilized
  - Performance near that of crystal oscillators
    - ~100dBc phase noise @ < 1MHz
  - Traveling-wave design reduces the impact of noise at any given transistor
- Both have uniform 12-24 tap poly-phase output, both very hardened







Potential to Share

- High Performance Digital/Timing/IO IP
  - With process/application tuning: (easy technology tuning)
    - Pulse gates are standard cells so can use P&R tools with custom interconnect constraints for medium scale IP.
    - Pads are very technology specific, but likely needed for any high speed design (>300MHz IO/pin).
- Link IP is tough in practice: (hard technology, environment and use-case tuning)
    - Fiber is potentially much easier if willing to go slower!
      - Vcel and APD TID is likely serious problem.
    - Preliminary studies suggest at least ~30% performance left on the table with generic designs, far more if consider mitigation overhead.

Share IP (Cont'd)

- Timing IP (Medium Complexity, requires Variability Mitigation)
  - Voltage to delay (1.1pS jitter)
  - Pulse/Edge Arbiter (1.2pS)
  - Vernier Digital Delay (16_17: 1.2pS digital resolution)
- These can be used to make:
  - Arb. Asynch/Synch Sequential Circuits
  - Digital Time of Arrival with ~1pS resolution (130nm)
  - Low power/footprint Digital links w. cable compensation
  - PLL/DLL/Coupled Clocks

Other Technologies

- 65nm Differential Pad IP (TSMC/INFN Pisa)
- 130nm TSMC (1.2V) Pulse Gates
  - 20% slower than IBM 8rf (1.5V) 130nm
- 65nm TSMC Pulse Gate study (14 GHz Rapidity)

- Recent Collaboration with Prof. Buckwalter (UCSB)
  - 22nm (Global FDSOI) 4-phase TM pulse clock at 14GHz
  - Pulse width allows direct N-path filter drive at 56GB/s
  - Plan to measure dynamics and arbitration resolution in 22nm.
  - Gate Re-implementation in 22 + Full-Custom TM-line layout