Cross-Institutional Training and Continuing Education in ASIC Design

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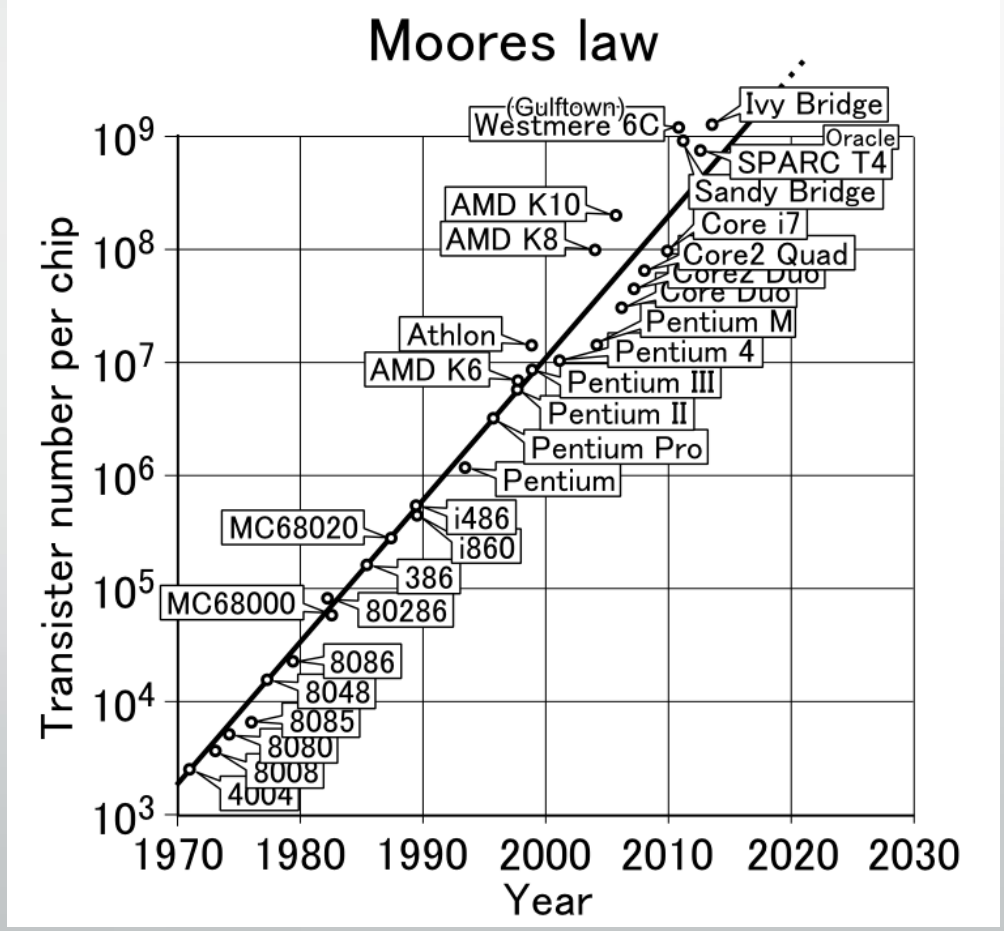
The Perils of the Microelectronics engineer!!!

We have all seen this before…



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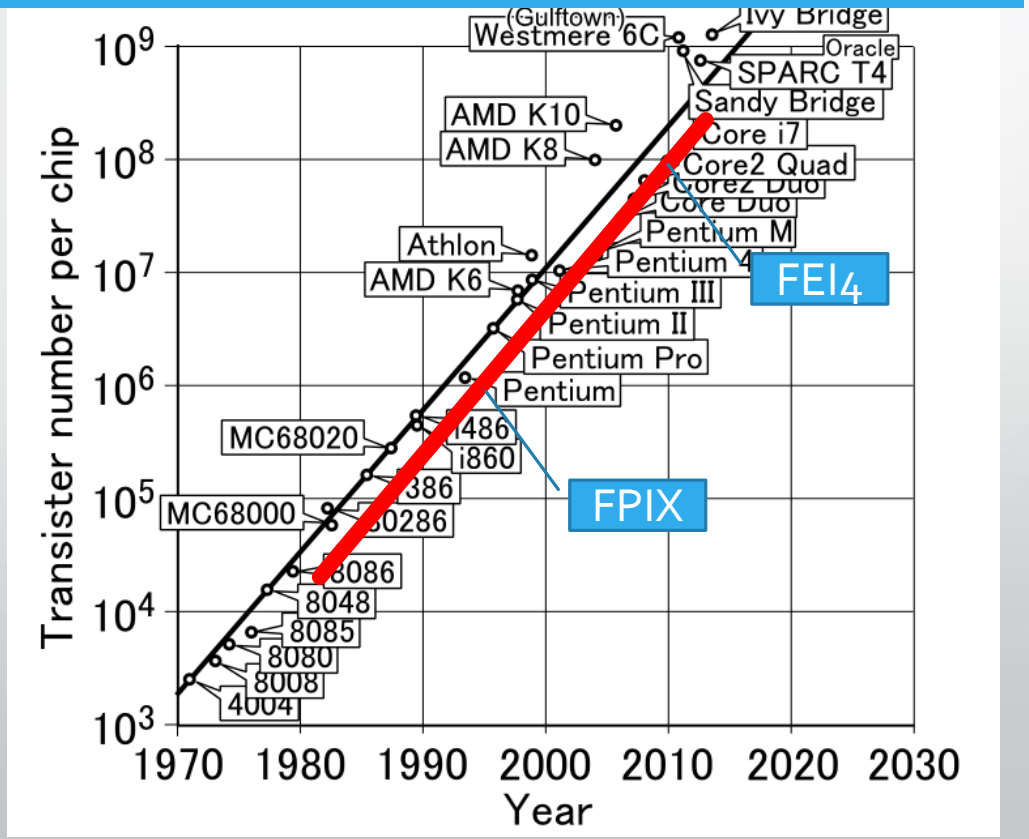
Very Approximate HEP Moores Law



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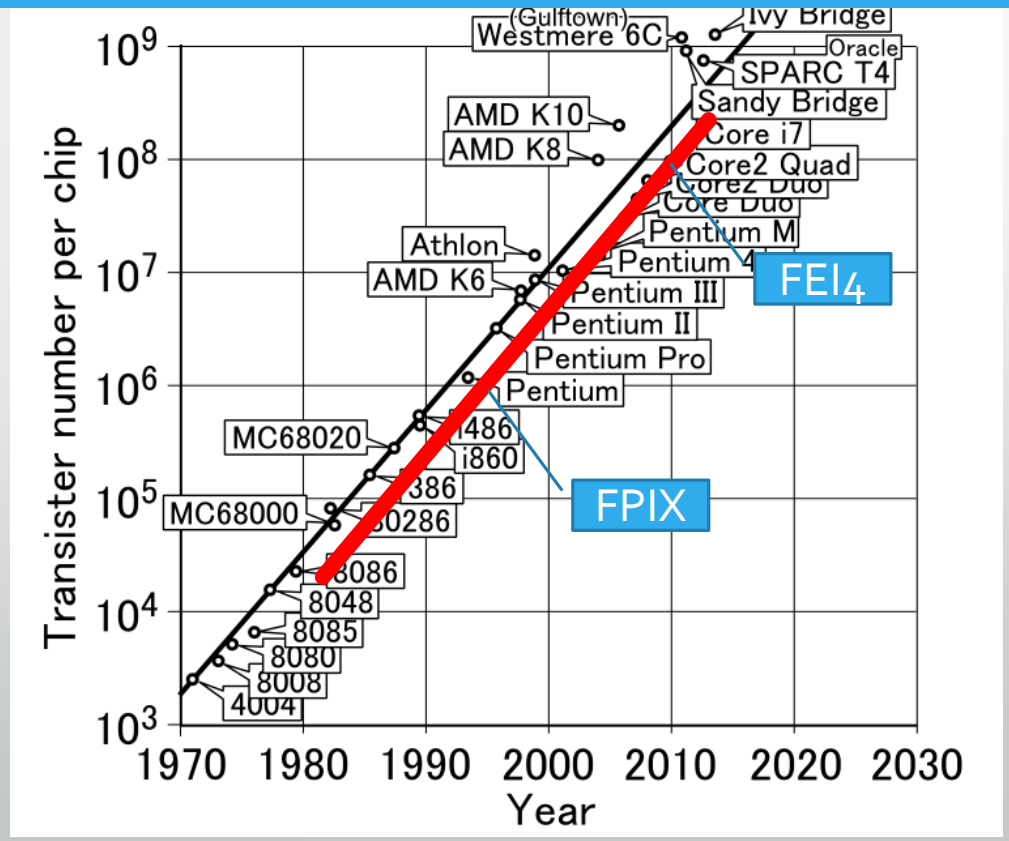


We could probably enjoy ourselves by debating endlessly over this and add our favorite chips to the graph, but that is not the point.

The point is simply that we share in many of the same successes
…and many of the same pains.

Remember the Good Old Days?

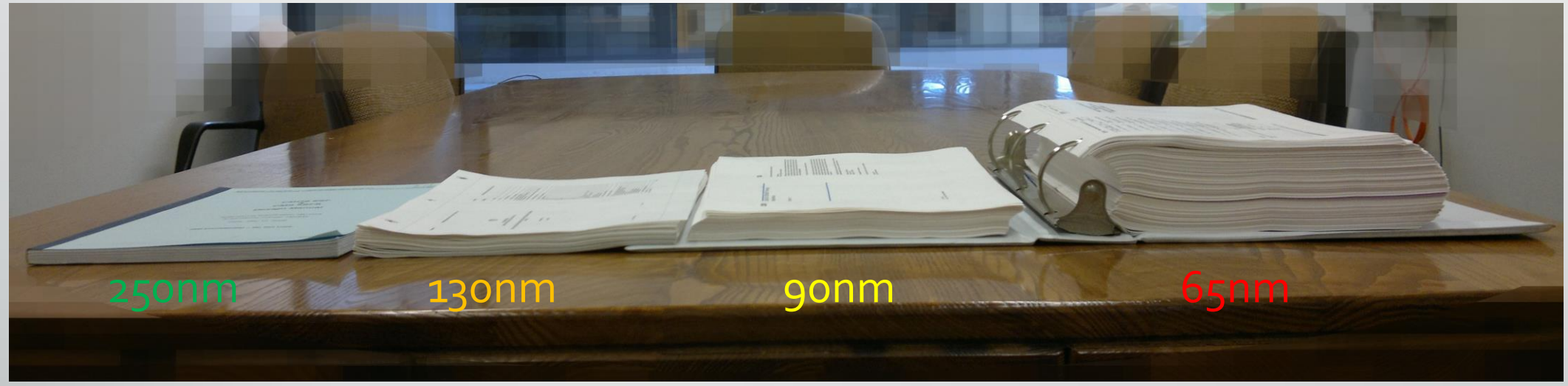
The 80s and the Early 90s

- We designed with Magic and the Berkeley VLSI Suite
- Design rules were Mead-Conway and Lambda-based
- Everybody was a full custom designer
- Everybody simulated with SPICE
- Visual verification still had merit

The Late 90s and the 2000s

- The beginnings of the dominance of Cadence and Mentor
- Increase in the complexity of technology files
  - Switching technologies is more than just adjusting Lambda
- Verilog and the rise of the digital designer
- Standard Cell Libraries

The Perils of the Microelectronics Engineer, Part 2: What Do We Face Now?



- Design Rule Explosion
- Emergence of Electrical Rules
- Emergence of Design for Manufacturability Rules

} They existed before, but have grown more commonplace and critical.

The Perils of the Microelectronics Engineer, Part 2: What Do We Face Now?

- Emergence of Verification requiring 50-70% of the design cycle
- Verilog->SystemVerilog->UVM
- Growing dominance of digital design by transistor count
- Shrinking analog headroom
- PLLs everywhere!!!
- Faster…faster…faster…faster…faster…faster…

The Perils of the HEP Microelectronics Engineer

- Industry overcomes the increasing process and tool complexity with Numbers and Specialization and lots of Support.
- Individual labs will always be low on numbers, but as a group, we can make up for that.
- Engineers in HEP are discouraged from Specialization (even though it is inevitable in many respects – e.g. digital vs. analog designer) because we are encouraged to wear so many hats.
- We get some support from our tool manufacturers.
  - Mutual, inter-lab support can help a great deal
  - Proper, thorough and continuous training is the only thing that can trump a lack of support

The Perils of the HEP Microelectronics Engineer

How do we do this without breaking the bank?

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In May of 2017, Fermilab hosted a 5-day, 2-part class

"System Verilog Design and Cross-Domain Clock Training"

Prior to the start of the class – for the first time - we opened the enrollment to anyone in HEP who was interested. In the end, we had multiple FPGA designers from Fermilab and some Universities (postdocs) and one ASIC designer from Berkeley.

- The presence of the other participants reduced the cost of the training from ~$2500 per student to ~$1800 per student.
- We were able to customize the course to exactly what we wanted
- We were able to schedule the course exactly when we wanted
- Course Feedback Surveys given after the class show that the course accomplished its goals and was very appreciated by its students

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"System Verilog Design and Cross-Domain Clock Training"

This class effectively

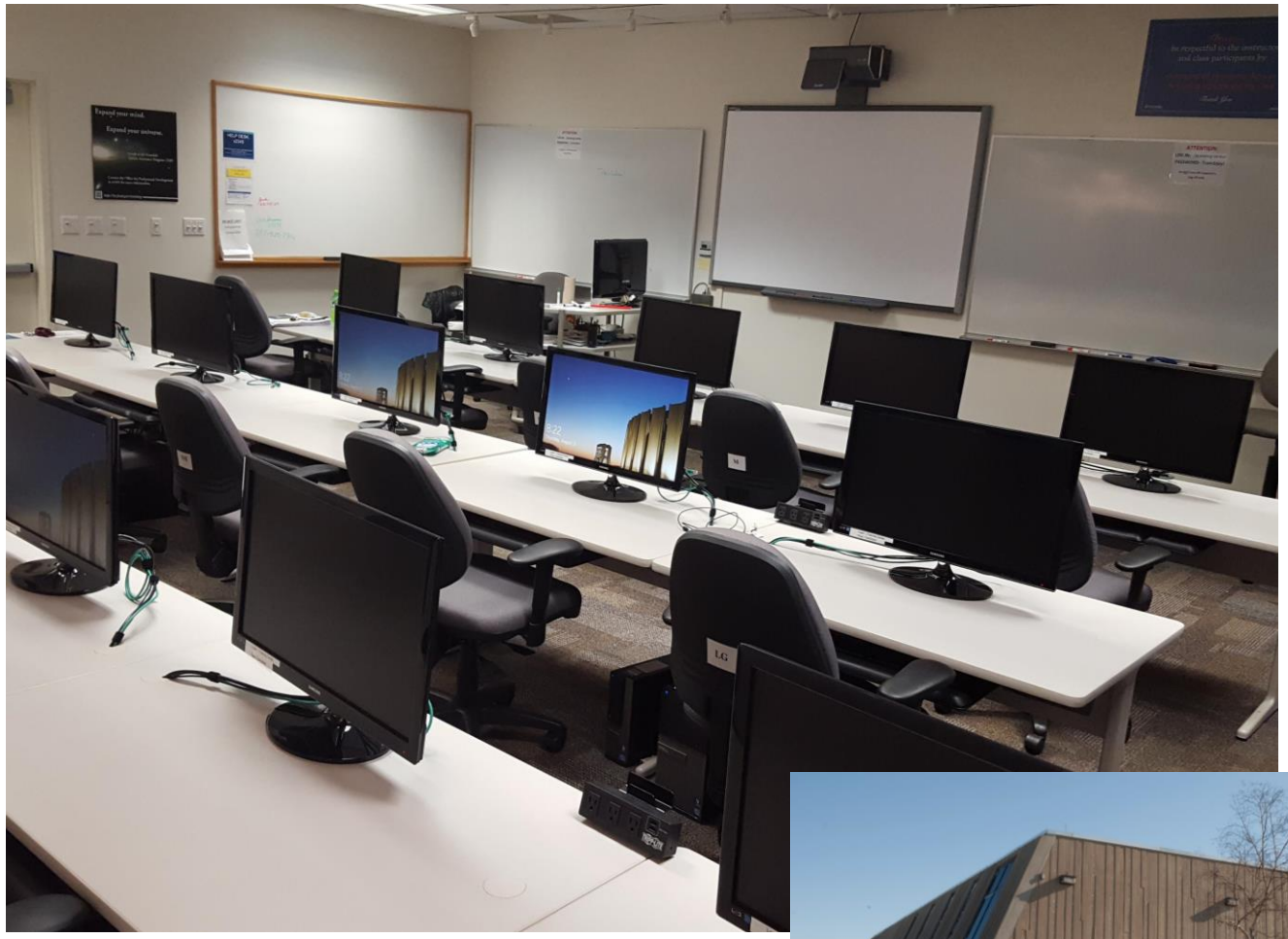
- Leveraged the numbers we have across the HEP community
- Leveraged the mutual support we can give one another across the HEP community
- Brought us together to talk about future possible classes

What if we were to expand on this idea?

- 4 Training Classes per year
  - Perhaps 2 focused specifically on analog
  - Perhaps 2 focused specifically on digital (possible overlap with needs of FPGA community)
- 2 Training Steering Committee Meetings per year
  - Can be by phone/video conference
  - Class subjects decided in advance by the HEPIC community
- Additional classes added as required by the community. For example, CERN "Design Flow" classes could be held in the United States, reducing travel costs.

Fermilab Facilities

- Dedicated Training Center
- 16-seat Computer-based Classroom
- Separate Lecture-only Classroom
- Access to all Cadence/Mentor/Synopsis software available at Fermilab.



Class Suggestions (so far…)

ASIC

- Intro to SystemVerilog
- SystemVerilog for Verification
- UVM (Universal Verification Methodology)
- SystemVerilog Synthesis in ASICs
- Cadence Mixed-Signal Design and Simulation
- Analog-to-Digital Converter Architectures
- Noise Modelling
- Any Mead Mixed-Signal Course

overlap

FPGA

- Intro to SystemVerilog
- SystemVerilog for Verification
- UVM (Universal Verification Methodology)
- SystemVerilog Synthesis in FPGAs
- Timing Constraints
- FPGA Model building
- Advanced VHDL for timing constraints

Let's Talk About this

- Steering Committee
  - Volunteers?
  - One from each lab?
- What classes are of greatest need?
  - Digital/Verification
  - Analog
- What other, related ideas do people have? How can we support this?

Other ideas

Front-end Electronics Meeting

- Add a day to either end of FEE
- The community picks one project (ahead of the conference)
- The designers of that project present a "deep dive" into that project for a full day – what choices were made and why, pitfalls, etc.
- (two projects each for a half day)

Nuclear Science Symposium

- 2-day Tutorial –
  "Design by Designers for Designers"
- Day 1 – Front end
- Day 2 – Back end

POSSIBLE First Class

High-Level SystemVerilog Intro (2-days) and UVM Verification (3-days)

December 4-8, 2017

-OR-

SystemVerilog for Verification (2-days) and UVM Verification (4-days)

November 30-December 1 and December 4-7, 2017