ASIC work at SMU.Physics for ATLAS upgrades and future HEP experiments

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Outline of this report

- An introduction to the HW group in SMU.Physics
- ASICs for ATLAS phase-1 upgrade
- ASICs for ATLAS phase-2 upgrade
- ASICs for future HEP experiments
- Summary

The Hardware group in SMU.Physics

- The hardware or electronics group in SMU.Physics was established in 1998 when we joined ATLAS Liquid Argon Calorimeter (LAr) and took on the work to develop the optical link for LAr's detector front-end.
- The group played a leading role in the development of the optical link system (1524 fiber channels) that reads out the ATLAS LAr. This link is based on the G-Link chipset, but operates at 1.6 Gbps per fiber. This was just before the time of the CERN ASIC GOL, a serializer based on 0.25 um CMOS.
- We started ASIC design in 2004. Thanks to Ping who helped us to get started, and introduced us to the 0.25 um SOS process with which we designed ASICs for the ATLAS phase-1 upgrade.
- We learned how to design ASICs, in particular the serializer, from the GOL design that CERN (Paulo Moreira) shared with us. We appreciate the decades long help that we receive from the CERN group, together with help from the community (Mitch Newcomer, BNL, Nevis, U.of.Michigan, etc). We also follow Sandro Marchioro's advice to "recycle" physicists into designers while at the same time we try to learn as much as possible from our EE professionals.

The Hardware group in SMU.Physics

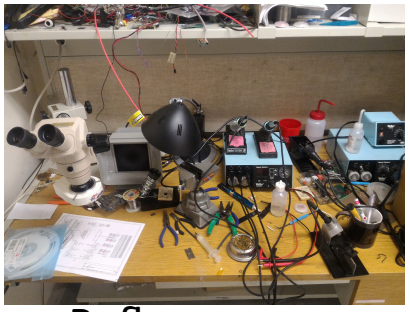
- We are (were) a member of the ATLAS collaboration, the Versatile Link, VL+ and the lpGBT common projects.
- The group has research staffs + students that cover a range of work from ASIC designs, PCB level circuit designs and testing which include R&D or production tests, accelerated stress tests, and irradiation tests.
- Over time we have established a lab of about 3,000 ft^2, with instruments that range from wire-bonders, probe-station to real-time and sampling scopes, from reflow oven, rework-stations to x-ray machine and cryogenic (LN2) test station. In data transmission we can characterize signals up to 30 Gbps.

The Hardware group in SMU.Physics

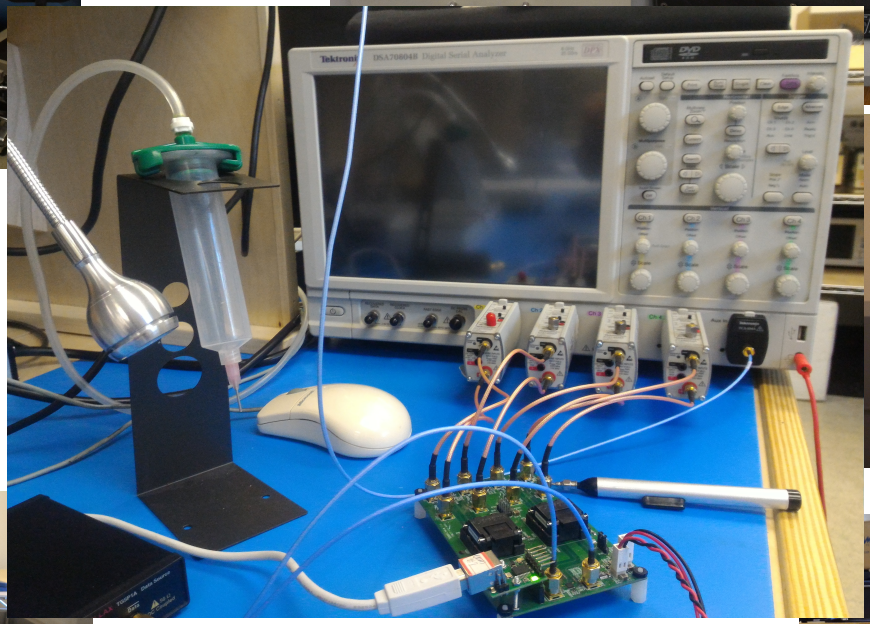
One of the rooms of the lab in Physics SMU

The Hardware group in SMU.Physics

Ball and wedge bonders, probe-station

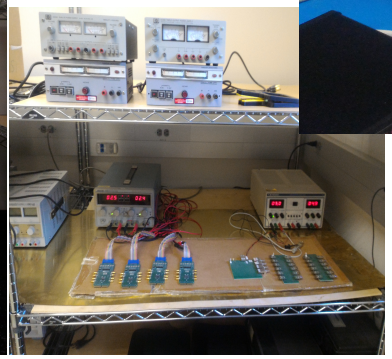


Reflow oven, rework stations



Characterization or QA/QC tests

X-ray chamber

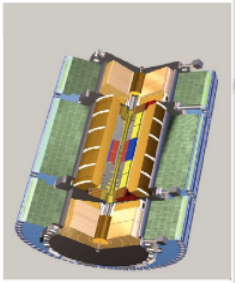


Accelerated stress and life tests

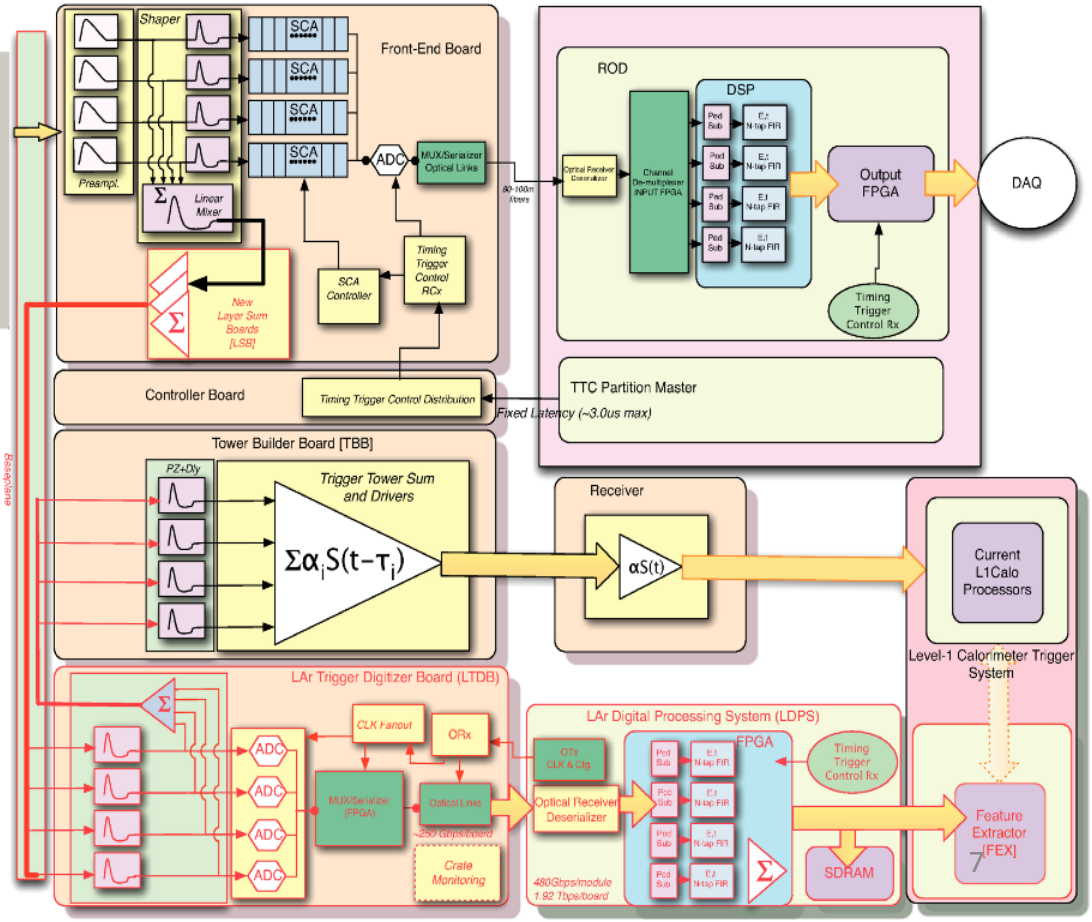
LN2 Dewar with temp control/ monitoring

ASICs for ATLAS phase-1 upgrade

For ATLAS phase-1 we designed two ASICs, LOCx2 [ref] and LOCld [ref], a dual-channel serializer and VCSEL driver with 5.12 Gbps each channel. LOCld will be used in the mid-board optical transmitter and transceiver MTx and MTRx [ref] which are also developed in the lab.



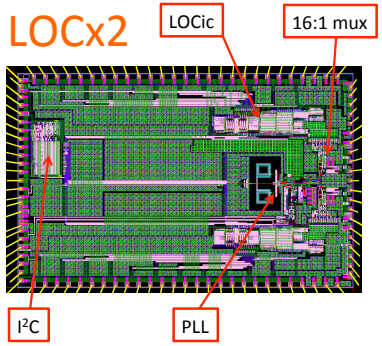
ATLAS/LAr



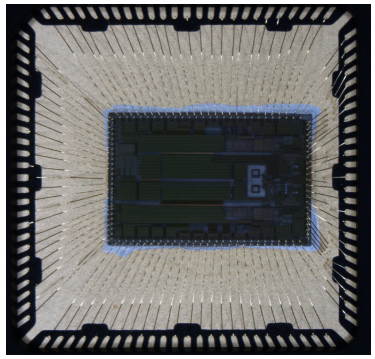
- ATLAS LAr trigger upgrade (phase-1), an effort of many institutions.
- LTDB uses ASICs from CERN, Columbia, and SMU

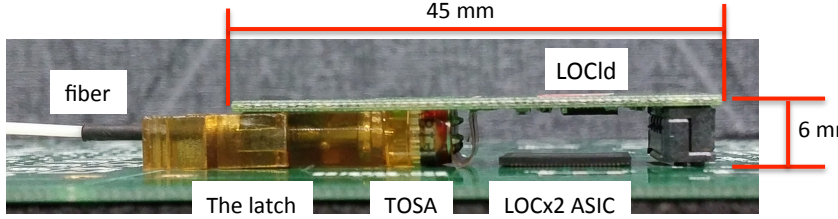
ASICs for ATLAS phase-1 upgrade

In the digital readout of LTDB, we contribute to two ASICs and two optical modules:

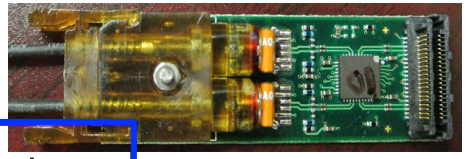


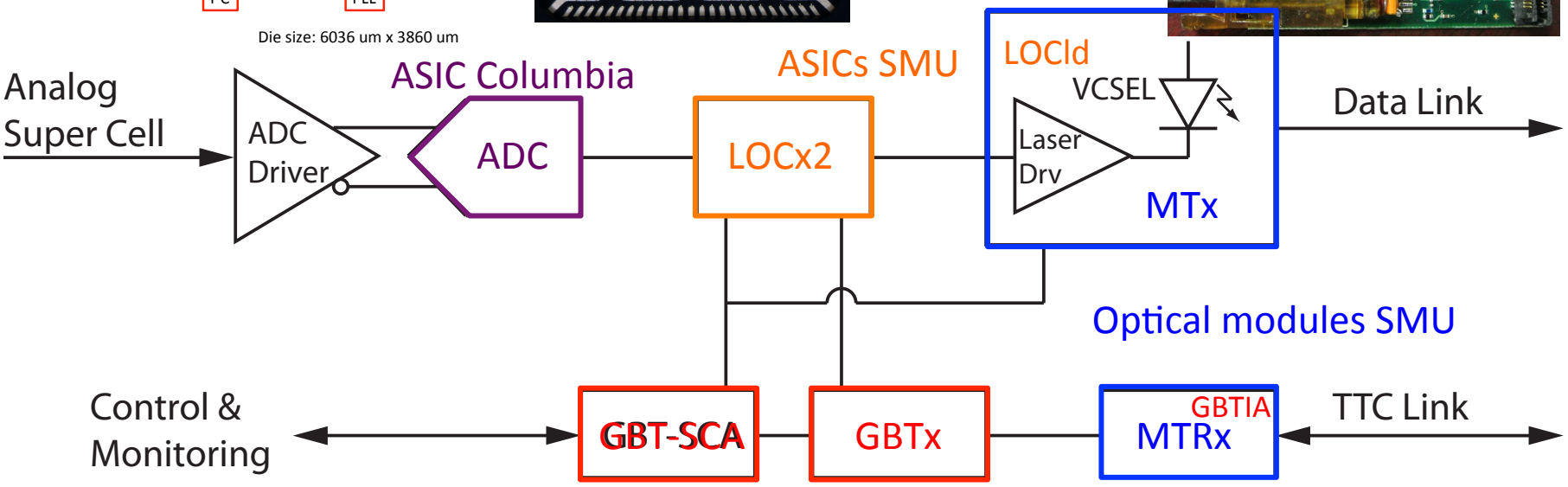
Die size: 6036 um x 3860 um





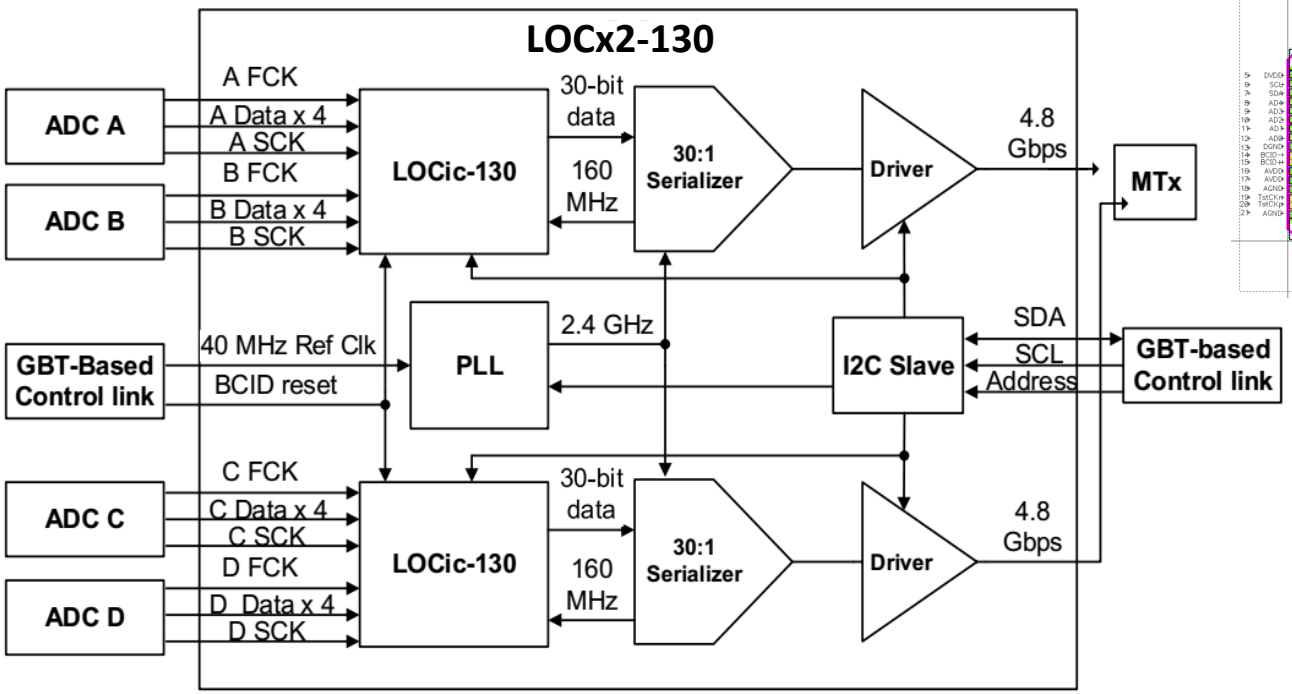
MTx

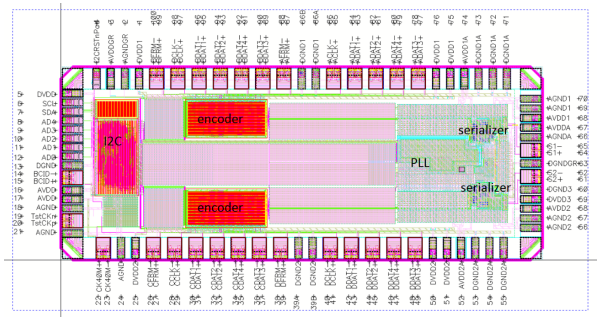


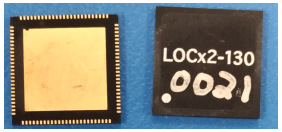


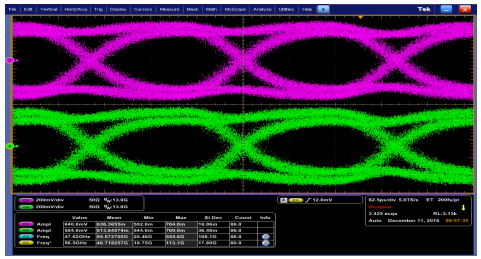
ASICs for ATLAS phase-1 upgrade

- As the 0.25 um SOS process is not mainstream and not the ones (130 nm and 65 nm CMOS) used in our community, there has been a lot of worries about the reliability of the ASICs. We designed a drop-in backup to LOCx2 and LOCld. They are called LOCx2-130 and LOCld-130. LOCx2-130 will be produced with several other chips in US-ATLAS that use the same process.
- In LOCx2-130, we adapted the digital interface (LOCic) from LOCx2 to achieve the required low latency, we use the core IPs of GBTx (the PLL and the serializer), we still share the PLL to save on power.



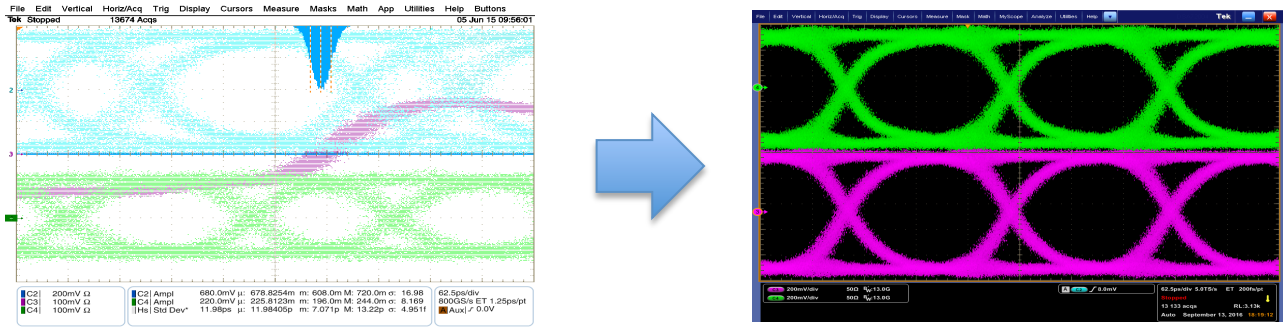






ASICs for ATLAS phase-1 upgrade

- We have gone through the stages of ASIC design, prototyping, wafer fabrication and chip packaging. We are now in the phase of performing quality control/assurance and life testing.
- Many lessons learned:
  - Should use IC technologies CERN identifies and chooses:
    - Designing ASICs that withstand radiation takes time and efforts.
    - High NRE cost in wafer fabrication.
  - When the number of chips needed are in hundreds to thousands but not millions, Packaging needs to be taking into consideration even at the R&D stage for yield and cost effectiveness.
  - Time and efforts need to be foreseen to achieve high overall (die and packaging) yield, effective (or even automated) chip screening, and conducting accelerated stress tests to understand the reliability of the ASICs.



It took us two years' time and several MPWs to understand radiation induced distortion in LOCx2's eye diagrams and to find the way to correct that.

ASICs for ATLAS phase-2 upgrade

- For phase-2, we joined the two common projects, lpGBT and Versatile Link+ for the developments of ASICs and optical modules. Limited by funding in US-ATLAS, we recently had to stop our activities in VL+, giving priority to our involvement in the lpGBT project.
- In lpGBT we have contributed to several designs (next slide).
- These IP blocks not only are integrated in lpGBT, some of them also find use in other designs through the IP sharing process established at CERN (also next slide).

ASICs for ATLAS phase-2 upgrade

- Design IPs we contribute to lpGBT:
  1. The PhaseAligner: Align the ePort input parallel data with rates range from 160 Mbps to 1.28 Gbps
  2. The PhaseShifter: lpGBT recovered clock output phase, programmable with a resolution of 50 ps
  3. The lpGBT deserializer's 2.56 Gbps equalizer
  4. The ePort eRx SLVS receiver
  5. The vBuffer
- Design IPs we contribute to other groups
  1. The PhaseAligner for MPA (Macro Pixel ASIC), the ASIC for CMS' outer tracker HL-LHC upgrade. The design had to be slightly modified.
  2. The PhaseAligner for CIC, the ASIC also for CMS' outer tracker HL-LHC upgrade
- IPs through CERN that we have used so far
  1. We use the I2C slave from CERN in several designs, sometimes with modification.
  2. We use the GBT/TDS PLL and serializer from CERN/Univ. of Michigan, also with a small modification.
  3. We adapted the SLVS receiver from GF-130nm (CERN) to SOS-250 nm in LOCx2.

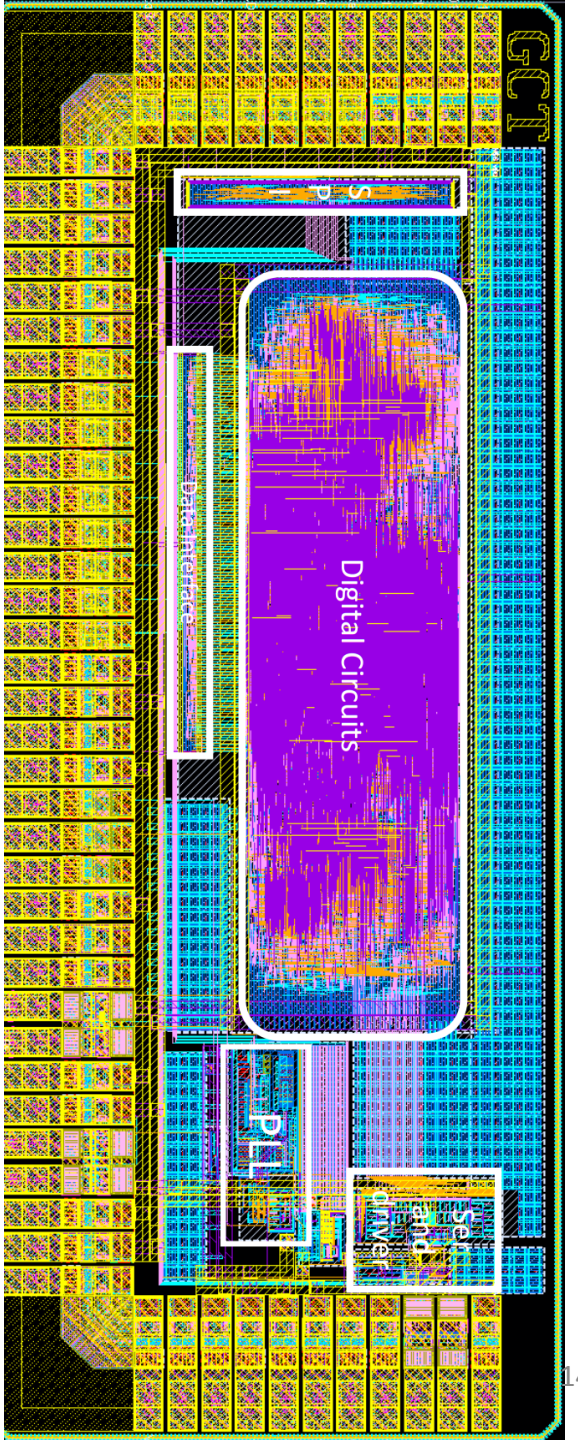
ASICs for future HEP experiments

- Recently we have designed and prototyped the following ASICs for future HEP experiments:
  - GCT (next slide, and please poster)
  - VLAD14 and TIA14 (please see poster)
- The design work is through collaborations with CERN and other institutions like IN2P3 (Strasbourg) and CCNU (China).

GCT Summary

GCT (Gigabit CMOS Senor Transmitter) is an ASIC IP block designed for multi-gigabit-per-second serial link data transmission in CMOS Monolithic Active Pixel Sensor(MAPS). It features:

- TowerJazz 0.18 um CIS process, 2360um X 760um
  - Compatible with MAPS process for future HEP experiments
- 3.2 Gbps data rate
- Reed-Solomon encoder, correcting burst bits error up to 20-bit
- Digital circuits are fully triplicated to tolerate SEU
- CML driver with 3-tap pre-emphasis
- 174 mW power consumption from 1.8V supply



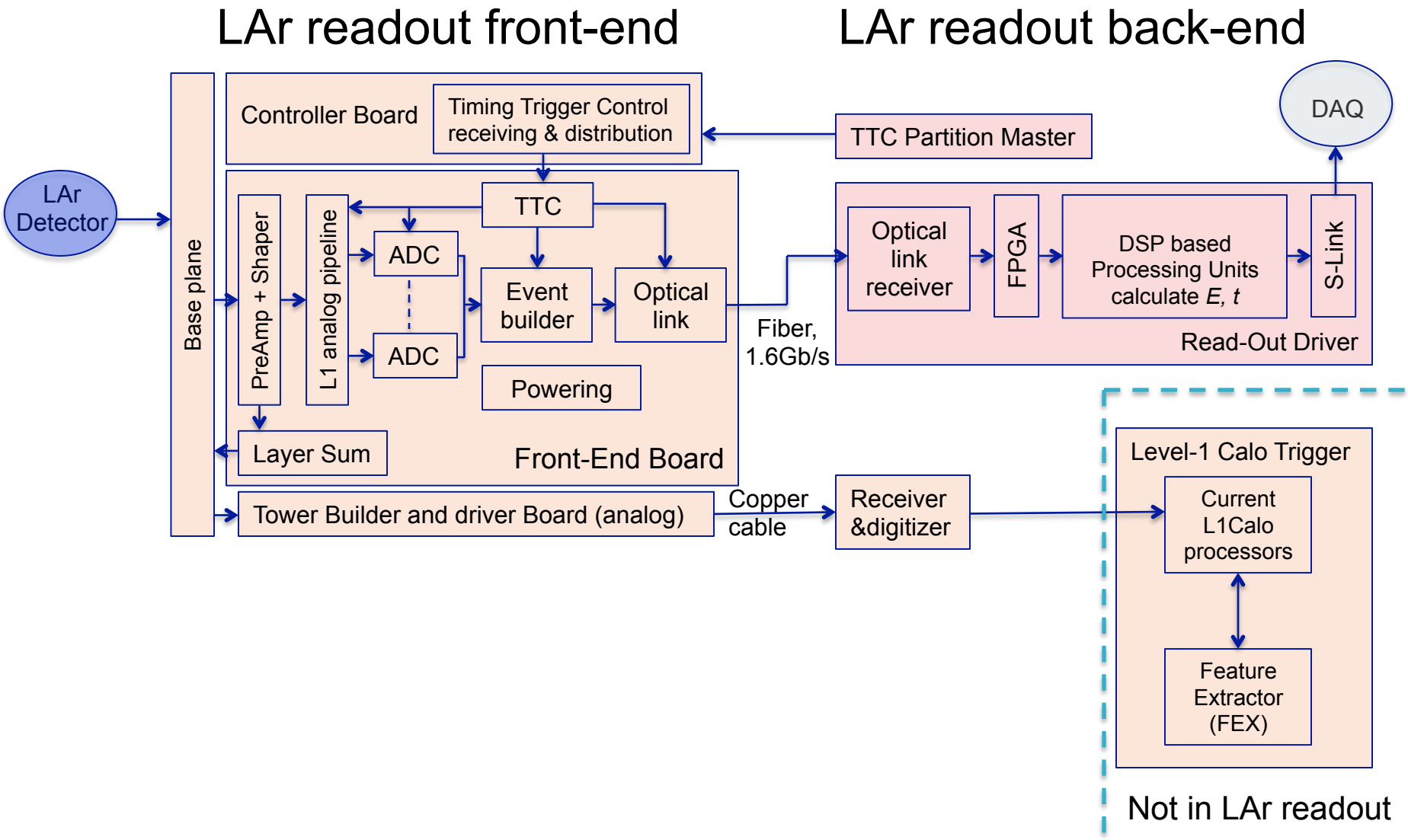
Summary

- SMU.Physics has a hardware group that is active in ATLAS phase-1 and phase-2 upgrades, and in R&Ds for future experiments.
- It is challenging for a university group to follow through ASIC developments from design to fabrication to packaging and to all types of testing. Collaboration among university groups, and with national and international labs is essential.
- Although we involve our graduate students and postdocs in the ASIC work for physics, it is beyond the time scale of the training for these people to develop the expertise of this highly specialized endeavor. We must rely on research staffs, especially those who have gone through one full cycle of R&D + construction of an experiment.

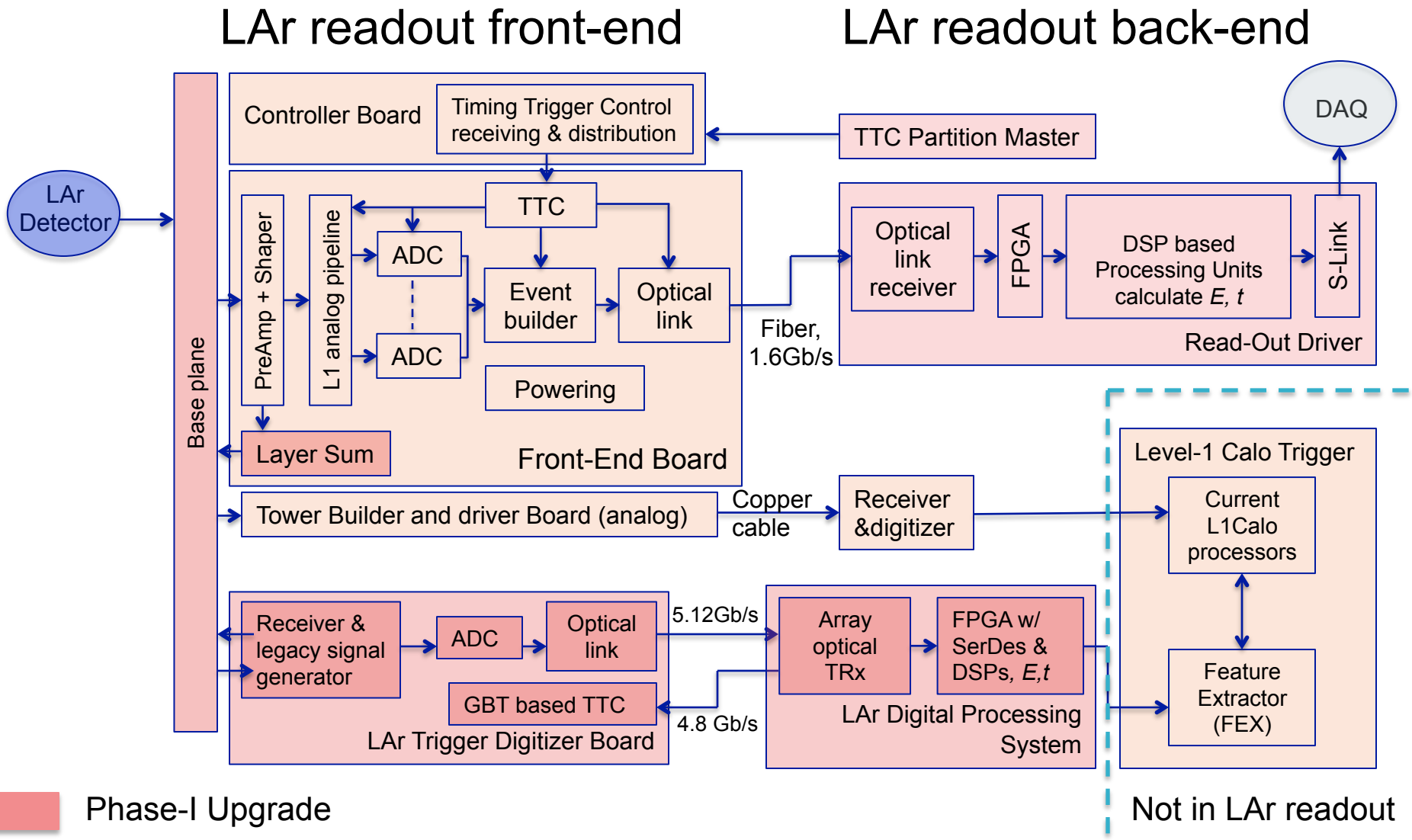
Thank you!

Backup Slide

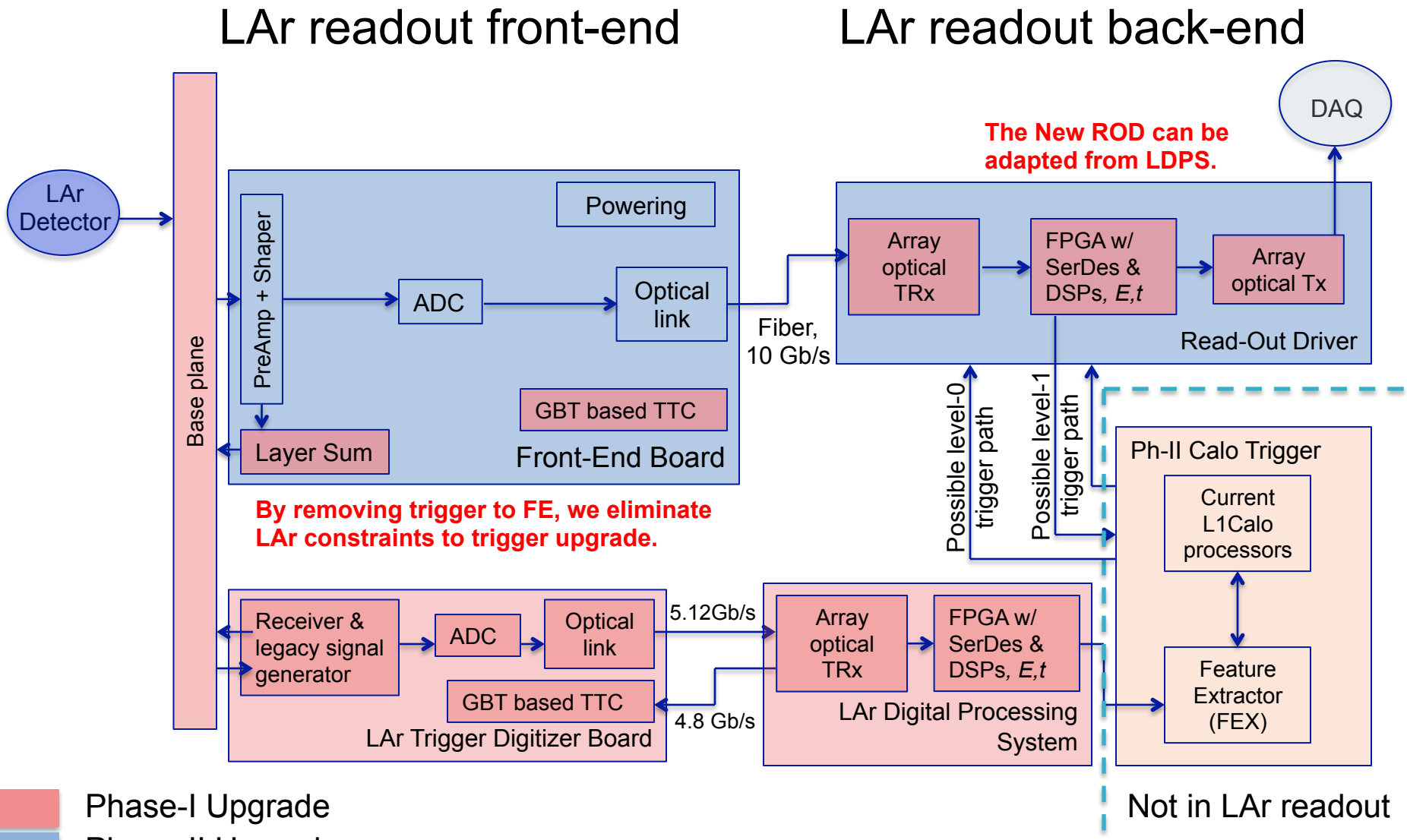
LAr Readout


LAr readout front-end
LAr readout back-end
LAr Detector
Base plane
Controller Board
Timing Trigger Control receiving & distribution
TTC Partition Master
DAQ
TTC
PreAmp + Shaper
L1 analog pipeline
ADC
ADC
Event builder
Optical link
Powering
Layer Sum
Front-End Board
Fiber, 1.6Gb/s
Optical link receiver
FPGA
DSP based Processing Units calculate E, t
S-Link
Read-Out Driver
Tower Builder and driver Board (analog)
Copper cable
Receiver &digitizer
Level-1 Calo Trigger
Current L1Calo processors
Feature Extractor (FEX)
Not in LAr readout

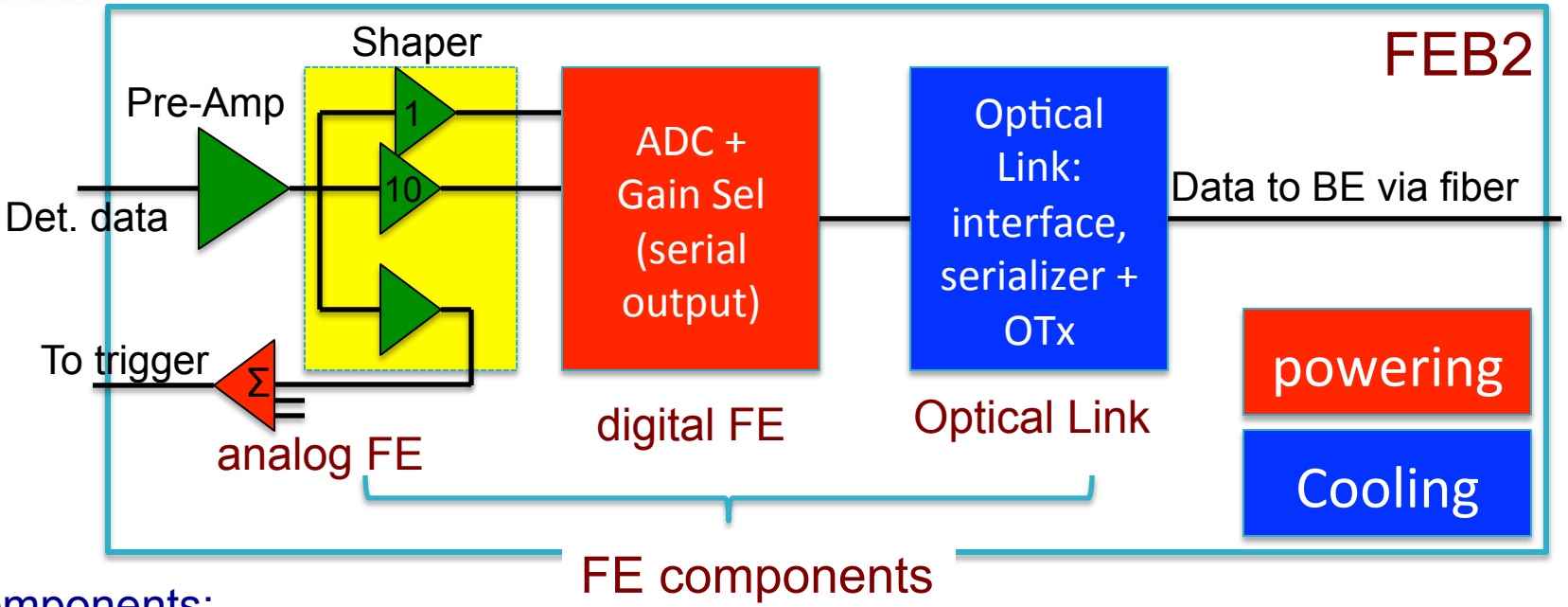
LAr Readout with Ph-I Upgrade



LAr Readout with Ph-II Upgrade



Key R&Ds for the Front-End



Components:

- Pre-Amplifier + Shaper → one ASIC. Prototyped with SiGe, just start with 65 nm CMOS
- ADC ASIC: 40 or 80 MSPS with 16-bits effective dynamic range, likely with 65 nm CMOS.
- Optical Link ASICs and optical transmitter: 10 Gbps per fiber. ASIC with 65 nm CMOS. OTx likely with array optics.

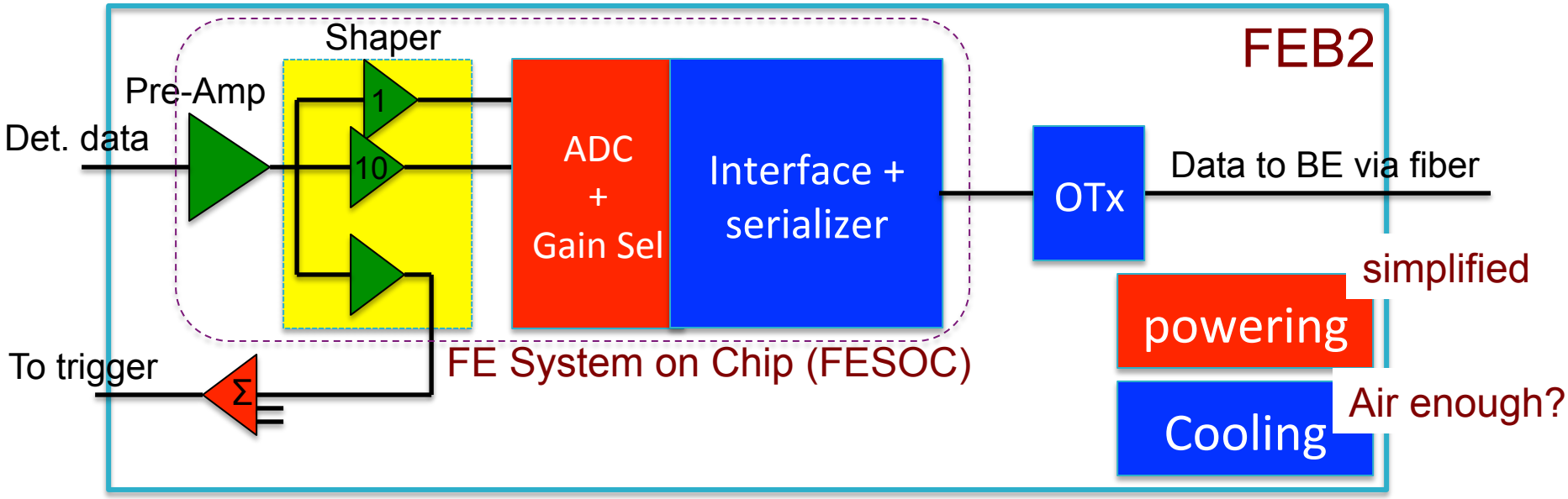
System Integration:

- Module 0 demonstrator.
- Powering.
- Cooling.

- Prototype on Silicon-Germanium with IBM and IHP. IBM is selling its foundry. IHP is a research oriented small company. ➔ technical risk.
- We plan to work with CERN on 65 nm CMOS (TSMC) which is mainstream and expected to be available for Phase-II production.

FE System-on-Chip

A new idea since 2013



- FESOC, a one die or two die chip that integrates the three key ASICs. By combing the ADC with the serializer (both in 65 nm CMOS), one eliminates the output circuits for the ADC hence saves power.
- Impact on system integration and in construction:
  - Simplified FEB2, powering and potentially cooling.
  - Reduce production cost in chip packaging and QA, and in FEB PCB.
  - The impact on yield may be small as the yield of 65 nm CMOS is expected to be high and the cost of die is small.