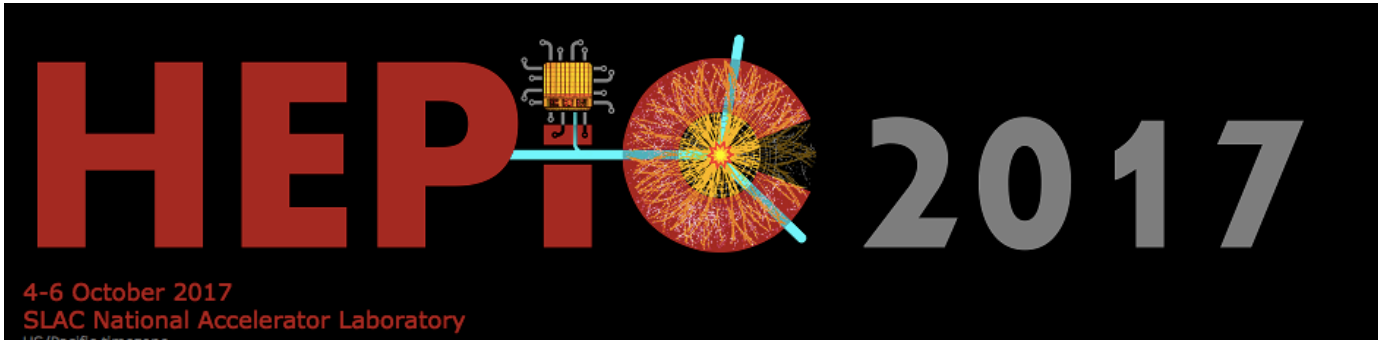
IC Design at SMU EE Led by Ping Gui



Ping Gui, Professor
Department of Electrical Engineering
Lyle School of Engineering
Southern Methodist University

HEPIC 2017 @SLAC
Oct. 4-6, 2017

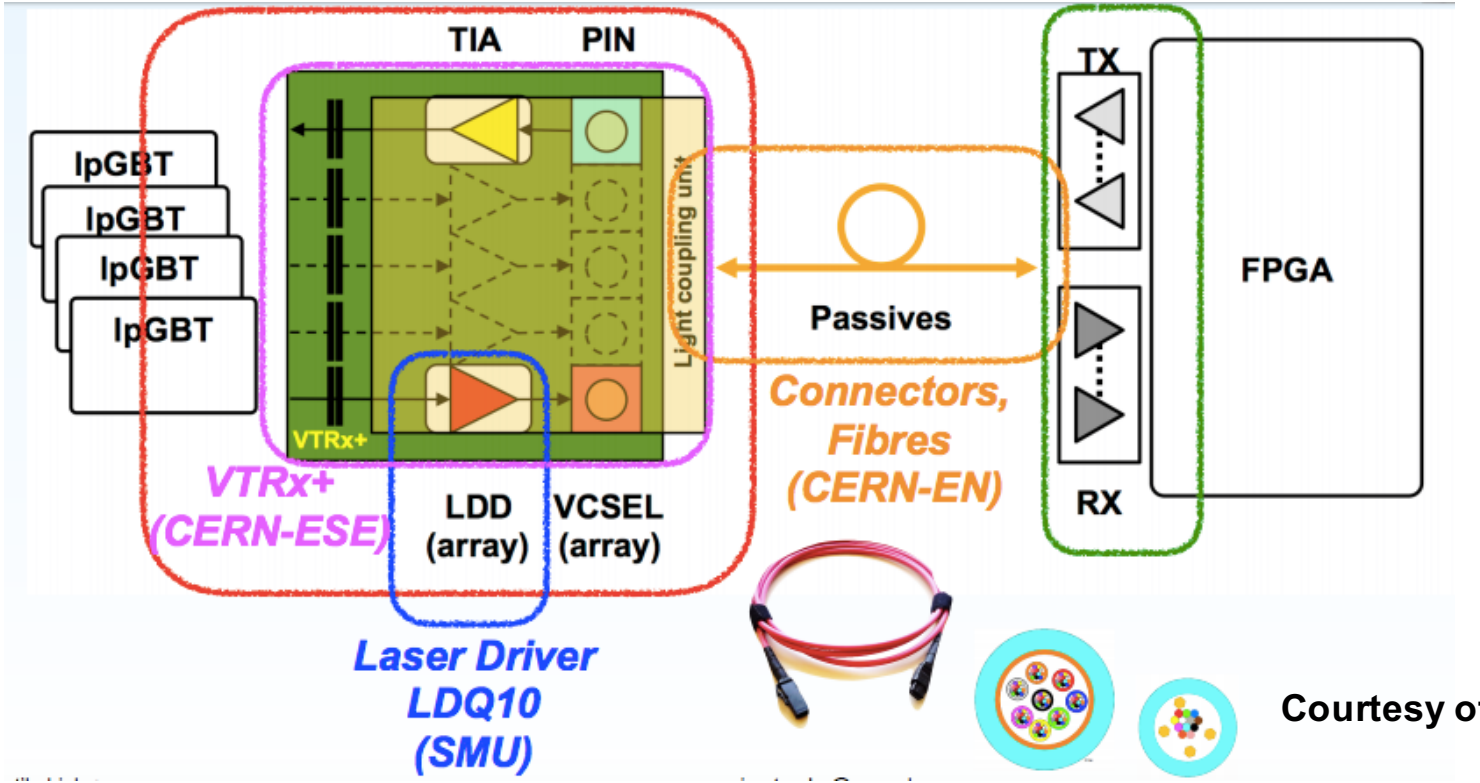
Ping Gui's Research on IC Design

- Analog, Mixed-signal and RF IC design for a variety of applications
- Funded by federal agencies, industry, foundations etc.
- Currently 8 full-time Ph.D. students, several MS and undergraduate students

Recent and On-going Research Projects

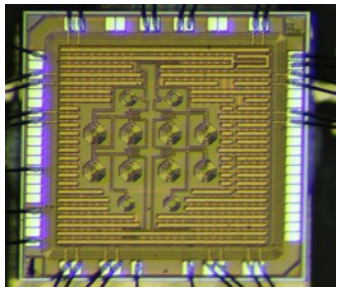
- ICs for HEP experiments
  - with CERN: GBT, LpGBT, Versatile Link
  - Fermilab: COLDATA
- ICs for consumer electronics and communications
  - High-speed optical and wireline communications
  - 5G wireless and automotive radar
- ICs for Biomedical applications

GBT, LpGBT, and Versatile Link Projects

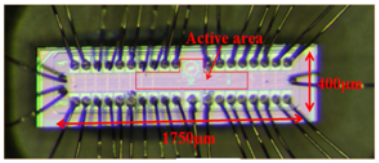


Courtesy of Jan Troska

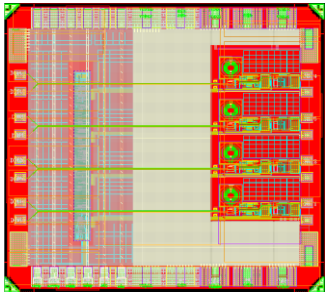
ICs Designed as Part of GBT, LpGBT, and Versatile Link Projects



10Gb/s GBLD10
0.13μm CMOS (2014)

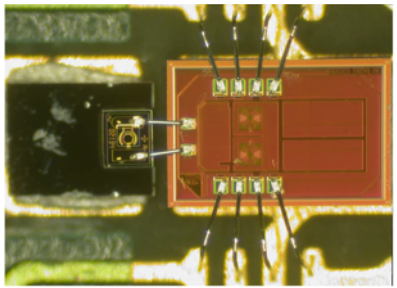


Low-power compact
10Gb/s LpGBLD10
65nm CMOS (2015)

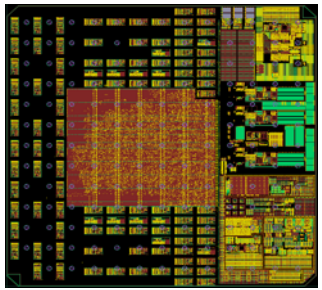


4x10Gb/s Quad Laser
Driver (LDQ10) in
65nm CMOS (2016)

Sponsored by DoE
Collider Research Program

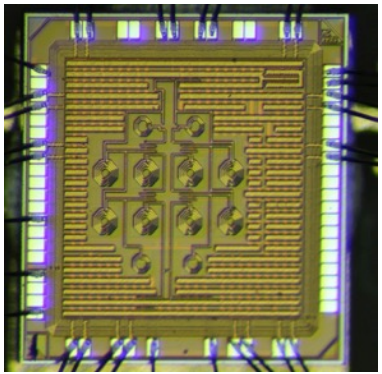


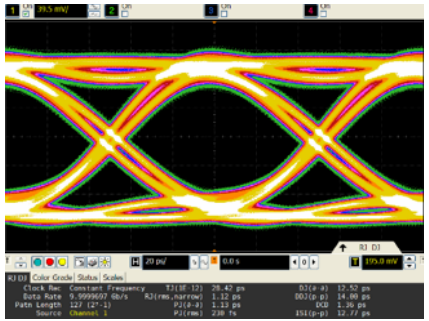
5Gb/s GBTIA
0.13μm CMOS (2009)



High-resolution Phase Shifter as part of GBT
In 0.13μm CMOS (2010)

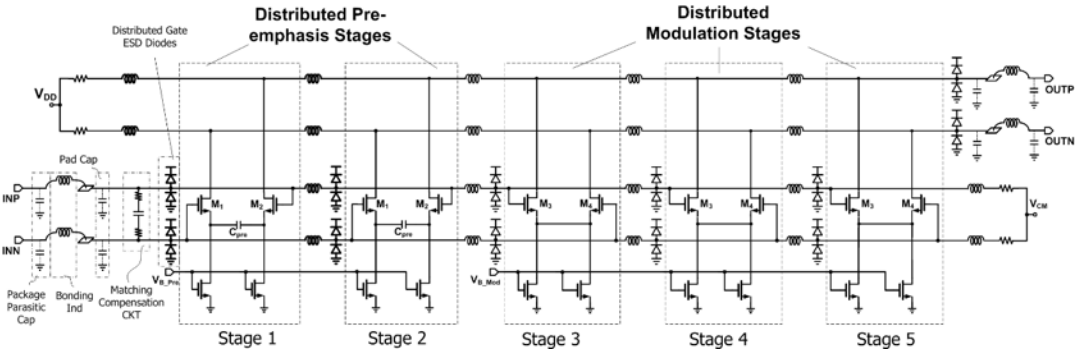
Low-Power 10 Gb/s Laser Driver (GBLD10) in 0.13 μm IBM CMOS





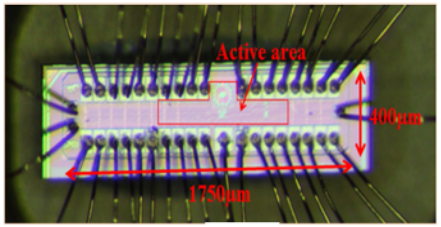
10Gb/s optical eye diagram

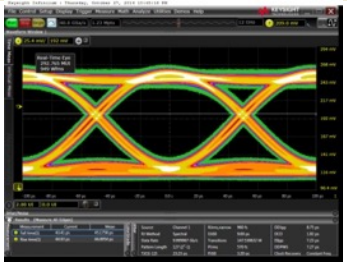
- Data rate: DC to 10 Gb/s
- Power consumption: 86 mW
- Jitter: < 20 ps
- Silicon area: 2mm x 2mm
- TID tolerance up to 500 Mrad
- Distributed amplifier technique for high speed operation



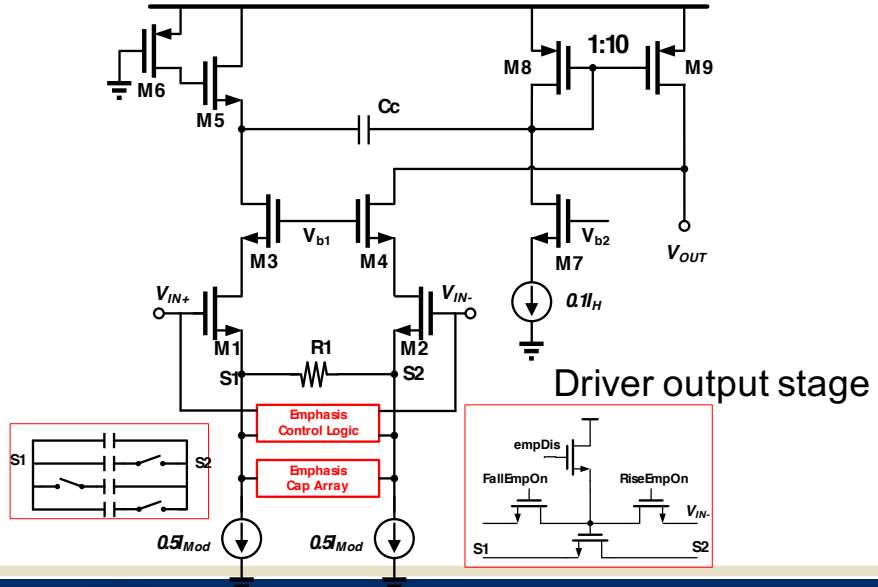
T. Zhang, P. Gui, P. Moreira, et. al, IEEE Trans. on VLSI Systems, Vol. 24, Iss. 7, 2016.

Compact Low-Power 10 Gb/s Laser Driver (LpGBLD10) in 65 nm TSMC CMOS





10Gb/s optical eye diagram

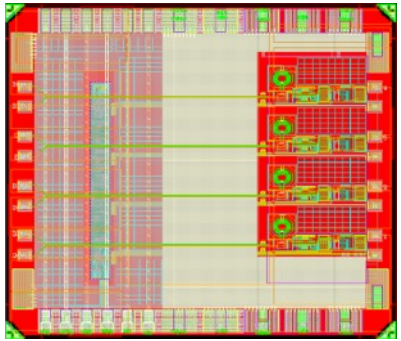


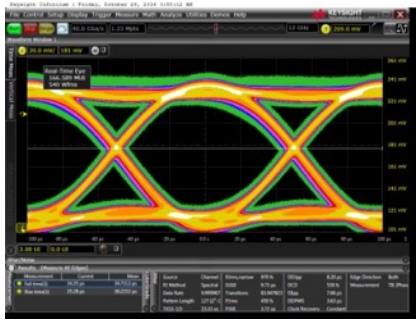
Driver output stage

- Data rate: DC to 10 Gb/s
- Power consumption: 31 mW
- Jitter: < 27 ps
- Silicon area: 1.75 mm × 0.4 mm
- Single-ended direct bonding to VCSEL
- TID tolerance up to 300 Mrad

T. Zhang, P. Gui, P. Moreira, et. al, Journal of Instrumentation 11(01):C01015-C01015, January 2016,

4x10 Gb/s Quad Laser Driver (LDQ10P) in 65 nm TSMC CMOS



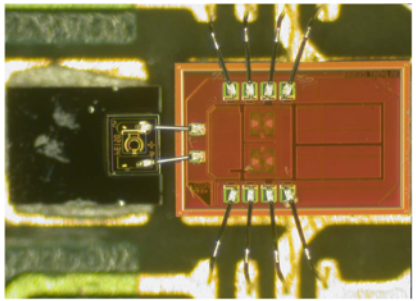


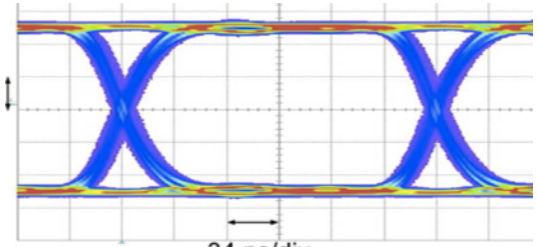
10Gb/s optical eye diagram

- 4 channels integrated with 250um pitch
- Data rate: 4 x10 Gb/s
- Crosstalk between channels minimum
- Power consumption: 130 mW for 4 channels
- Jitter: < 27 ps
- Silicon area: 1.7 mm × 1.9 mm
- TID tolerance up to 300 Mrad

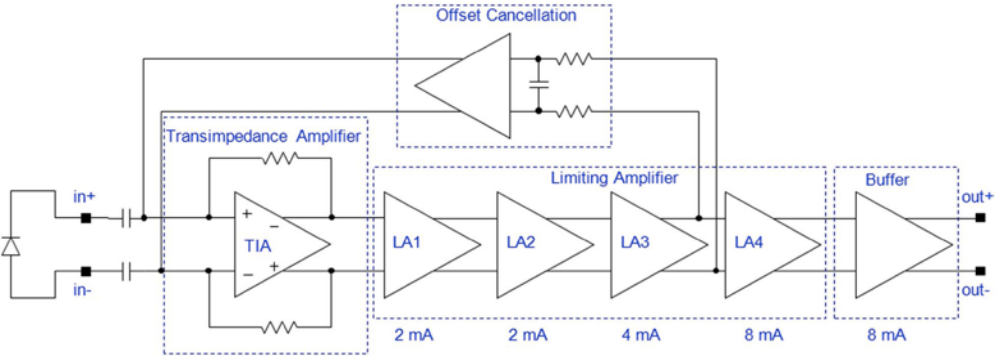
Z. Zeng P. Moreira, and P. Gui, et al.,
IEEE Trans. on Nuclear Science, Vol. 64, Iss. 4, 2017.

5 Gb/s GBTIA in 0.13 μm IBM CMOS





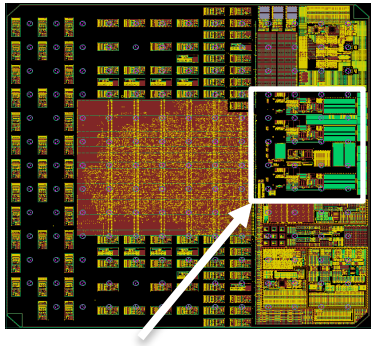
5 Gb/s optical eye diagram



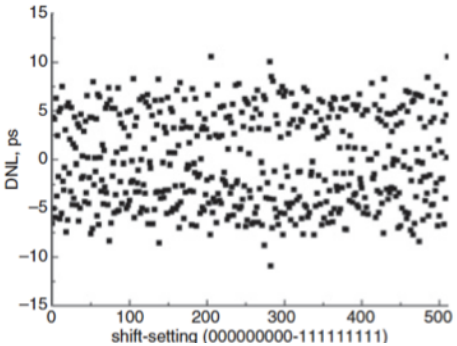
- Data rate: DC to 5 Gb/s
- Power consumption: 120 mW
- Sensitivity: -19dBm
- Transimpedance gain: > 20 kΩ
- Silicon area: 0.75 mm × 1.25 mm
- TID tolerance up to 200 Mrad
- In collaboration with CERN and CPPM

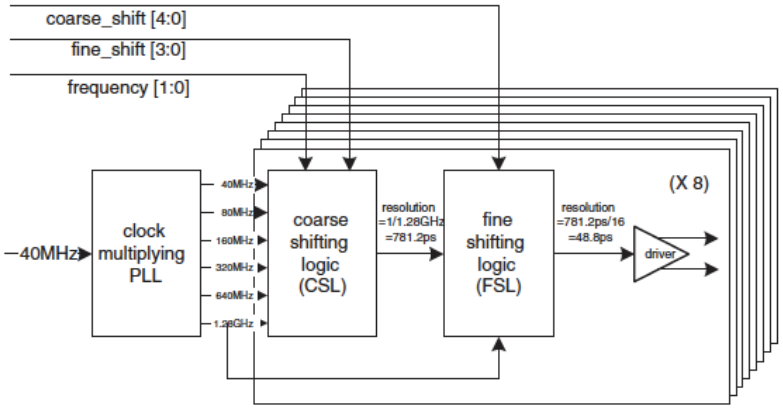
M. Menouni, P. Gui, and P. Moreira,
IEEE Trans. on Nuclear Science, Vol 60, Iss 4 2013

High-Resolution Clock Phase Shifter as Part of the GBT in 0.13 μm IBM CMOS



8-Channel Phase Shifter





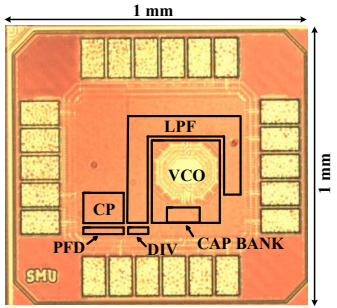
- Clock frequencies: 40, 80, 160 and 320 MHz
- 8 phase shifting channels
- Phase shifting resolution: < 50 ps
- Phase shifting range: 25 ns
- Power consumption: 4.8 mA/channel
- DNL: σ<4.7 ps, INL: σ <4.3 ps
- Silicon area: 0.07 mm^2 / channel
- TID tolerance up to 200 Mrad

G. Wu, P. Gui, P. Moreira,
IET Electronics Letters, Volume 49, Issue 10, pp642-644, Oct.2013.

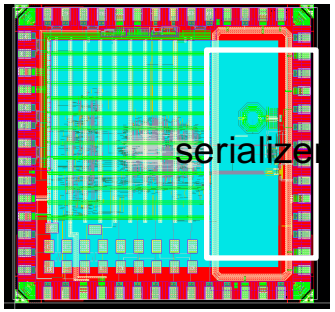
IC Designs in Collaborations with Fermilab

- Cold PLL, serializer and line driver as part of COLDATA chip for protoDune
  - PLL designed and demonstrated in room and cryogenic in 2015-2016
  - Serializer as part of COLDATA chip in 65nm submitted in May 2017
- Transistor characterizations under room and cryogenic (77K)
  - Both 0.13μ**m** and 65nm technologies
- Thermal analysis for the proto-VIPRAM00 chip
- URA (University Research Association) visiting scholars with Fermilab
- One MS thesis and 4 joint journal publications (IEEE TCAS-I 2017, IEEE TNS 2015, JINST 2015, and IEEE TDMR 2014)

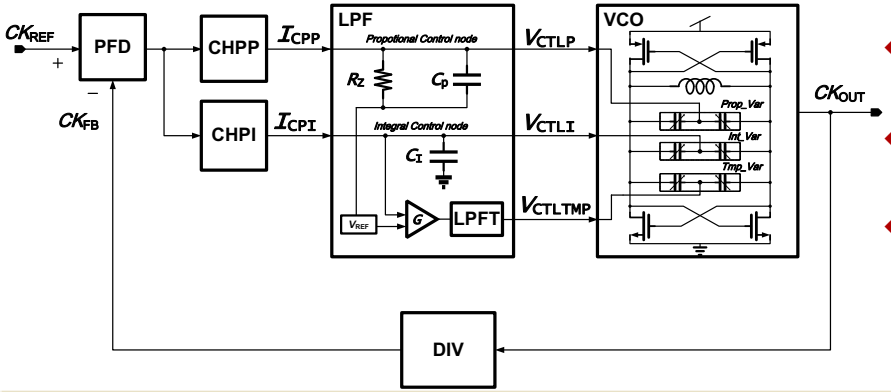
2.56 GHz PLL and 1.28 Gb/s Serializer as Part of COLDATA Operating at 77K for DUNE



PLL chip



COLDATA Prototype (CDP-1)

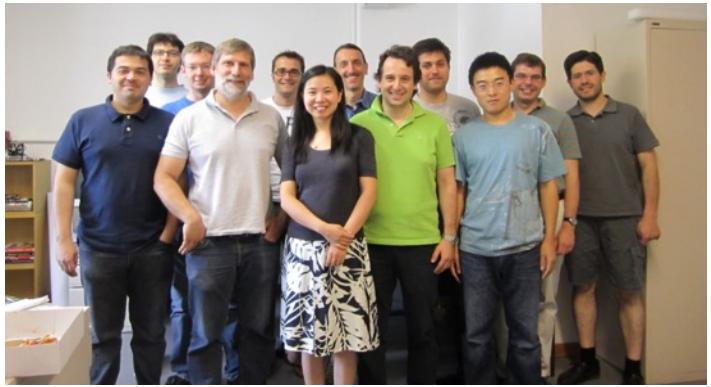


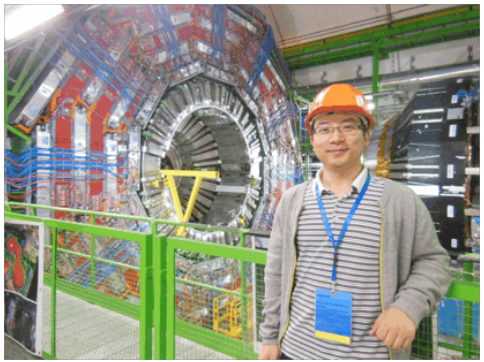
- Triple-path PLL for temperature compensation
- PLL working range: from 300K to 77K
- Frequency drift reduction by 99% over temperature change
- Power consumption of PLL: 8.5 mW
- 65nm TSMC CMOS; Silicon area: 0.08 mm^2
- Jitter rms: 0.89ps at 300K; 0.42ps at 77K
- CDP with serializer submitted in May 2017
- Funded by LBNE-DUNE project

T. Liu, P. Gui, et. al,
IEEE Tran. on Circuits and Systems I, 2017

Collaborations with CERN and Fermilab

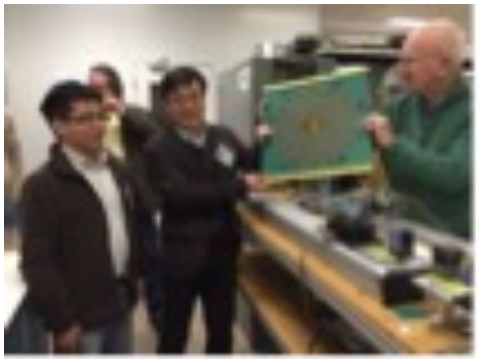
Dr. Gui visiting CERN, Geneva, Switzerland, 2011





Zhang visiting CERN, Geneva, 2013

Liu and Zhang visiting BNL, Long Island, 2015



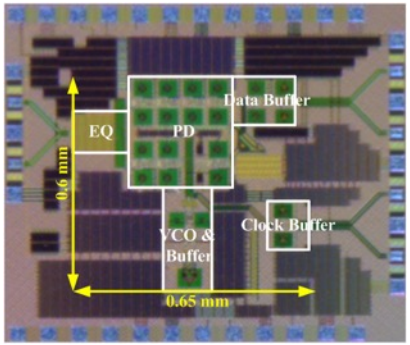
Wu and Liu visiting Fermilab, Chicago, 2015

On-going Research Projects

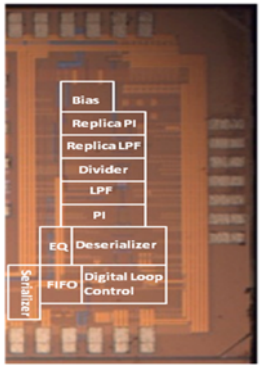
- ICs for HEP experiments
  - with CERN: GBT, LpGBT, Versatile Link
  - Fermilab: COLDATA, proto-VIPRAM00
- ICs for consumer electronics and communications
  - Optical and wireline communications
  - 5G wireless and automotive radar
- ICs for Biomedical applications

High-Speed Low-Power Clock Data Recovery (CDR) for Wireline Transceivers

- **25 Gb/s 0.6V Low-Power Clock-Data-Recovery (CDR) (IEEE RFIC2015)**
- **1-16 Gb/s any-data-rate phase-interpolator based CDR (IEEE Tran. On VLSI 2016)**
- **Design and fabricated in 65nm CMOS**



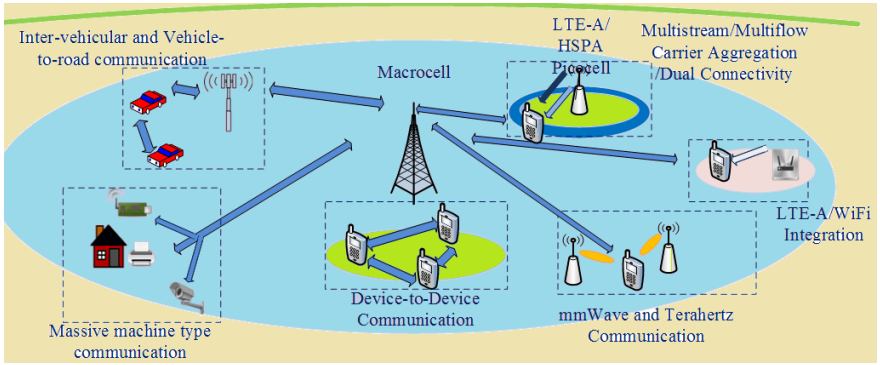
25 Gb/s 0.6V CDR



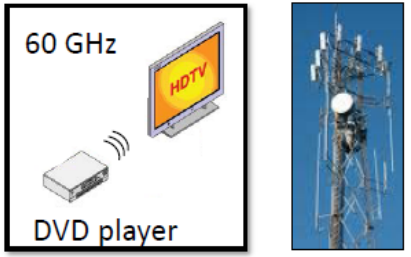
1-16Gb/s CDR

Sponsored by Semiconductor Research Corporation /Texas Instruments

mmWave (28/39 GHz, 60 -100GHz) IC for 5G Communications and Automotive RADAR an other Sensors

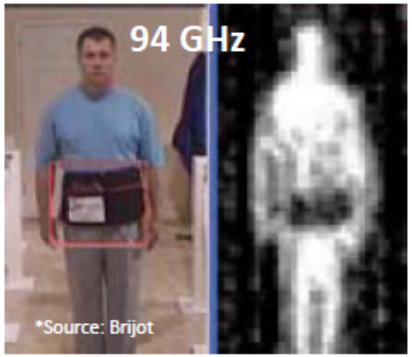


5G communications, 28/39Ghz

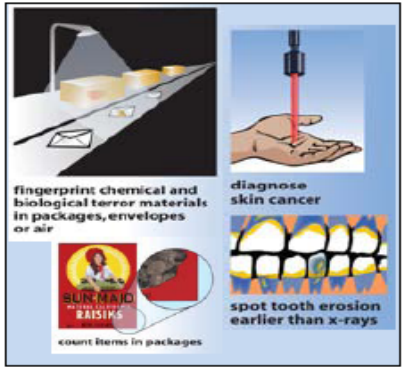


Data communications
(60GHz, 71-76/81-86GHz, 120GHz)

Automotive Radar
(24/77/79 GHz).



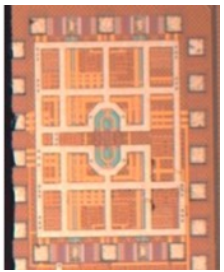
Imaging
(94GHz, >100GHz)



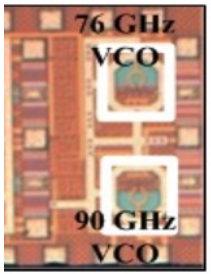
Sensors (>100GHz):
Spectroscopy, imaging…

mmWave ICs Developed by P. Gui's Group

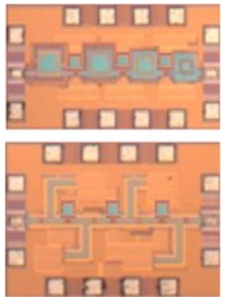
- **25GHz VCO and 25Gb/s CDR (IEEE RFIC2015)**
- **54GHz transformer-coupled QVCO (IEEE RFIC2014, IEEE T-MTT 2016)**
- **76GHz and 90GHz VCO (IEEE RFIC 2014, IEEE T-MTT 2016)**
- **54GHz LNAs (IEEE A-SSCC 2014, IEEE T-MTT 2016)**
- **76-86GHz Power amplifier (PA) (IEEE IMS2015, IEEE TCAS-II 2016)**
- **Passive CMOS mmWave Mixer (IEEE MWCL 2016)**
- **85-100 GHz CMOS circulator for full-duplex (IEEE RFIC 2017)**



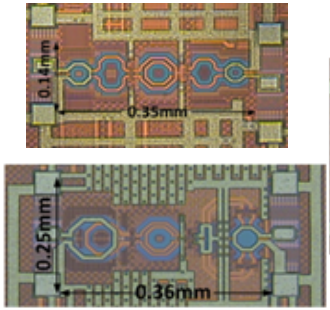
QVCO



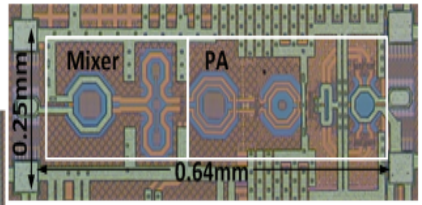
VCOs



LNAs



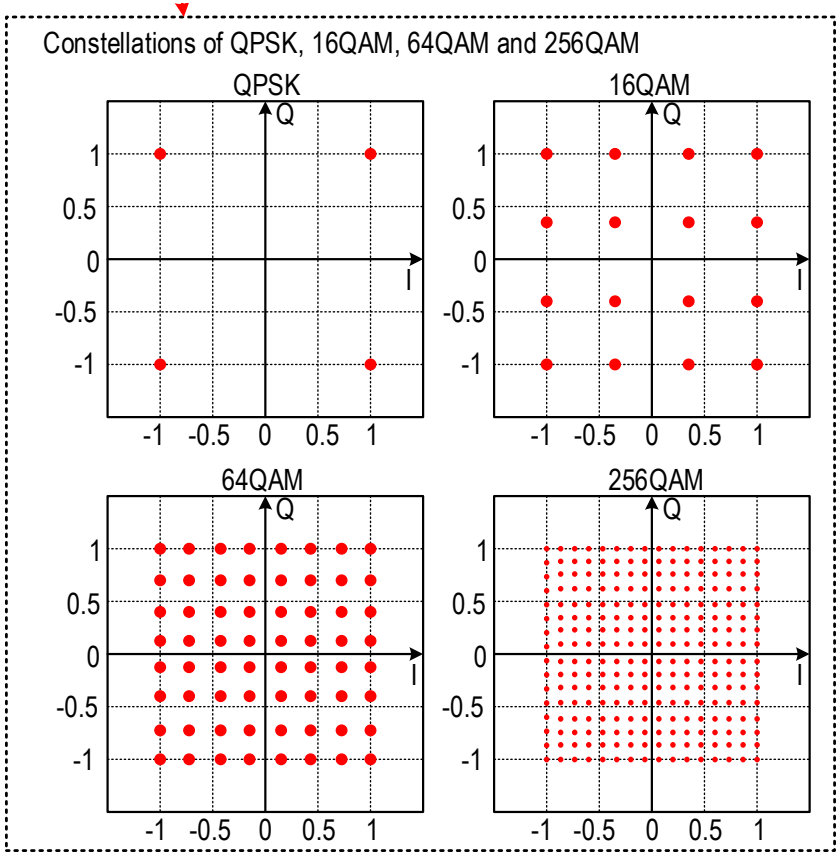
PAs

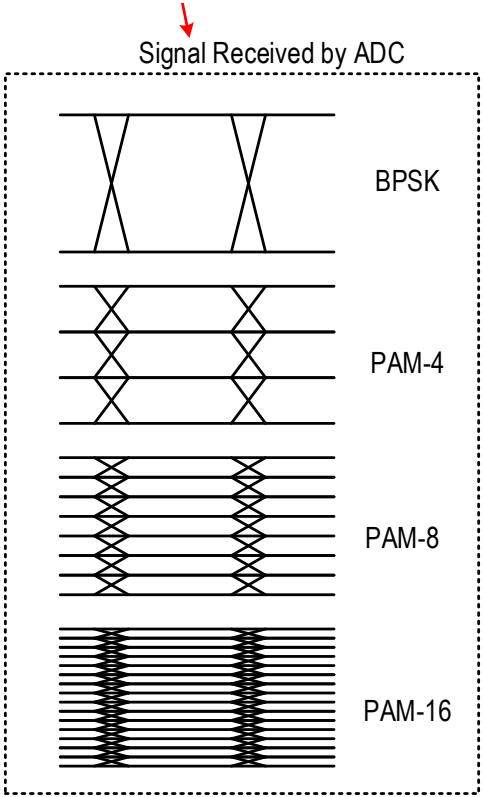


Transmitter (Mixer+PA)

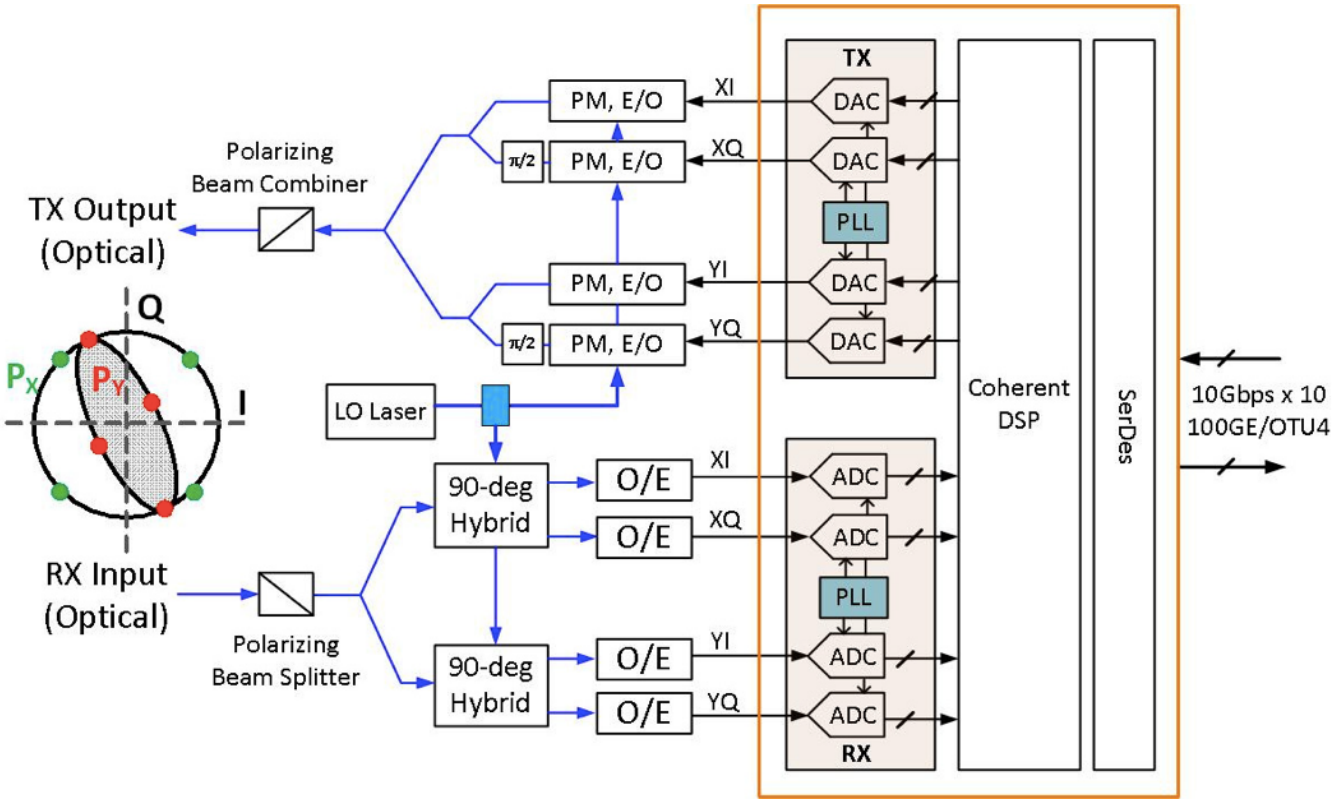
Sponsored by Texas Instruments

PAM or QAM-based High-Speed Data Links



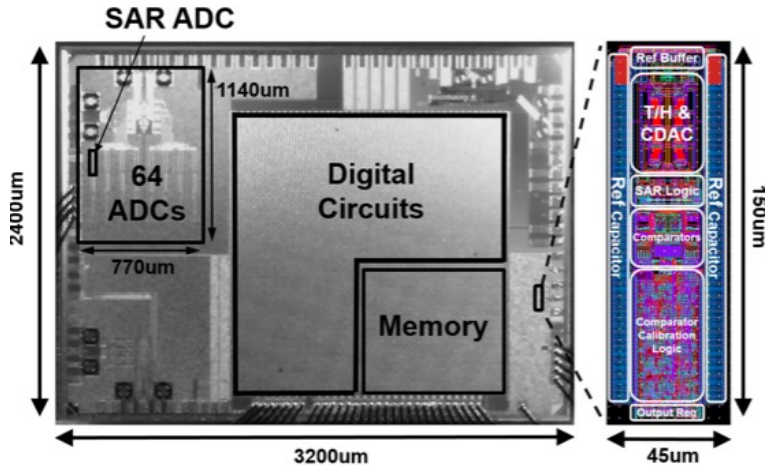


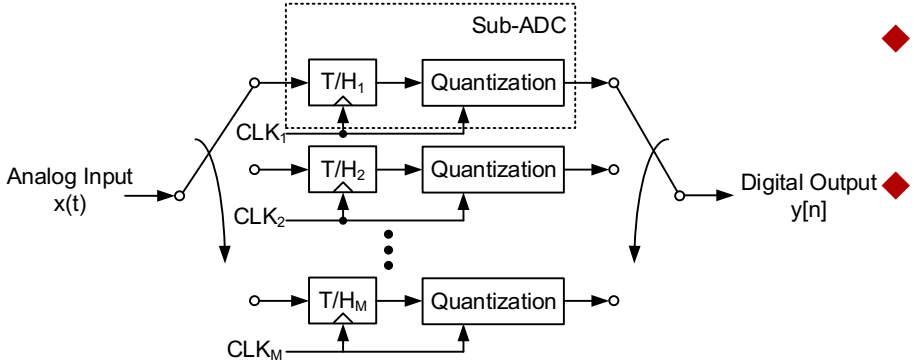
ADC/DAC Based Coherent Optical Transceiver for 100G/400G Optical Communications



[Image from Broadcom, ISSCC 2017]

56GS/s 8-bit ADC in 28nm CMOS Process





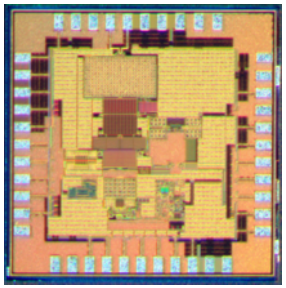
- 56 GS/s, 31GHz bandwidth
- 64 ADC time-interleaved channels each operating at 0.875GS/s
- Calibrations for inter-channel mismatches
- 6.4b ENOB @ 7GHz, 5.2b ENOB @ 27.1GHz
- Single channel SAR ADC: 1GS/s, 43.6db in SNDR, 6.96-bit, 3.2mW
- Project sponsored by DARPA SBIR between Menara Networks and SMU

G. Wang, P. Gui, et. al, IEEE ESSIRC 2017

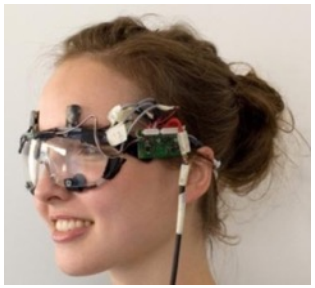
On-going Research Projects

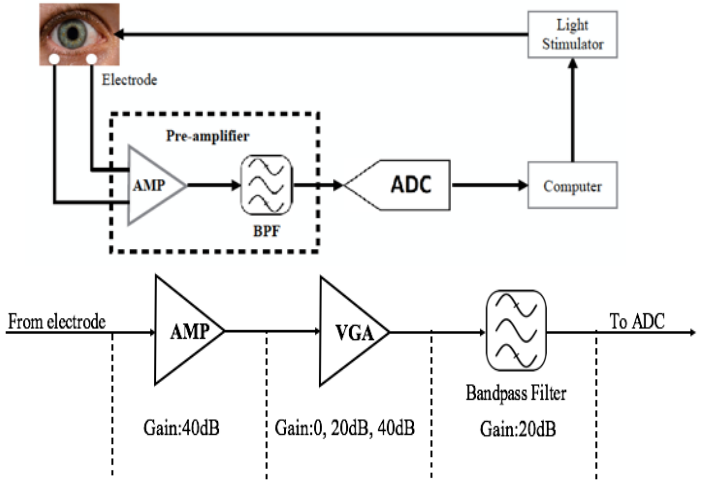
- ICs for HEP experiments
  - with CERN: GBT, LpGBT, Versatile Link
  - Fermilab: COLDATA, Proto-VIPRAM00
- ICs for consumer electronics and communications
  - Optical and wireline communications
  - 5G wireless and automotive radar
- ICs for Biomedical applications

Ultra-Low-Noise Amplifier IC for ERG Acquisition



Low-noise amplifier IC





- Objective: designing ultra-low-noise amplifier and front end circuit to detect very small Electroretinogram (ERG) signals for age-related macular degeneration diagnosis and treatment.
- Low-noise amplifier can detect very weak signals on the level of μV
- Reconfigurable Gain of 60-100dB
- IC fabricated in 0.18 μ**m** CMOS
- IC measurement underway
- Funded by Retina Foundation of Southwest

Summary

- We work on analog/mixed-signal IC design with HEP community as well as with semiconductor industry and other foundations
- Extensive design experiences have been gained on high-speed and low-power design and on using advanced technologies from 180nm down to 28nm CMOS
- Continuing the efforts and collaborations

Thank You for your attention!

Q & A