HEP Electronics Development at UT Austin

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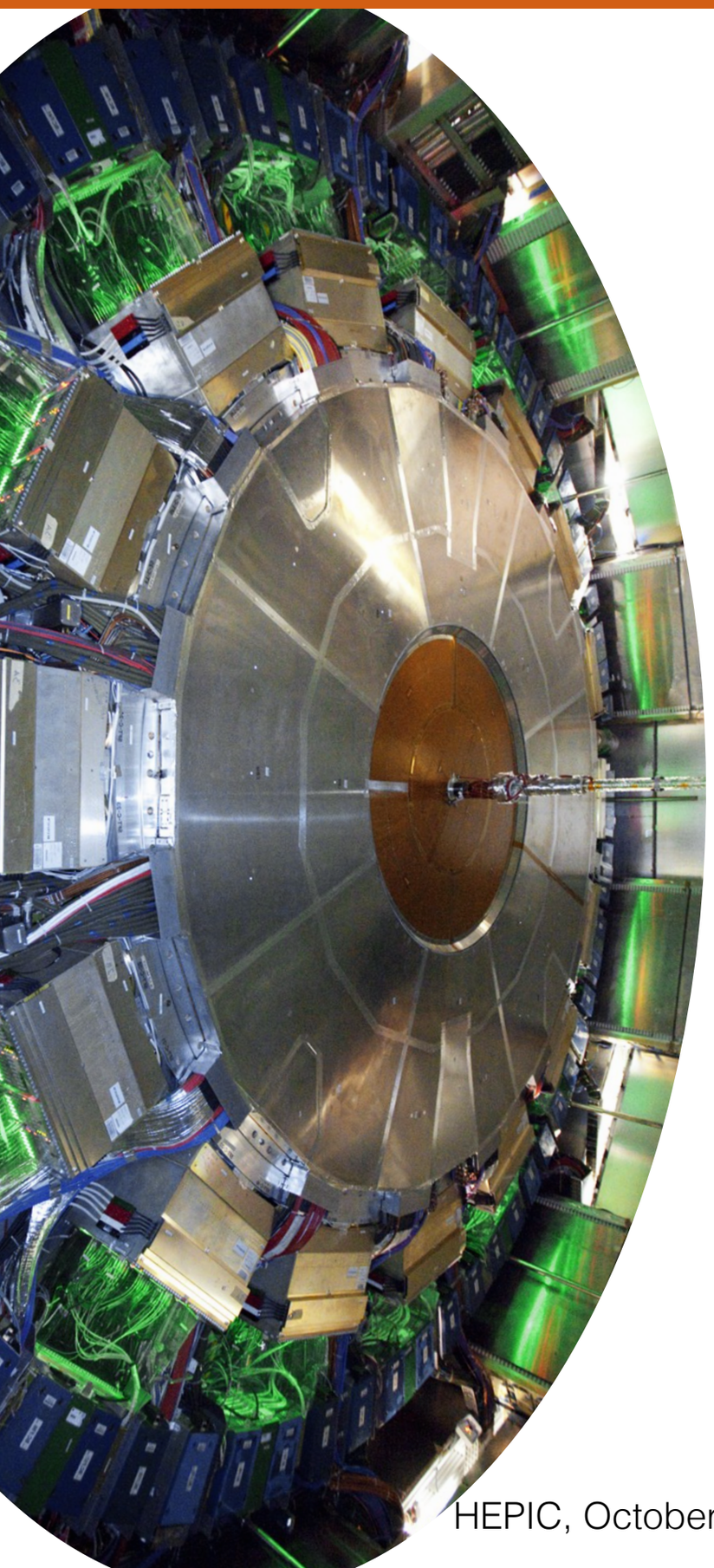
TEXAS
The University of Texas at Austin

HEPIC
SLAC, 4 October 2017

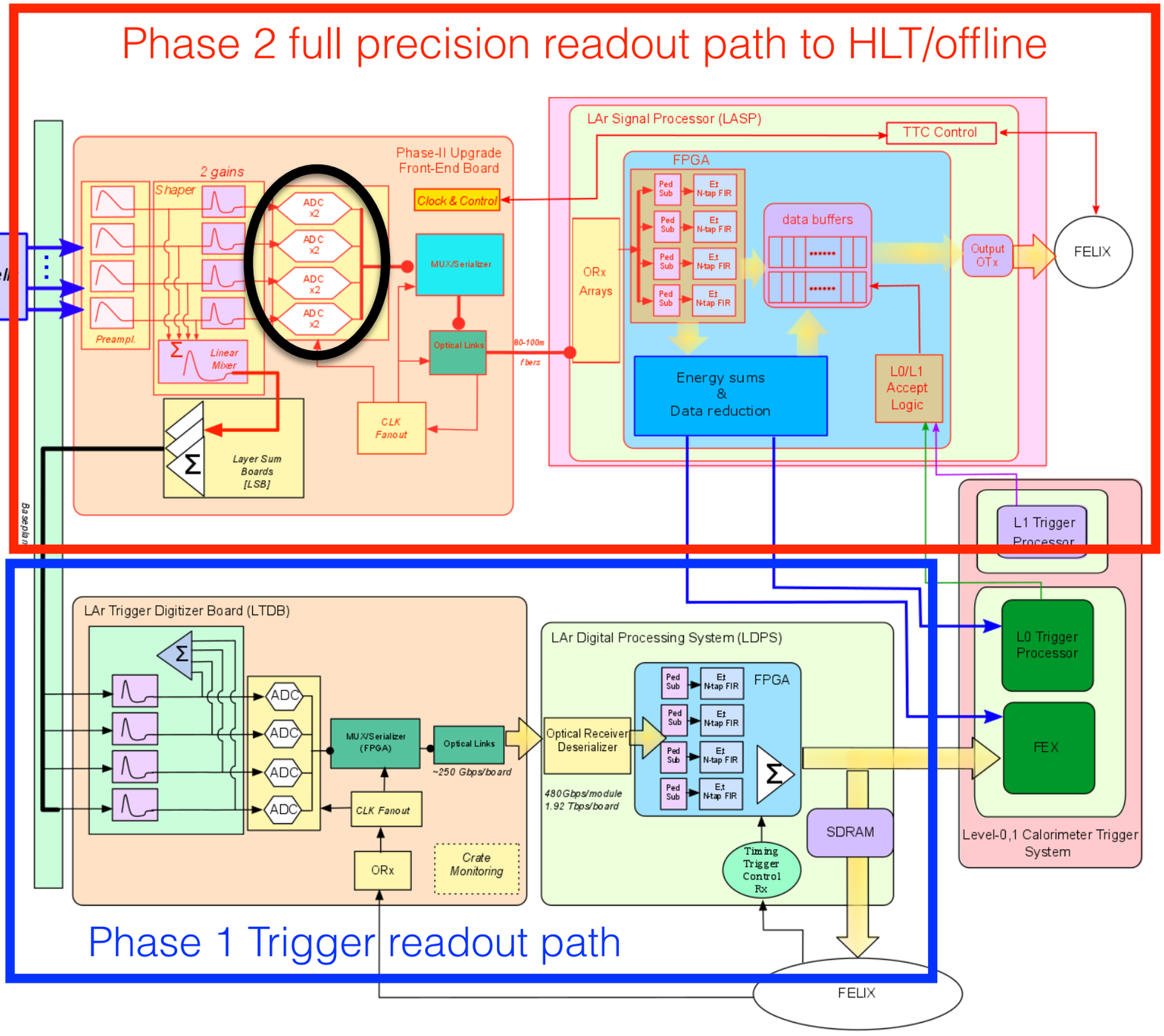
UT-Austin HEP Group



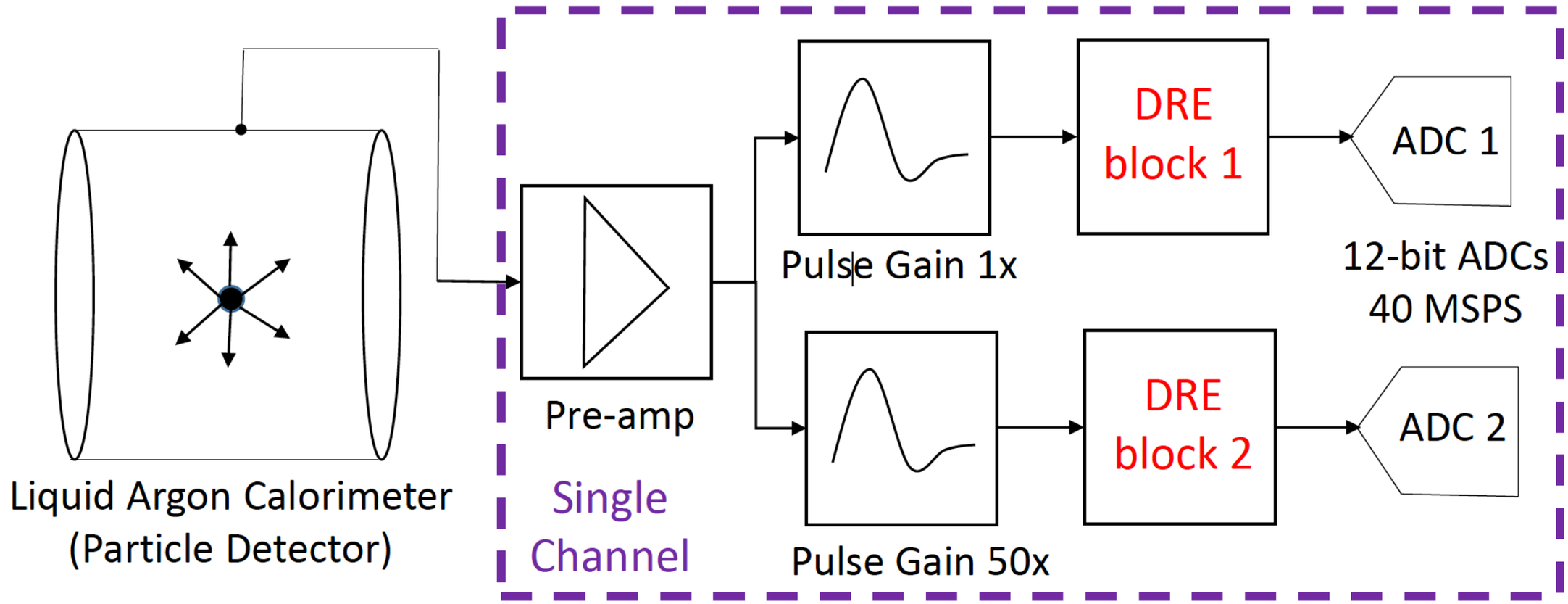
- **Neutrino group** established ~1995. Today focused on Muon *g*-2, No*v*a and DUNE experiments (photosensors, SiPMs)
- **ATLAS group** recently established (2012), TA joined in 2015.
  - Hardware focus is on **electronics for LAr readout at the HL-LHC**
  - Building collaborations and experience in electronics.
- HEP group benefits from subsided machine shop (9 FT machinists).

Electronics Requirements

- Cover **full energy range** from electronics noise level to highest possible energy deposited in a single cell: 50 MeV to ~3 TeV.
- **Linearity** of 0.1% up to ~10% of the dynamic range.
- **Low electronics noise**, below intrinsic calorimeter resolution:
  - effectively ~11-bit precision at high energy
  - equivalent precision in analog signal shaping
- **All data sent off-detector**:
  - 1.3 Gbps per channel if we send two gains
  - ~180 Gbps per front-end board
  - ~275 Tbps for the full LAr calorimeter.



DRE + ADC Design - 65 nm TSMC

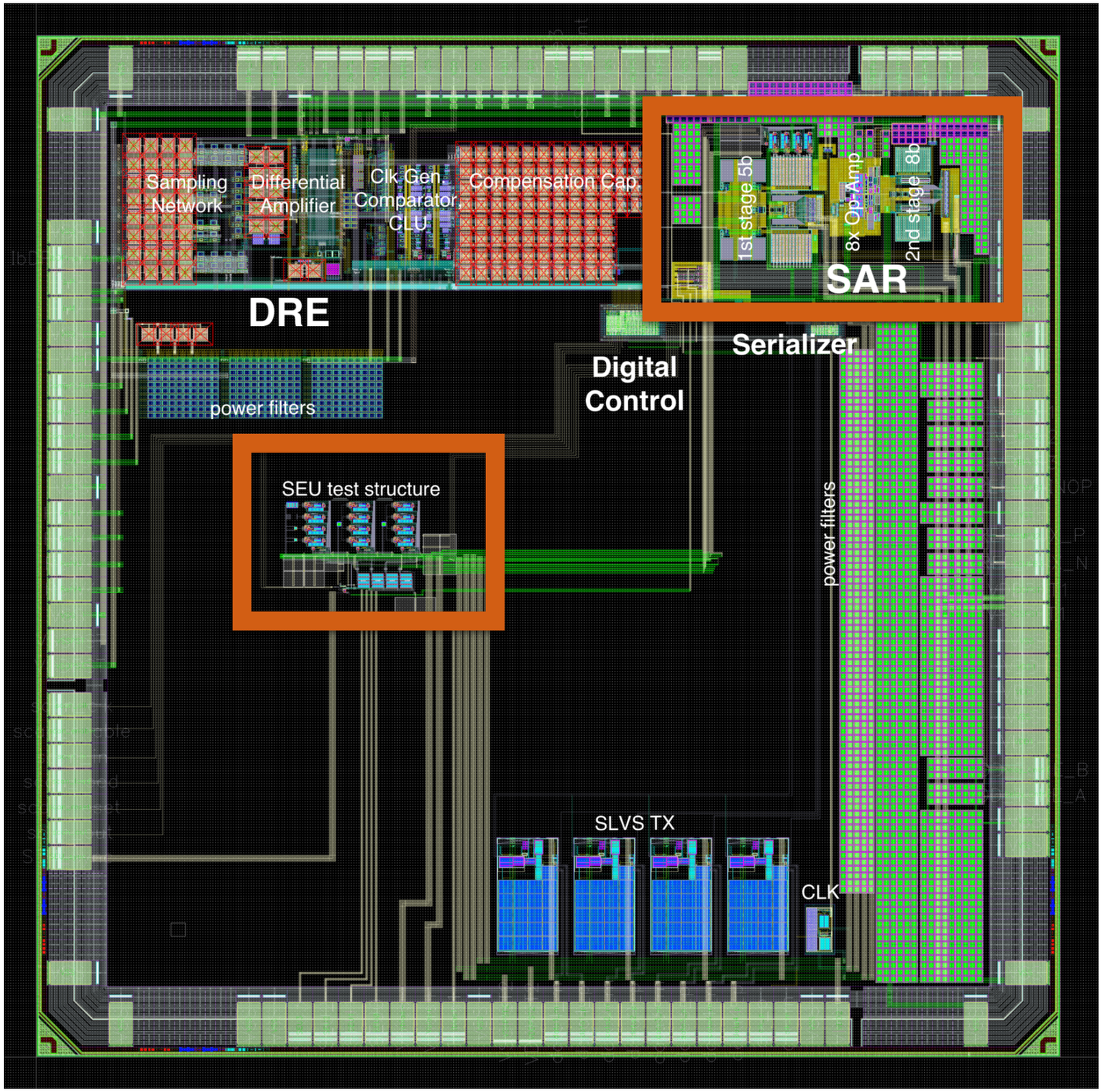


- ADC specification :
  - 14-bit dynamic range
  - 11-bit resolution
  - 40 MSPS
  - Low power, rad hard

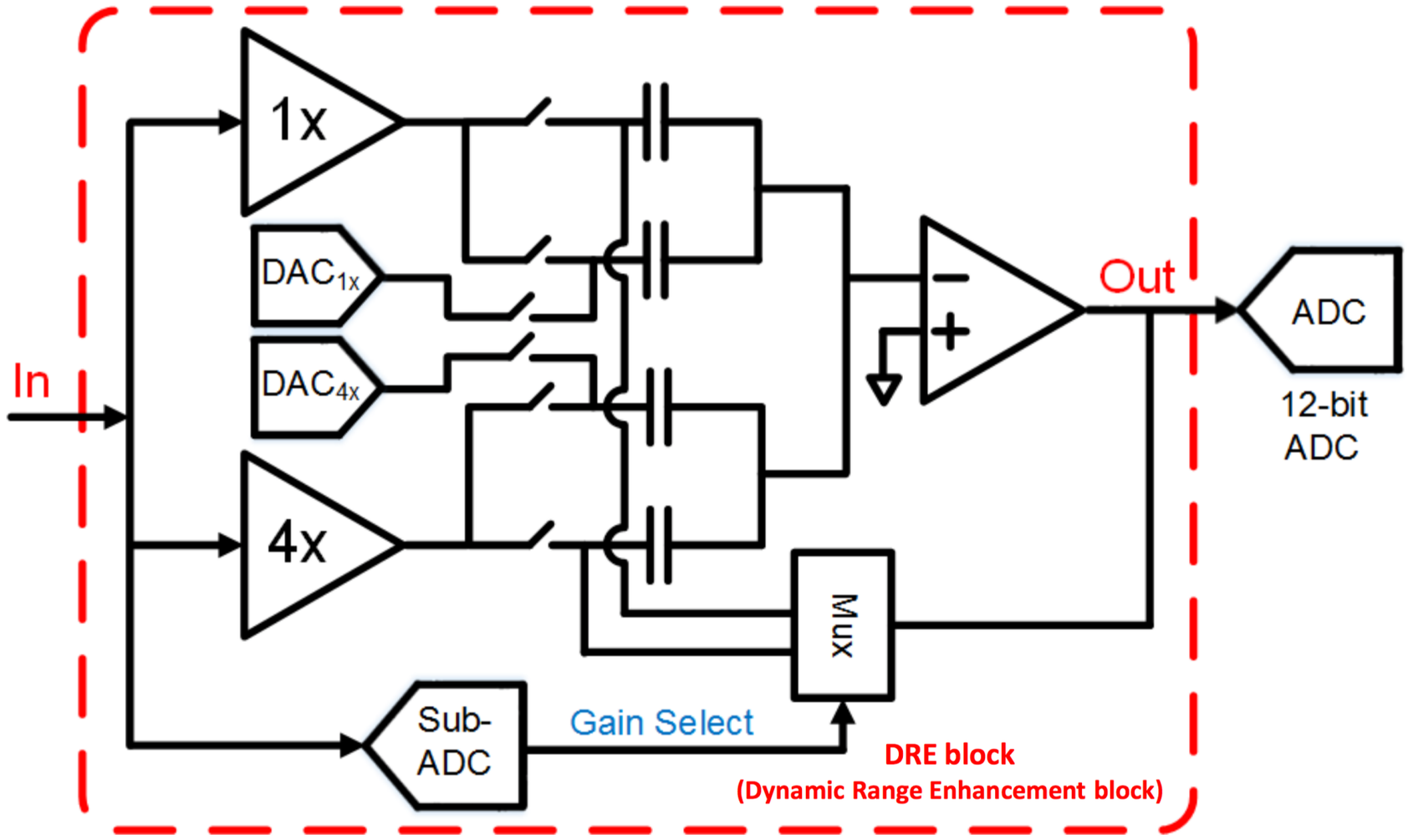
- Two blocks :
  - Dynamic Range Enhancer (DRE) with internal 4x gain to reach 14-bits
  - 12-bit Pipeline SAR ADC.

DRE + ADC Design - “COLUTA” Chip

- Collaboration between **UT-Austin** Physics and ECE departments, and **Columbia University** Physics (Nevis) and EE departments.
- Columbia is developing the DRE and provides chip services
- UT-Austin is developing the rad-hard SAR ADC.



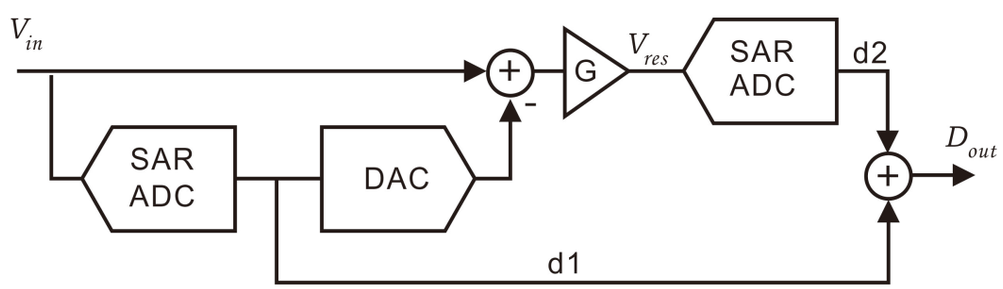
DRE Concept - Columbia University



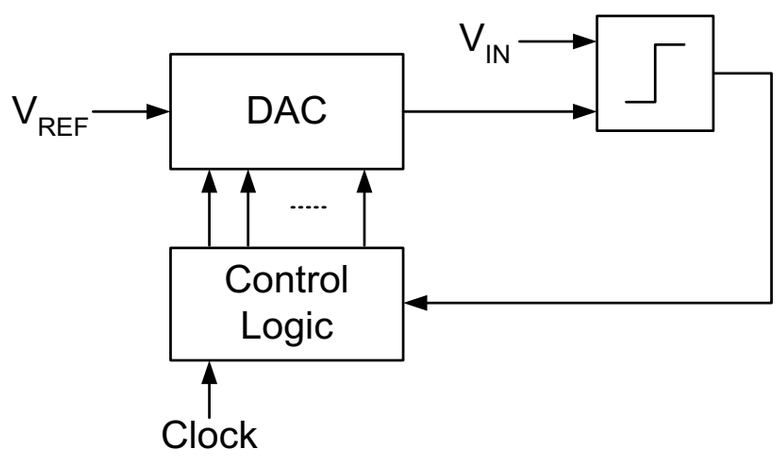
- Need to resolve 2 bits: Internal gain selection (g=4) with 12-bit accurate output for sampling.
- Exact gain values can be determined through inter-calibration (similar to inter-stage calibration).

Pipeline-SAR technique

- Pipelined SAR ADC:
  - Smaller area
  - More design work



- SAR ADC:
  - Larger area
  - Simpler design



- Design for:

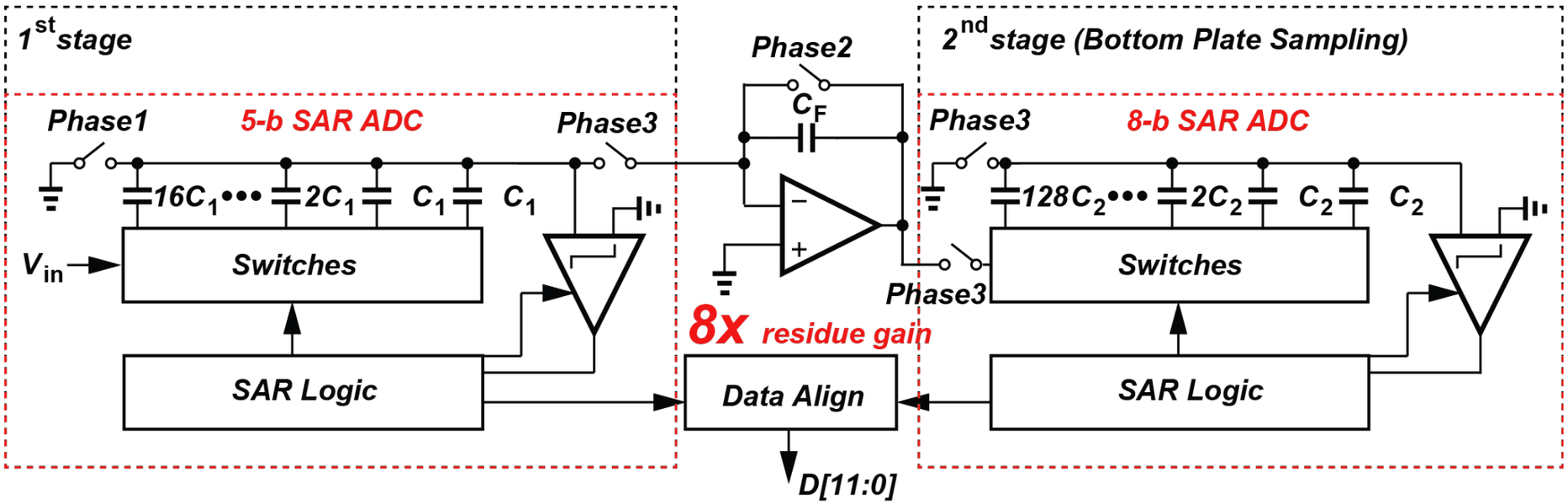
Technology:	TSMC 65 nm
Precision:	12 bit
ENOB:	**>11.2**
Sampling frequency:	**40 MHz**
Power :	**15-20 mW**
Supply voltage:	1.2 V
Input common mode:	0.6 V
Input voltage:	differential +-0.5 V, full scale 2 V
Reference voltage:	+-1V with common mode of 0.6V
Digital control:	1.2V CMOS
PLL:	On-chip, up to 160/320 MHz

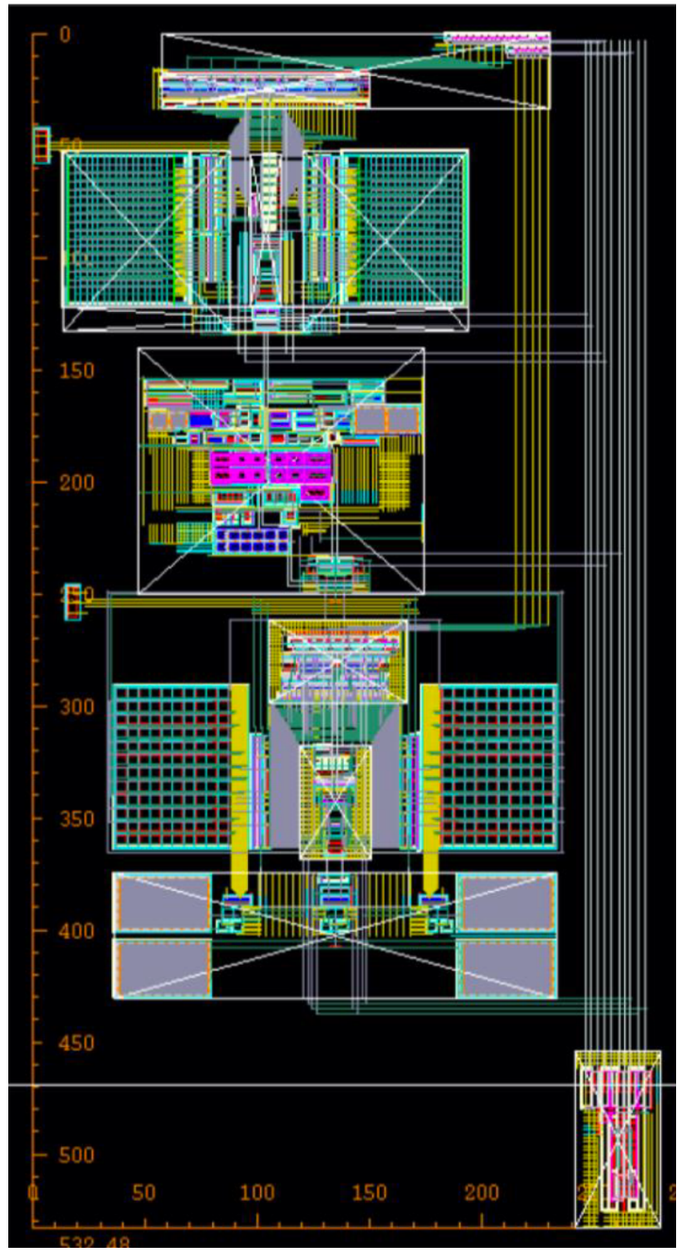
Y. Lim and M. P. Flynn, "A 1 mW 71.5 dB SNDR 50 MS/S 13b fully differential ring-amplifier-based SAR-assisted pipeline ADC," ***in Proc. IEEE ISSCC. Dig. Tech. Papers***, Feb. 2015, pp. 1–3.

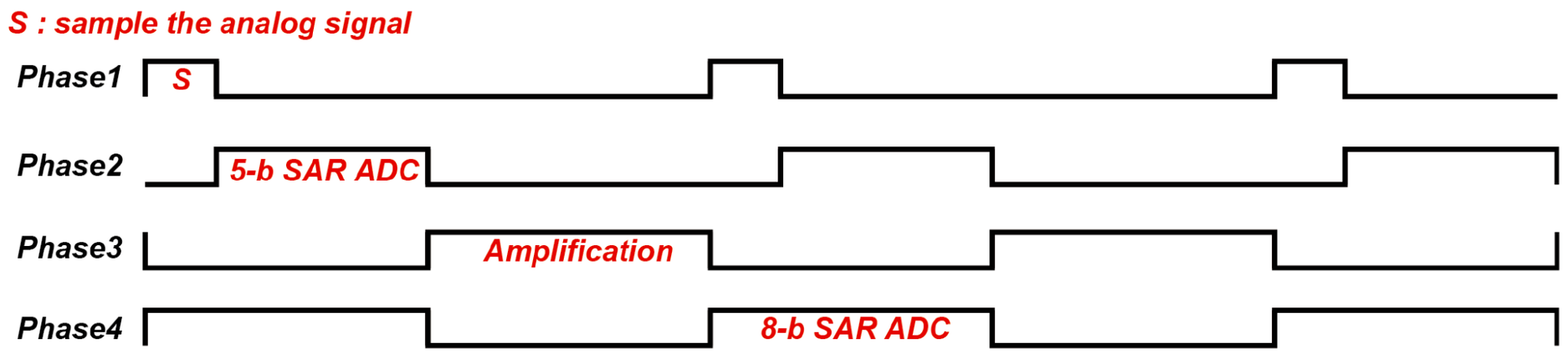
Wenjuan Guo, and Nan Sun , "A 12b-ENOB 61µW noise-shaping SAR ADC with a passive integrator ," ***ESSCIRC,*** pp. 405-408, Oct. 2016.

Pipeline-SAR

- 40 MHz, two step design: 5-bit first stage + 8-bit second stage with 1-bit interstage redundancy.

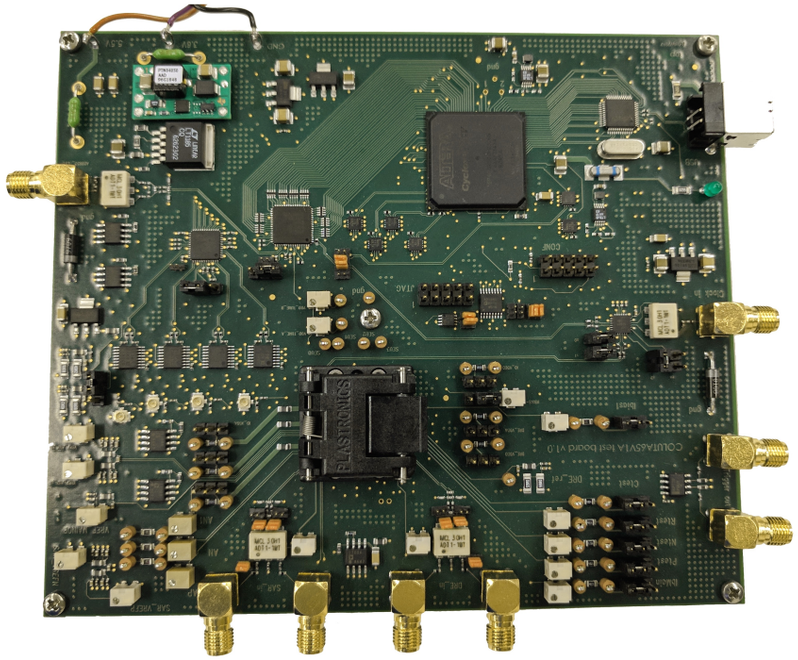




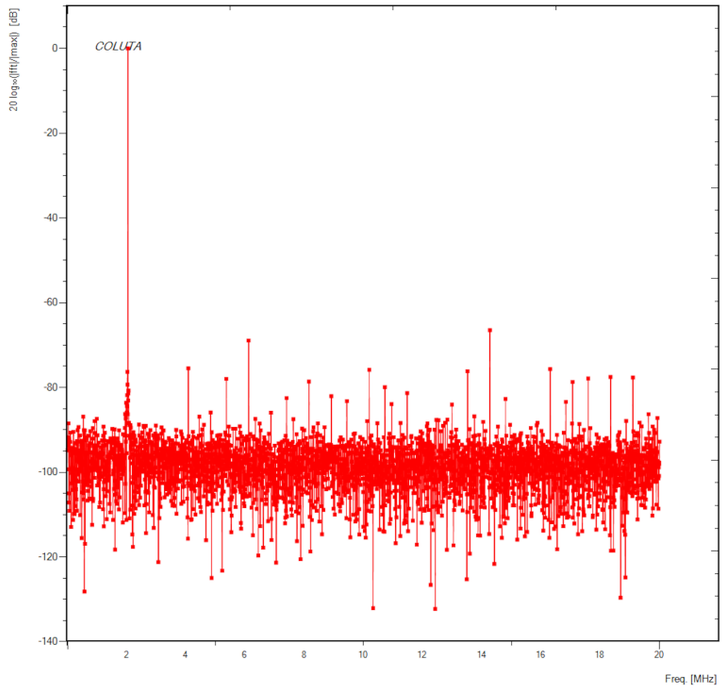


Submission and Packaging

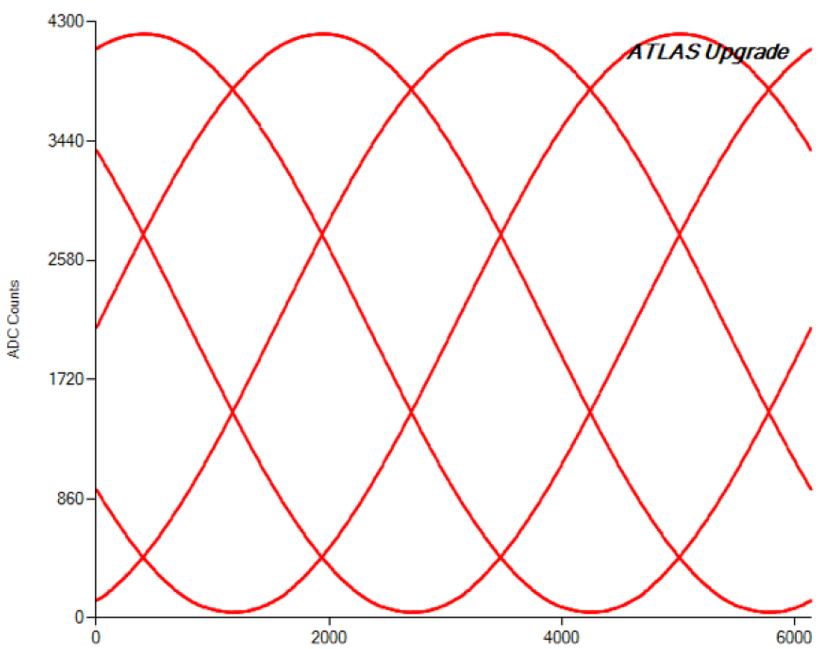
- Post-layout, whole chip simulation gives performance ~12-bit precise.
- Submitted (CERN-IMEC) May 2017, **Packaged September 2017**.
- Testing of COLUTA65v1 currently at Nevis and Austin in both EE and Physics labs.



First data from DRE

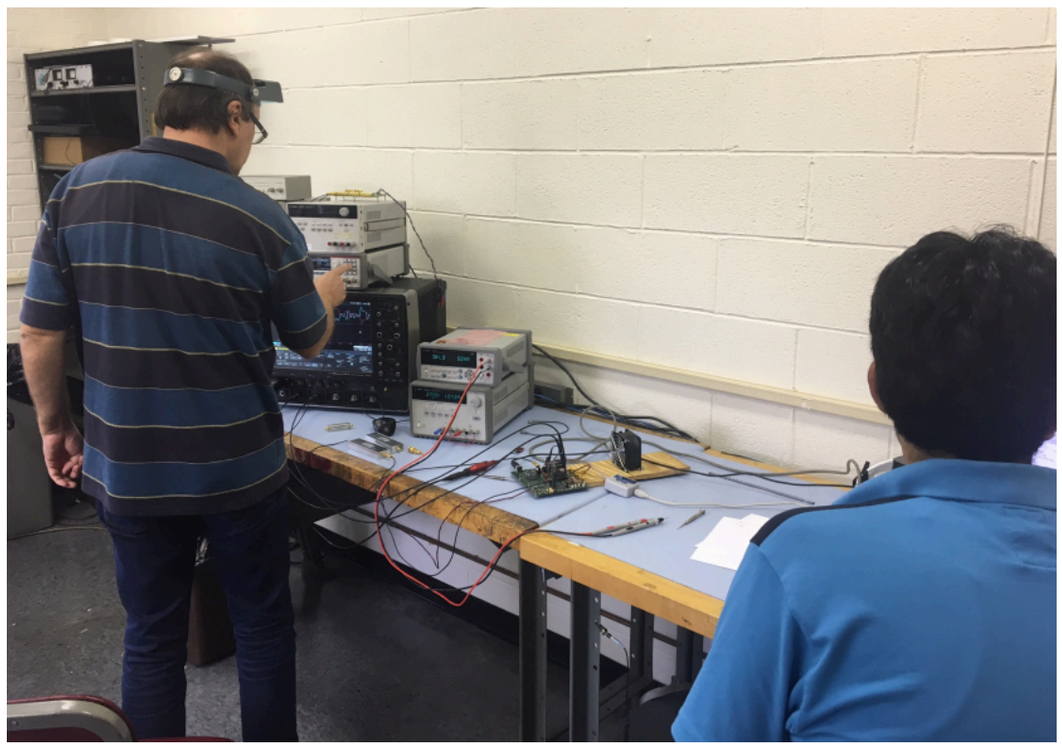


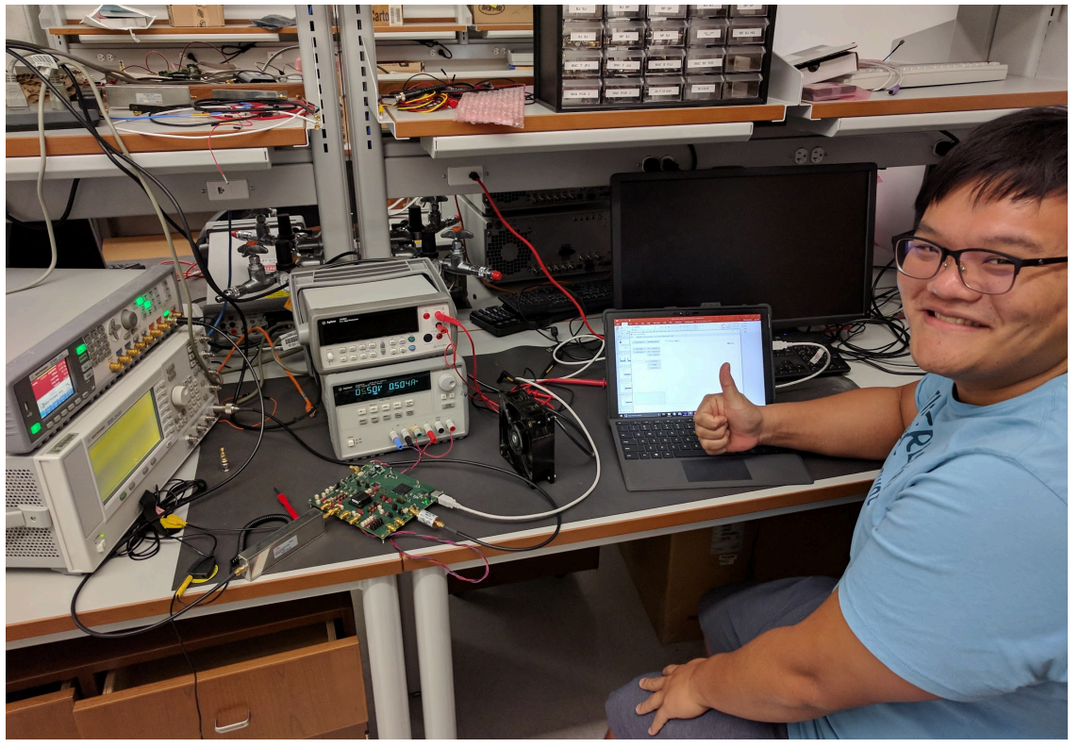
First data from SAR

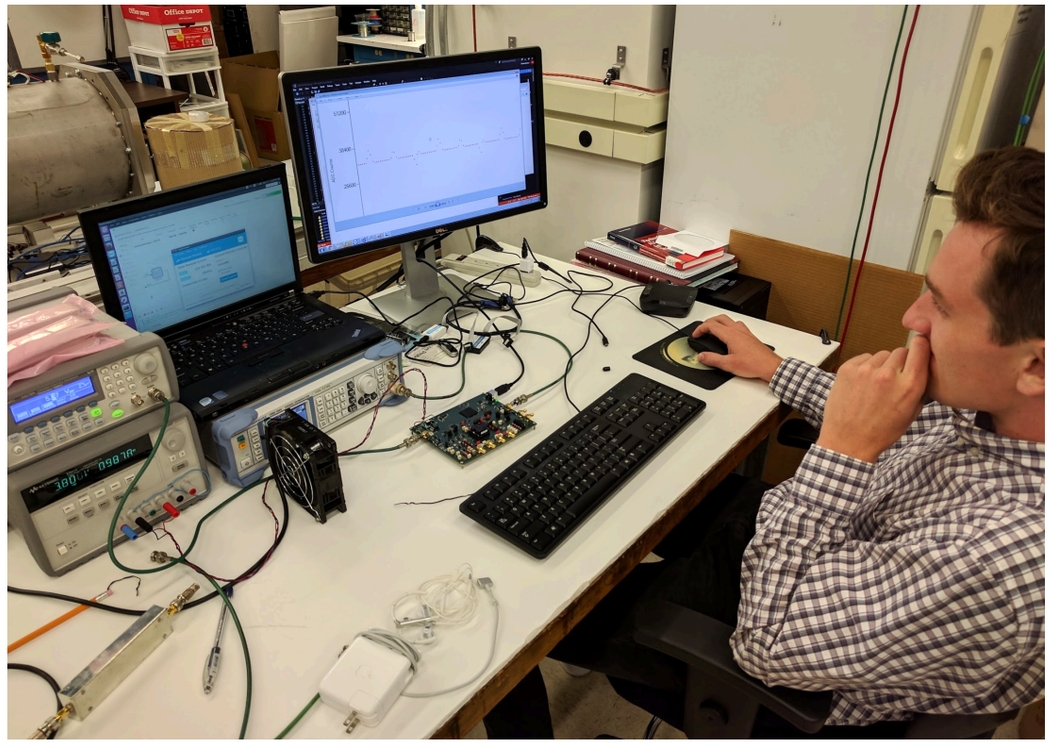


Testing at UT-Austin and Columbia

- At Austin we're grow testing facility preparing for radiation testing (next year) and for bulk testing of production chips (after 2020).







C-K. Hsu (bottom left) and C. Burton (bottom right) J. Ban and S. Kalani (top)

Plans and Collaboration

- **Planning annual cycle of submissions until production for HL-LHC.**
  - ➡ Collaborate on **design** -
    - EE grad students at UT Austin and Columbia design primary blocks. Share all design files, *video meetings, Skype calls/chats* to coordinate.
      - Grad student advisors (**Sun** and **Kinget**) provide significant expertise.
    - Simulation done at both UT-Austin and Columbia
    - Integration with chip services (clock, PLL, I/O (CERN), etc) done at Nevis by senior engineer, project files hosted there.
    - Submission to IMEC through CERN.
  - ➡ Collaborate on **testing** -
    - PCB + firmware for testing designed by engineers at Nevis (and eventually at UT-Austin). *Travel for work side-by-side* in initial testing.
    - Physics grad students and postdocs at UT-Austin and Columbia write software for testing, work with EE students and engineers in debugging, measurements, radiation testing.
  - ➡ Repeat!

Summary

★ **UT-Austin is a new group in HEP IC development.**

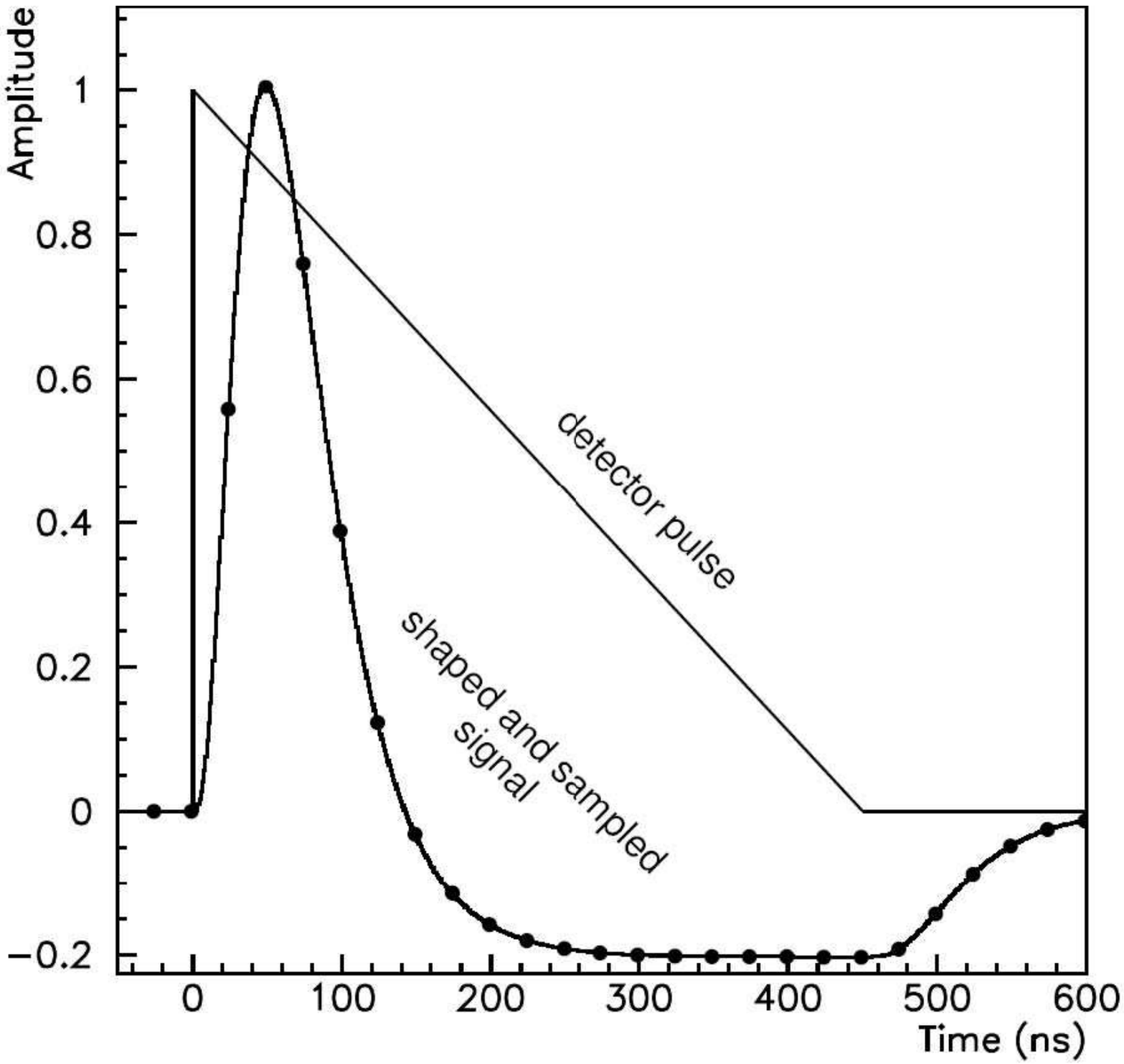
- Developing rad-hard SAR ADC for ATLAS LAr electronics readout.

1. As a new group we need collaborators. We work with a **local EE** group and **Columbia University/Nevis**. These collaborations are critical for us.
2. As a new group we also have excited students and postdocs with new ideas:

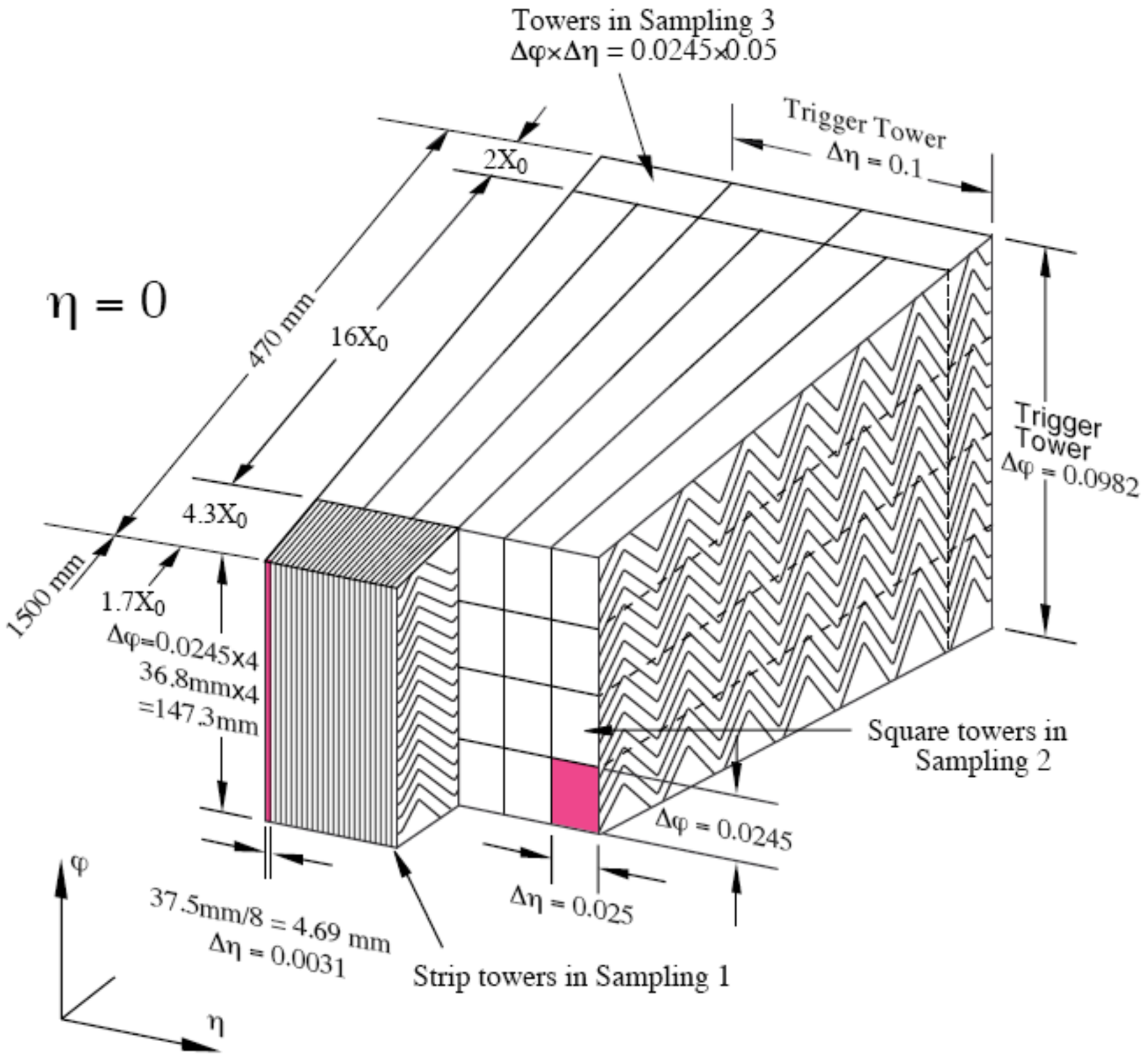
- Testing separate “Research chip” with new SAR design
- Testing on-chip SEU measurement and detection
- Planning for large-scale testing.
- Finding collaborations aligned with HEP group activities at UT-Austin

Extra Slides

LAr Pulse


Amplitude
1
0.8
0.6
0.4
0.2
0
−0.2
0
100
200
300
400
500
600
Time (ns)
detector pulse
shaped and sampled signal

Detector Segmentation

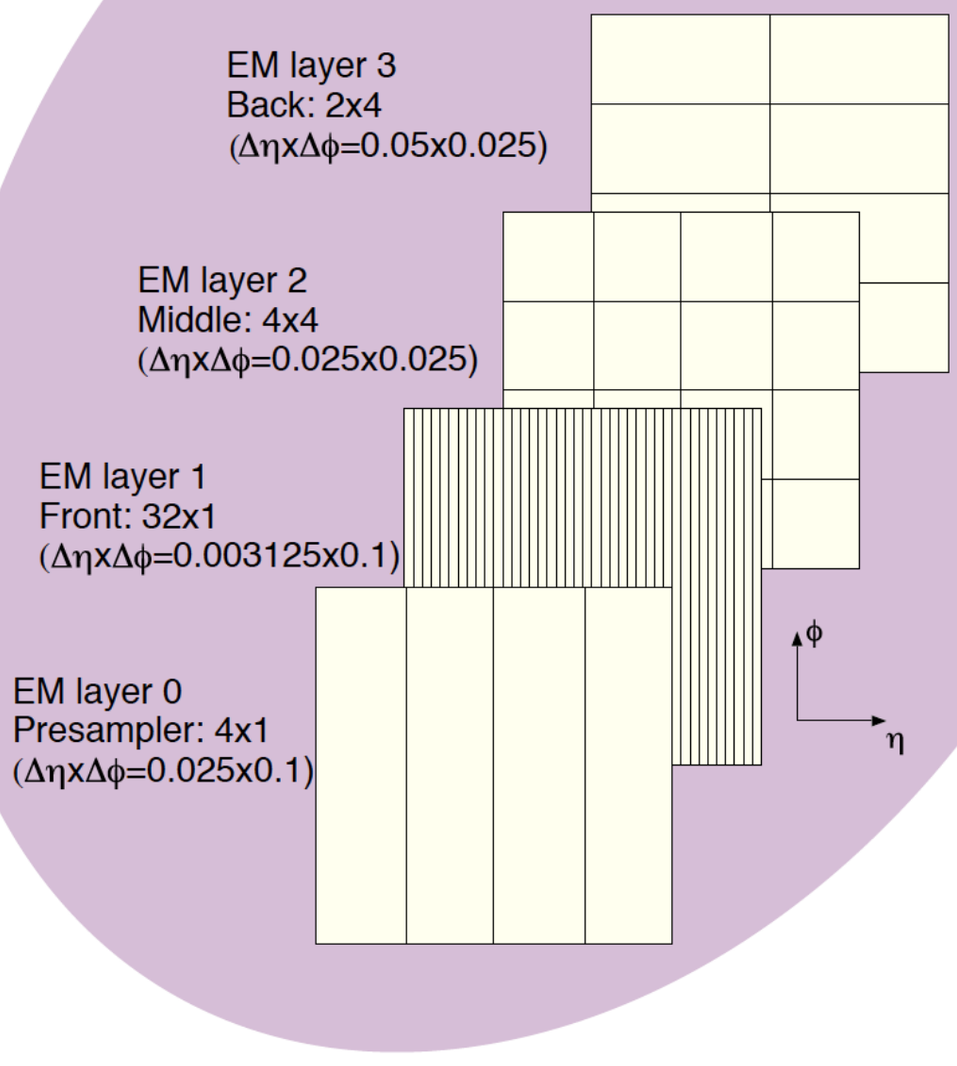


Phase 1 Super cells

Existing System

Level-1 Trigger Granularity (Trigger Towers)

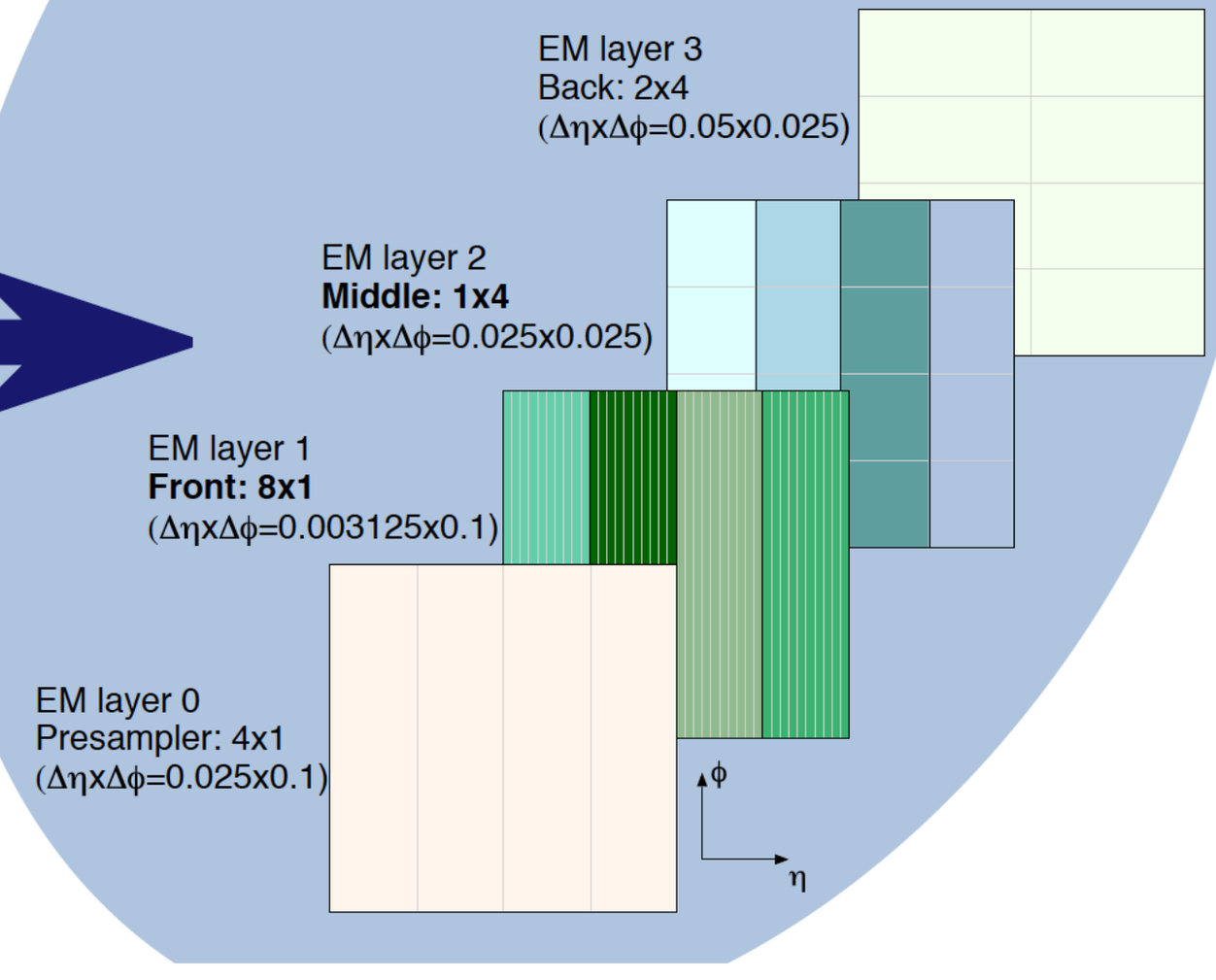
60 cells per Trigger Tower; all layers summed



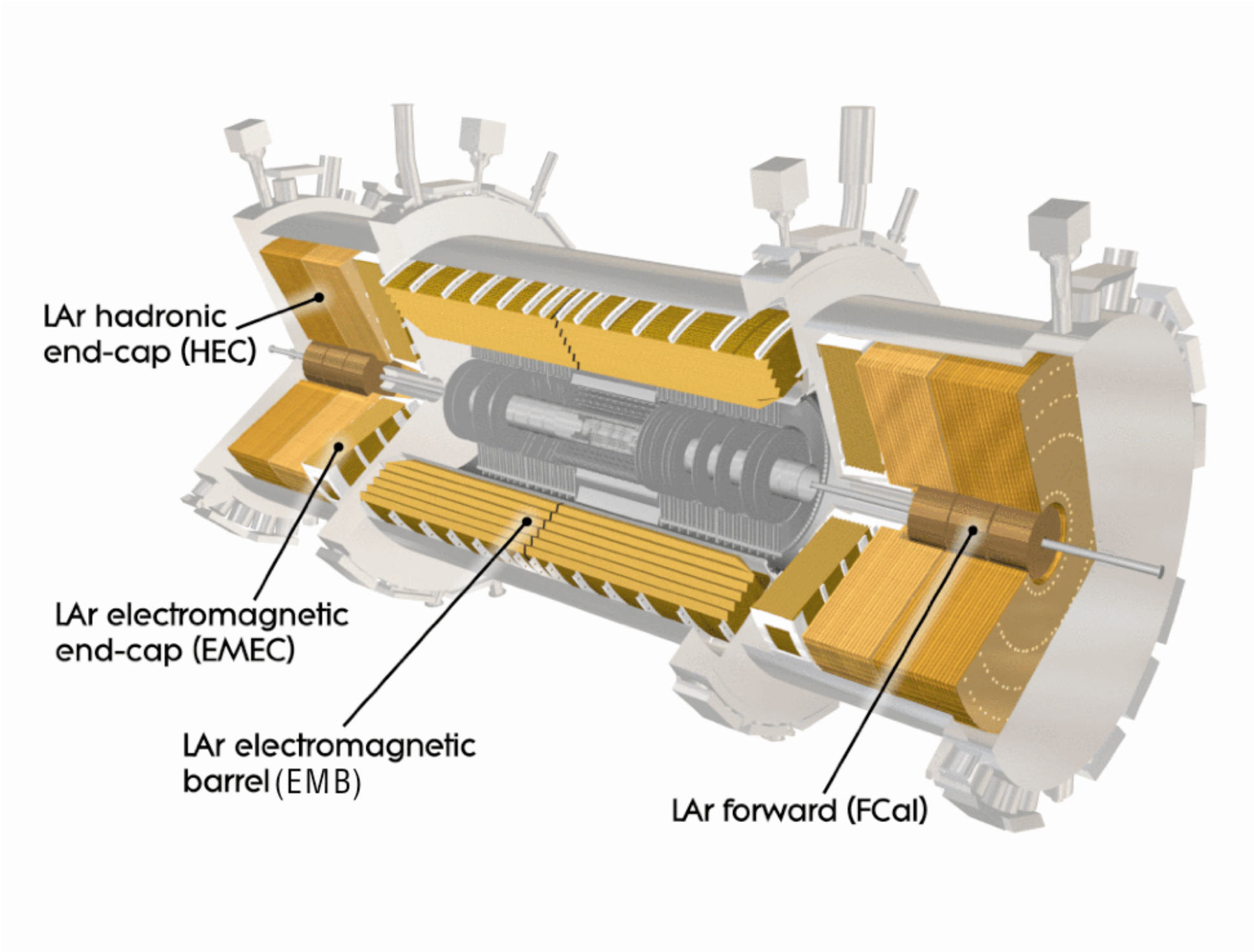
Phase-I Upgrade

Level-1 Trigger Granularity (Super Cells)

10 Super Cells per Trigger Tower



LAr Detector



Front-end crate location