Collaborating between Institutes: the CERN experience

Michael Campbell

Section Leader ESE-ME

4th October 2017

Context

- Many 10's of institutes contribute with ASIC design to the LHC and other CERN experiments
- The CERN Microelectronics Section seeks to propose common technology platforms with supported PDK's and tools as well as foundry access at favourable rates for prototyping and production
- The aim is also to allow access to wafers (sometimes needed for post processing, bumping, TSV, etc)
- Another key consideration is understanding the behaviour of supported CMOS processes in a high radiation environment
- These requirements raise a number of organisational issues

Outline

- Overview of activities in the CERN ME Section
- Common technology platforms
  - Technology support (PDK and Tools)
  - Foundry access
  - Radiation hardness studies
- Some examples of projects
  - CMS tracker upgrade
  - RD53: ATLAS and CMS pixel upgrade
  - ALPIDE and MALTA
- Conclusions

Activities in the ME Section

- Common projects (useful for many detector subsystems)
  - Technology support and foundry services
  - Radiation hardness qualification/monitoring of CMOS processes
  - High speed data links
  - DCDC convertors

- Experiment specific activities and projects
  - Muon detector readout for CMS
  - Tracker readout for CMS
  - Full custom front-end design (ATLAS and CMS)
  - RD53 – very rad hard pixel detector development (ATLAS and CMS)
  - Monolithic pixel detector development for Alice and now ATLAS
  - Medipix and related hybrid pixel readout (CLICpix etc)
  - picoTDC
  - etc

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  - etc

ASIC design support for HEP

- CERN evaluates and qualifies CMOS processes
- Provide support to HEP community for selected technologies
  - Technology Support Services
    - Develop ASIC design platforms for common use
    - Develop specific IP blocks of general use
    - Organize distribution and maintenance
    - Provide technology support to designers
  - Access to Fabrication Services
    - Establish Commercial Contracts with silicon vendors
    - Develop productive working relationships
    - Establish NDAs that allows for collaborative work
    - Organize & coordinate silicon fabrication

Supported Technologies

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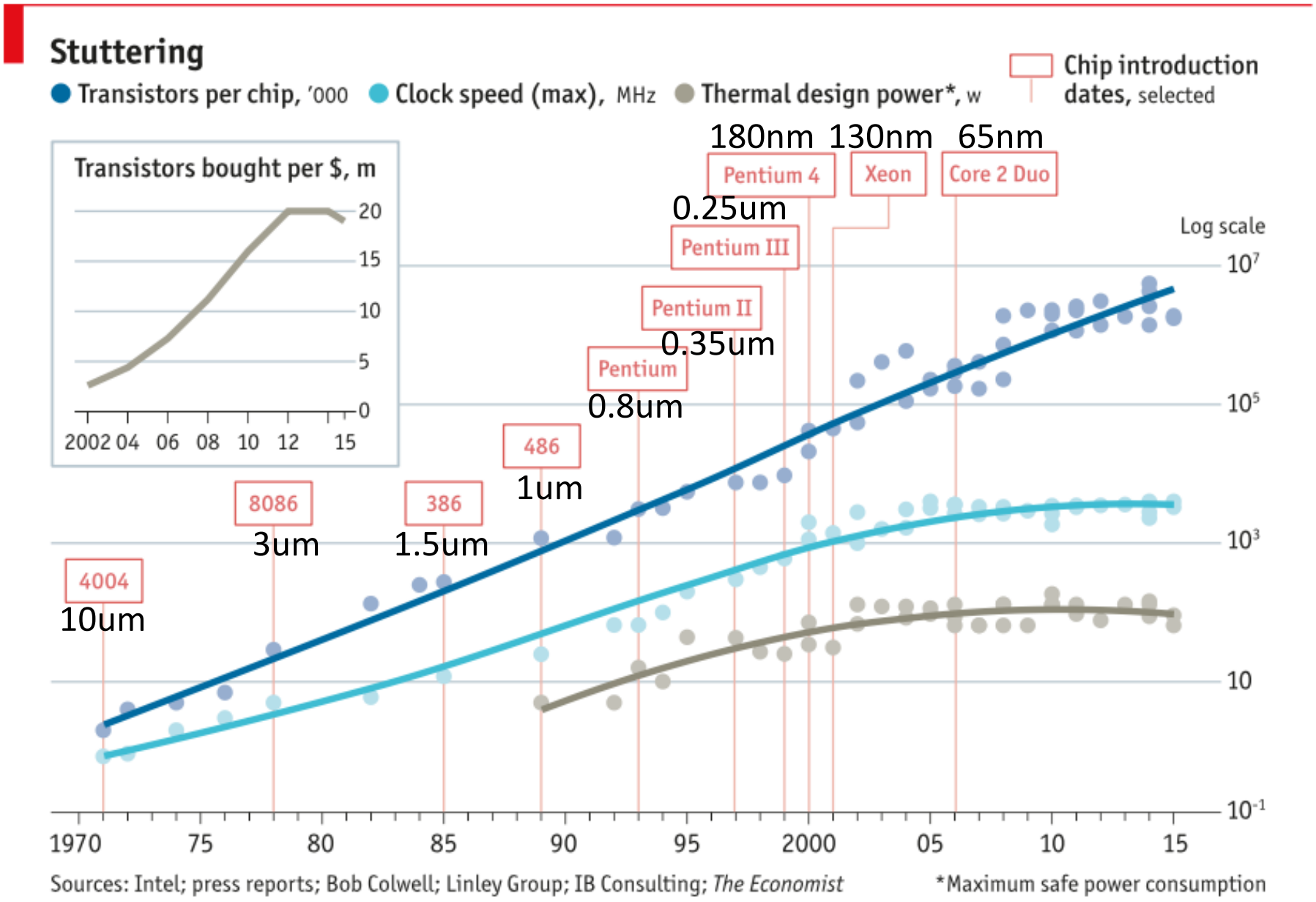
Moore's uncertain future



Technology Support Services

- Mixed-Signal-PDK (MS-PDK) & Workflows
  - TSMC
    - **CERN:** Development of MS-PDK and support of the Digital-On-Top flow
    - **IMEC:** Distribution of MS-PDK and support of the native foundry PDK & provides foundry specific technical information
  - GlobalFoundries
    - **CERN:** Distribution & support of the MS-PDK

Design Kit Support in 2016-17

- All design kits have received updates:
  - GF 130nm design kit
    - CAE tools platform update*
  - TSMC 130nm
    - Standard cell & IO pad integration fixes
    - Fixes on DRC and EXT rule files
    - Cumulative foundry PDK patches
    - CAE tools platform update*
  - TSMC 65nm
    - Additional standard cell libraries available
    - Cumulative foundry PDK patches
    - CAE tools platform update*

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Design tools 2016-2017

The following list describes supported design tools for CERN PDKs and digital design flows:

- ASSURA_04.15.107_IC617OA
- CONFRML_16.10.240
- EXT_15.26.000 (QRC)
- GENUS_16.12.000 (RTL compiler)
- IC_6.1.7.704 (Virtuoso)
- INCISIVE_15.20.010
- INNOVUS_16.13.000
- MMSIM_15.10.627
- PVS_15.17.000
- SSV_16.13.000 (Tempus & Voltus)
- VIPCAT_11.30.044_UVM

This toolset is supported for the following technologies:

TSMC 130nm
TSMC 65nm
GF 130nm

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GF/IBM 130nm

- Mixed-signal design kit updated to support the latest design tools (available from CERN website)
- Digital flow scripts updated (Genus & Innovus)
- Added training material/workshop for digital design tools, (available from CERN website)

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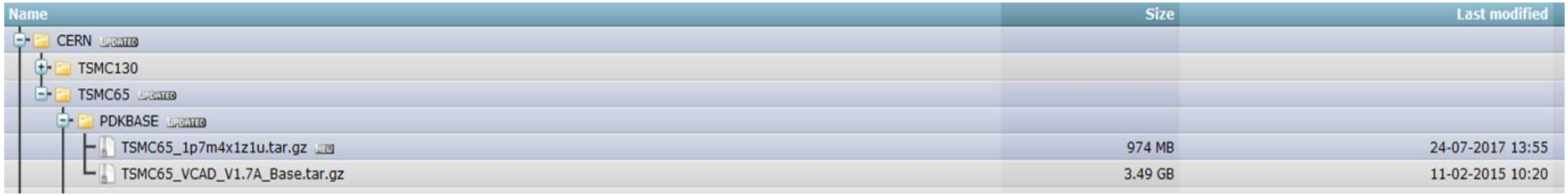
TSMC 130nm news and updates

- Updated PDK supporting latest tools available since October 2016, download via IMEC ftp server
- Digital flow scripts updated (Genus & Innovus), consult CERN website
- Added training material/workshop for digital design tools, consult CERN website

TSMC 65nm news and updates



- Metal stack 1p7m4x1z1u is now available (requires 1p6/1p9 base PDK) available from IMEC ftp server
- Digital flow scripts updated (Genus & Innovus), consult CERN website
- Added training material/workshop for digital design tools, consult CERN website
- See also Signoff Timing recommendations for digital designs on CERN website

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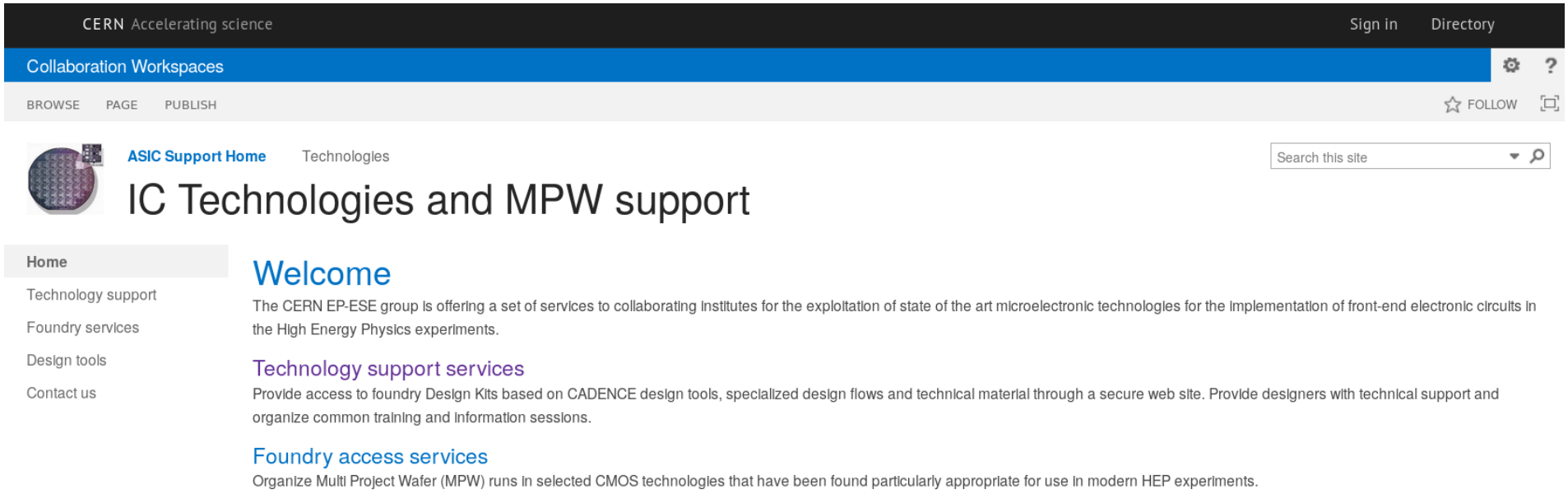
Website: cern.ch/asic-support

Tuomas Poikela

New Website available to facilitate the:

1. Distribution of CERN digital flows (Genus & Innovus)
2. Distribution of the Global Foundries 130nm design kit
3. Distribution of training material/workshops for digital design tools
4. Information about the TSMC 130nm and 65nm technologies
5. Information about the available macro cells



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Foundry services

- **GF 130nm process**
  - MOSIS MPW service ends in 2017
    - MOSIS & CERN could possibly organize dedicated MPW runs (based on demand)
    - Contact CERN to inform about your short-term and long-term requirements
  - Engineering & Production runs available in 2018
- **TSMC 130nm process**
  - Cybershuttle MPW runs
    - 1 run/month
  - 2 Fabs
    - Fab. 6 (8" wafer), **preferred for HEP designs**
    - Fab. 12 (12" wafer)
- **TSMC 65nm process**
  - Cybershuttle MPW runs
    - ~1 run/month
  - mini@asic MPW runs
    - 6 runs/year
    - Cost effective solution for small designs (2mmx2mm, **1mmx1mm *exclusively for HEP designs***)
  - 2 Fabs
    - Fab. 12 & Fab. 14 (12" wafer), of equal preference for HEP designs

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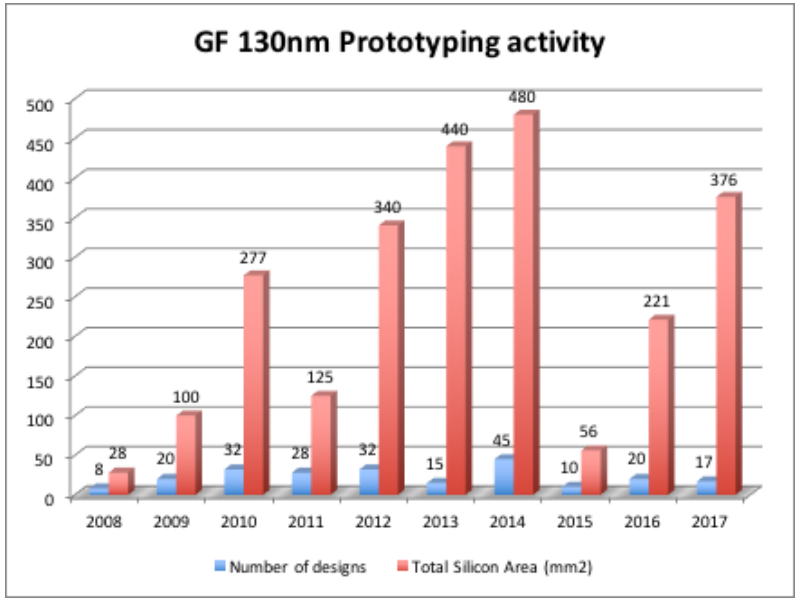
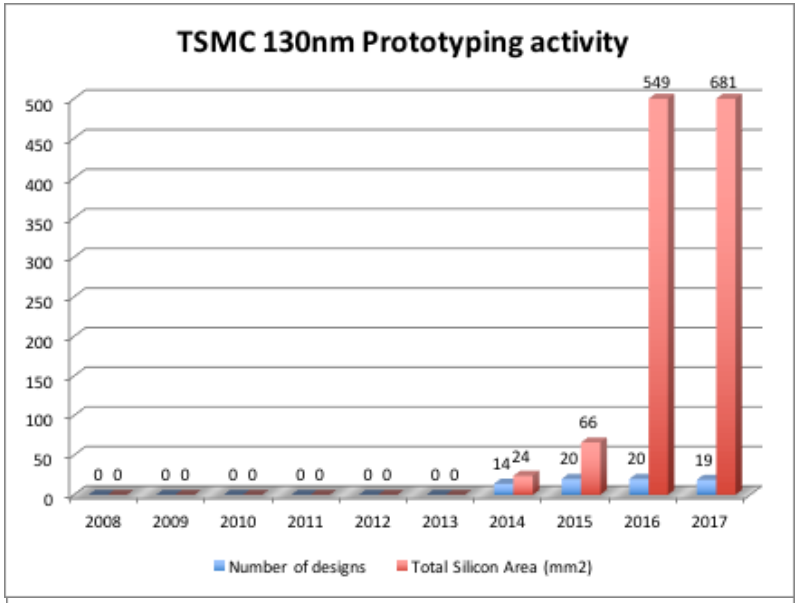
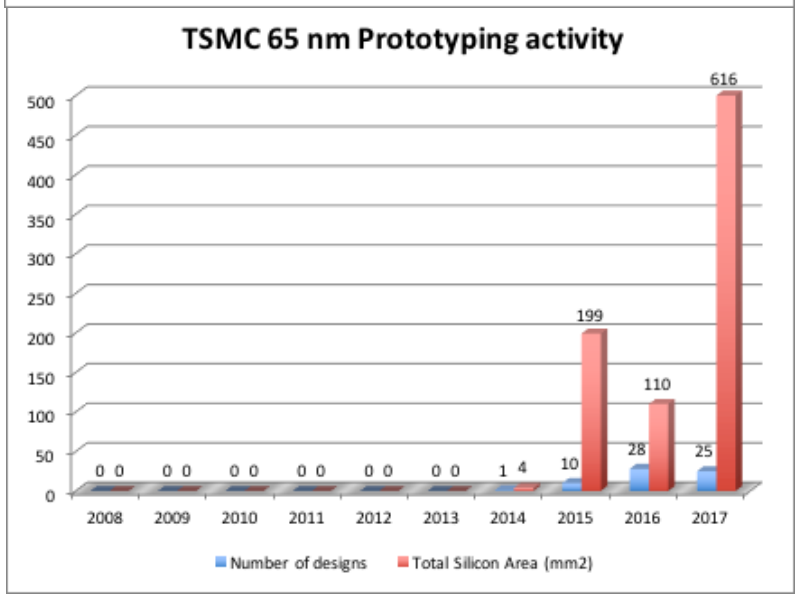
Prototyping Activity







- GF/IBM 130nm: 1 engineering run
- TSMC 130nm: 5 engineering runs
- TSMC 65nm: 1 engineering run

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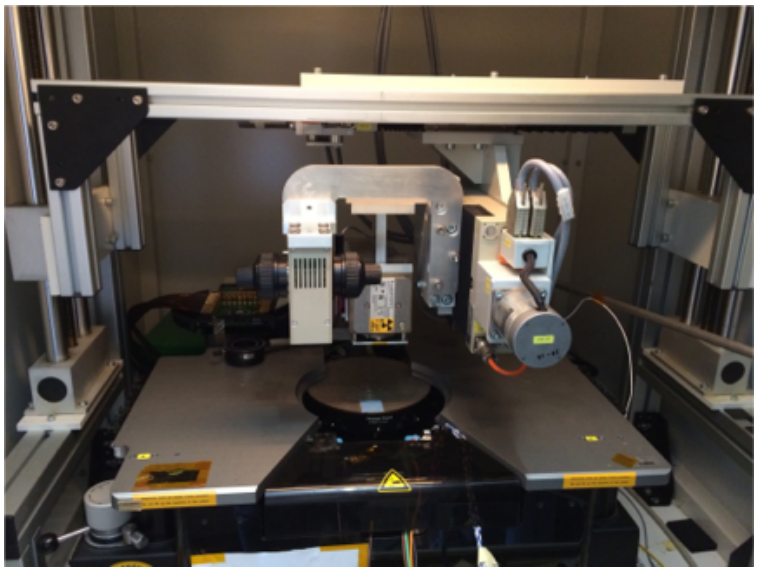
Radiation effects on microelectronics technologies

The study of radiation effects started at the beginning of the 90's: we have covered all CMOS nodes from 1.5μm down to 65nm!

During the years, we have acquired the components and assembled a unique irradiation system for Total Ionising Dose:

- Dose rates up to 9Mrad(SiO_2)/hour
- Controlled temperature of the DUT from -30 to +200°C
- Possibility to irradiate, bias and measure naked dice (with a semi-automatic probe station)
- Fully automatic measurement of individual transistors on naked dice (dedicated software controlling a semiconductor parameter analyser and a switching matrix)

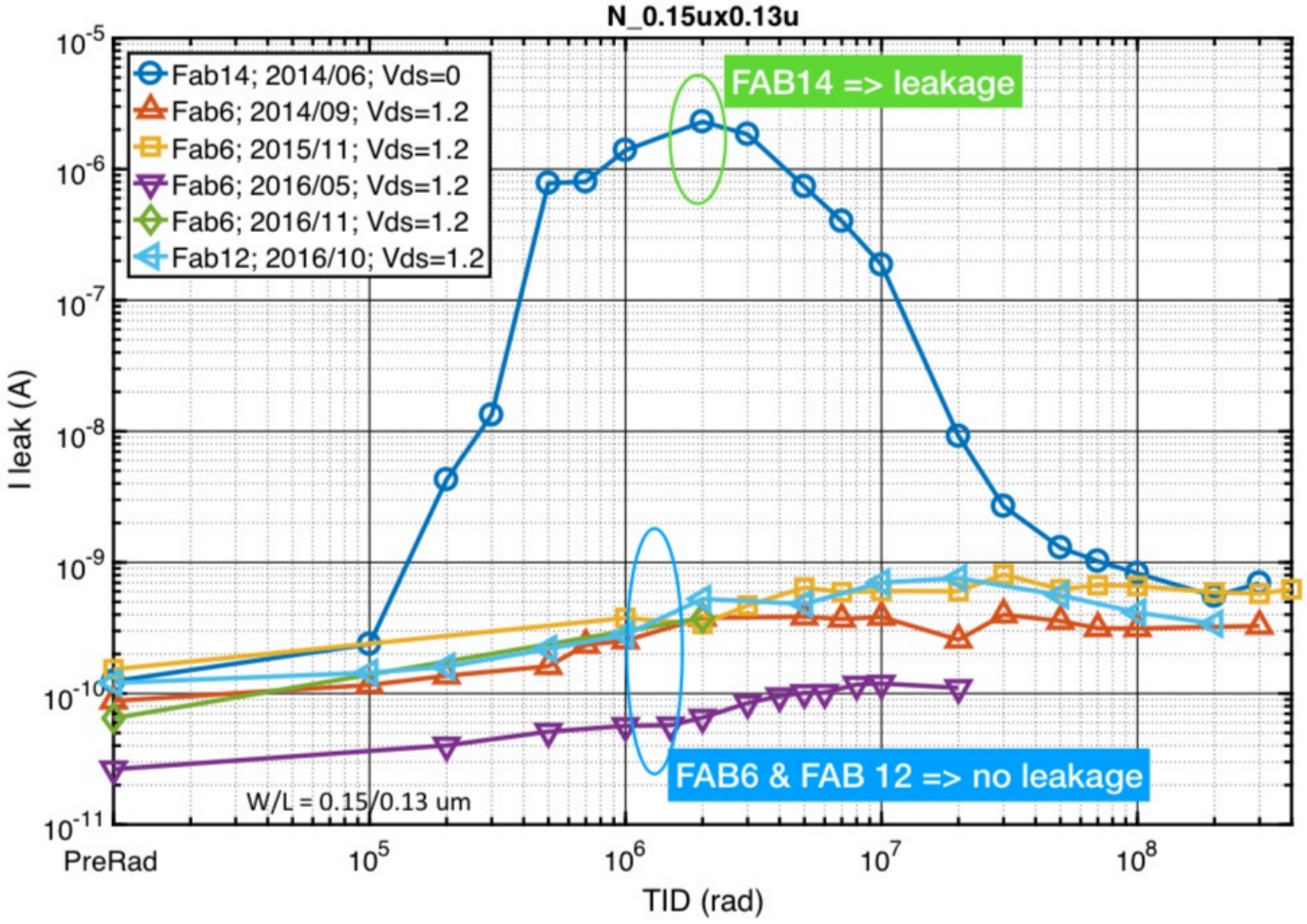


The latest characterisation work is done on 130 and 65nm technologies up to 1Grad!!!

F. Faccio

Stability of Rad hardness in TSMC 130nm CMOS

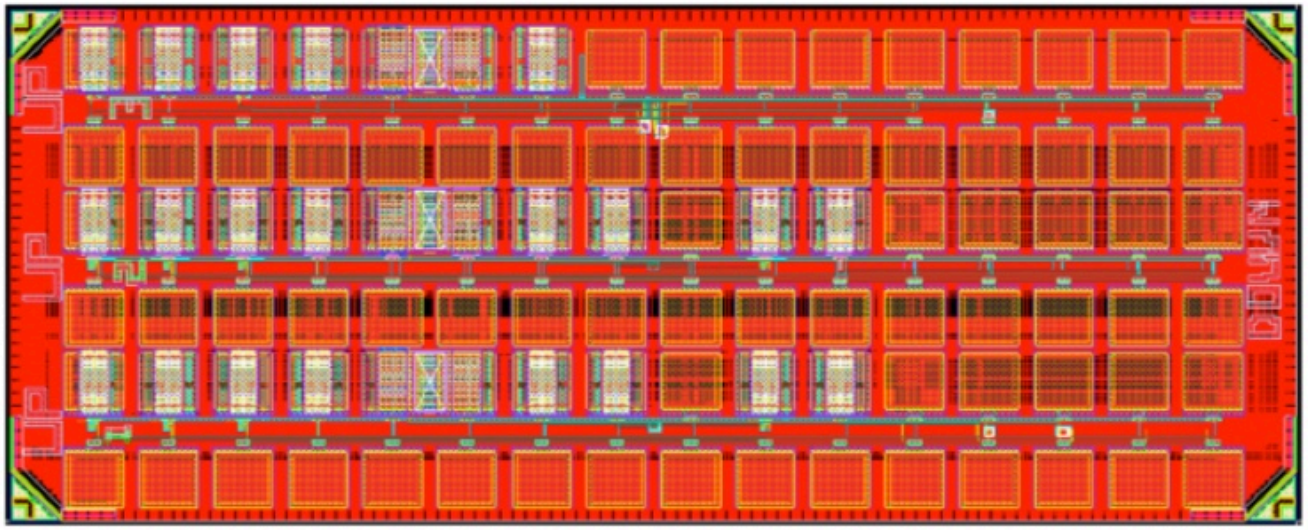
Only NMOS transistors from FAB14 have shown a considerable source-drain leakage current.
Samples from FAB12 and 14 have only been measured from one run.
Samples from FAB6 have been measured several times with consistent results.



F. Faccio

Stability of Rad hardness in TSMC 130nm CMOS (contd)

A dedicated chip has been developed to monitor the TID tolerance of the process, and it is added to almost all MPW runs (and engineering runs if possible).
This is measured with identical procedure every time.



Size: 2160 μm x 600 μm

G. Borghello

Stability of Rad hardness in TSMC 130nm CMOS (contd)

We have measured the TID response of 130nm transistors from the following list of runs.

130nm

	2014	2015	2016	2017
FAB 6 (8")	September(MPW)	November(MPW)	June(Velopix) July(VFAT) November (MPW)	July (Velopix V2) July (VFAT 3B)
FAB 14 (12")	June(MPW)			
FAB 12 (12")			October MPW)	

Not yet available

G. Borghello

Rad hardness in TSMC 65nm

- Situation is much more complicated at very high dose (>>100Mrad)
- PMOS shifts substantially depending on temperature, bias voltage, dose rate
- Many detailed studies (led by Federico Faccio) have been carried out
- Effects determined by STI, spacers and Dose rate have been identified
- Details available in 2 recent publications :
  - "Influence of LDD spacers and H+ transport on the total-ionizing-dose response on 65 nm MOSFETS irradiated to ultra-high doses," Federico Faccio et al., *presented at NSREC 2017*
  - "Dose rate sensitivity of 65 nm MOSFETs exposed to ultra-high doses," Giulio Borghello et al, *presented at RADECS 2017*
- Test on another 65 nm process show similar behaviour

Activities in the ME Section

- Common projects (useful for many detector subsystems)
  - Technology support and foundry services
  - Radiation hardness qualification/monitoring of CMOS processes
  - High speed data links
  - DCDC convertors

- Experiment specific activities and projects
  - Muon detector readout for CMS
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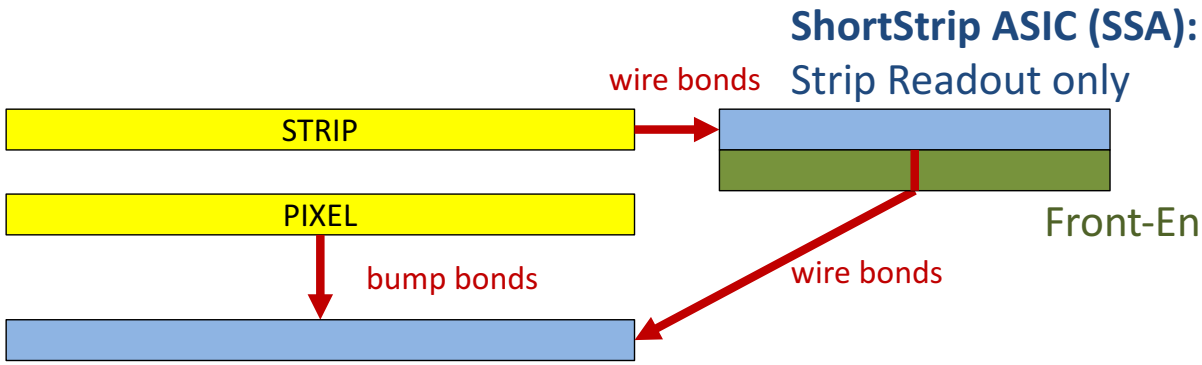
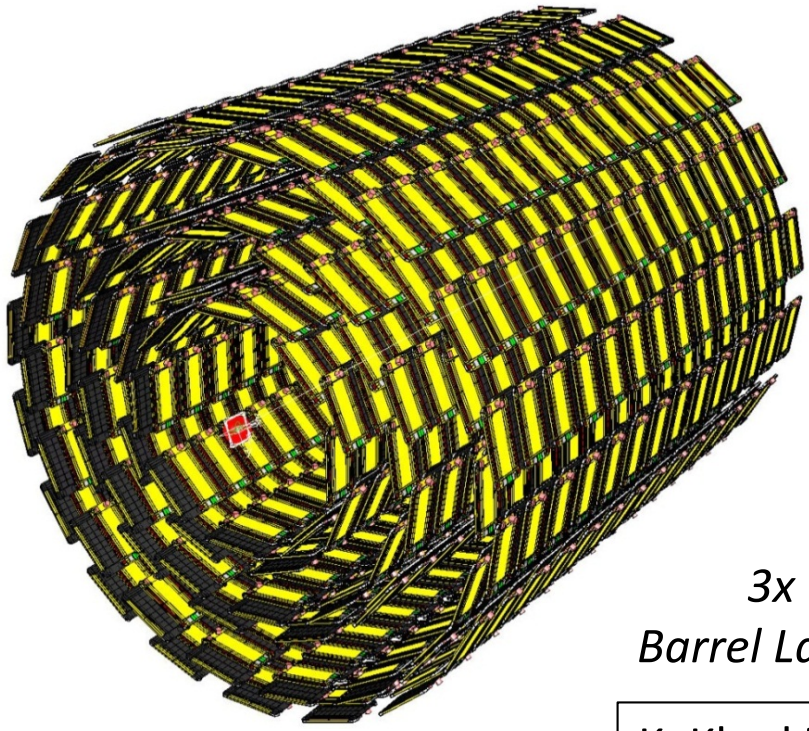
  - picoTDC
  - etc

Pixel + **S**trip module readout scheme



MacroPixel ASIC (MPA):
Pixel readout +
Correlation +
Data storage



3x
Barrel Layers

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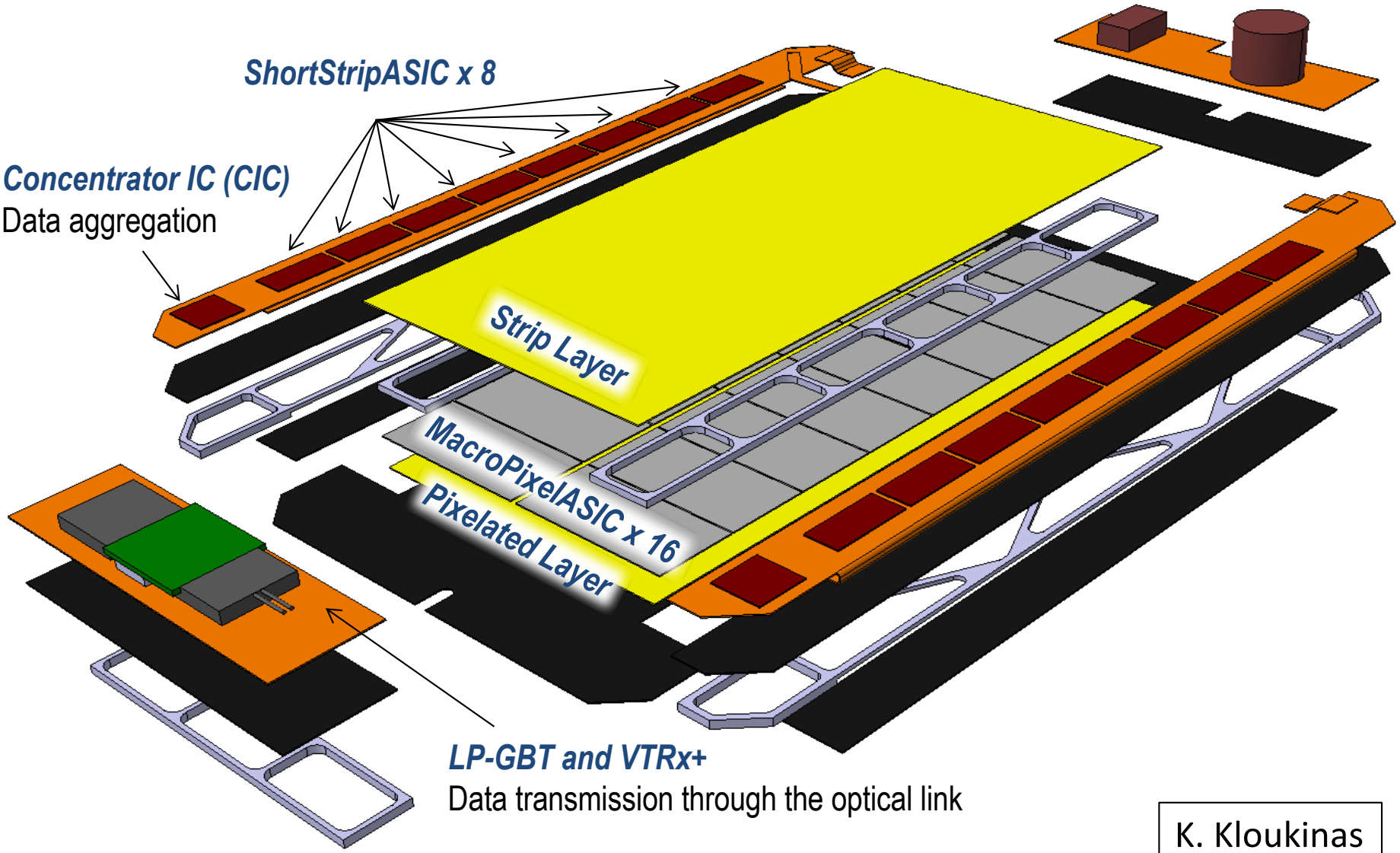
Pixel + **S**trip module exploded view

PS module is fully integrate entity

DC-DC converters



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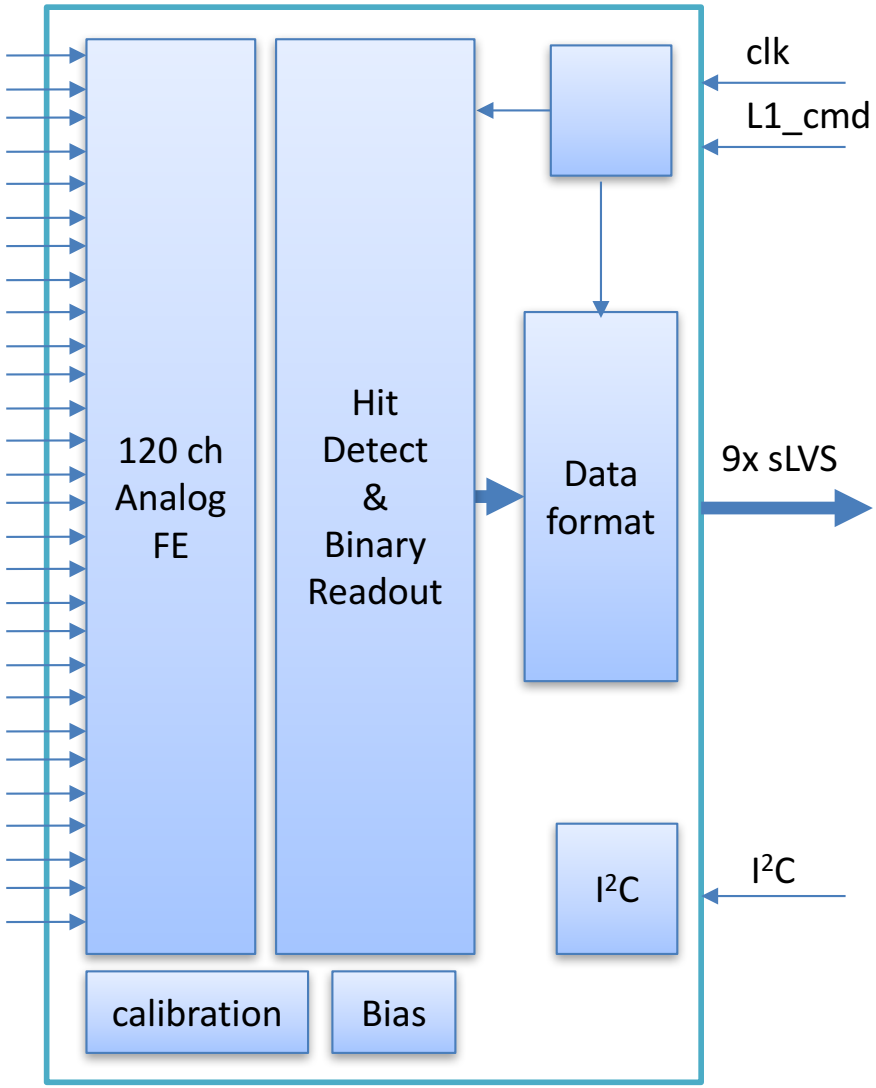
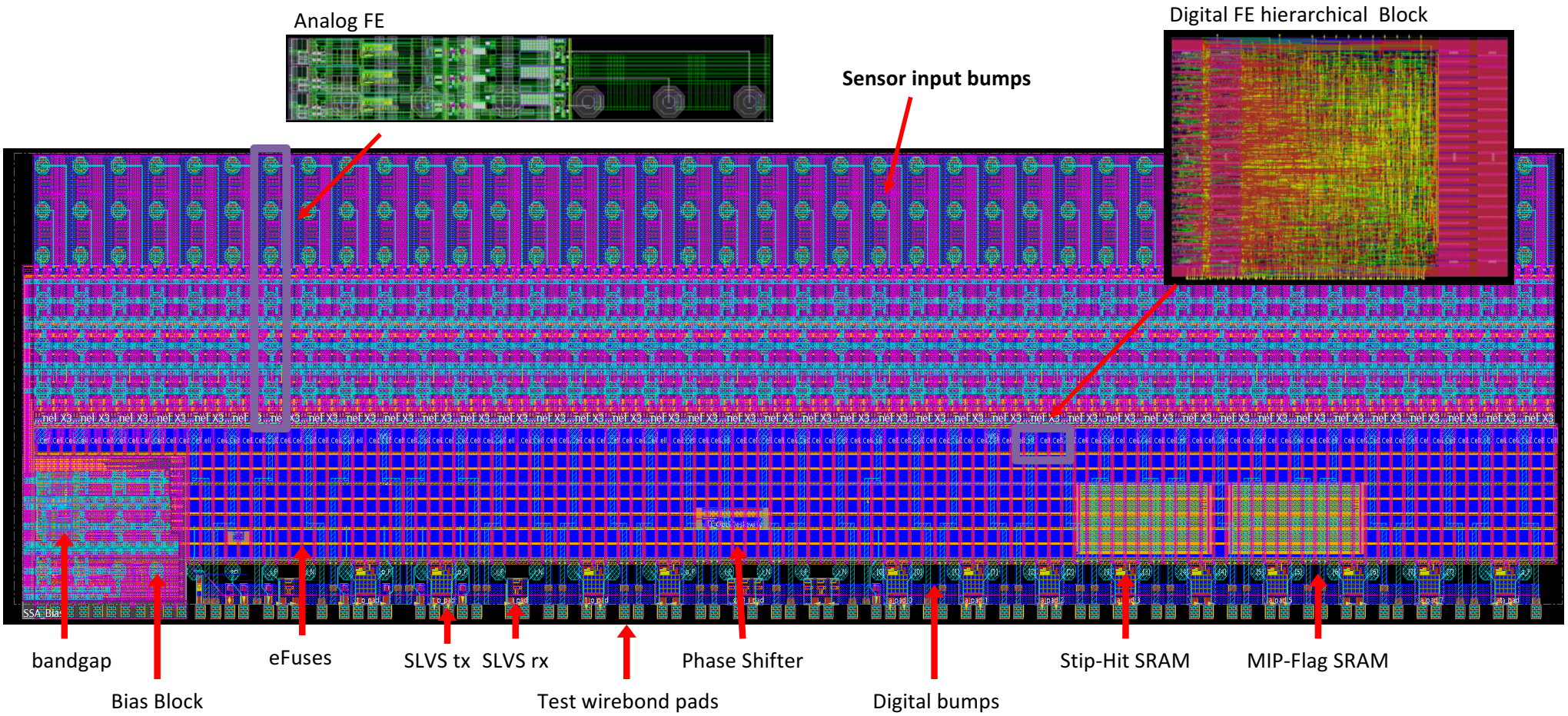
SSA ASIC specs

- Short Strip readout ASIC
  - 120 channel
  - Bump bonded on hybrid, AC coupled
  - Strip capacitance Cd=5pF,
  - Max strip leakage I_{leak}=1uA
  - ENC < 1,000 e^- (after irradiation)
  - Hit Threshold = 3,700 e^-
  - HIP Threshold* = 21,000 e^-
  - Output: (120 strip hit + 24 bit MIP info) /BX
  - Data Link: 9x 640Mbps sLVS lines
  - Vdd = 1.15V – 1.25V (1.2V nominal)
  - Temp= -30 to +50C (nominal -20C)



* Highly Ionizing Particles (HIPs) produced by nuclear interactions in the tracker sensors, producing large signals that they can momentarily saturate the FE resulting in signal loss.

SSA Floorplan and Integration

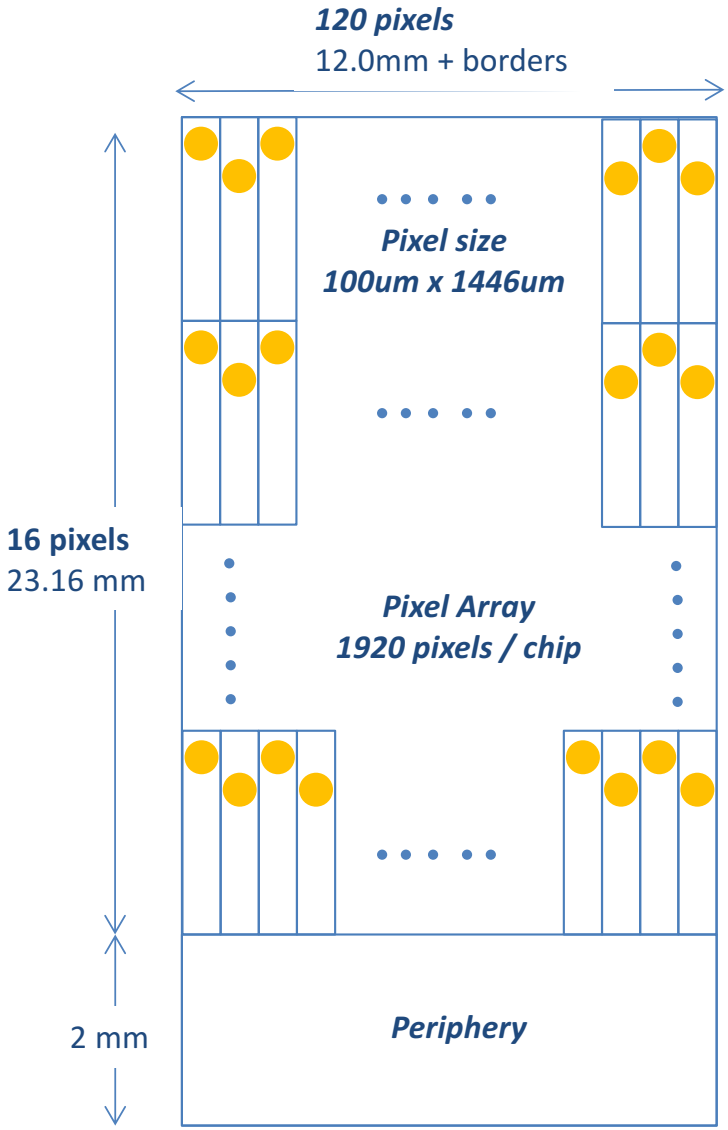


- Full size prototype implementing all required functionalities
- Design submitted for fabrication on 30/8/2017

A. Caratelli

MPA ASIC specs

- MacroPixel readout ASIC
  - Pixel Arrangement: 120 x 16 = 1,920 pixels
  - Bump bonded on sensor, DC coupled
  - Pixel capacitance Cd ~ 280fF
  - Max leakage I_{leak}= 50 nA after total dose
  - ENC < 200 e^-
  - Nominal Signal = 15,000 e^-
  - Data Output:
    - Trigger data path bandwidth: 1.6 Gbps
    - DAQ data path bandwidth: 0.32 Gbps
  - Vdd = 1.15V – 1.25V (1.2V nominal)
  - Temp= -30 to +50C (nominal -20C)
  - Power budget: 220 mW
  - 65nm CMOS process



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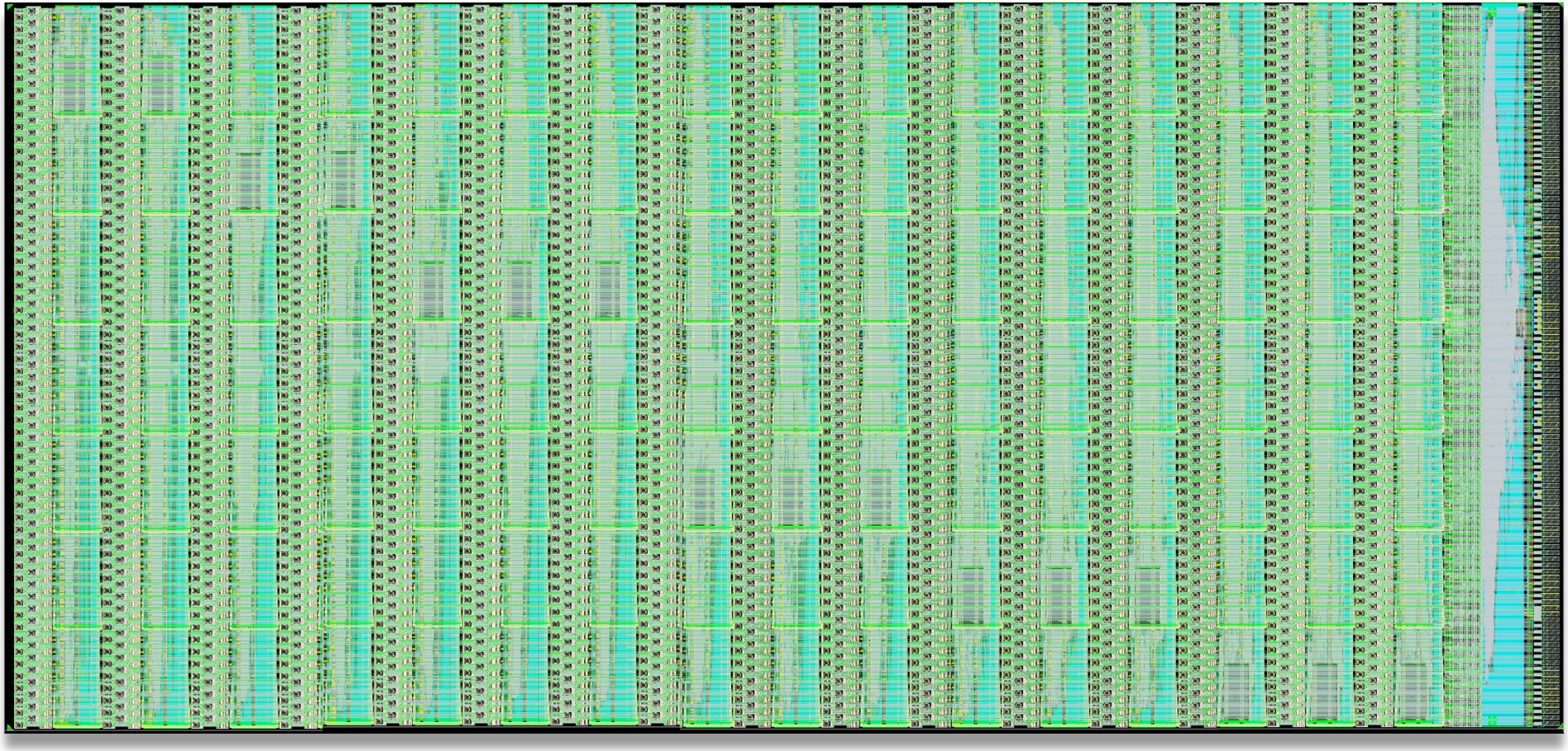
MPA final design layout



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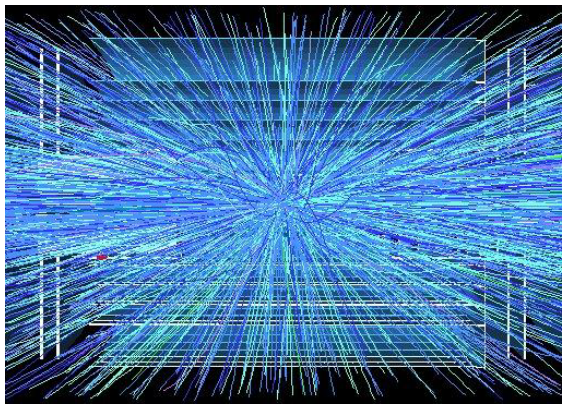
RD53

- Focussed R&D developing pixel chips for ATLAS/CMS upgrades



- Extremely challenging requirements for HL-LHC:
  - Small pixels: 50x50um^2 (25x100um^2) and larger pixels
  - Large chips: ~2cm x 2cm (~1 billion transistors)
  - Hit rates: 3 GHz/cm^2
  - Radiation: 1Grad, 2 10^{16} neu/cm^2 over 10 years
  - Trigger: 1MHz, 10us (~100x buffering and readout)
  - Powering: Serial Powering

- 18 collaborating institutes and many Guests
  - Bari, Bergamo-Pavia, Bonn, CERN, CPPM, Fermilab, LBNL, LPNHE Paris, Milano, NIKHEF, New Mexico, Padova, Perugia, Pisa, Prague IP/FNSPE-CTU, RAL, Seville, Torino,
  - 162 on collaboration Email list,
    103 on RD53 guests list (ATLAS/CMS people involved in phase 2 pixel but not on chip design)
    89 on RD53 NDA list (65nm TSMC technology access),
    81 on serial power list (ATLAS/CMS people interested/working on serial powering)
    34 on RD53A core design team
    108 on RD53A testing mailing list
  - ~12 PhDs, ~80 conference/workshop/ publications presentations

J. Christiansen

RD53A large scale demonstrator

- Large complicated chip:
  - Chip size: 20mm x 12(20)mm, small pixels (50x50um^2), 3 alternative analog FEs.
    Two alternative buffering scheme. Very high hit and trigger rates, Radiation and SEU tolerance,
    600e- threshold, 1200e- in-time threshold, “Low” power, Serial powering,
    Extensive analog and digital monitoring, Calibration features, Fully functional in test beams, etc.
- Specification document agreed with CMS and ATLAS phase 2 pixel communities: https://cds.cern.ch/record/2113263
- Core design team of ~10 designers for ~1year
  - 9 months remote collaboration with weekly meetings, common repository, Gitlab, blog, Emails, etc.
  - 3 months together at CERN with daily coffees and weekly meetings
  - 3 months for extensive verification: multiple problems and bugs resolved
  - Not forgetting major work before on radiation, IPs, simulation framework, prototypes with testing, ,
- Engineering run ~1M$ (last minute 25% reduction):
- Implementation document of ~80pages

J. Christiansen

MPA-RD53 “combo” run

- Process: **TSMC 65nm LP**
- Target fab: **FAB 12, 12” wafer**
- **Different BEOL metal stacks**
  - MPA/SSA:
    7+1 (5-thin, 1-thick, 1-UTM , RDL)
  - RD53:
    9+1 (7-thin, 1-thick, 1-UTM , RDL)
  - **Process split** to accommodate the two metallization options
- FBEOL3, "Wire bond with AP RD"

  - std Vt devices
  - low Vt devices
  - high Vt devices
  - zero Vt devices
  - triple well isolation
  - No POLYIMIDE
  - MOM capacitors
  - 2.5V IO devices

- Quantity requested
  - 25 engineering wafers
  - Keep 4 wafers at FEOL
  - MPA/all other projects split : 10 / 10 wafers
  - 70 ”set-up wafers”
  - Additional production lots ordered later

- Foundry agreed to assemble the reticle & receive designs on their “native” stack

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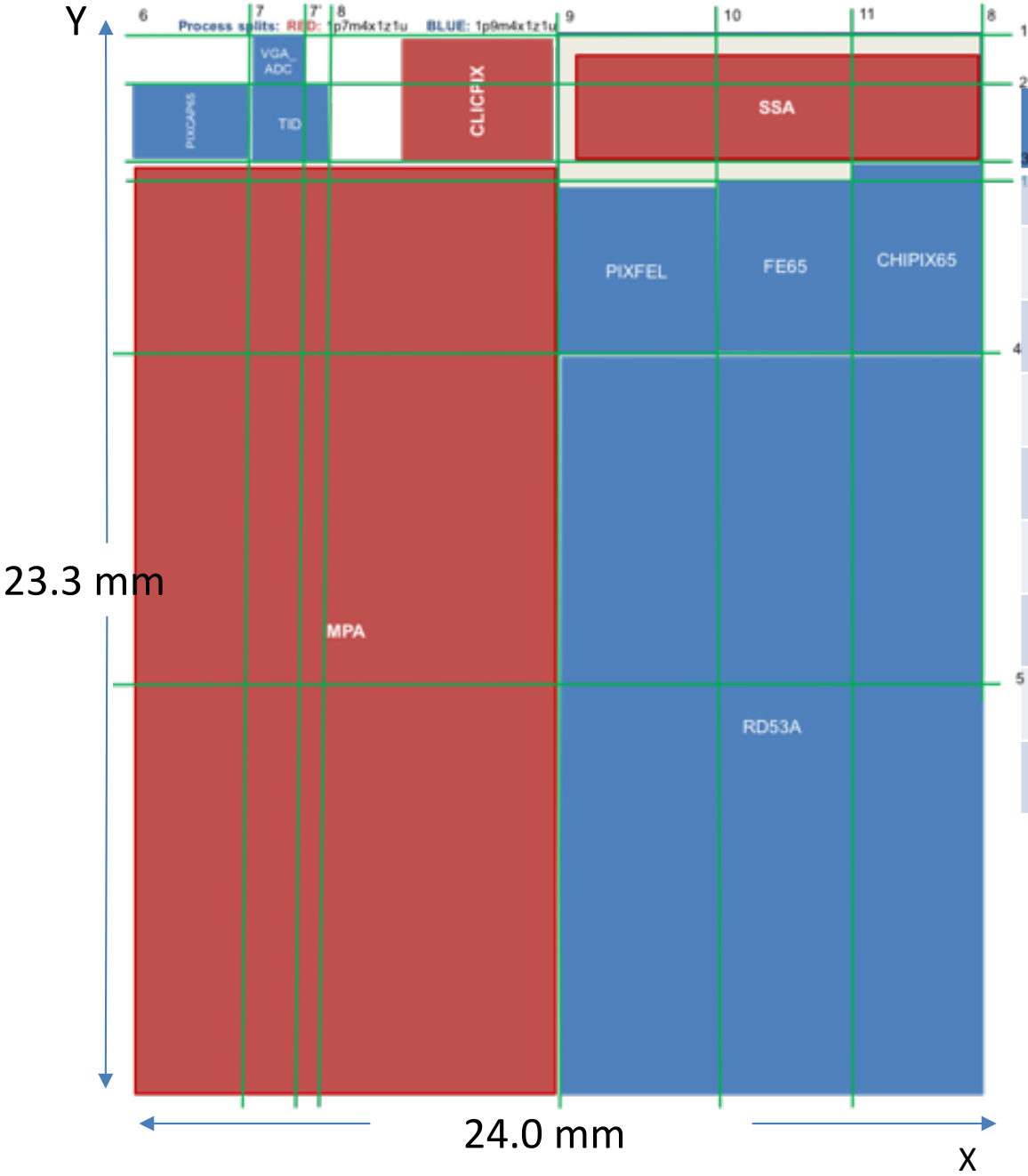
MPA-RD53 Reticle design



	Design Size (with sealring)	Design Name	Process split
1	25.00 x 12.00	MPA	7+1
2	3.24 x 10.80	SSA	7+1
3	3.35 x 4.06	Clicpix	7+1
4	20.06 x 11.54	RD53A	9+1
5	4.25 x 4.49	Pixfel	9+1
6	5.15 x 3.46	CHIPIX65-FE1	9+1
7	4.20 x 3.50	FE65-P2B	9+1
8	3.07 x 2.04	PIXCAP65	9+1
9	2.0 x 2.0	TID	9+1

Estimated delivery: end of November 2017

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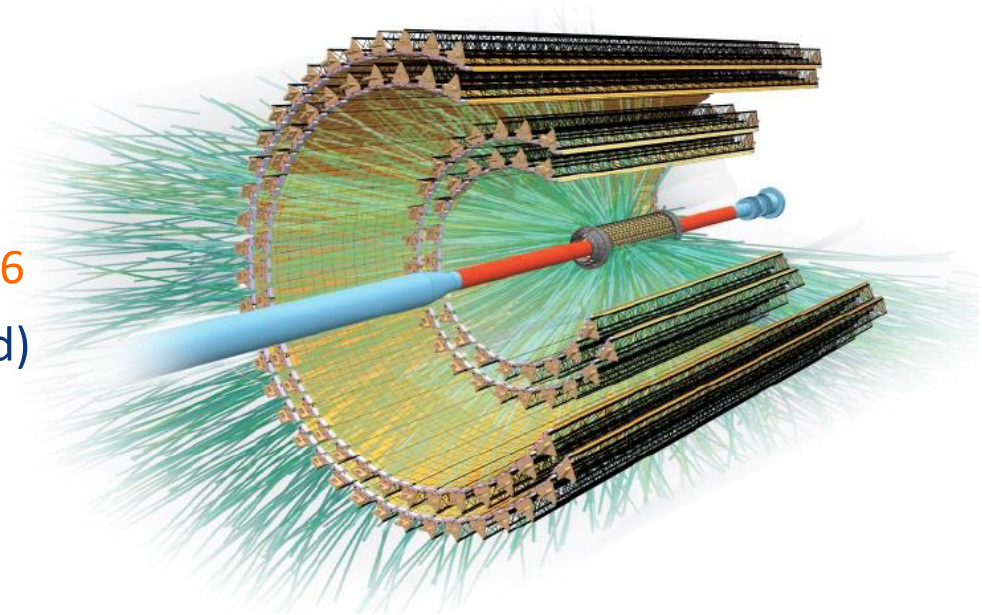
ALPIDE & ITS Upgrade status



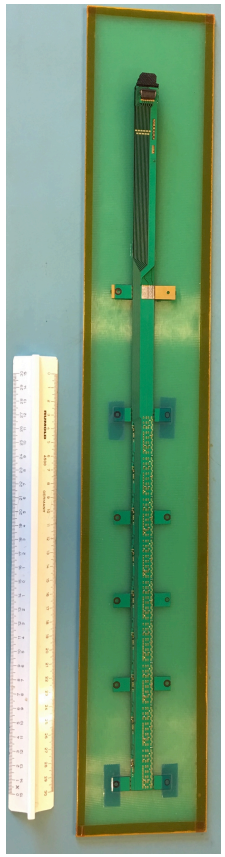
ALPIDE – production readiness review 25/11/2016

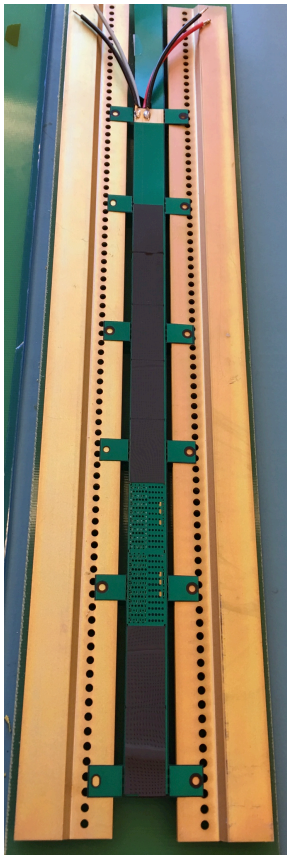
Production well underway (>500 wafers produced)

Module construction in progress

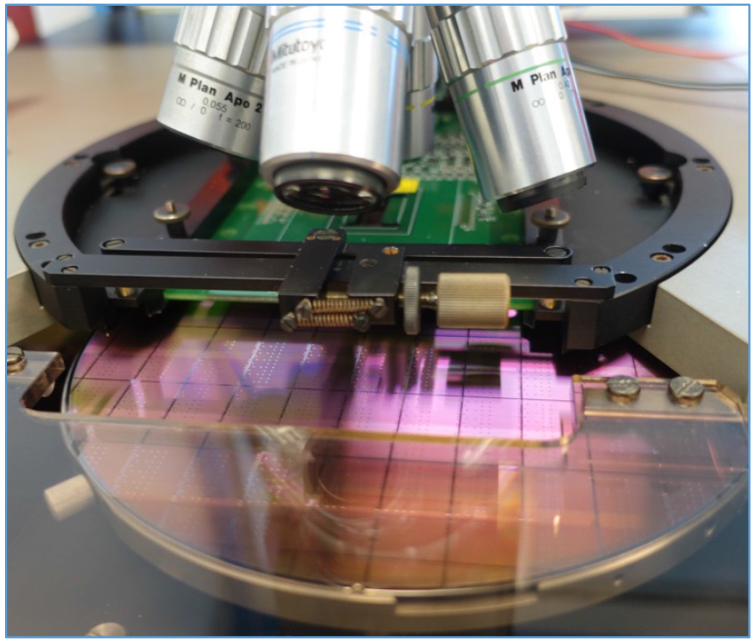
W. Snoeys

Inner Barrel Module (9 chips)

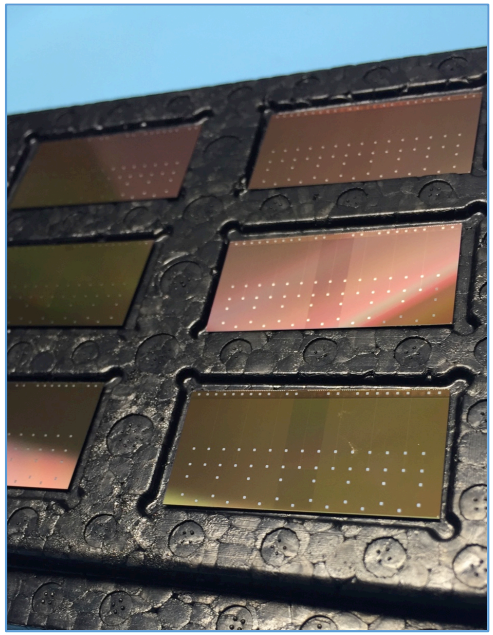




Wafer probe testing



Single chips after thinning & dicing



Monolithic pixel development for ATLAS

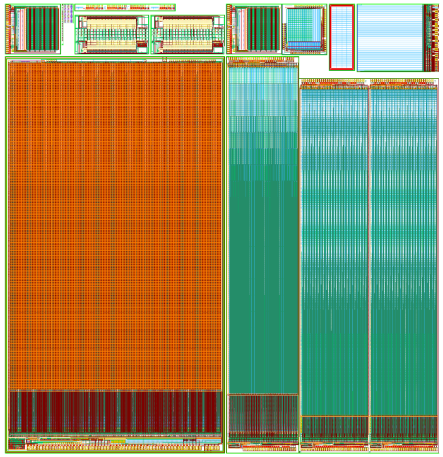
- Large effort on many technologies
- Concentrating on depleted MAPS for radiation tolerance
- Large chips and very encouraging results become available

W. Snoeys

Large chips become available in several technologies

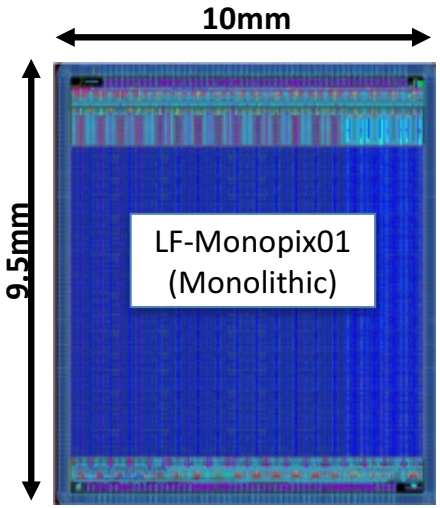
Chip name	Technology	CE Size*	Pixel size [µm²]	R/O architecture	Staust
aH18	AMS 180nm	Large	56 × 56	Asynchronous	Measurements
Malta	TowerJazz 180nm	Small	36 × 36	Asynchronous	Submitted
TJ Monopix		Small	36 × 40	Synchronous	
LF Monopix	LFoundry 150 nm	Large	50 × 250	Synchronous	Measurements
Coolpix		Large	50 × 250	Synchronous	
LF2		Large	50 × 50	Synchronous	

* CE Size = Collection Electrode Size



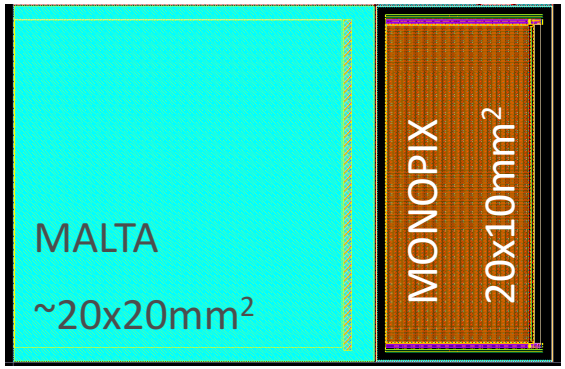
ATLAS Pix & MuPix

AMS 180 nm



MONOPIX, LF2 & COOLPIX

Lfoundry 150 nm



MONOPIX & MALTA

TowerJazz 180 nm

W. Snoeys

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Work towards final chip for outer pixel layer

- Building design team, start organizing weekly meetings
- Small collection electrode size has significant advantages for the electronics design (power, speed, noise performance, in-pixel circuit complexity…). The process modification in TJ (DOI 10.106/j.nima.2017.07.046) achieves radiation tolerance with a small collection electrode. Working with other foundries to do the same.
- Concentrate on conceptual full module design, architecture and system issues
- Investigating fast path to full module (e.g. aggregator chip, same or very similar to one needed for hybrid pixels)
- Groups committed and others expressed interest to proceed for a common design

Conclusions

- The CERN Microelectronics Section has 2 categories of activities:
  - Common Projects
  - Experiment specific developments and projects
- Many (if not all) activities are carried out in collaboration with outside institutes
- We aim to (where appropriate) propose common technology platforms for the HEP community
- We evaluate processes for radiation hardness, negotiate foundry access and support tools and PDKs for the selected processes
- This permits and encourages collaborative effort on large scale designs
- A number of projects illustrating this approach have been described