MOSIS Roadmap

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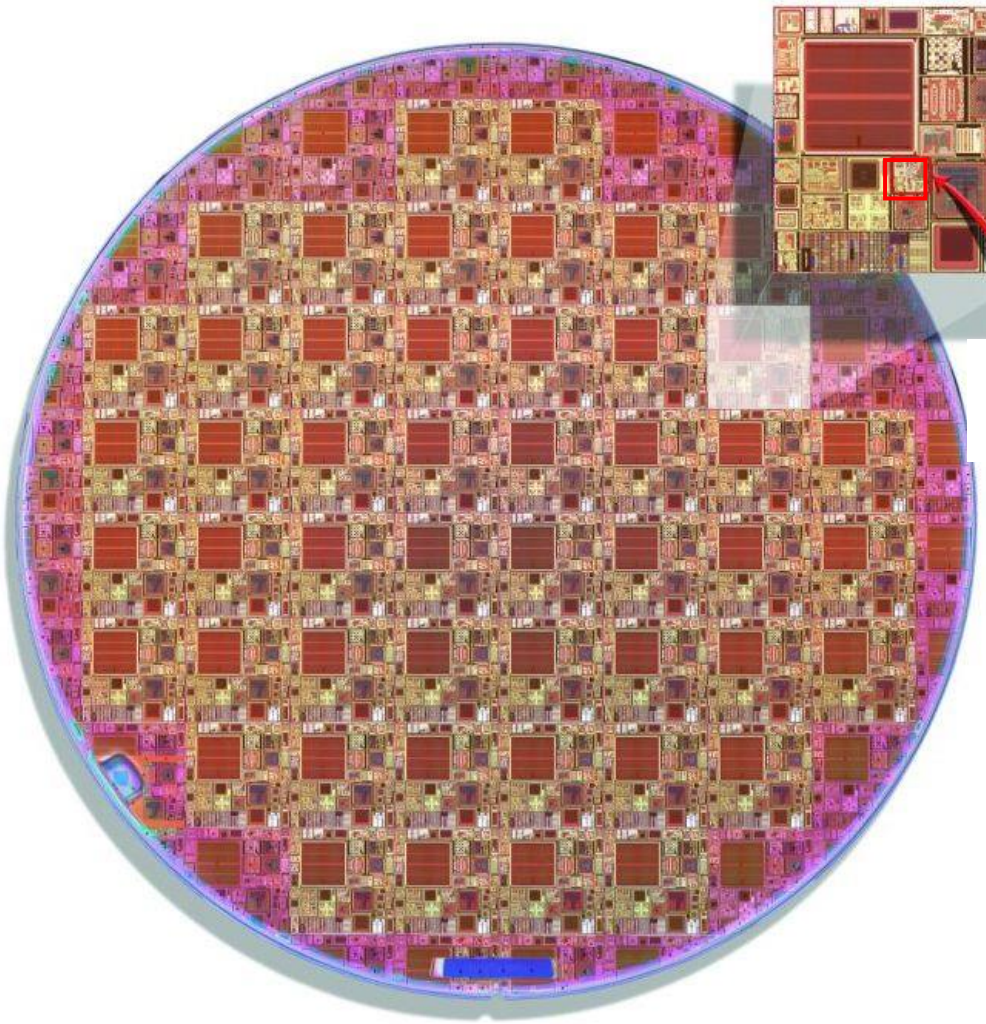
Overview

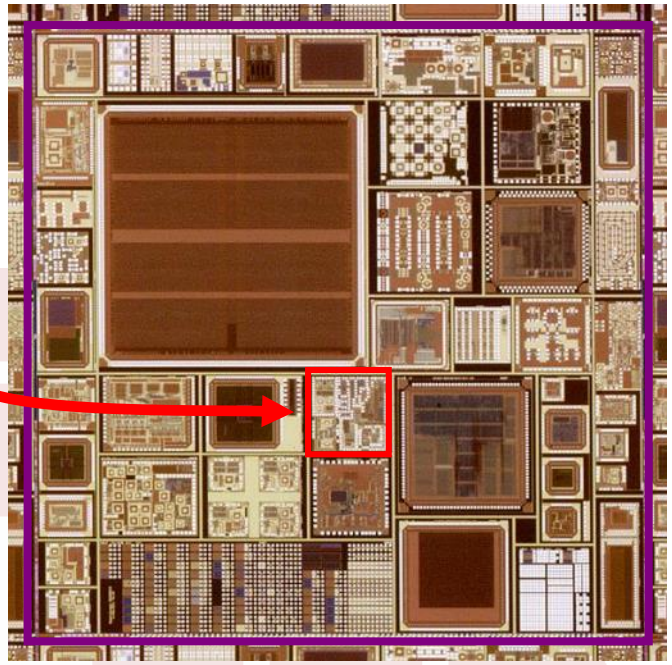
- **Founded 1981. Total of ~30 staff.**
  - Provides foundry services to a wide variety of customers
- **Based in California, USA**
  - Self funded since 1994
- 35+ Years of Providing MPW Runs
  - Including LVP (Low Volume Production)
- **Strong technical support:**
  - 60,000+ designs managed
  - Can provide direct answers to 98% of technical questions
- **Test lab**
  - Parametric test systems, 300 mm automated wafer probers, etc.
- **Computing**
  - High-capacity servers for design pre-fabrication processing

MOSIS Multi-Project Wafer



Many Dedicated Runs

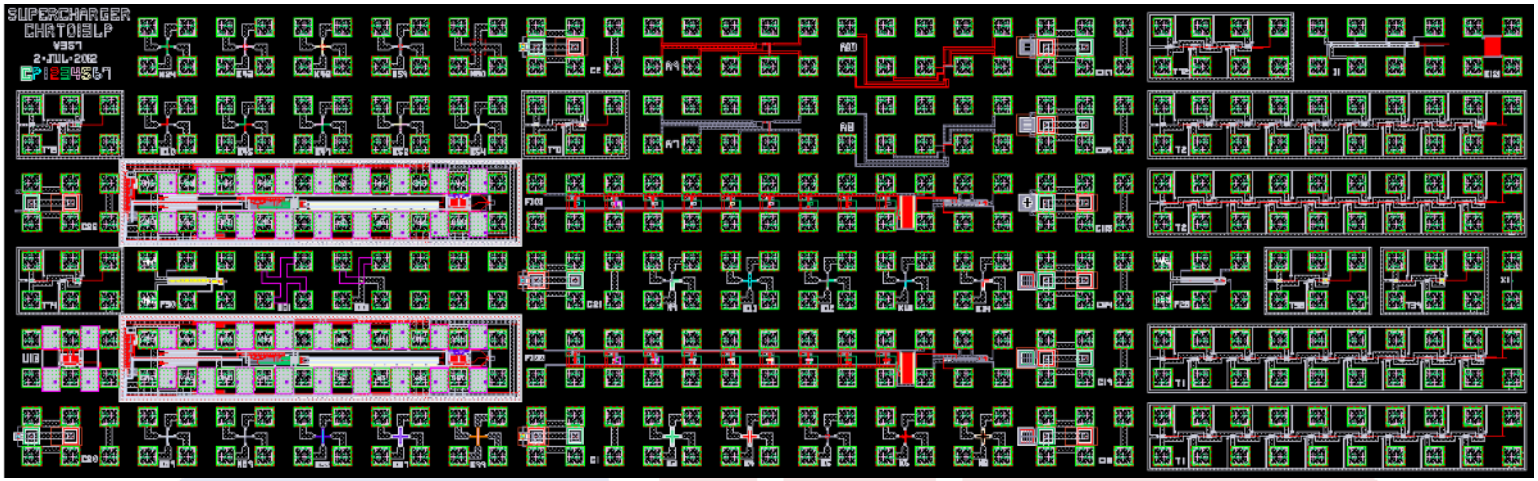
Example User



Multi-Project Reticule
~ 50 Different Designs

<u>Shared Costs:</u> Mask, Wafer, Foundry and Packager Interface

MOSIS Process Monitor



- Sheet Resistance - 15 layers
- Via/Contact Resistance - 12 vias
- Inverters - 5 sizes
- Transistors- N/P* Enhancement - 34 sizes
- Transistors- N/P Thick Enhancement - 3 sizes
- Transistors- N zero Vt common - 3 sizes
- Transistors- Extended N Enhancement - 5 sizes
- Transistors- N/P Low Vt common - 3 sizes
- Capacitors - 27
- Ring Oscillators - Thin and Thick oxide
- Operational Amplifiers - 3

Assembly Options

- MOSIS Offers a Variety of Packaging Options
- Packages - QFPs, BGAs, etc. - Plastic, Ceramic
- Flip Chip Wafer Bumping (e.g. Third Party Vendors)
- Work with US-Based Medium Volume Vendors in Addition to High Volume Offshore Partners

Foundry Partners

GLOBALFOUNDRIES

austriamicrosystems

ON Semiconductor®

Supported GF Processes

Technology	Base Logic	RF CMOS	High Voltage	SiGe BiCMOS	RFSOI
14 nm	X				
28 nm	X				
40 nm	X				
45 nm					X
55 / 65 nm	X				
90 nm				X	
0.13 µm	X	X	X	X	X
0.18 µm	X	X	X	X	X

SiGe vs. RF CMOS

- **Maximum Application Frequency**
  - SiGe Increased Operating Speed than RF CMOS
- Reduced Electronic Noise
- **Lower Power Consumption**
- Wafer Costs
  - Fewer Masks Required for RF CMOS Resulting in Lower Wafer Costs
  - **As Geometry Scaling Decreases,**

    # Masks for RF CMOS Increases

    Bringing Wafer Costs of RF CMOS Closer To SiGe

Supported TSMC Processes

Technology	Standard Logic	RF CMOS	Mixed Mode
16 nm	X		
28 nm	X		
40 nm	X		
65 nm	X	X	X
90 nm	X	X	X
0.13 µm	X	X	
0.18 µm	X	X	X
0.25 µm	X	X	X
0.35 µm	X	X	X

MOSIS TSMC Tiny2

- MOSIS Tiny2 access for Commercial University customers (COM, not MEP)
  - Lower Cost
  - Fixed Size
- Runs identified on the TSMC fabrication schedule as access restricted to university accounts.
- Technologies
  - 65nm
  - 180nm

Silicon Photonics

- **Albany CNSE (AIM)**
  - Full Silicon Photonics
  - Passive Silicon Photonics
  - Interposer (for Photonics)

- **GlobalFoundries** – 9WG/90WG
  - Was IBM process, 45nm in development
  - 90nm CMOS with Photonics
  - Target is Data Center applications

Community Access

- Work With HEP Community in Regard to Minimum Quantity Orders
- Remain Flexible to HEP Community Needs
- Address All Levels Needed
  - Prototype – MPW
  - Medium – MPW / Taxi
  - Dedicated – Continued Availability
- Suggestions
  - HEP-MOSIS User Group (Web Based)
  - Workshops

MOSIS Summary

Working with MOSIS As Their Fabrication Partner,

HEP Designers Speed Their Route to Design Implementation:

- **Access to Broad Range of Production Services**
  - MPWs → Low Volume Production
  - Foundry/Test/Packaging
  - Leverage Network of IP/Design Partners
- **Strong technical support**
  - 30+ Years Experience (60,000+ Designs Managed)
  - Can Provide Direct Answers to 98% of Technical Questions
- **Build On Long Term Relationship With HEP Community**
  - Future Access
  - Workshops, Web Forums, Training, etc.
  - Help Us Help You

HEP-MOSIS Dialogue

- Open To Further Dialogue
- How Can MOSIS Best Support the HEP Community?

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MOSIS Login Center:
https://www.mosis.com/pages/account-login

Thank you