HEP-IC Workshop 2017

Thursday, 5 October 2017

New developments, trends and plans (08:00 - 15:00)

time	[id] title	presenter
08:00	Breakfast / Registration	
08:30	[21] Introduction	O'CONNOR, Paul
08:40	[22] Digital-on-top Mixed Signal Design	HOROWITZ, Mark
09:00	[23] Trends in pixel readout chip designs for high rate and radiation	GARCIA-SCIVERES, Maurice
09:20	[24] Precision Timing in HEP experiments	Prof. VARNER, Gary
09:40	[26] Front-end in extreme conditions	Dr LI, Shaorui
10:00	[27] Rad-hard methodology and cad tools	MIRYALA, Sandeep
10:20	Cofee break	
10:40	[28] Advanced Interconnections between Sensors and Integrated Circuits	KENNEY, Chris
11:00	[29] 3D-IC status and trends	Dr LIPTON, Ronald
11:20	[30] Content addressable memories for HEP	Dr LIU, Ted
11:40	[31] Information-centric analog interfaces	MURMANN, Boris
12:00	Lunch Break / Poster Session	
13:00	[32] Cadence: trends in CAD tools and services	NIZIC, Mladen
13:20	[33] MOSIS technology Roadmap	Mr PINA, Russ
13:40	[34] Roundtable	O'CONNOR, Paul
14:40	Coffee break	