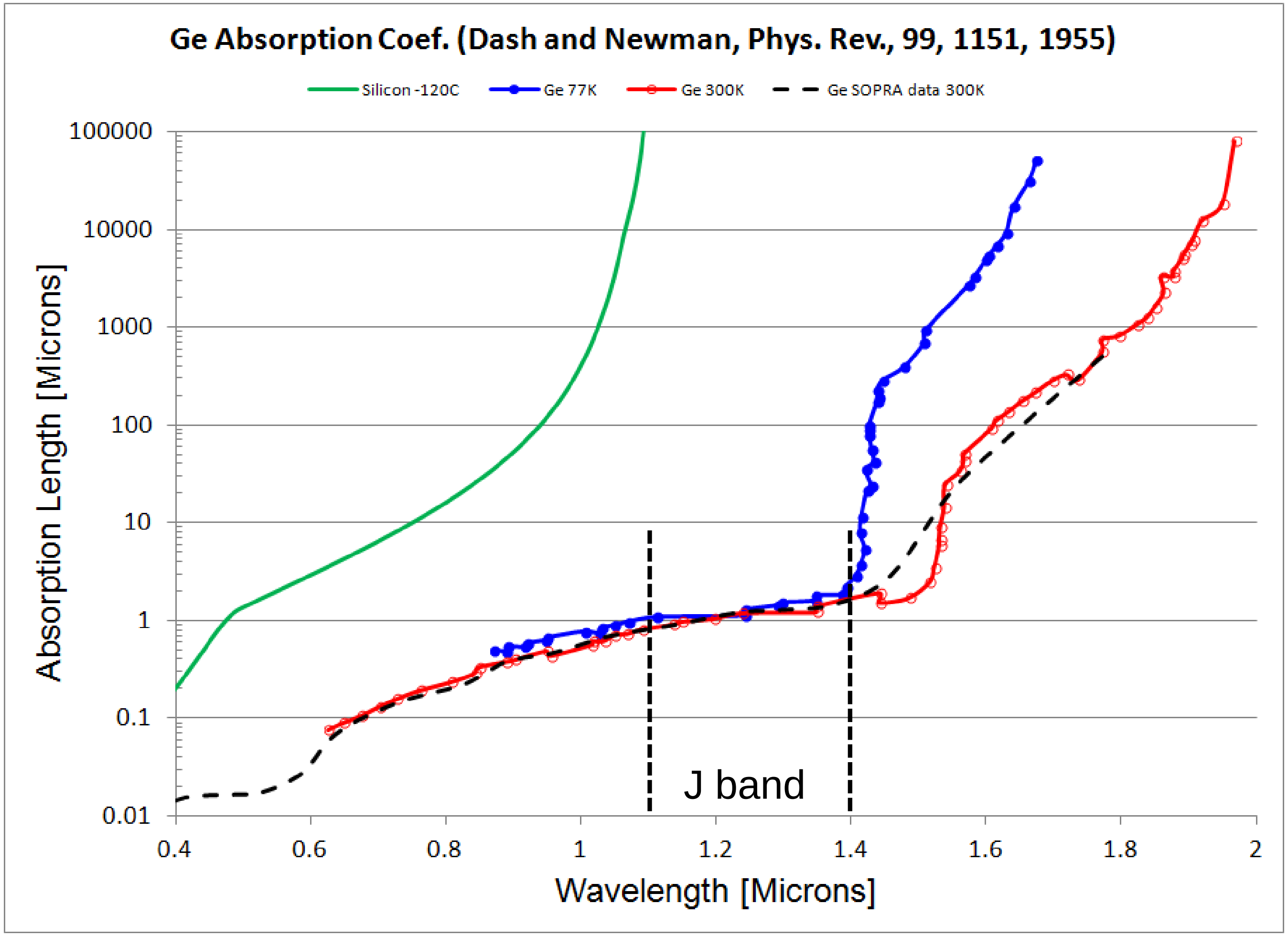
Germanium CCD R&D

Steve Holland, David Schlegel / LBNL

Outline

- Motivation for Ge CCDs / Facilities for R&D work
- Germanium technological considerations
- Work in progress
- Deep sub-electron noise with Skipper CCDs
  - Silicon CCD collaboration with FermiLab and others

Germanium CCDs / Expected NIR benefits



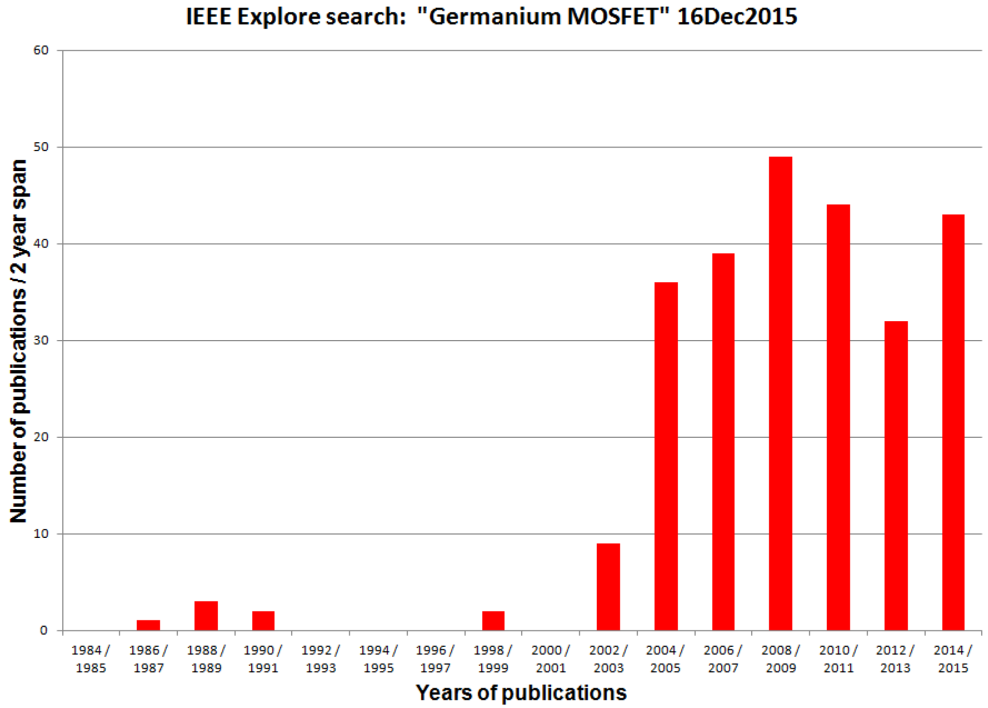
- Extend near IR response with Ge
- Higher redshifts, e.g. z = 1.6 to 2.6 for DESI [O II] (Si to Ge)
  - 2x volume
- Ge CCD effort underway at Lincoln Laboratory

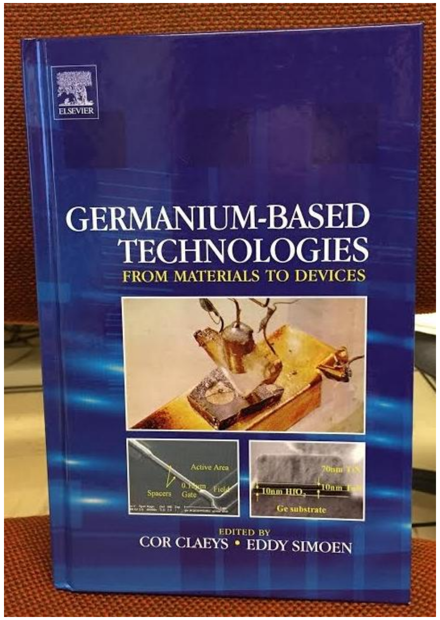
Opportune time for Ge CCD development

– Significant uptick in Ge MOSFET R&D

» Ge has high carrier mobility for both electrons and holes, e.g Ge hole mobility is the highest of any semiconductor and > Si electron mobility

» Of interest for high performance CMOS



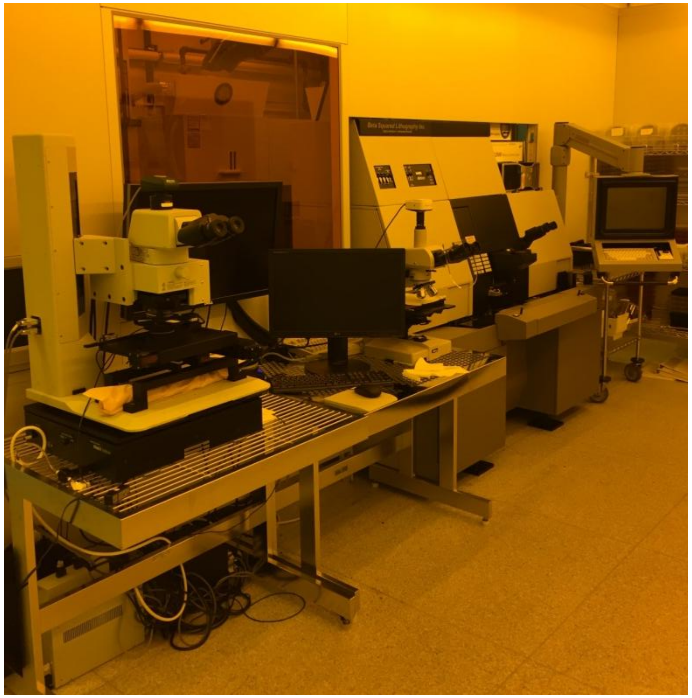


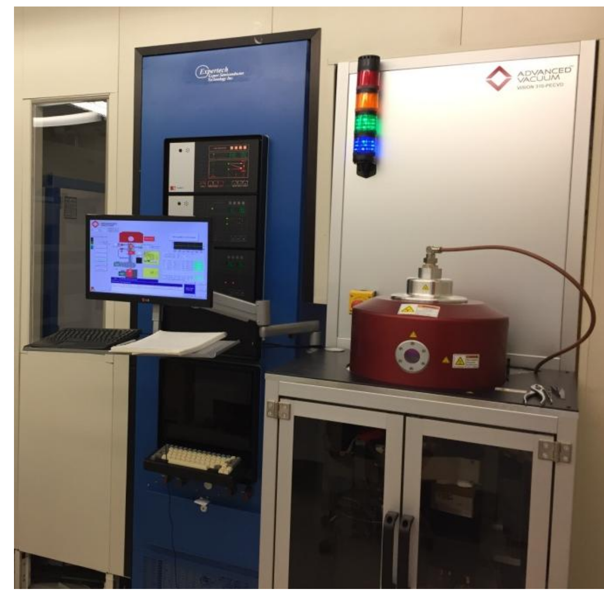
LBNL Interest in Germanium

- Ge CCDs natural fit for future Dark Energy studies
  - Longer wavelength cutoff → higher redshift objects
  - Potentially higher performance / lower cost than existing HgCdTe detectors

- Facilities available for LBNL Ge R&D
  - LBNL MicroSystems Laboratory
  - LBNL Molecular Foundry
  - UC-Berkeley Marvell Nanofabrication Laboratory

LBNL MicroSystems Laboratory





- Class 10 clean room
  - 150 mm wafer processing
  - DECam / DESI CCDs with DALSA
  - Origin of the fully depleted CCD utilizing a substrate bias voltage (mid to late 1990's on 100 mm high-ρ silicon)

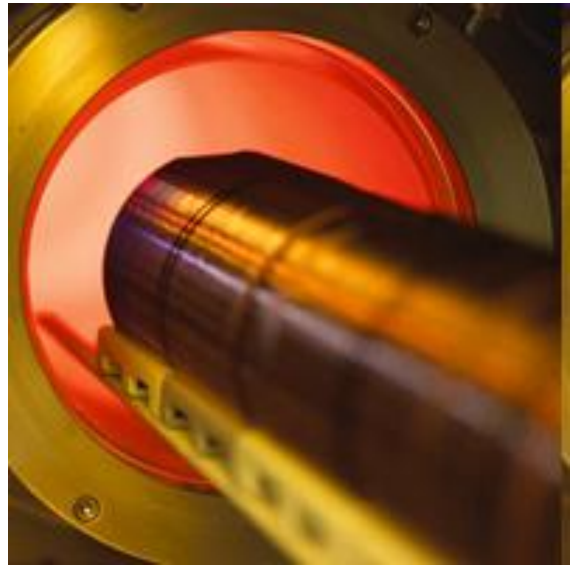
LBNL Molecular Foundry

- Electron-beam lithography for CCD gate electrode development and atomic layer deposition (ALD)

UC-Berkeley Marvell Nanolab'

- Polycrystalline Ge (in-situ doped) capabilities
- Deep UV wafer stepper (250 nm lines / spaces)
- TCP polysilicon etcher (deep submicron)
- Atomic layer deposition

Teledyne DALSA Semiconductor



TELEDYNE DALSA Everywhereyoulook™

e2V is now Teledyne!

- We established a hybrid fabrication model with DALSA Semiconductor starting in 2001 (Zarlink/Mitel/DALSA)
- DALSA also supplies CCDs for LSST (STA / U of A)
- LBNL Ge R&D emphasizes possible future collaboration with DALSA, but we need to demonstrate viability as was done with the fully depleted CCD

Outline

- Motivation for Ge CCDs / Facilities for R&D work
- Germanium technological considerations
  - Gate insulator/electrode materials, wafer cleaning
  - Can't just call DALSA and ask for Ge CCDs
- Work in progress
- Deep sub-electron noise with Skipper CCDs
  - Silicon CCD collaboration with FermiLab and others

Germanium: Considerations

- Native gate insulator GeO_2 has good electrical properties, but is water soluble and degrades for post-oxidation temperatures exceeding ~ 400°C

ACS APPLIED MATERIALS & INTERFACES
Research Article
www.acsami.org

Stabilization of the GeO_2/Ge Interface by Nitrogen Incorporation in a One-Step NO Thermal Oxynitridation

Gabriela Copetti,[†] Gabriel V. Soares,[†] and Cláudio Radtke*[,‡]

[†]Instituto de Física and [‡]Instituto de Química, UFRGS, 91509-900 Porto Alegre, Brazil

However, the lack of a stable passivation layer for Ge surface hinders the development of such technology. Unlike silicon dioxide (SiO_2), germanium dioxide (GeO_2) is water-soluble and also thermally unstable at temperatures usually employed during device processing.[2] This instability is due to the interfacial reaction $GeO_2 + Ge \rightarrow 2GeO$ that occurs at temperatures greater than 400 °C. Oxygen vacancies generated at the GeO_2/Ge interface diffuse through the oxide toward the surface, where they promote GeO desorption (as evidenced by thermal desorption spectroscopy[3]), leading to the deterioration of the device's electrical properties.[4] First-principles calculations predicted that

Germanium: Considerations

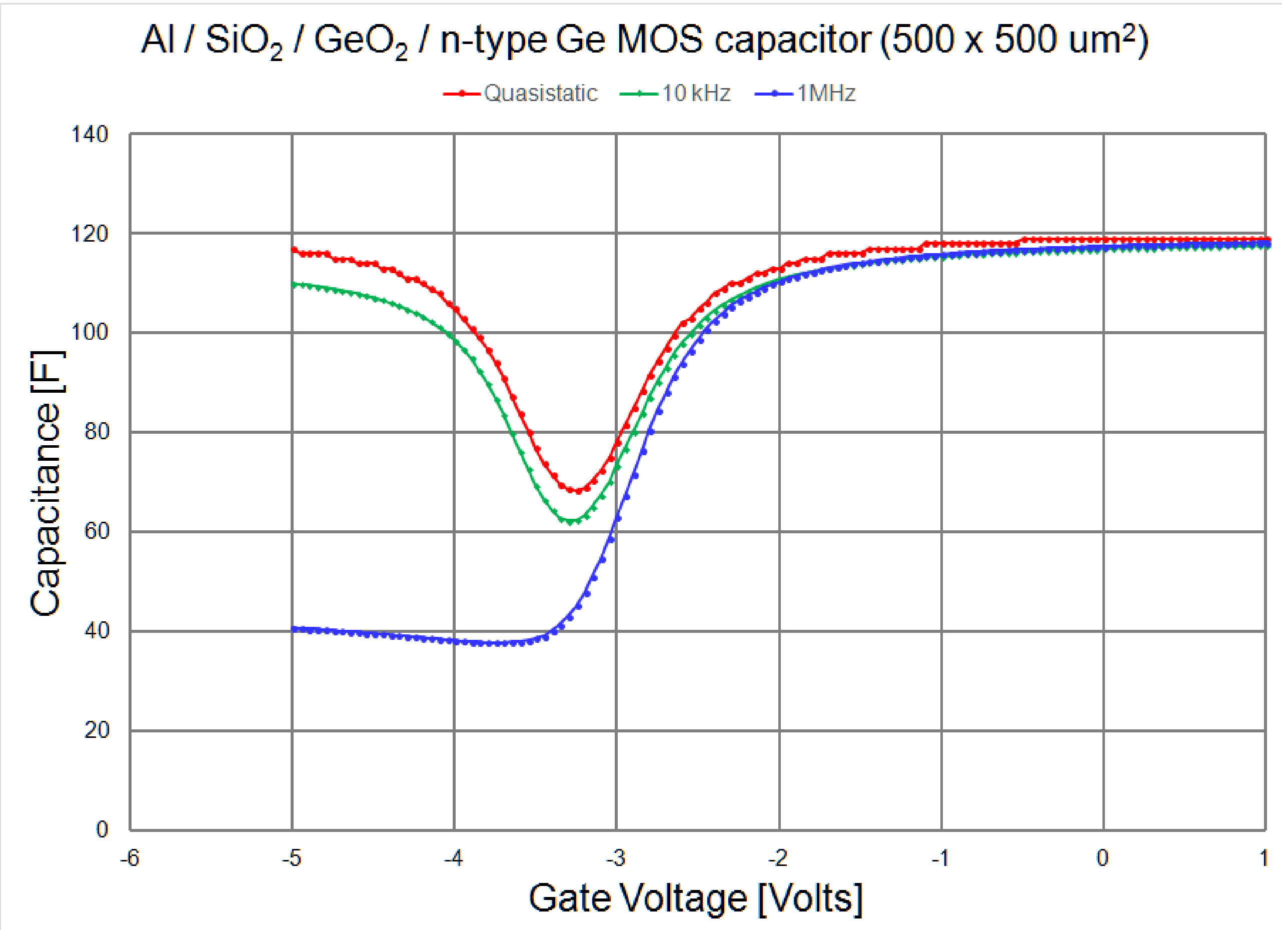
- Water solubility of GeO_2 was considered a show stopper for Ge MOSFETS, but not so much now

- For CCDs, cap with another insulator
  - Silicon CCDs typically use SiO_2 and Si_3N_4
    - » Lincoln Labs approach is thermally-grown GeO_2 capped by Al_2O_3 (high-K using ALD)
    - » We have plasma-enhanced CVD SiO_2 and Si_3N_4 in the MSL as well as access to ALD

- Advanced CMOS: Deposit high-K with ALD

Germanium: Considerations

- Aluminum-gate / SiO_2 / GeO_2 / Ge MOS capacitor
  - Fabricated in the LBNL MicroSystems Laboratory



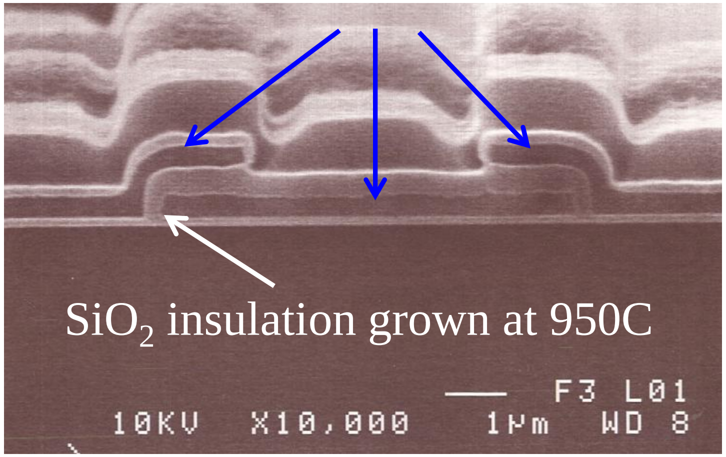
- Capacitance-voltage measurements used to extract information about the quality of the gate insulator
- Good electrical properties in this first attempt
- D_{it} in low 10^{11} cm^{-2}
- Need to demonstrate high yield

Germanium: Considerations

- GeO_2 limitations lead to "Gate-last" process that affects the choice of gate-electrode technology
  - 400C limitation implies low-temperature processing after the GeO_2 is grown
  - Triple-polysilicon works very well for silicon CCDs, but not practical for Ge
  - This low-temperature limitation results in a major paradigm shift in the gate-electrode technology

The virtues of polysilicon for CCDs

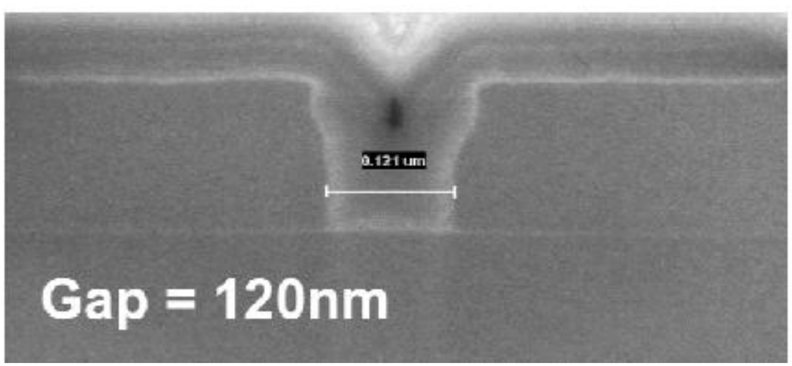
- Silicon CCDs utilize polySi gate electrodes isolated by SiO_2 grown at ~ 950°C (too high for Ge)
- Intra-poly shorts rare (large spacing) and only cause cosmetic defects in the 3-phase, triple-polySi process
- Very narrow gap between electrodes defined by oxidation of the polysilicon (vs lithography and etching)
  - » Excellent charge transfer efficiency (high E_{fringe})



Silicon CCD cross section (arrows point to polysilicon)

Germanium: Considerations

- "Gate-last" process for Ge
  - Single-layer conductor is one approach
    - ~ 100 – 200 nm wide gaps defined by lithography / etching
  - Concern is intra-level shorts
    - 2k x 2k CCD would have 63 m of sensitive length
  - Not unprecedented, single-layer polysilicon under investigation for CCD integration into



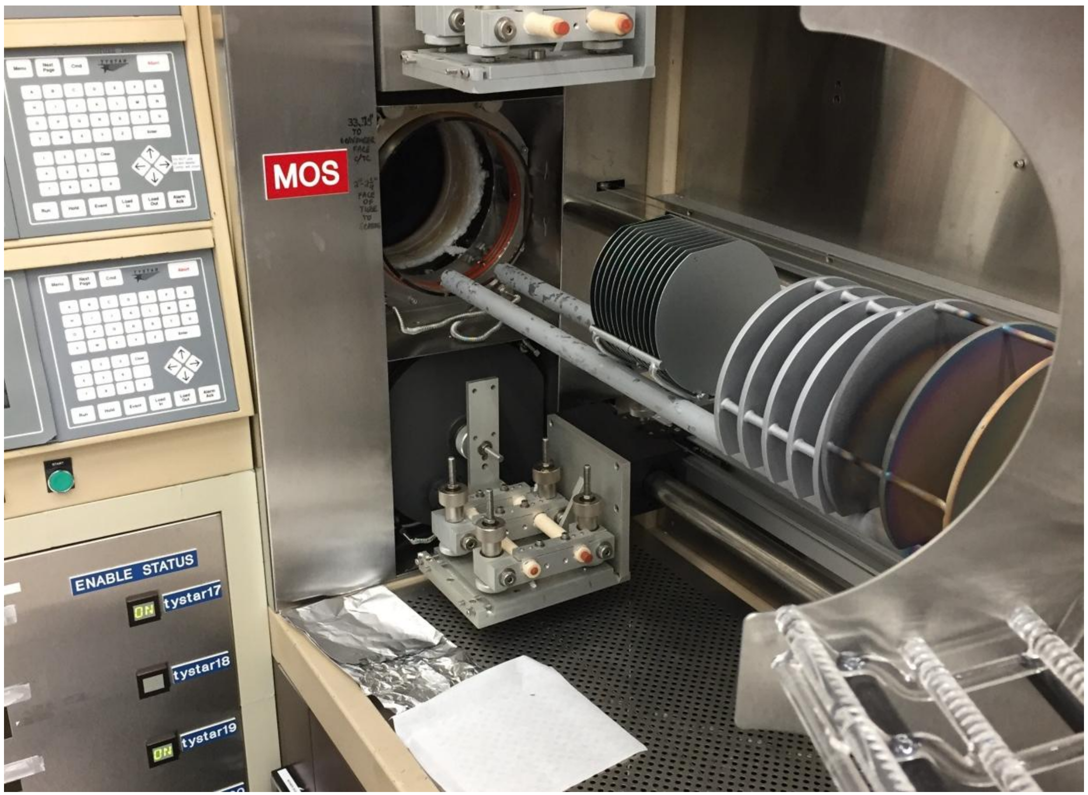
ICSO 2016 **Biarritz, France**
International Conference on Space Optics **18 - 21 October 2016**

HIGH SPEED TDI EMBEDDED CCD IN CMOS SENSOR

P. Boulenc[1], J. Robbelein[1], L. Wu[1], L. Haspeslagh[1], P. De Moor[1], J. Borremans[1], M. Rosmeulen[1]
[1]IMEC, Kapeldreef 75, B-3001 Leuven, Belgium
Email: pierre.boulenc@imec.be, Phone: +32 16 28 15 44

Germanium: Gate electrode R&D

- LBNL "Gate-last" gate-electrode technology
  - We are investigating a conductive, polycrystalline Ge film that can be deposited at low temperatures, e.g. 350°C

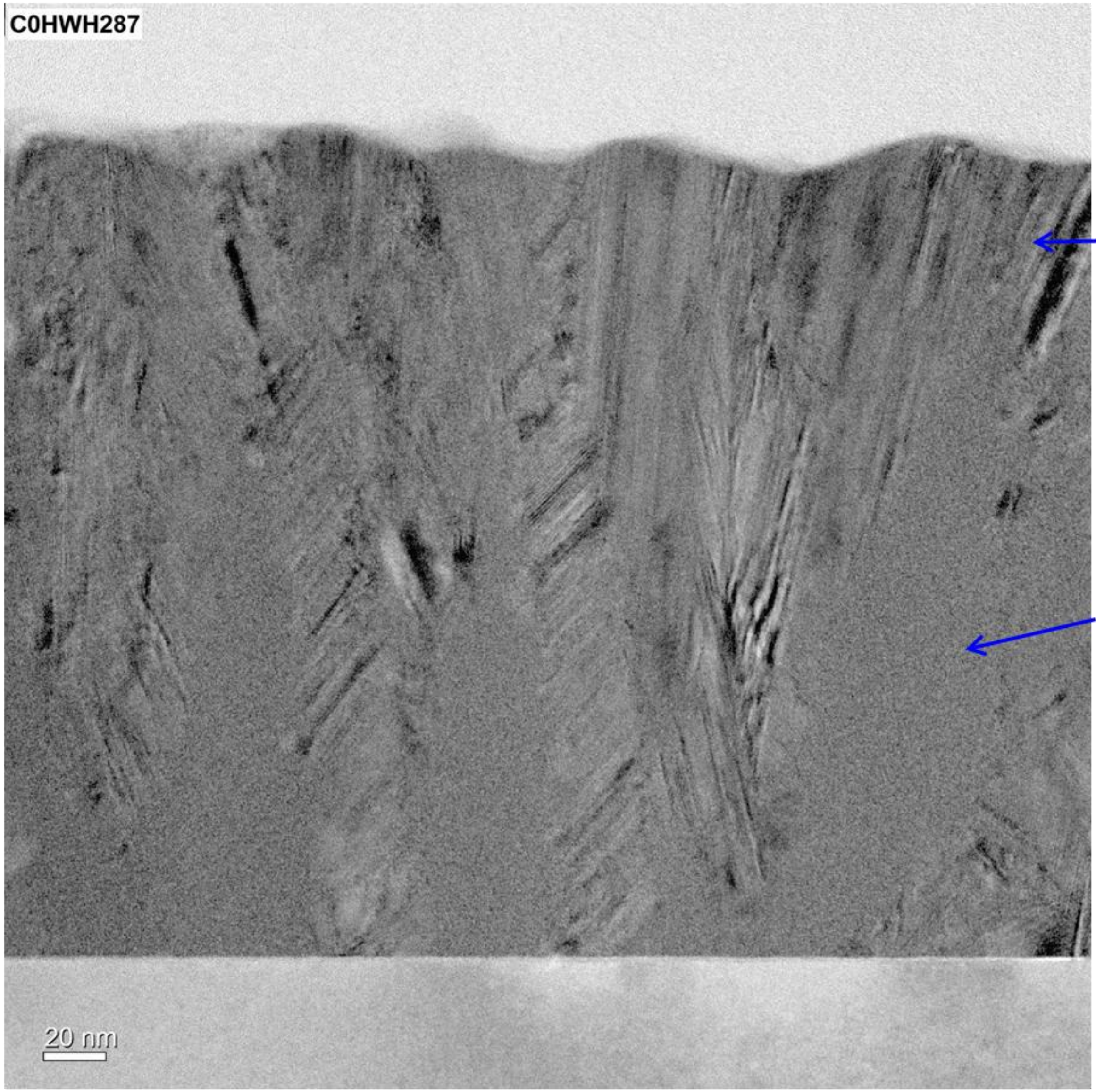


- Conventional low-pressure CVD process similar to polysilicon
- In-situ doped (BCl_3)
- Etching similar to polySi
- DALSA compatible at some point?

UCB Marvell Nanofabrication Laboratory

LPCVD Polycrystalline Germanium

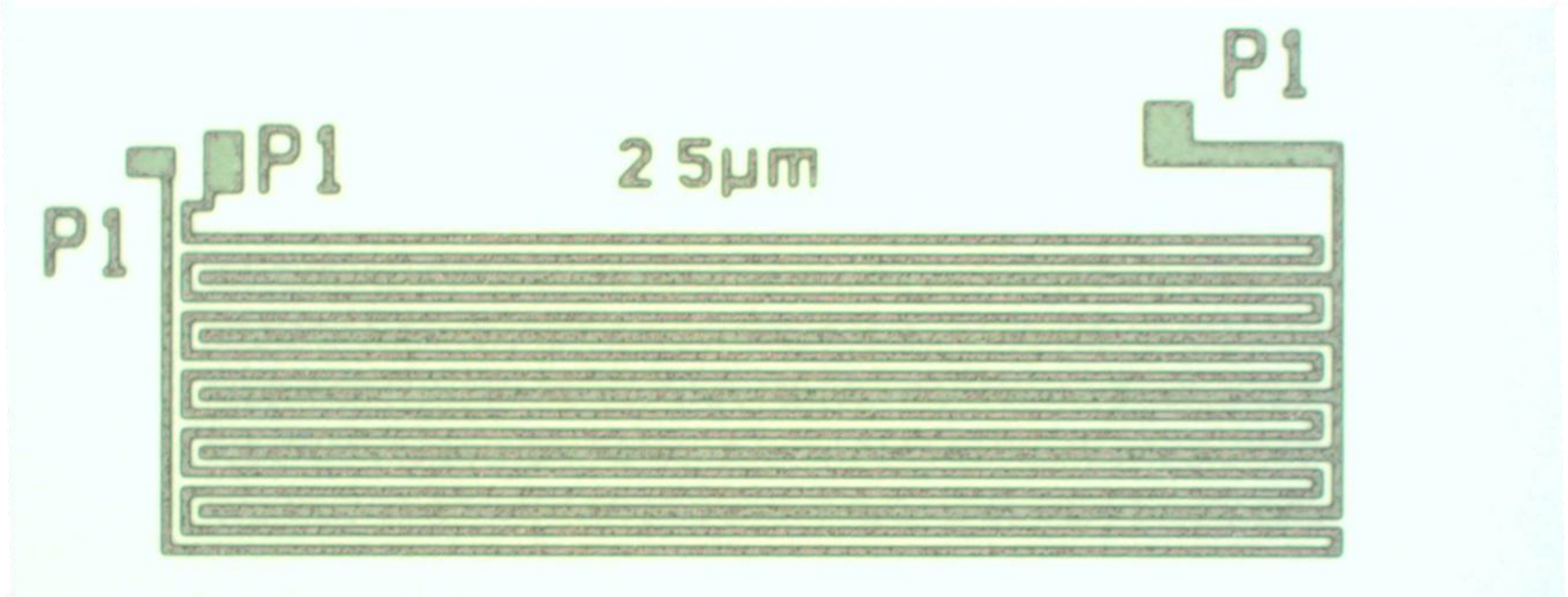
BF TEM image



EAG LABORATORIES | eag.com

LPCVD Polycrystalline Germanium

- Photoresist mask on polyGe on SiO_2 on Silicon
  - » PolyGe deposited at the UC-Berkeley Nanolab
  - » Etch development in progress

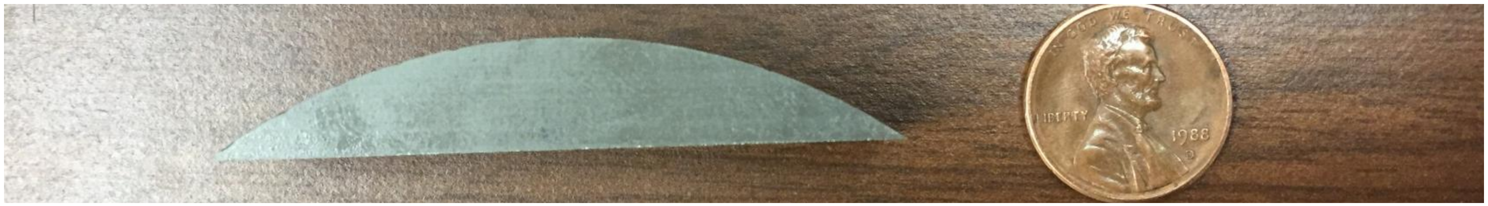


Germanium: Considerations

- Only one viable Ge wafer vendor at present
  - Umicore (Belgium): Excellent so far, can produce 150 and 200 mm diameter Ge
    - » Limited to about 10 ohm-cm (~ 1.5 x 10^{14} cm^{-3})
    - » CCDs are demanding in terms of wafer quality
  - Through the SBIR program we are developing high-purity Ge wafers from γ-ray quality Ge
    - » PHDs Co. Inc awarded SBIR grant
    - » Wafer production from 170 mm ingot in progress
    - » Less impurities -> lower dark current, better CTE

High-purity Germanium

- Sample of Ortec high-purity Ge sent to Lakewood Semiconductors for hole lifetime measurements



Used for double-sided Ge strip detectors (γ-ray detection, courtesy Mark Amman)

Richard Ahrenkiel

to me

Hi Stephen
In the attached document, I have supplied relevant figures and calculations for the Ge samples that you provided.
The bulk lifetime is about 15 ms and the SRV is quite low.
Please get back to me if you have any questions.
Regards

Richard K Ahrenkiel
Lakewood Semiconductors LLC
P. O. Box 260888
Lakewood, CO 80226
303 728-9653
303-949-3797 (cell)
rahren@mac.com
www.mr-lifetime.com

Richard Ahrenkiel

to me

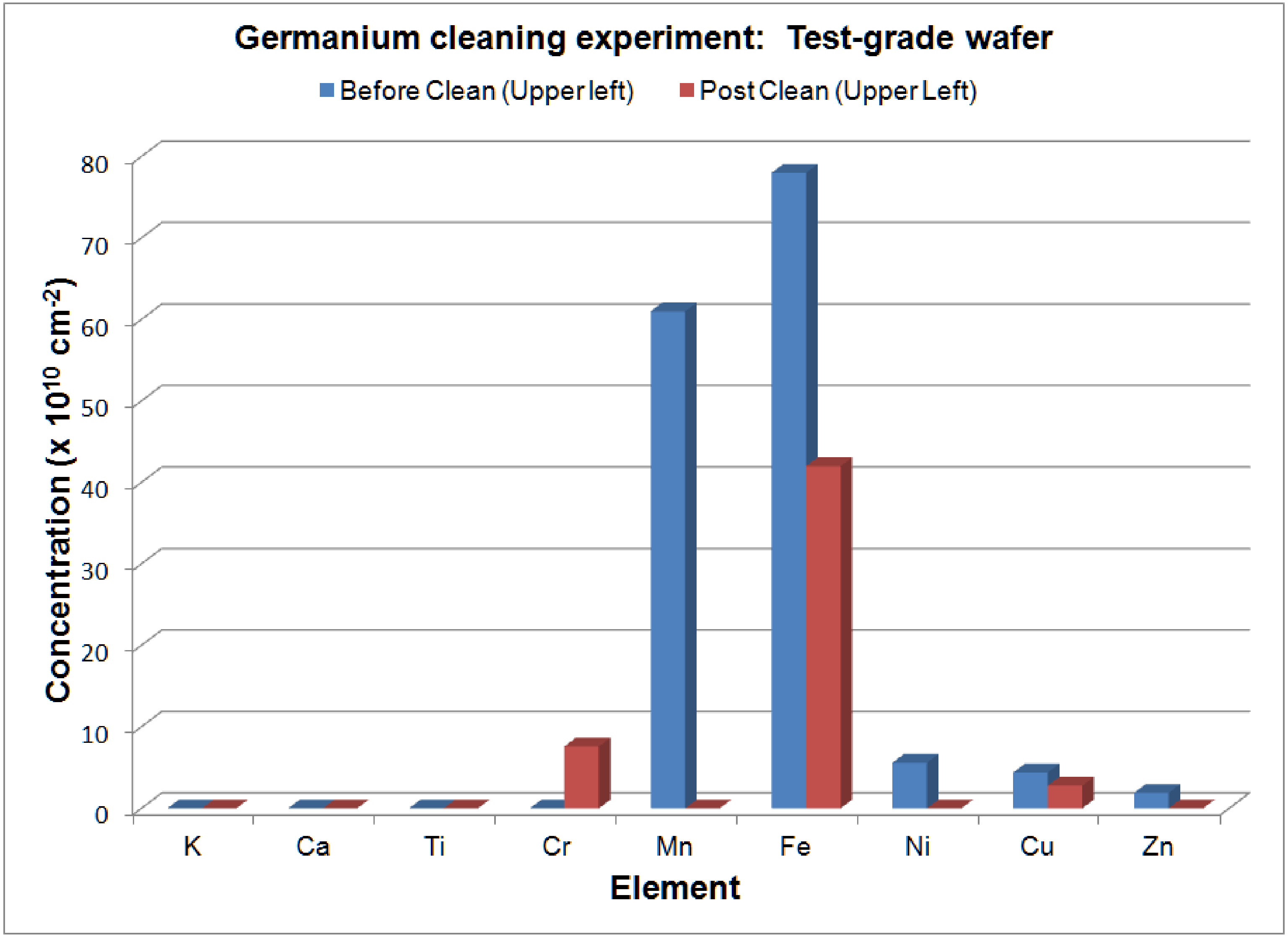
Hi Stephen
I am glad that you liked the work and hope to do more for you.
No, I have never seen a Ge sample with lifetimes like this before.
I measujred several hundred last year and this is quite unique.
Yes, I will send the sample back to you.
Thanks

- Low-ρ Ge lifetime 10's of μsec

Germanium: Considerations

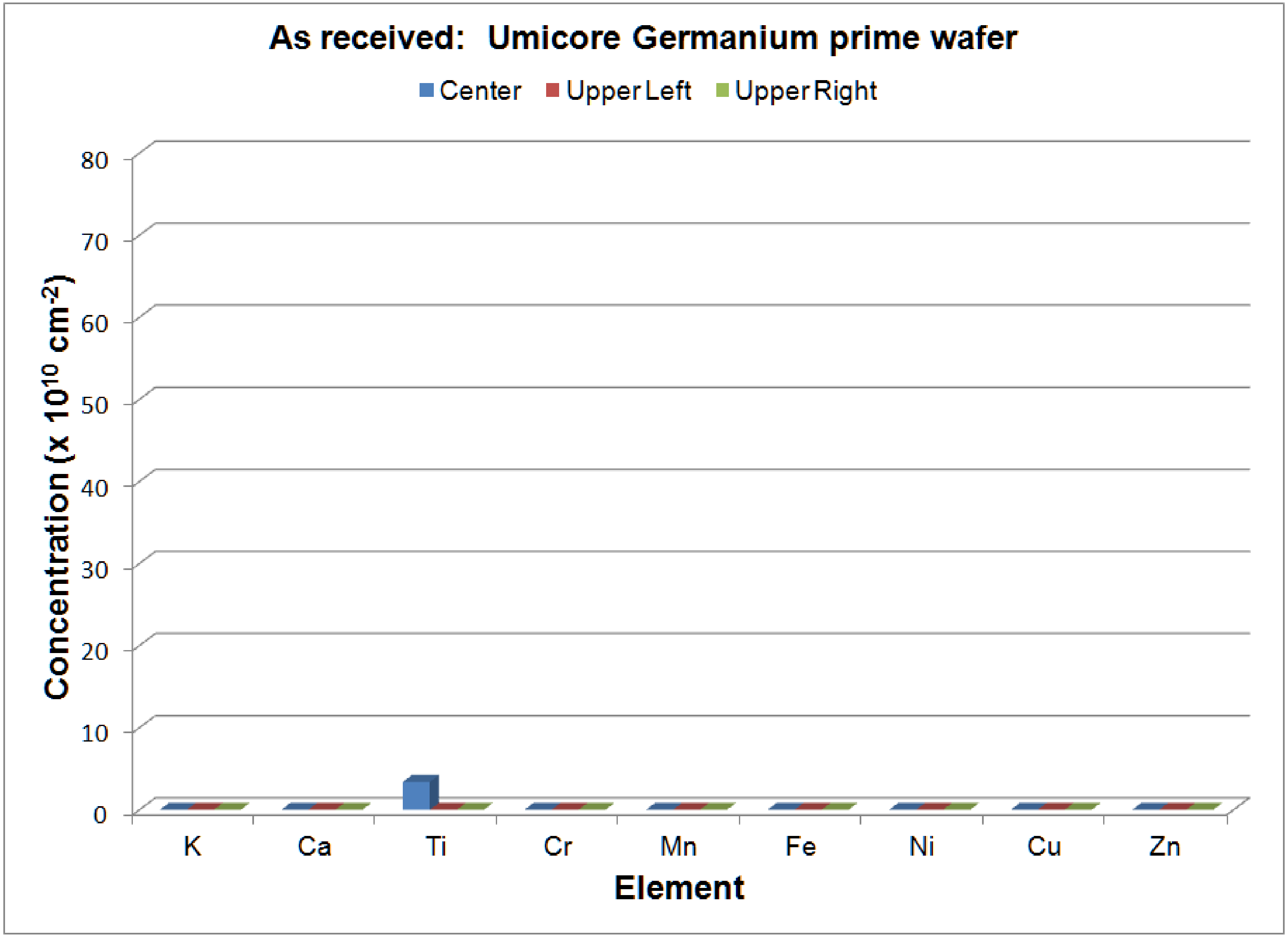
- Water-soluble GeO_2 leads to high etch rates in chemicals typically used in silicon processing
  - Silicon cleans to remove particles and metallic contamination are based on strong oxidizers, e.g. H_2O_2 in the RCA and piranha cleans
  - When Ge is oxidized during a chemical clean, the resulting GeO_2 is etched away leading to high Ge etch rates
  - Requires very dilute chemistries

Germanium cleaning



DALSA cutoff for silicon is 10 x 10^{10} cm^{-2}

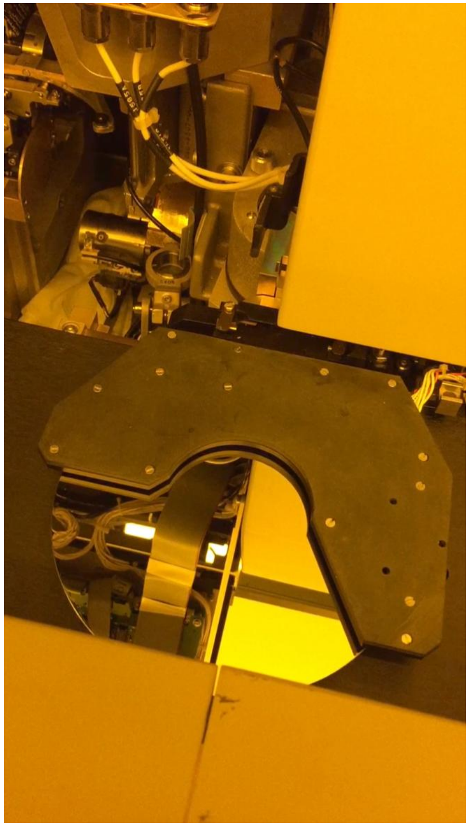
Umicore Germanium

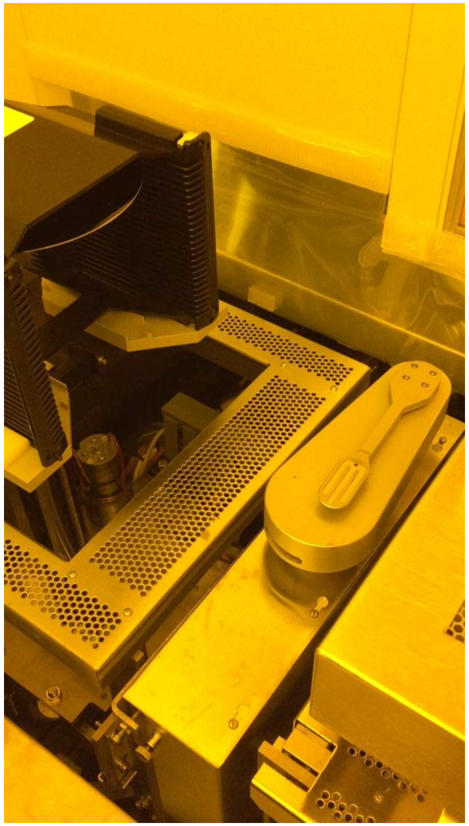


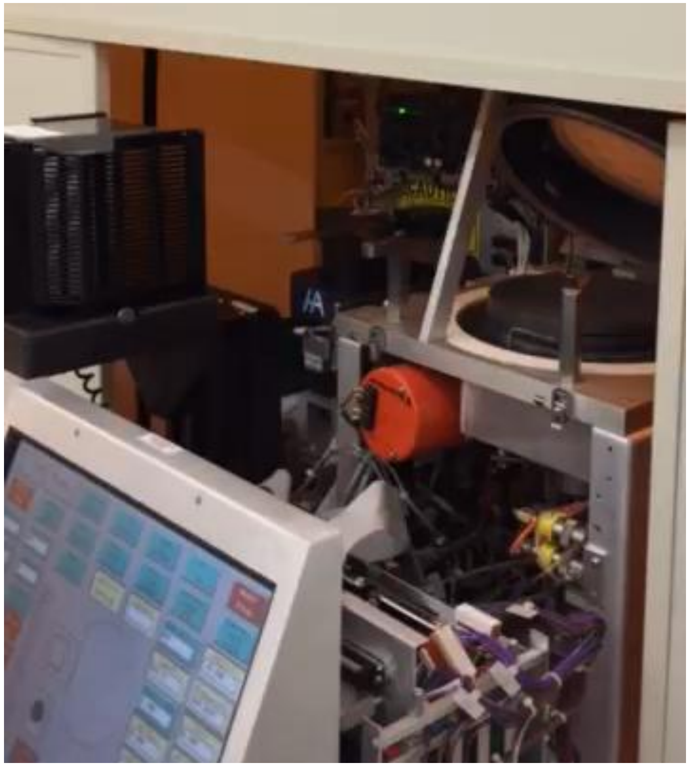
Umicore 10 ohm-cm, n-type Ge wafer for CCD processing: Very clean

Germanium: Practical issues

- Ge wafers are heavy (2.3 x denser than Si)
  - Evaluated 250 and 650 um thick Ge for compatibility with the automated wafer handling equipment in the MicroSystems Laboratory





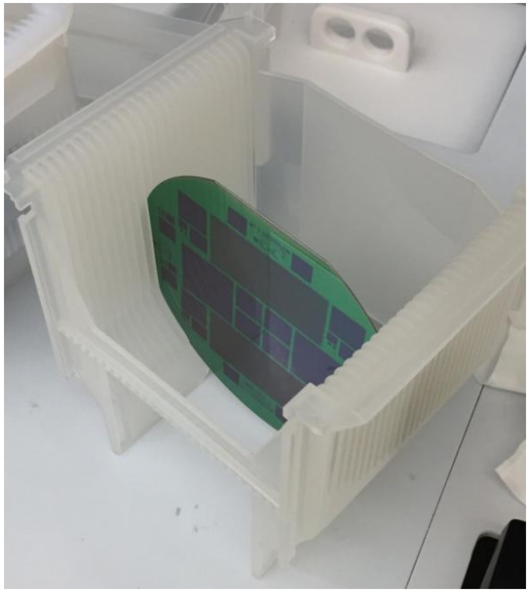


Outline

- Motivation for Ge CCDs / Facilities for R&D work
- Germanium technological considerations
- Work in progress
- Deep sub-electron noise with Skipper CCDs
  - Silicon CCD collaboration with FermiLab and others

LBNL LDRD[1] CCD effort

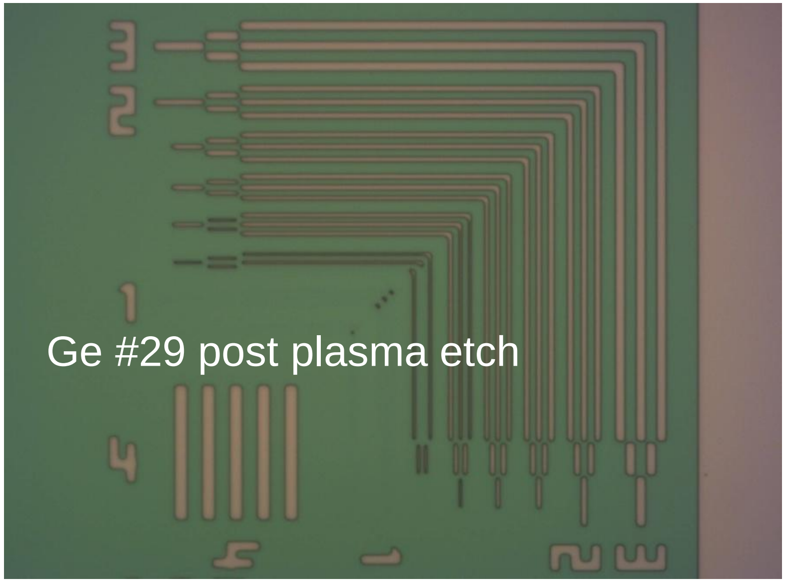
- Develop key components of Ge CCDs
  1) Buried channel MOSFETs on Ge
     - » In progress
  2) Ge-compatible gate electrode
     - » PolyGe doping vs deposition conditions
     - » PolyGe etch development
     - » Single versus multi-layer
- High purity Ge
- CCD process integration

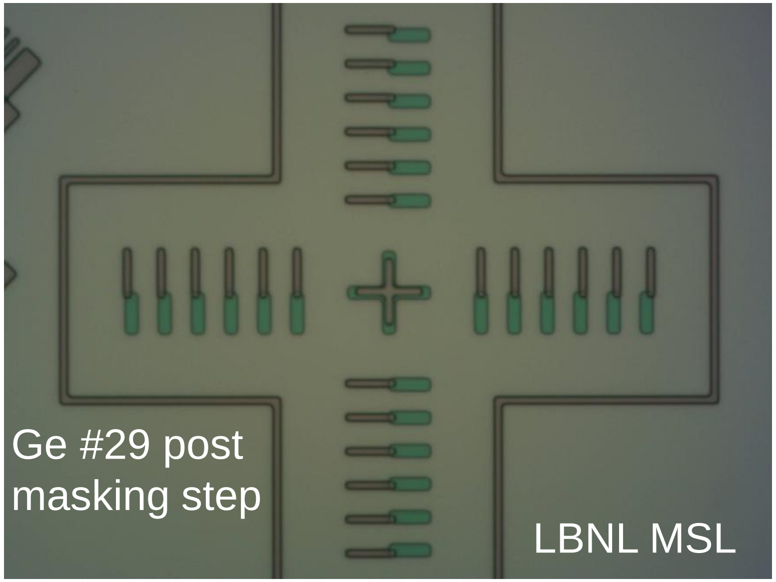


[1]Laboratory Directed R&D (internal LBNL Director's funds from the DOE)

LBNL LDRD[1] CCD effort

- Custom mask set contains many test structures, e.g.
  - » DALSA CCD process control monitors
    - MOS capacitors, contact chains, shorts structures, etc
  - » Structures to extract doping profiles (SRP / SIMS)
  - » In-process aids, e.g. resolution / alignment test structures





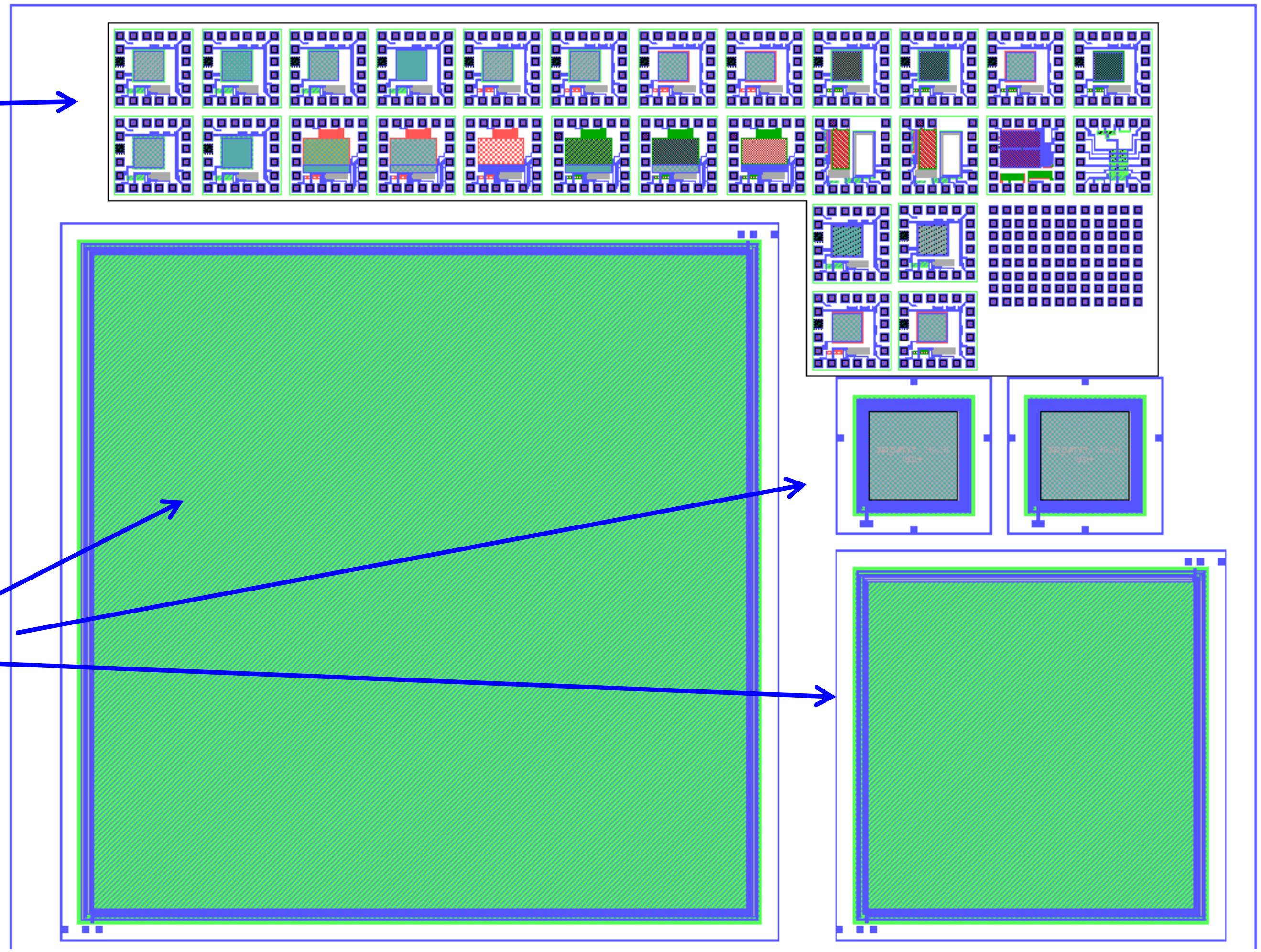
[1]Laboratory Directed R&D (internal LBNL Director's funds from the DOE)

LBNL LDRD[1] CCD effort

- Test structures for technology development

DALSA-style test structures modified for Ge

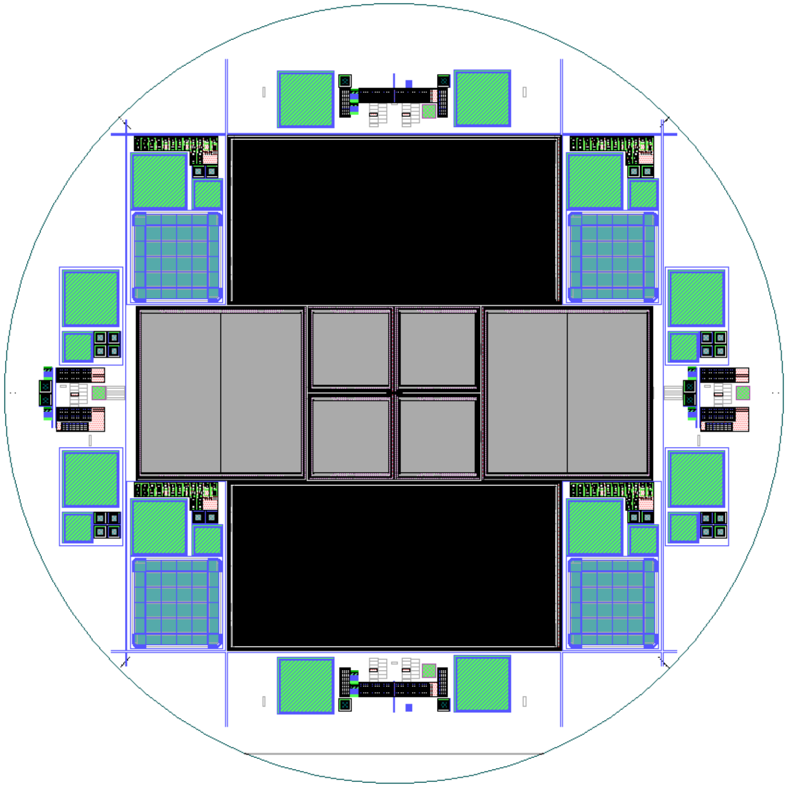
Photodiodes



[1]Laboratory Directed R&D (internal LBNL Director's funds from the DOE)

LBNL LDRD[1] CCD effort

- Custom mask set also includes
  - Large format CCDs for yield studies and (hopefully) near-future (at least partially) functioning CCDs



- Large format CCDs allow us to study yield issues early on
- 4k x 2k CCDs for multi-layer polyGe technology development
  - Etching, inter-polyGe isolation
- 2k x 2k and 1k x 1k CCDs compatible with e-beam and deep UV lithography
- All have 4-corner readout and frame-store clocks for partial CCD functionality (¼ serial / vertical short-free near corner)
- Designed for parallel process development

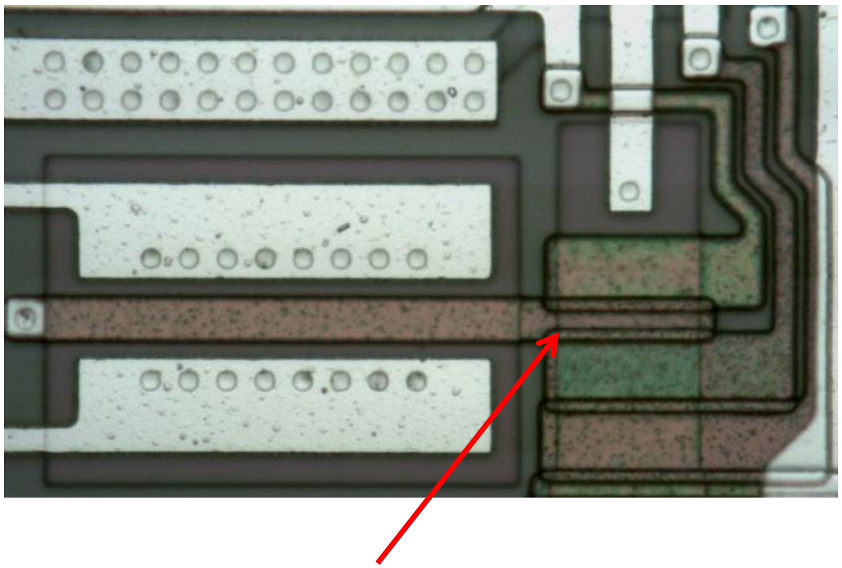
[1]Laboratory Directed R&D (internal LBNL Director's funds from the DOE)

Outline

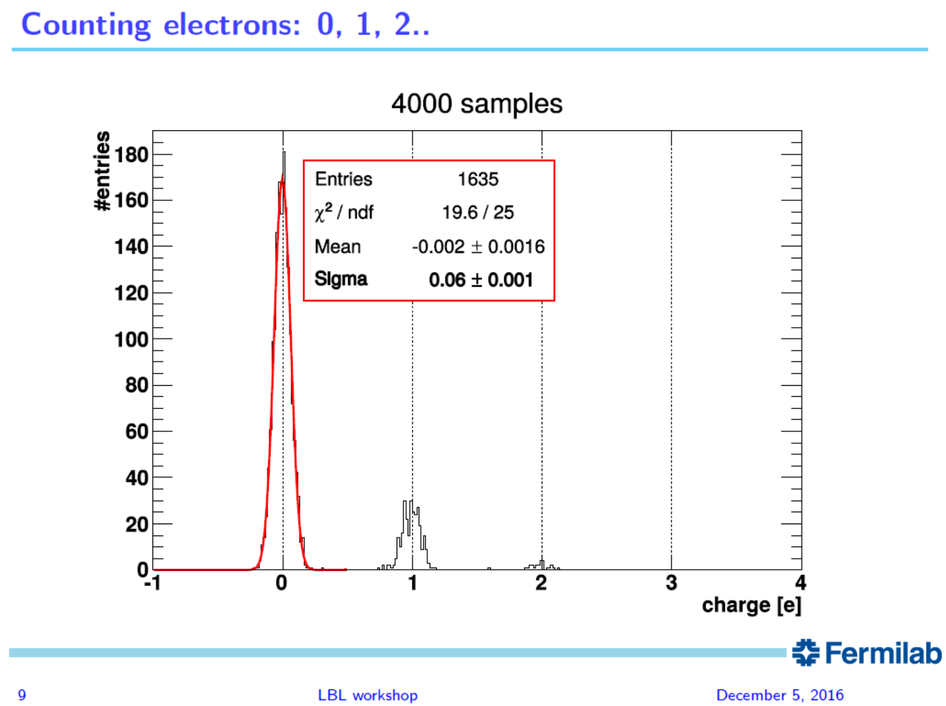
- Motivation for Ge CCDs / Facilities for R&D work
- Germanium technological considerations
- Work in progress
- Deep sub-electron noise with Skipper CCDs
  - Silicon CCD collaboration with FermiLab and others for direct dark matter detection with CCDs
  - Tom Diehl’s talk
  - Future design work on Skipper CCDs at LBNL planned

LBNL / FermiLab development

- Skipper CCD (silicon)



Floating gate



Backup slides

- Gate-last Ge transistor

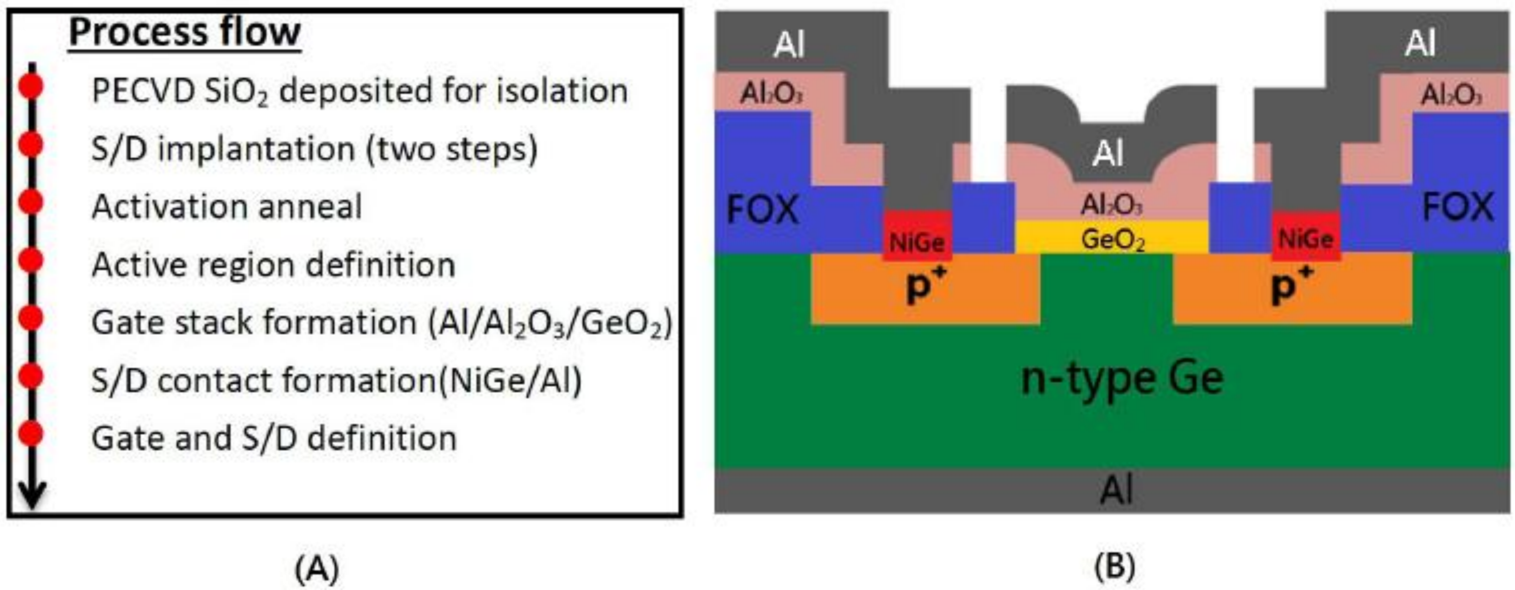
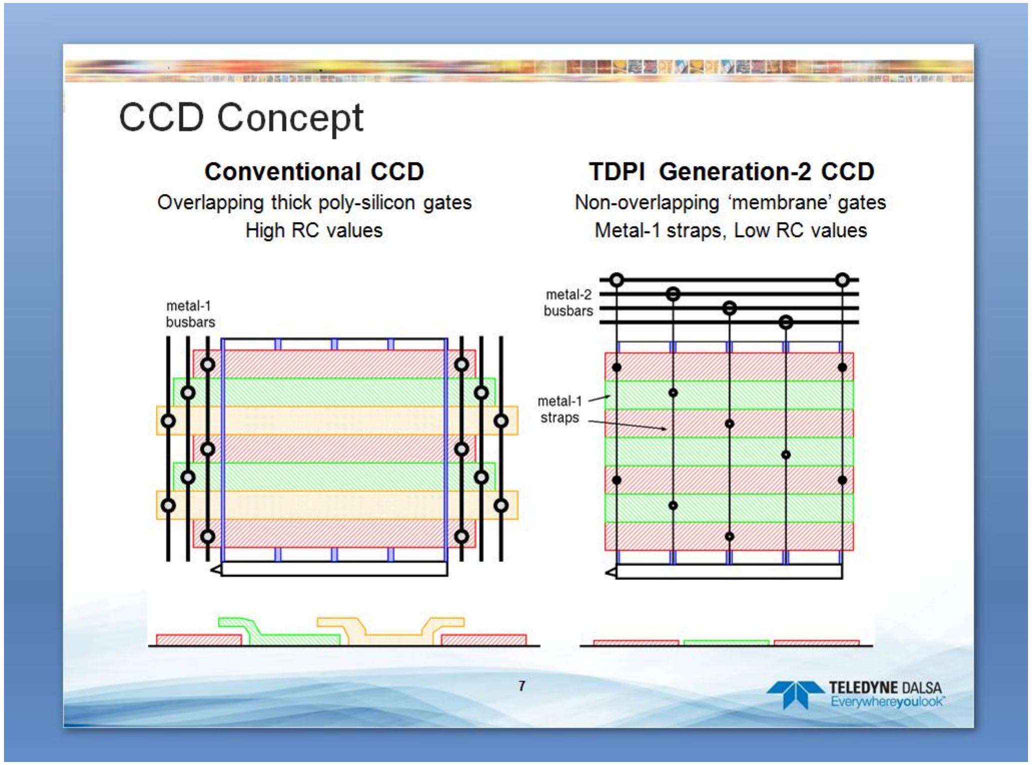


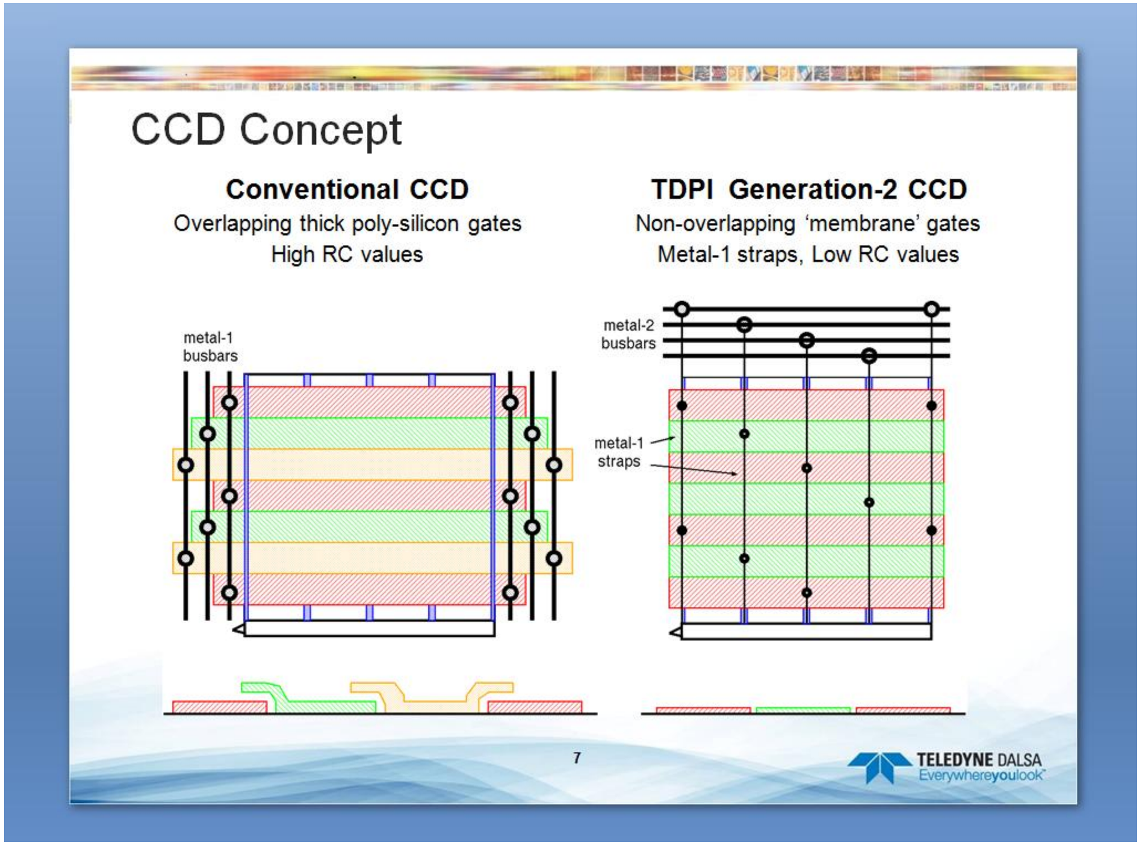
Fig. 1. (a) Gate-last process flow and (b) cross-sectional view of the Ge p-MOSFETs with $Al/Al_2O_3/GeO_2$ gate-stack and NiGe S/D contact.

DALSA single vs triple polysilicon

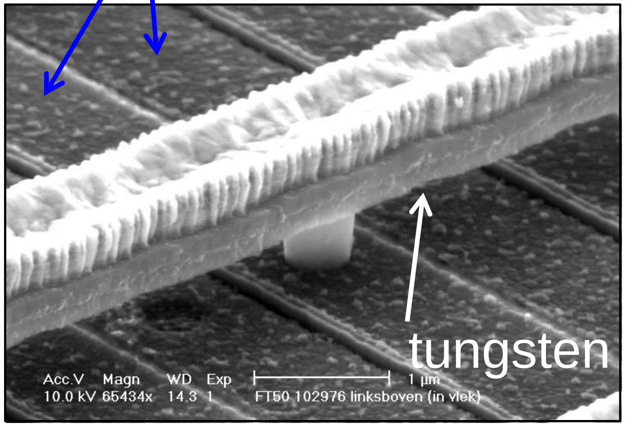
– Single-layer gate electrode with sub-μm gaps versus triple-poly overlapping gates



DALSA single vs triple polysilicon



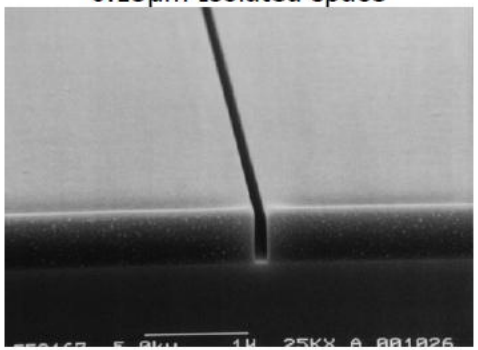
Non-overlapping polysilicon electrodes



E-beam lithography

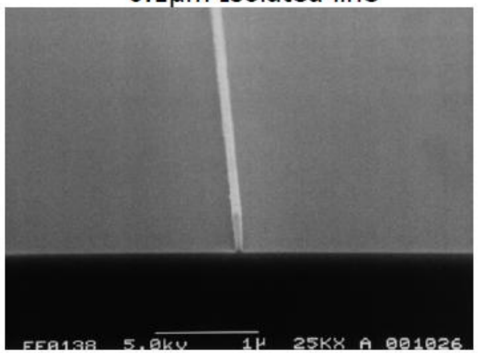
7. Examples of application

0.15μm Isolated space



Process Conditions
Resist : ZEP520
Film thickness : 5000 Å
PB temp. : 180℃
PB time : 2min.
Exposure : 30kV, 5 × 10^{-11}A, 1 line exp.
50 × 10^{-5}μC/cm
Dev. temp. : ZED-WN(end of sale),
23℃, 30sec.
Rinse : IPA, 23℃, 20sec.

0.1μm Isolated line



Process Conditions
Resist : ZEP520
Film thickness : 5000 Å
PB temp. : 180℃
PB time : 2min.
Exposure area :100μm□(20000 × 20000dot)
Exposure : 30kV, 5 × 10-11A, 1 line exp.
0.7μsec./dot
Dev. temp. : ZED-WN(end of sale),
23℃, 60sec.
Rinse : IPA, 23℃, 20sec.

Advertising brochure for ZEP520A photoresist, one of the e-Beam lithography resists used in the Molecular Foundry

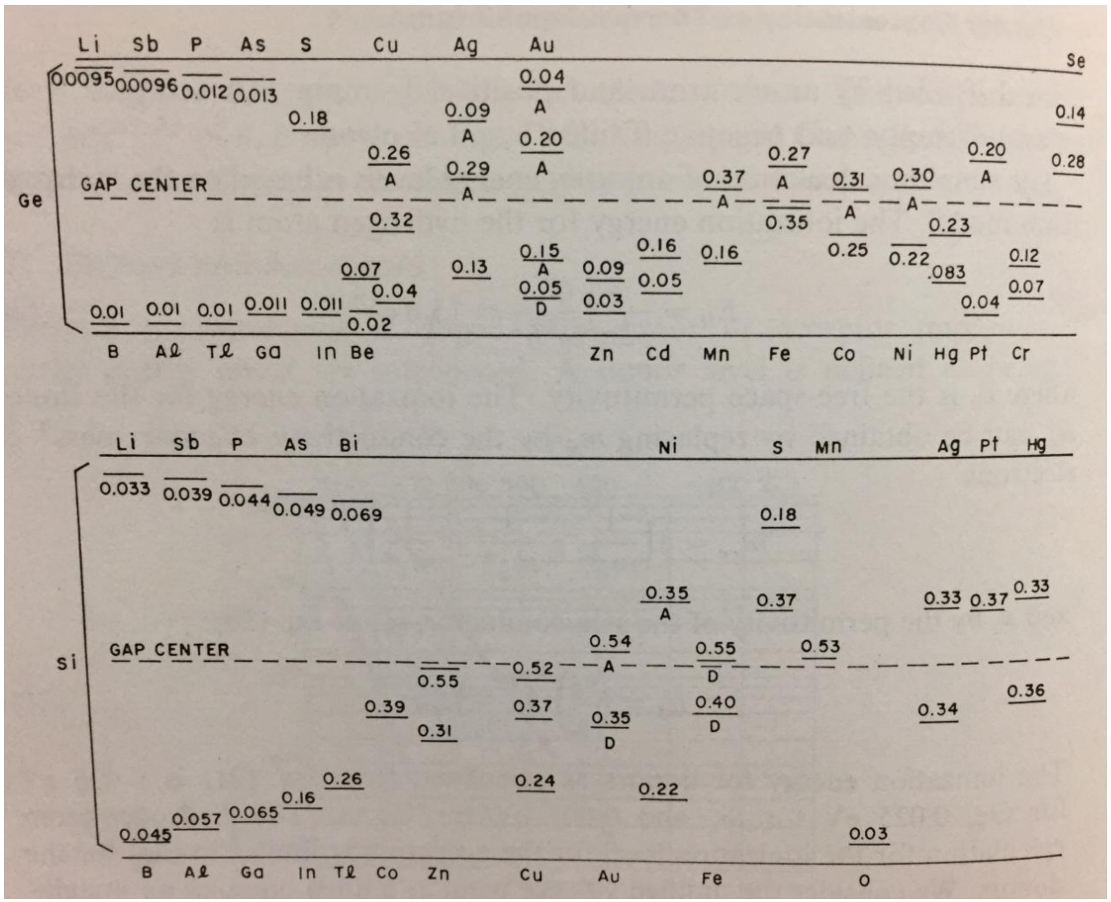
Germanium CCDs

Table 1. Comparison of some basic properties of Si, Ge, and GaAs at 300 K.

Properties	Si	Ge	GaAs
Atoms/cm^3	5.02×10^{22}	4.42×10^{22}	4.42×10^{22}
Atomic weight	28.09	72.6	144.63
Breakdown field (V/cm)	$\sim 3 \times 10^5$	$\sim 1 \times 10^5$	$\sim 4 \times 10^5$
Crystal structure	Diamond	Diamond	Zincblende
Density (g/cm^3)	2.329	5.326	5.317
Dielectric constant	11.9	16.0	13.1
Effective density of states in conduction band, N_c (cm^{-3})	2.86×10^{19}	1.04×10^{19}	4.7×10^{17}
Effective density of states in valance band, N_v (cm^{-3})	1.04×10^{19}	6.0×10^{18}	7.0×10^{18}
Optical phonon energy (eV)	0.063	0.037	0.035
Effective mass (conductivity)			
Electrons (m_n/m_o)	0.26	0.082	0.067
Holes (m_p/m_o)	0.69	0.28	0.57
Electron affinity, χ (V)	4.05	4.0	4.07
Energy gap (eV)	1.12	0.67	1.42
Intrinsic carrier concentration (cm^{-3})	1.45×10^{10}	2.4×10^{13}	1.8×10^6
Intrinsic resistivity (Ω-cm)	2.3×10^5	47	10^8
Lattice constant (Å)	5.431	5.646	5.653
Melting point (°C)	1415	937	1240
Minority carrier lifetime (s)	2.5×10^{-3}	10^{-3}	$\sim 10^{-8}$
Mobility (cm^2/V·s)			
Electron (μ_n)	1,500	3900	8,500
Holes (μ_p)	450	1900	450
Thermal diffusivity (cm^2/s)	0.9	0.36	0.24
Thermal conductivity (W/cm-°C)	1.5	0.6	0.46
Coef. Linear expansion (K^{-1})	2.5×10^{-6}	5.7×10^{-6}	5.9×10^{-6}

Germanium CCDs

- Energy levels in Ge and Si
  - $E_A - E_V$ (boron) = 0.01 / 0.045 Ge / Si



NUCLEAR INSTRUMENTS AND METHODS 54 (1967) 308–310; © NORTH-HOLLAND PUBLISHING CO.

GERMANIUM FET – A NOVEL ELEMENT FOR LOW-NOISE PREAMPLIFIERS*

E. ELAD and M. NAKAMURA

Lawrence Radiation Laboratory, University of California, Berkeley, California, U.S.A.

Received 18 July 1967

PERGAMON

Solid-State Electronics 44 (2000) 937–940

SOLID-STATE ELECTRONICS

Germanium junction field effect transistor for cryogenic applications

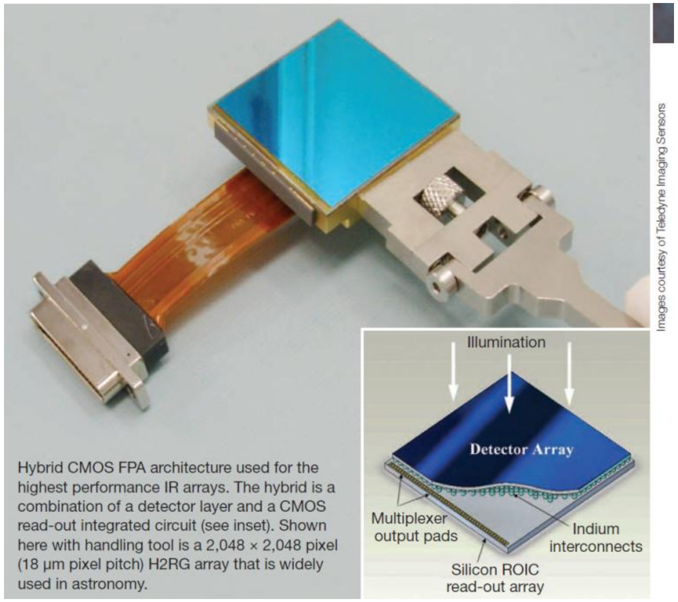
N.C. Das [a,*], C. Monroy [a], M. Jhabvala [b]

[a] *Raytheon/ITSS, 4400 Forbes Boulevard, Lanham, MD 20706, USA*
[b] *Solid State Device Branch, NASA/Goddard Space Flight Center, Code 553, Greenbelt, MD 20771, USA*

Received 15 December 1999; accepted 6 January 2000

Competition: Bump bonded HgCdTe / InSb

- State of the art: Keck MOSFIRE / 2.5 µm cutoff
  - Larger wavelength reach than Ge

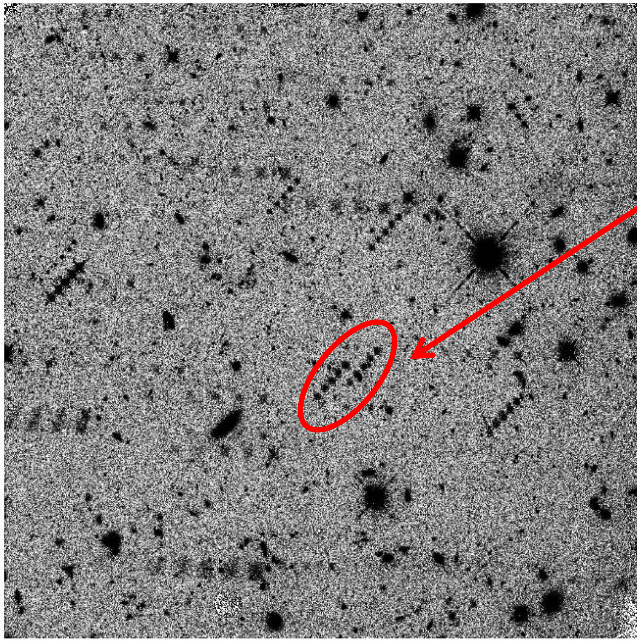


- Expensive
  - Bump bonded process
  - 4 Mpixel imagers cost $300 – 350k each
  - Gigapixel camera approaching $100M in detectors

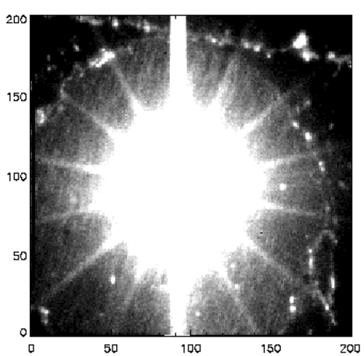
Competition: Bump bonded HgCdTe / InSb

- Conversion of charge to voltage on detector substrate has drawbacks compared to CCDs
  - Lack of double-correlated sampling / higher noise
    - » Keck MOSFIRE
    - » 2048 x 2048, 4.9 e- noise for Fowler 16
      - McLean, 2013 Scientific Detectors Workshop
  - Complicated point spread function due to capacitive coupling between pixels on the detector substrate
    - » DOE DE imaging experiments (DES / LSST) have substantial weak gravitational lensing components

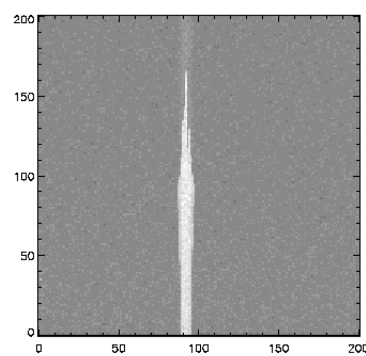
Competition: Bump bonded HgCdTe / InSb



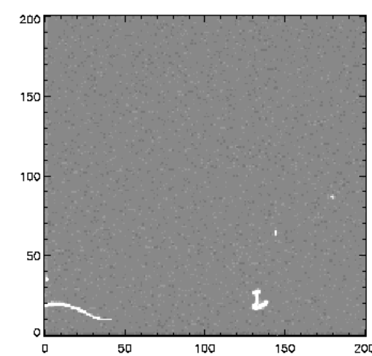
- Persistence in infrared detectors
  - Residual features from images taken 2-5 hours earlier
    - Hubble Space Telescope Wide Field Camera 3
    - Long et al, SPIE 8442, 2012
    - Straightforward to fix in CCDs



Saturating exposure



Persistent image



Erased image

Germanium: Practical concerns

H554 *Journal of The Electrochemical Society*, **155** (7) H552-H561 (2008)

Table I. Bulk Ge wet etch rates for a variety of wet chemistries. Etch rates are at room temperature unless otherwise noted. Composition is indicated in volume mixing ratios. The individual liquid components were at "commercial strength," i.e., CH_3COOH 100%, HBr 48%, HCl 37%, HF 49%, HNO_3 69%, H_3PO_4 85%, H_2SO_4 96%, NH_4OH 25%, and H_2O_2 30%, unless otherwise specified.

Wet chemistry	n-Ge (nm/min)	p-Ge (nm/min)	Etch Time
Water			
H_2O	0.0053	0.0065	60.5 h
H_2O (bubbling N_2)	0.00		Ref. 24
H_2O (bubbling O_2)	0.005		Ref. 24
H_2O (bubbling O_3)	4		Ref. 24
H_2O at 70°C	0.1	0.2	60 min
Acids			
Acetic acid [CH_3COOH]		<0.002	47.5 h
Hydrobromic acid [HBr] (bubbling N_2)	0.01		Ref. 24
HBr (bubbling O_2)	0.02		Ref. 24
Hydrochloric acid [HCl] (1 M)	<0.005	<0.004	17 h
HCl (bubbling N_2)	0.00		Ref. 24
HCl (bubbling O_2)	0.004		Ref. 24
Hydrofluoric acid [HF] (10%)	<0.006	<0.0012	60 h
HF (bubbling N_2)	0.00		Ref. 24
HF (bubbling O_2)	0.00		Ref. 24
Nitric acid [HNO_3] (1 M)		<0.01	20.5 h
Phosphoric acid [H_3PO_4] (1 M)		<0.002	47.5 h
Sulfuric acid [H_2SO_4]		<0.1	3 h
HF/HCl (0.5%/1 M)	<0.004	<0.010	19 h
Buffered Oxide Etch (7:1)	<0.0012	<0.006	1 h
$HF/HNO_3/H_2O$:1/1/1		744	5 min
Aqua regia [HCl/HNO_3:3/1]		290	5 min
H_3PO_4/HNO_3:3/1		3.6	30 min
Bases			
NH_4OH (1 M)	0.32	0.25	105 min
H_2O_2 solutions			
H_2O_2/H_2O:1/10	22	17	1.5 min
H_2O_2/H_2O:1/9	40		Ref. 24
$NH_4OH/H_2O_2/H_2O$:0.1/1/5000		1.25[a]	Ref. 29
$NH_4OH/H_2O_2/H_2O$:1/1/5000	N/A	3	10 min
$NH_4OH/H_2O_2/H_2O$:10/1/5000		2.6[a]	Ref. 29
$NH_4OH/H_2O_2/H_2O$:1000/1/5000		1.31	3 h
$NH_4OH/H_2O_2/H_2O$:1/10/5000	17 (Exp no. 1)	18 (Exp no. 1) 29 (Exp no. 2)	10 min
$NH_4OH/H_2O_2/H_2O$:1/10/5000		16.9[a]	Ref. 29
$NH_4OH/H_2O_2/H_2O$:0.1/100/5000		14.1[a]	Ref. 29
$NH_4OH/H_2O_2/H_2O$:10/100/5000		99.7[a]	Ref. 29
$NH_4OH/H_2O_2/H_2O$:1/7/40	210	230	1.5 min
$HCl/H_2O_2/H_2O$:1/1/7	171	144	1.5 min
$HCl/H_2O_2/H_2O$:50/1/5000, pH 1.3	3.7		5 min
$HCl/H_2O_2/H_2O$:0.5/1/5000, pH 3.1	3.3		5 min
$HCl/H_2O_2/H_2O$:5/10/5000, pH 2.0	23		5 min
$HCl/H_2O_2/H_2O$:0.5/100/5000, pH 2.9	92		5 min
$HCl/H_2O_2/H_2O$:50/100/5000, pH 1.0	94		5 min
H_2SO_4/H_2O_2:1/4	136	132	2 min
Organic-containing solutions			
Acetone	<0.004	<0.004	5.5 h
Isopropanol [IPA]	<0.004	<0.004	19 h
Methyl isobutyl ketone [MIBK]/IPA:1/2	<0.004	<0.004	19 h
OPD 262 (FFEM)	<0.1		75 min
Microstrip 2001 (FFEM)	<0.01	<0.01	165 min
EKC 265 at 65°C (EKC)	9.2		20 min

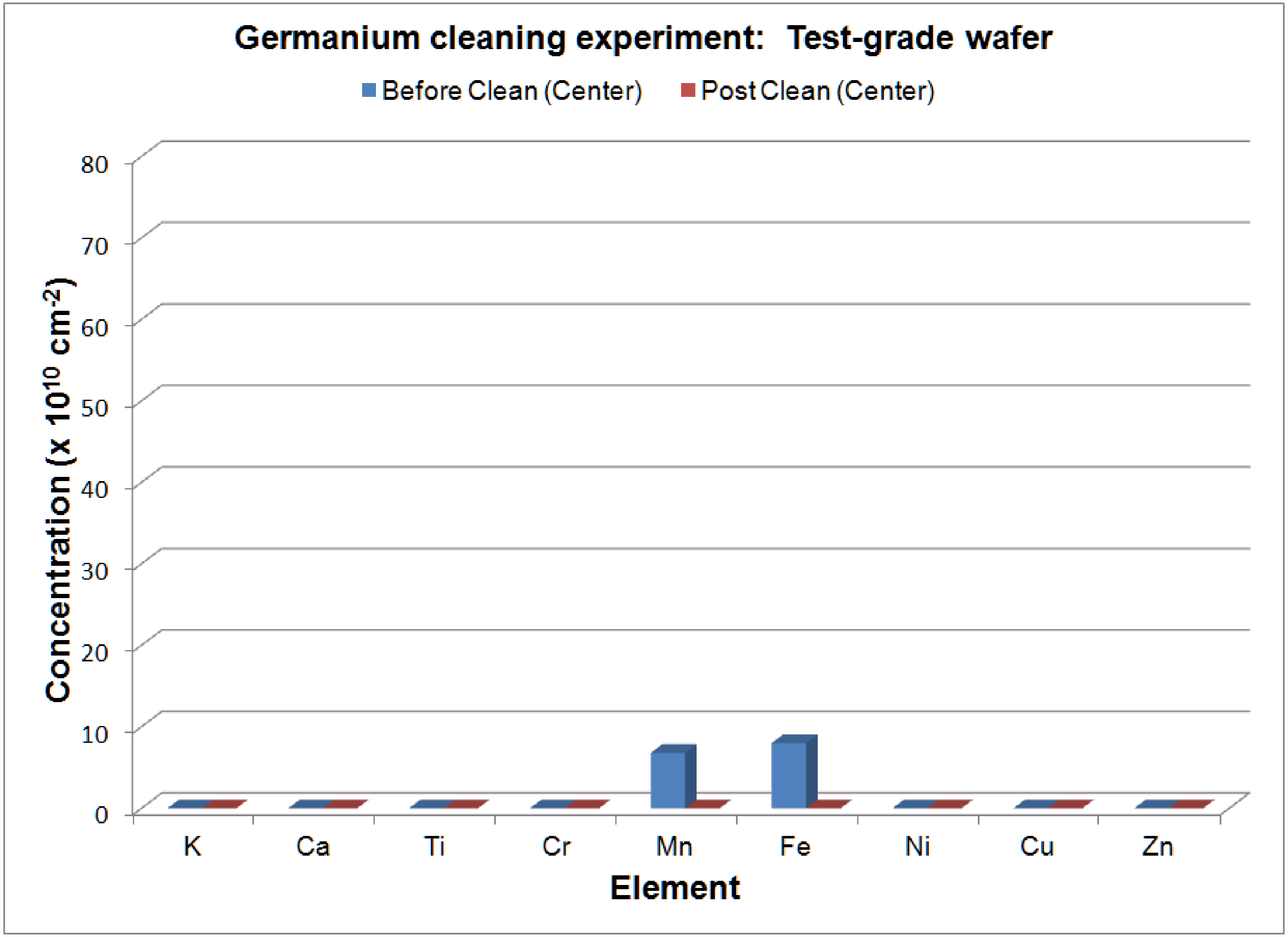
[a] Ge wafer type not recorded.

Wet chemistry	n-Ge (nm/min)	p-Ge (nm/min)
H_2O at 70°C	0.1	0.2

- We used
  1/1/5000 $NH_4OH/H_2O_2/H_2O$ for organics/particles
    - Silicon clean is 1/1/5

  1/200 HF/H_2O for metals
    - Silicon clean would use 1/1/5 $HCl/H_2O_2/H_2O$

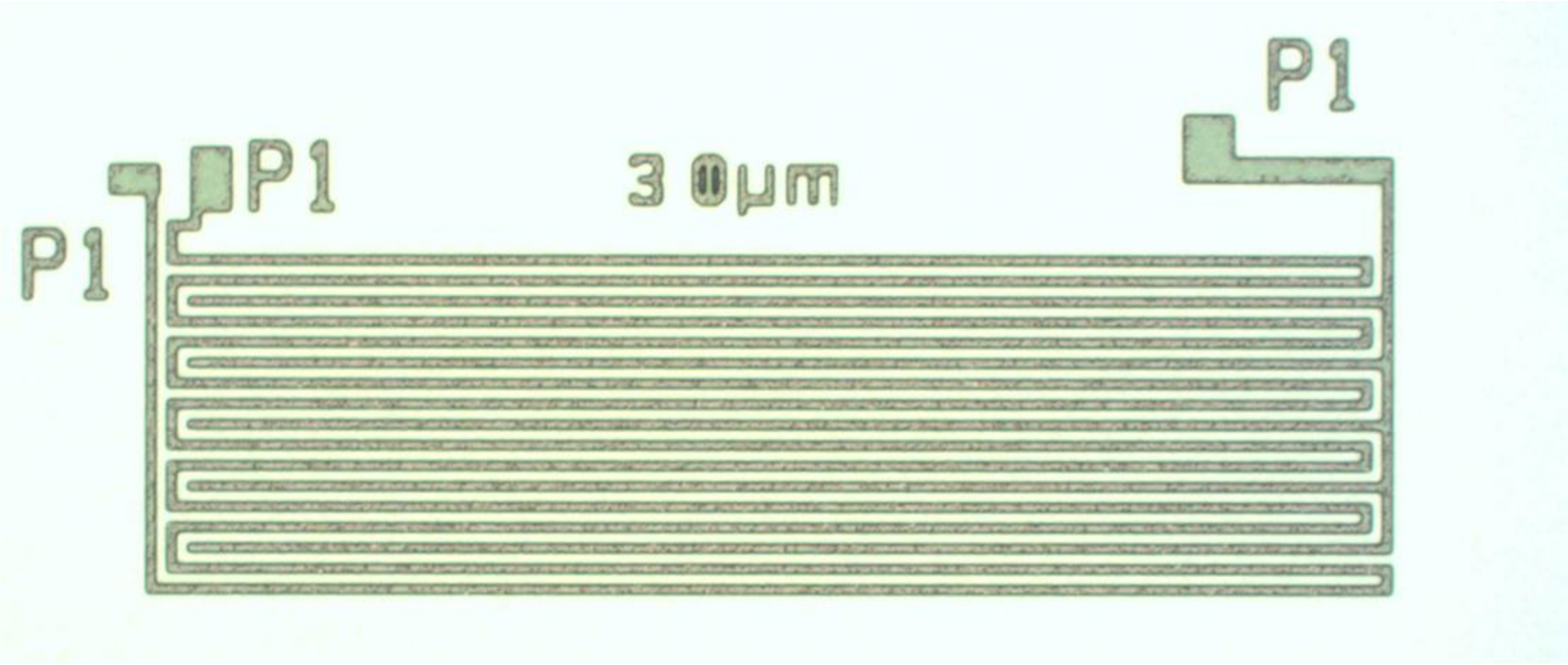
Germanium: Practical concerns



Same wafer as previous slide, different location

LBNL LDRD[1] CCD effort

- Test structures for technology development
  - Photoresist mask on polyGe on SiO_2 on Silicon
  - Example of intra-polyGe shorts test structure
    - » 3 um gap in this case



[1]Laboratory Directed R&D (internal LBNL Director's funds from the DOE)