CMOS Image Sensors and Prospects for High-Speed Applications

DARTMOUTH

Eric R. Fossum

September 14, 2018

ULITIMA 2018

Argonne National Laboratory

THAYER SCHOOL OF ENGINEERING AT DARTMOUTH

Where is Dartmouth College?

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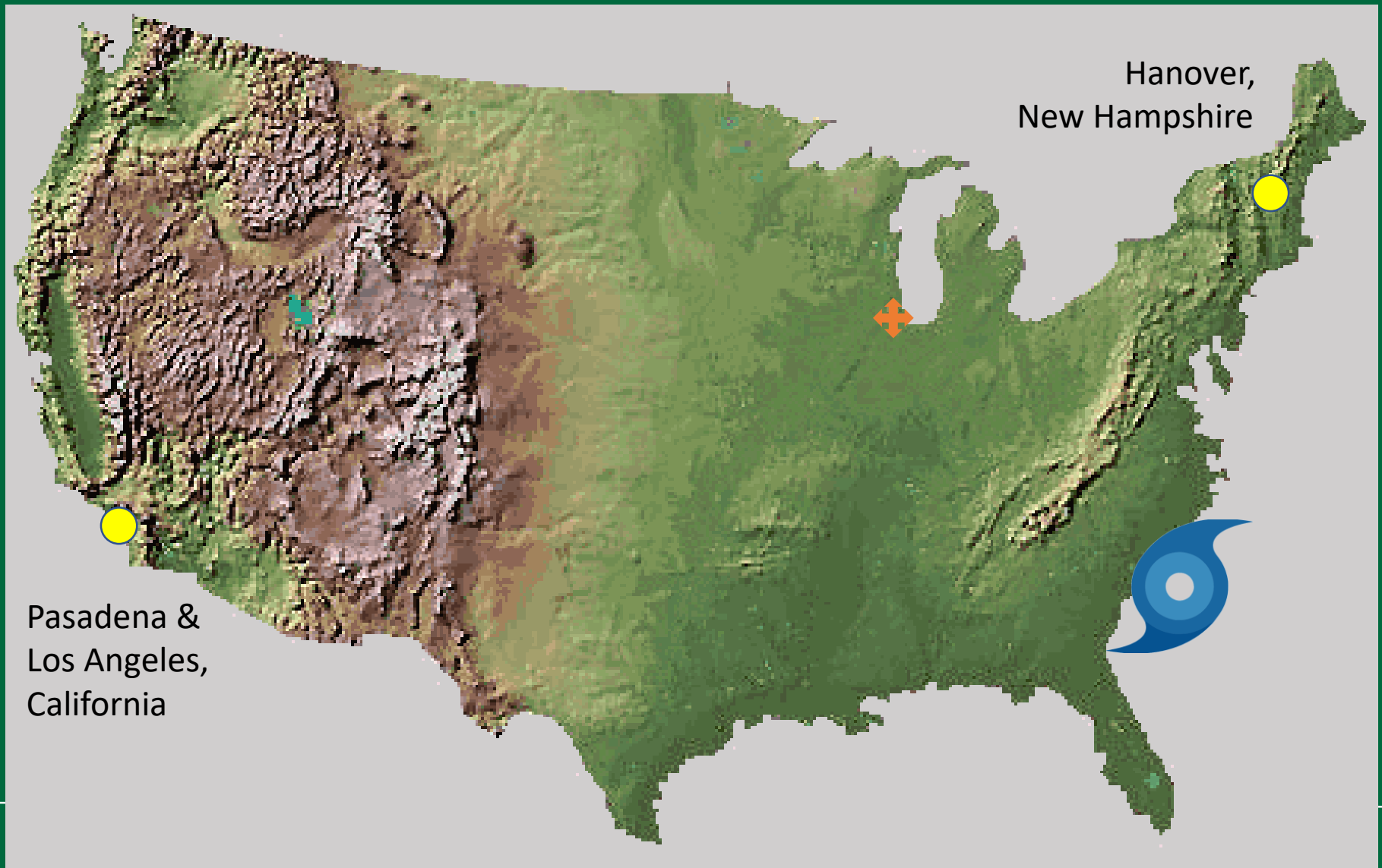

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CMOS IMAGE SENSORS

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CMOS Image Sensors Enable Billions of Cameras Each Year

https://www.nytimes.com/2018/04/27/arts/design/mona-lisa-instagram-art.html

About 5 Billion Cameras Made Each Year (More than 150 per second)

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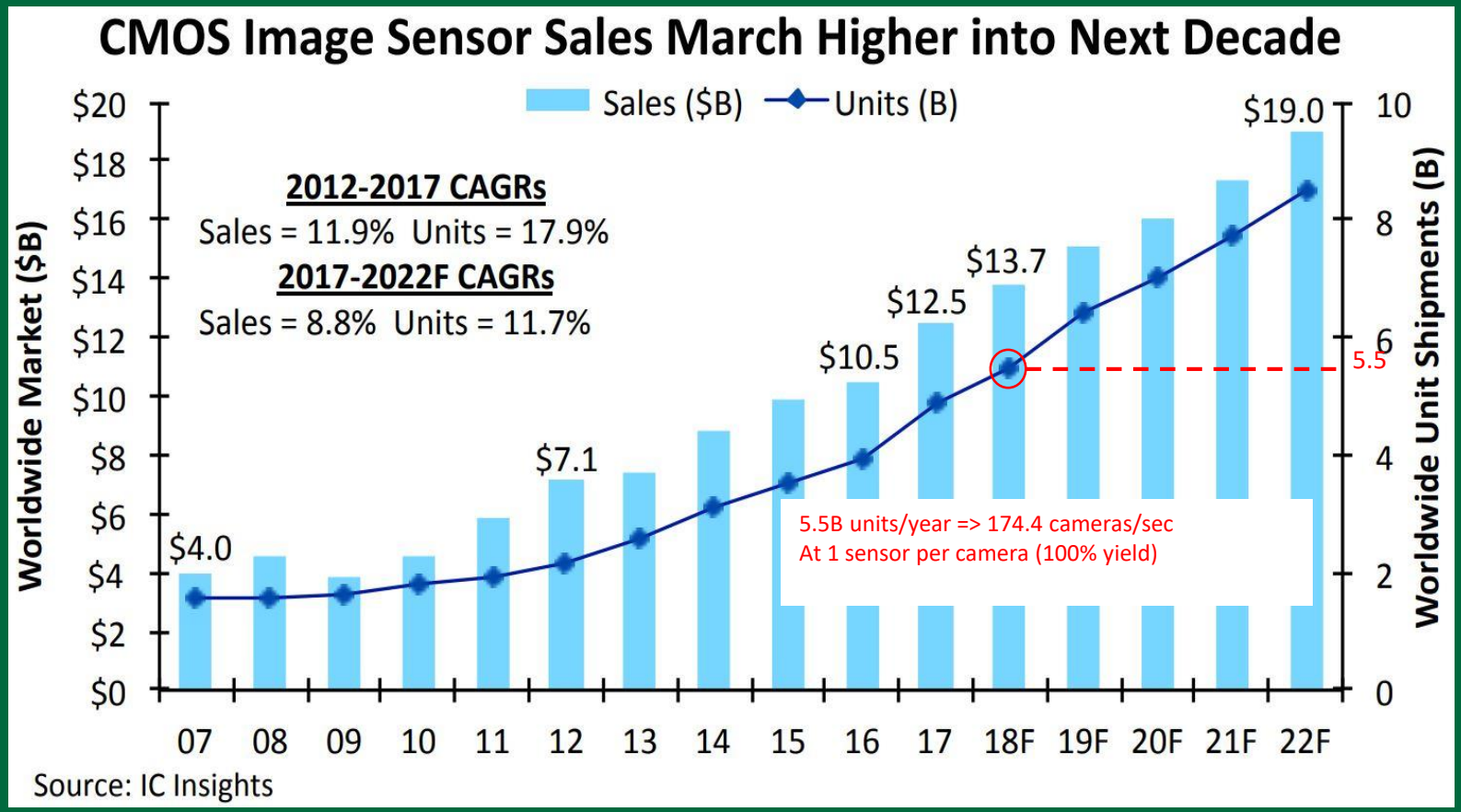

http://image-sensors-world.blogspot.com/2018/05/cmos-sensor-sales-grow-at-record.html

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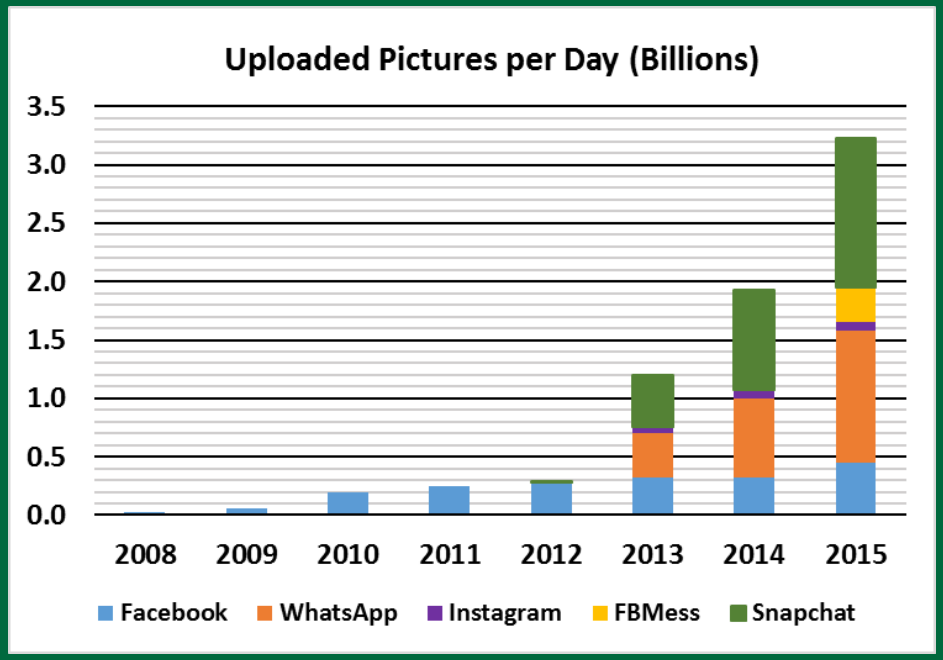
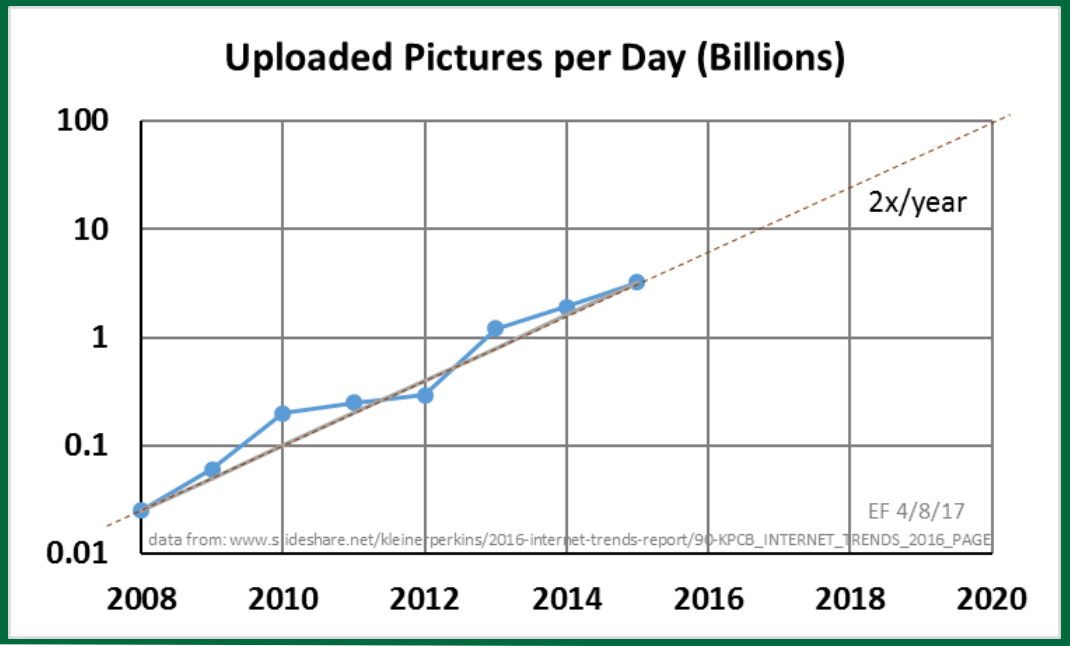
PIKES PEAK
ALTITUDE 14110 FT.
COG WHEEL ROUTE
PIKES PEAK RAILWAY


Uploaded Pictures per Day (Billions)
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
2008
2009
2010
2011
2012
2013
2014
2015
Facebook
WhatsApp
Instagram
FBMess
Snapchat


Uploaded Pictures per Day (Billions)
100
10
1
0.1
0.01
2x/year
EF 4/8/17
data from: www.slideshare.net/kleinerperkins/2016-internet-trends-report/90-KPCB_INTERNET_TRENDS_2016_PAGE
2008
2010
2012
2014
2016
2018
2020

Many Kinds Of Digital Cameras

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MOS "Photomatrices"
0th Generation Image Sensor

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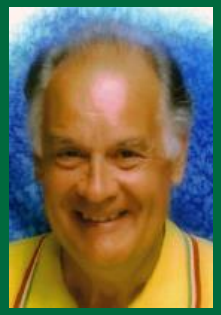
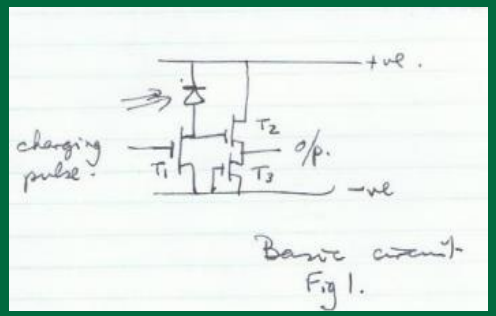
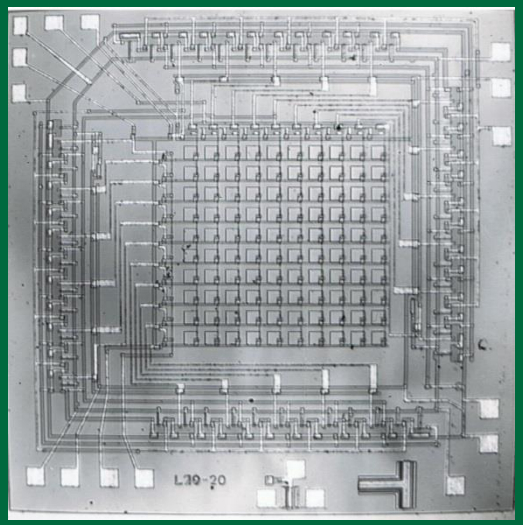


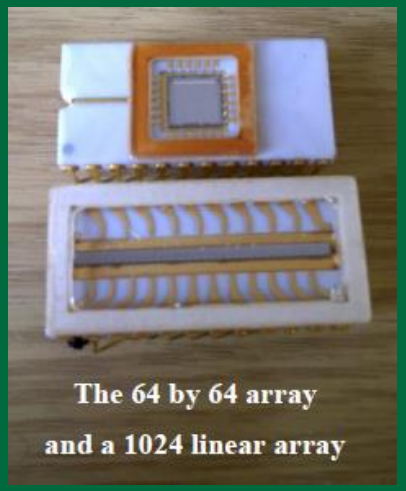
Peter JW Noble

~June 1966



First self-scanned →
Sensor 10x10 1966/67

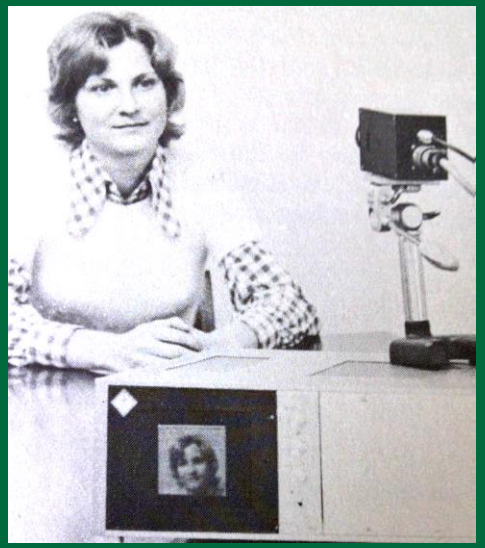




Mid-late 1960's
MOS arrays at Plessey
with startup Integrated Photomatrix Ltd. (IPL)

Gene Weckler

And Fairchild with startup Reticon



Charge-Coupled Device (CCD)
1st Generation Image Sensor

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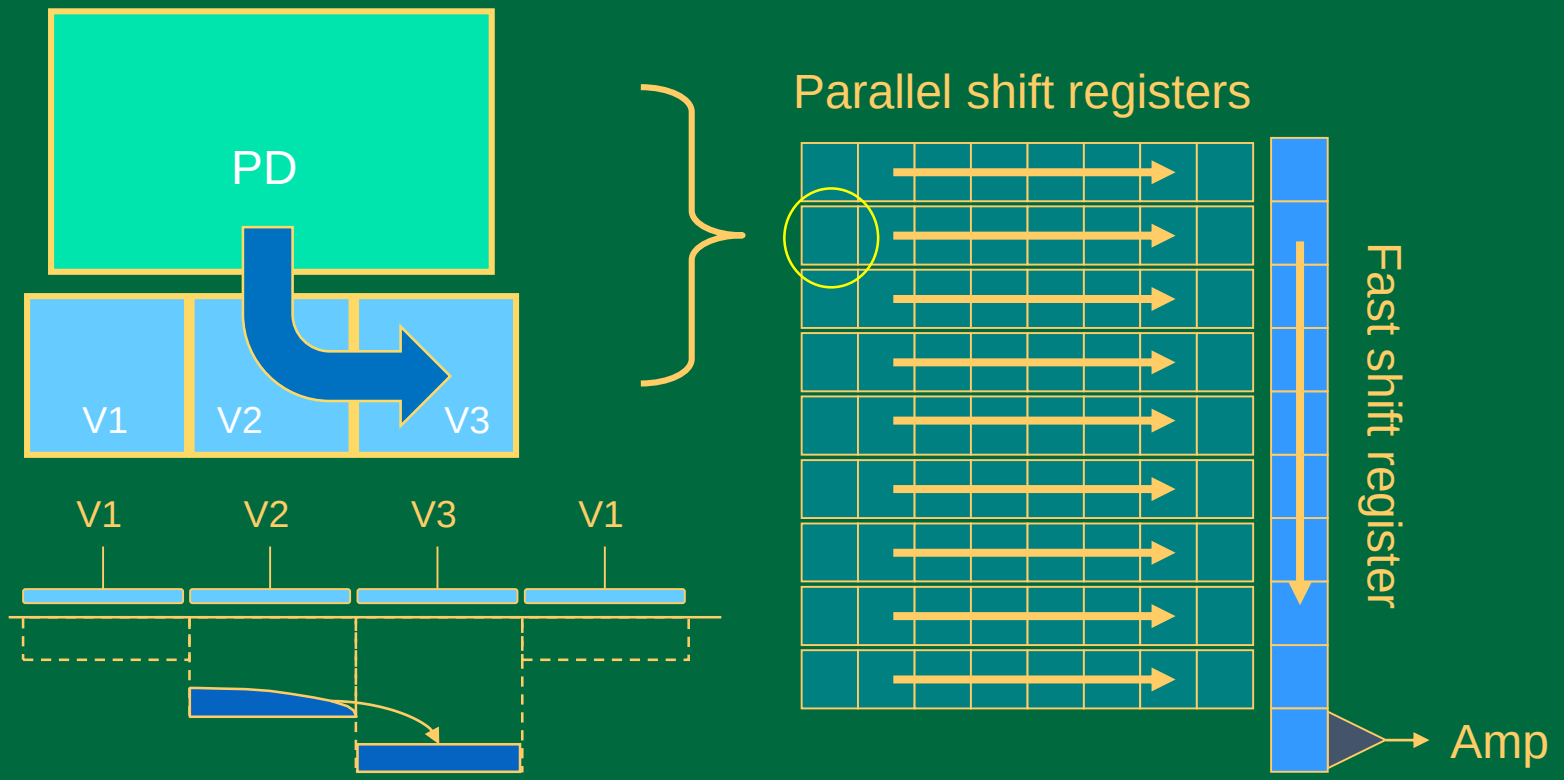
- CCD invented at Bell Labs 1969, then CCD image sensor in 1970.
- Perfected with mass production in Japan.
- Mainstay of digital cameras and camcorders in 1980's and 1990's.



CCD Cameras
1970's - 1990's

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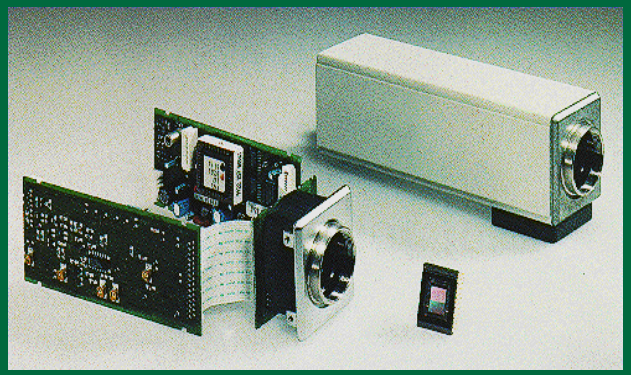
Early 70's Bell Labs CCD camera
by Mike Tompsett et al.

Steve Sasson with first
Kodak self-contained
digital camera (1975)

NASA Galileo Spacecraft CCD camera
(with optics) early '80s (800x800)

RCA Camcorder



DALSA industrial CCD
camera late '80's

Sony Camcorder
early 90's

2009 Nobel Prize in Physics

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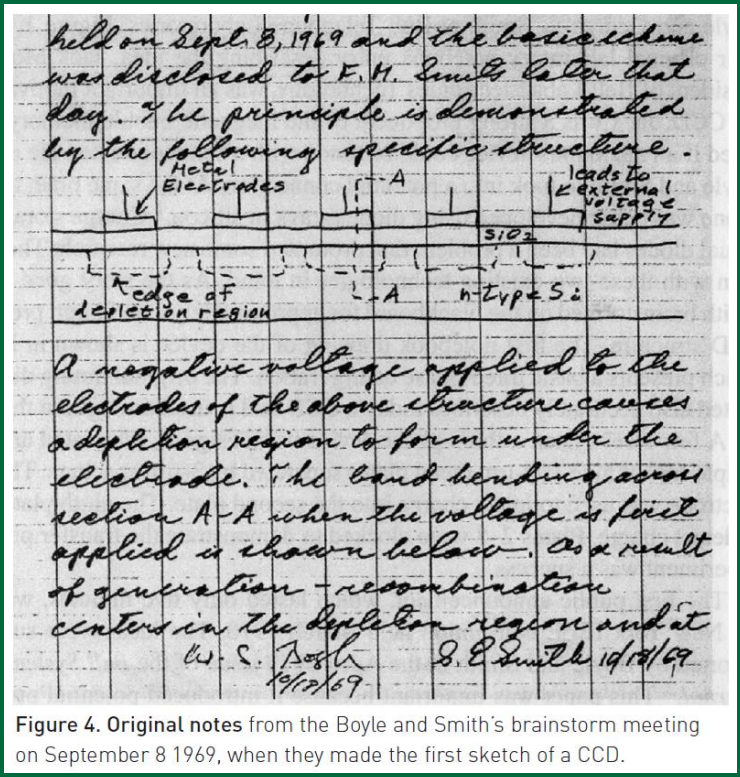

held on Sept. 8, 1969 and the basic scheme was disclosed to F. H. Smith later that day. The principle is demonstrated by the following specific structure.

Metal Electrodes — A — leads to external voltage supply

SiO_2

edge of depletion region — A — n-type Si

A negative voltage applied to the electrodes of the above structure causes a depletion region to form under the electrode. The band bending across section A-A when the voltage is first applied is shown below. As a result of generation-recombination centers in the depletion region and at

W. S. Boyle 9/12/69 — G. E. Smith 9/12/69

Figure 4. Original notes from the Boyle and Smith's brainstorm meeting on September 8 1969, when they made the first sketch of a CCD.

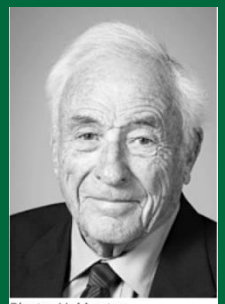
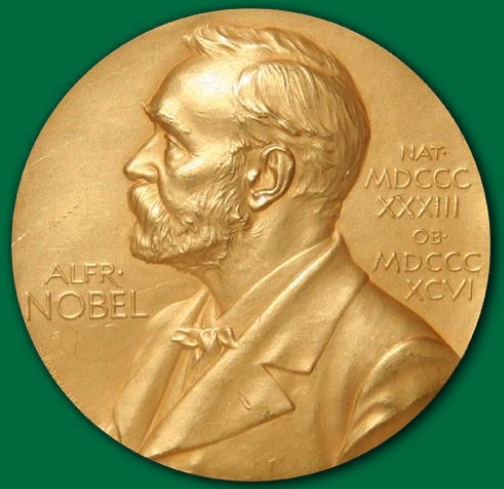


Photo: U. Montan
Willard S. Boyle

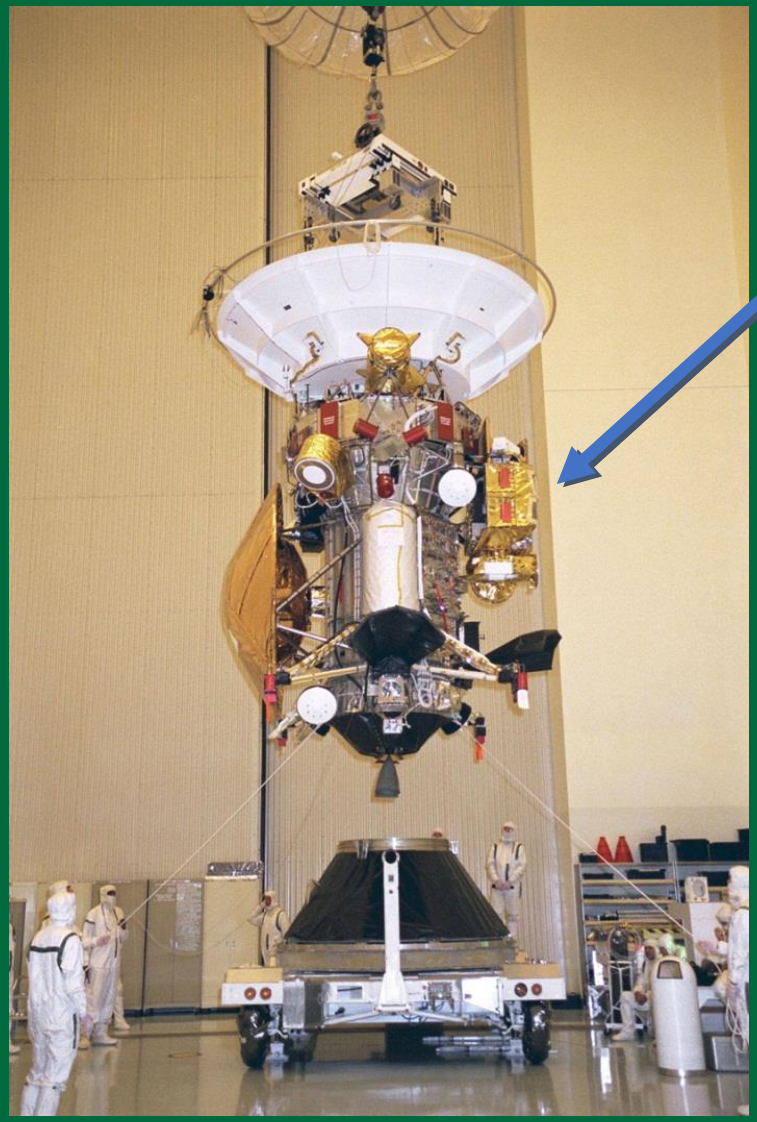
Photo: U. Montan
George E. Smith



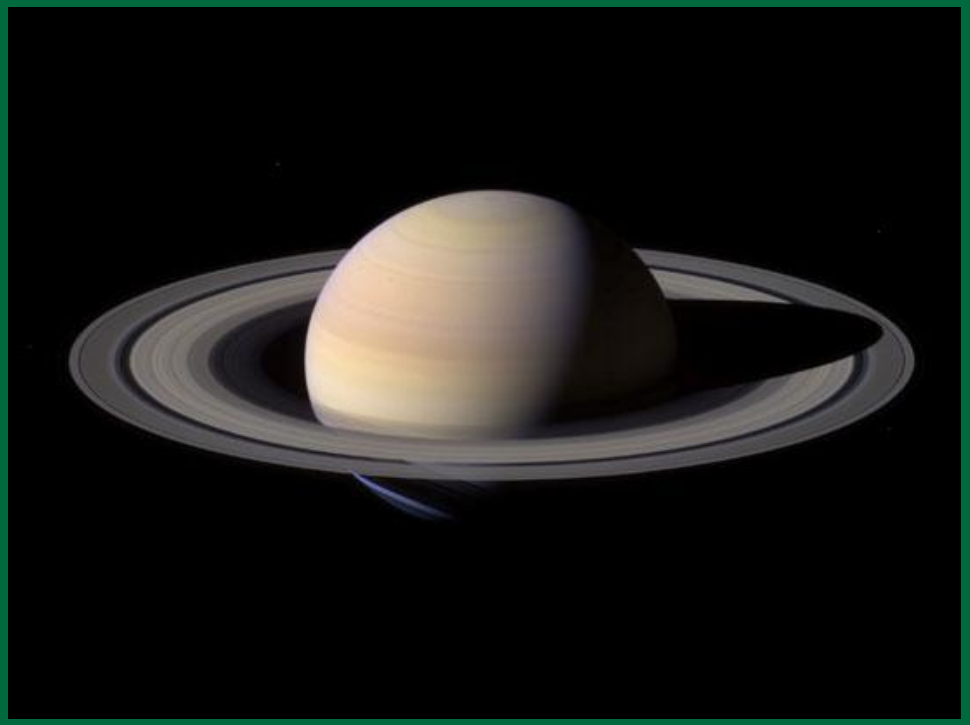
"for the invention of an imaging semiconductor circuit – the CCD sensor"

CCD image sensor inventor:
Michael F. Tompsett
US patent no. 4,085,456

1990's Need: Smaller cameras for smaller spacecraft at JPL/Caltech



Camera



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Some Problems with CCDs

- Charge must be perfectly transferred thousands of times to get to output amplifier.
  - Requires high voltages
  - Requires special device structures
  - Very susceptible to radiation damage and traps
  - Requires power to drive huge whole-chip capacitance
- Requires many support chips
- Difficult to make it work right
- Serial readout gives slow frame rate
- High bandwidth (noisy) output amplifier

Active Pixels with Intra-Pixel Charge Transfer

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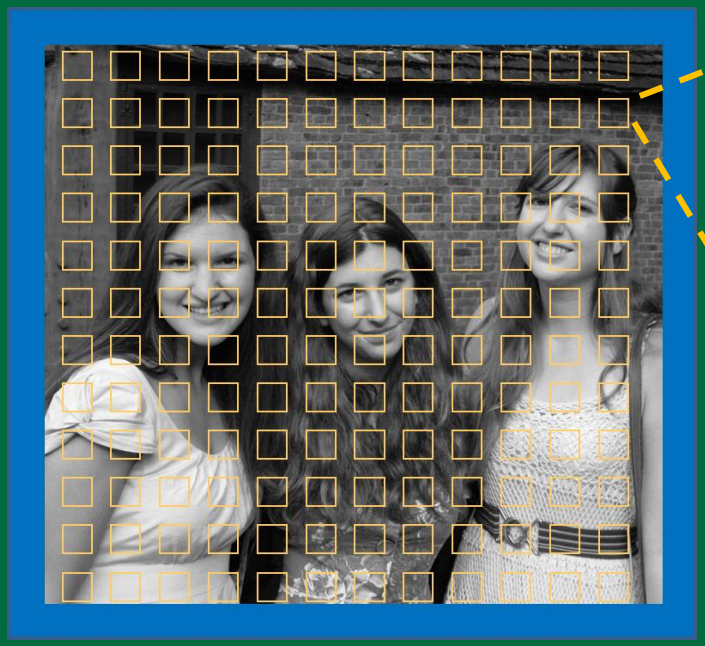

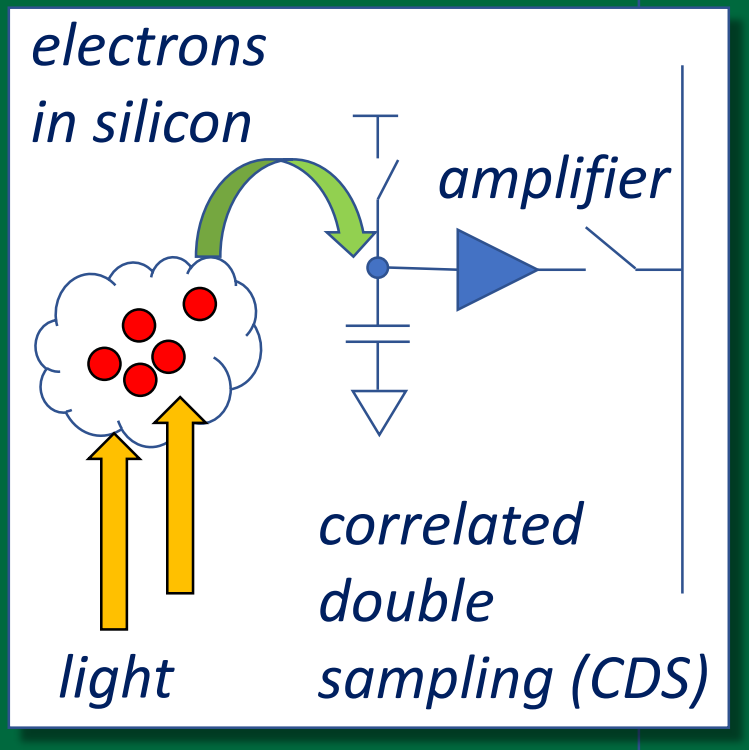

One pixel

- Complete charge transfer to suppress lag
- Correlated double-sampling to suppress kTC noise
- Double-delta sampling to suppress fixed pattern noise
- On-chip ADC, timing and control, etc.

“Camera-on-a-Chip” Enables Much Smaller Cameras

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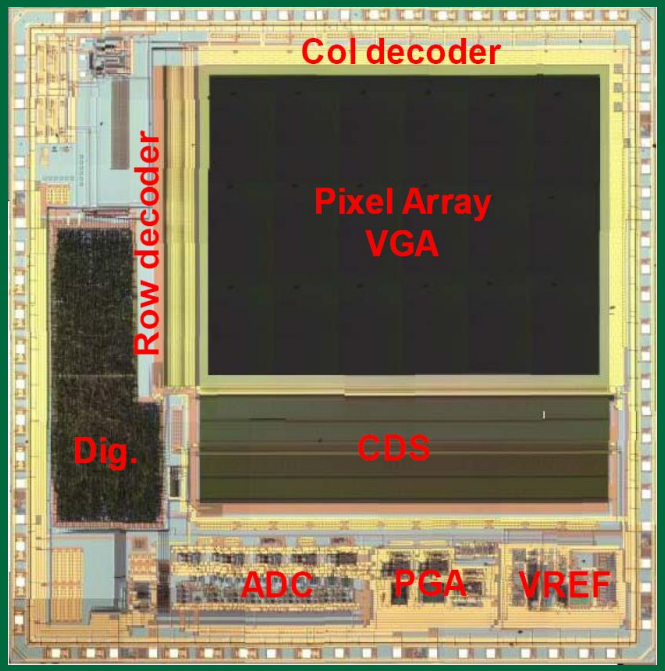

Camera-Phone

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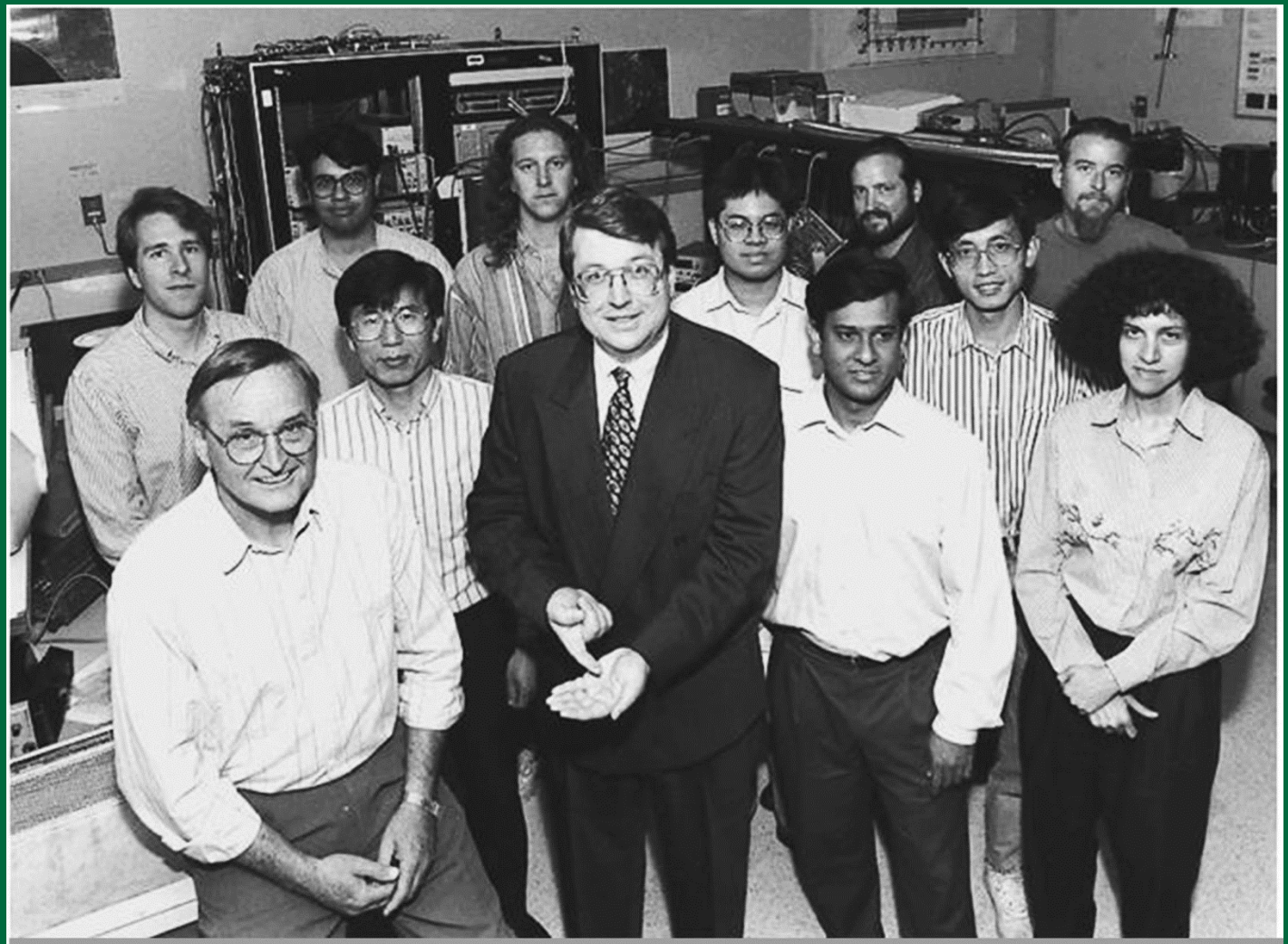
Most of the JPL Team circa 1995



Advanced Imager Technology Group, Jet Propulsion Laboratory, California Institute of Technology 1995
Back row: Roger Panicacci, Barmak Mansoorian, Craig Staller, Russell Gee, Peter Jones, John Koehler
Front row: Robert Nixon, Quisup Kim, Eric Fossum, Bedabrata Pain, Zhimin Zhou, Orly Yadid-Pecht

Missing: Sabrina Kemeny, Junichi Nakamura, Sunetra Mendis

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Technology Transfer

Entrenched industry moves slowly in adopting new technologies so in February 1995 we founded **Photobit Corporation** to commercialize the CMOS image sensor technology ourselves

S.Kemeny, N. Doudoumopoulos, E. Fossum, R. Nixon

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The Photobit Corporation Team (early 2000)

Perspiration Phase

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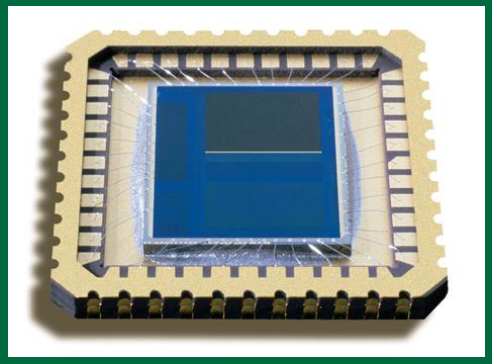
1995-2001 Photobit grows to about 135 persons

- Self funded with custom-design contracts from private industry
- Important support from SBIR programs (NASA/DoD)
- Later, investment from strategic business partners to develop catalog products
- Over 100 new patent applications filed
- Nov 2001 Photobit acquired by Micron Technology



The Technology Develops a Life of its Own

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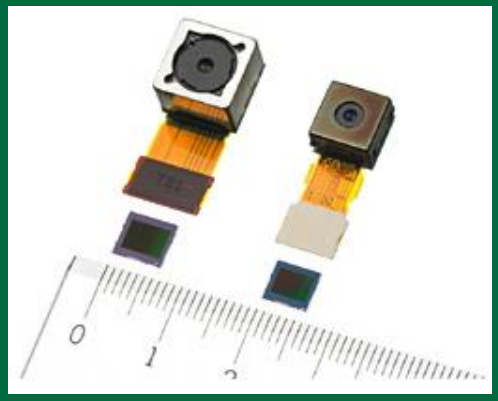
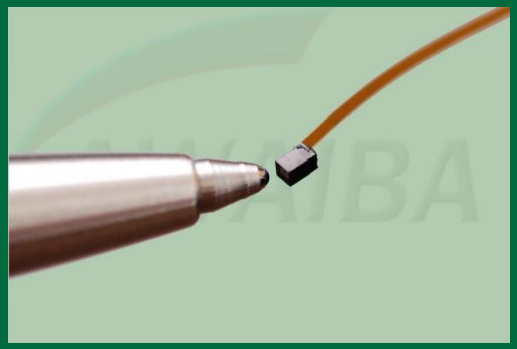
- Today, over 5 billion cameras are manufactured each year that use the CMOS image sensor technology we invented at JPL, or more than 150 cameras per second, 24/365.
- Semiconductor sales of CMOS image sensors are over $13B/yr in 2018.
- Thousands of engineers working on this around the globe.
- Caltech has successfully enforced its patents against all the major players.
- NASA is now just adopting the technology for use in space (e.g. Mars 2020).



16Mpix camera modules
From Sony ~2012



Endoscopy Camera
From Awaiba ~2012

~$14B Semiconductor Sales in 2018
~5 Billion Cameras in 2018

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2017 Queen Elizabeth Prize for Engineering

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For the creation of digital imaging sensors

Eric Fossum	Nobukazu Teranishi	Mike Tompsett

CMOS image sensor	Pinned photodiode	CCD image sensor

+ George Smith CCD

Buckingham Palace Reception
December 2017

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QUANTA IMAGE SENSOR

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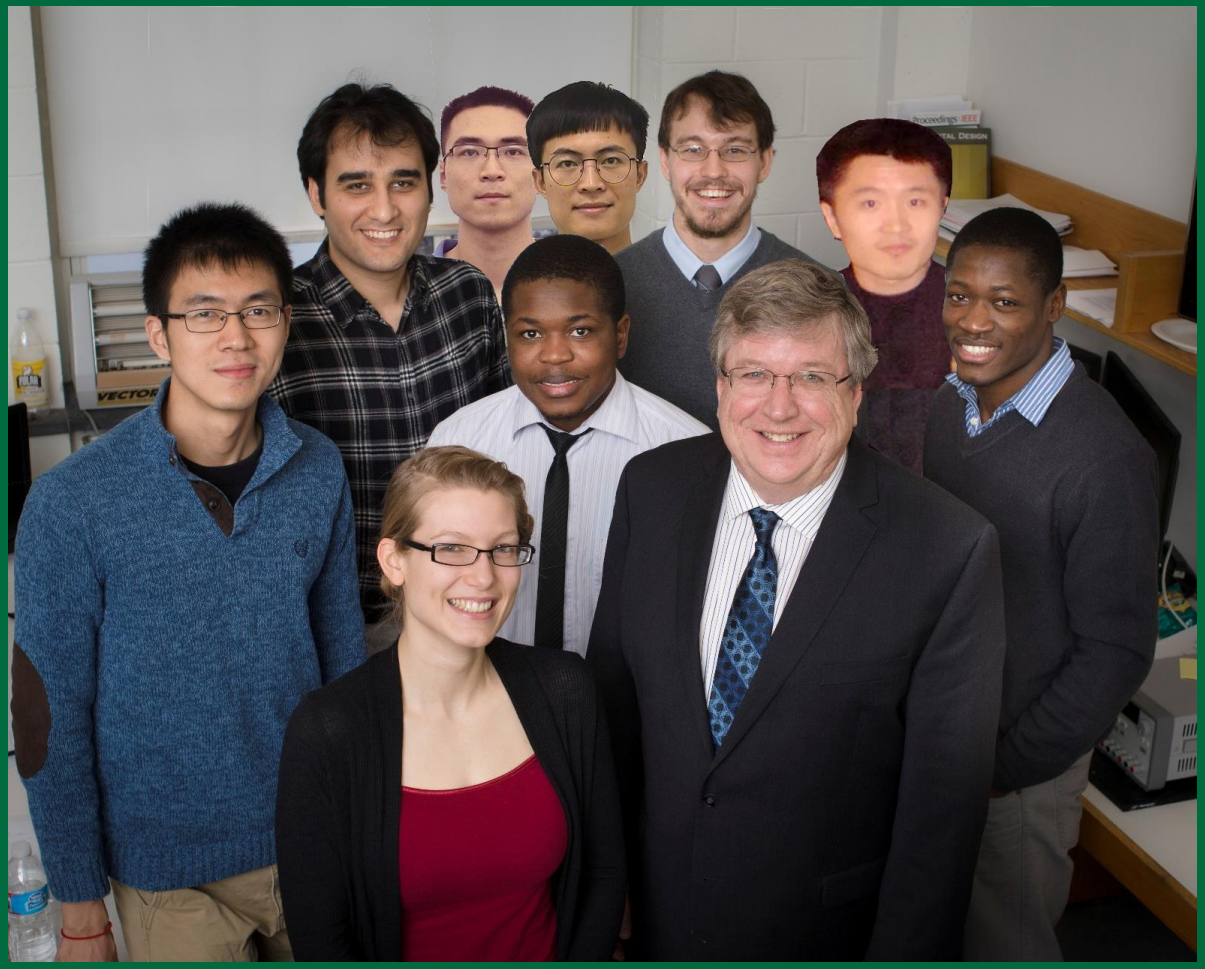
Group at Dartmouth



L-R: Song Chen, Saleh Masoodian, Rachel Zizza, Zhaoyang Yin, Donald Hondongwa, Wei Deng, Dakota Starkey, Eric Fossum, Jiaju Ma, Leo Anzagira

QUANTA IMAGE SENSOR
Photon-Counting Image Sensor Concept

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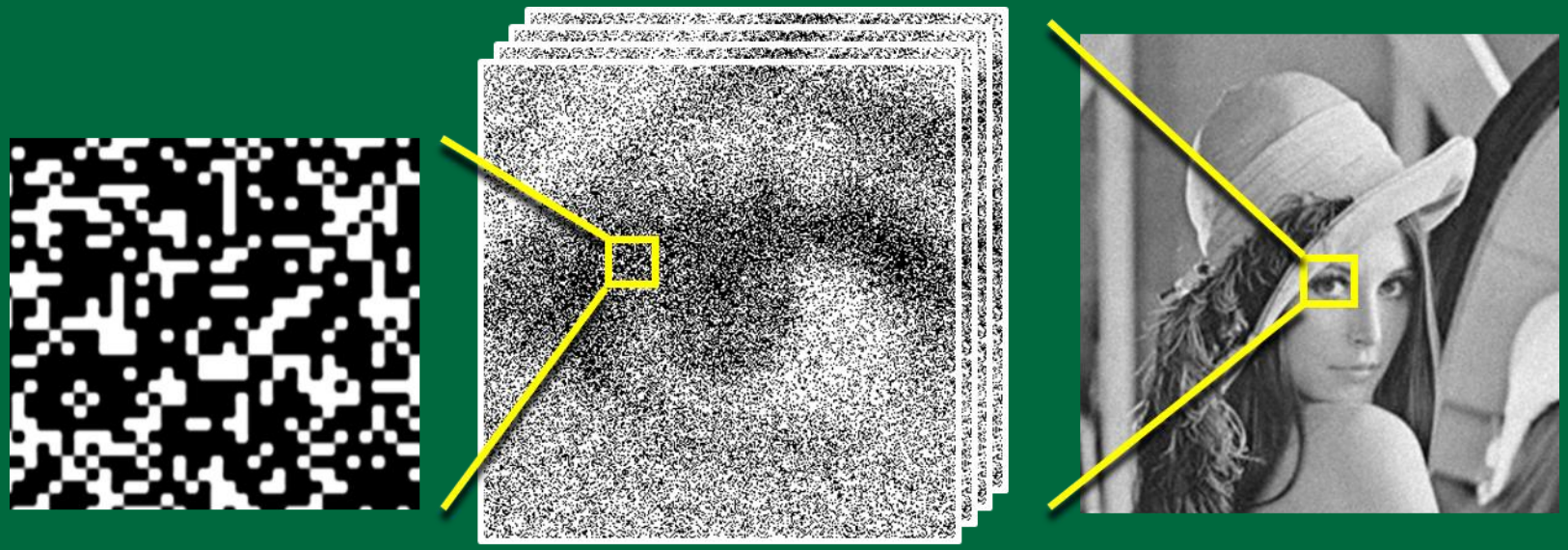
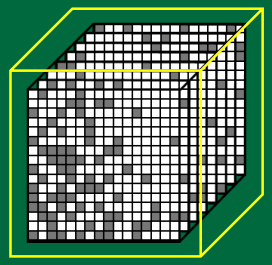


Image reconstruction
X-Y-t Bit Density ➔ Gray Scale



Cubicle

Vision: A billion jots readout at 1000 fps with single photon-counting capability (1Tb/s) and consuming less than a watt.

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Implementation Challenges in 2011

1. How to make a tiny sub-diffraction-limit (SDL) pixel (< 500nm) with deep sub-electron read noise in a mainstream process?

2. How to readout a very large array of binary pixels or jots at 1000 fps with less than 1Watt power?

3. How do you process the jot data to create pixels?

Photoresponse as Bit Density

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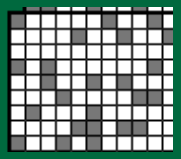
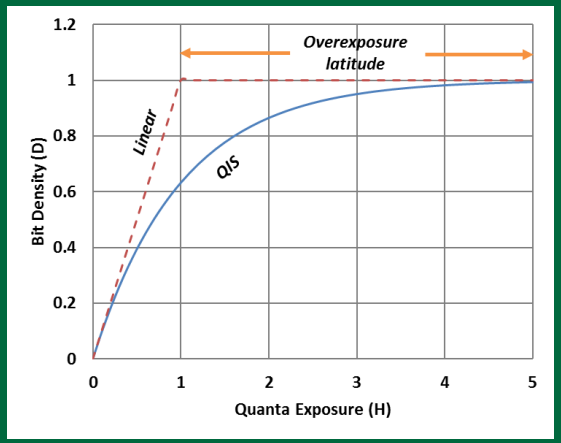
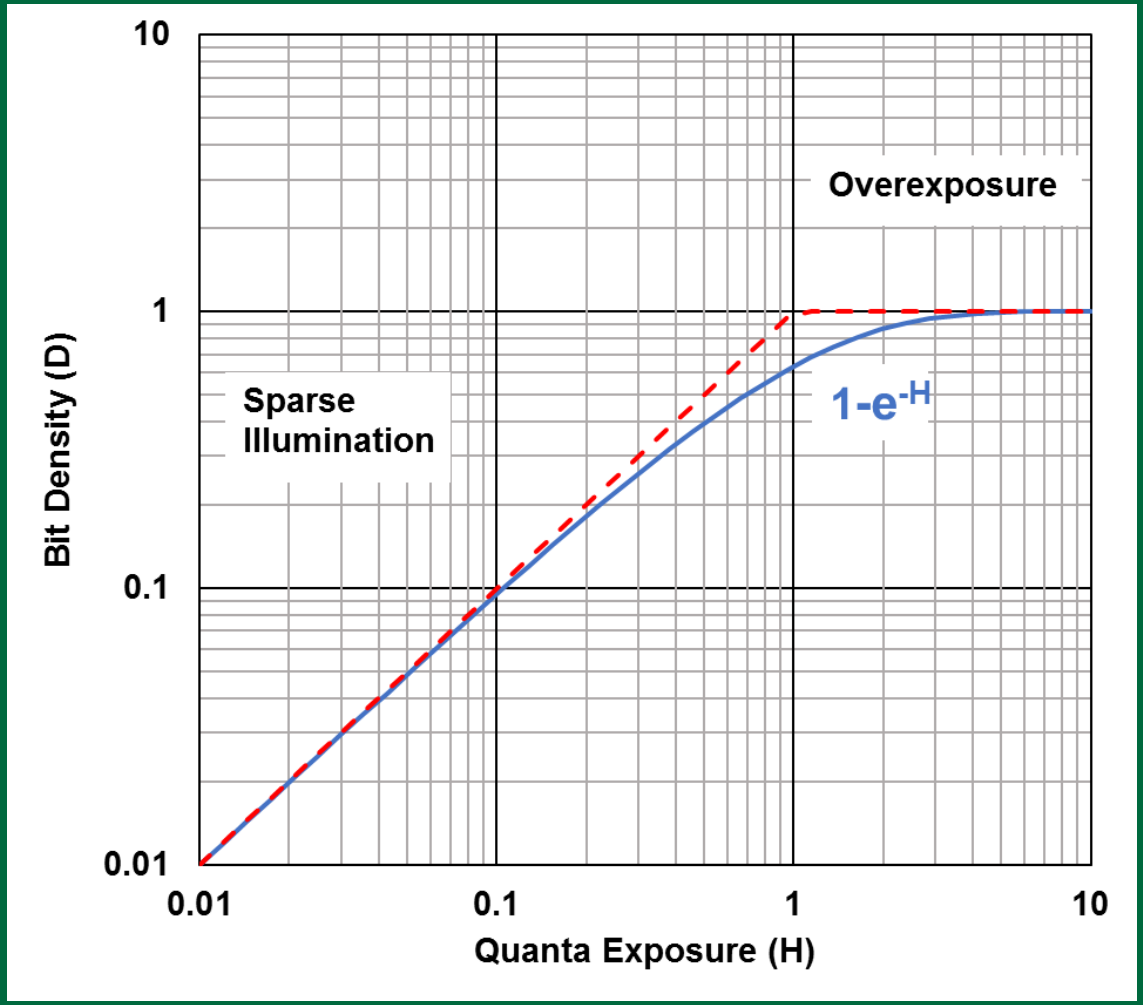


$$Bit\ Density\ D \triangleq \frac{M_1}{M} = 1 - e^{-H}$$



QIS Log D – Log H



Issues with Single Photon Avalanche Detectors (SPADs) for QIS Application

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SPADs use avalanche multiplication for gain

- High internal electric fields
- Higher operating voltages (15-20V)
- Larger pixels (8-25um)
- High dark count rates (100-1000Hz)
- Dead time
- Low fill factor (low PDE <50%)
- Low manufacturing yield
- Small array sizes (below 0.1M jots)

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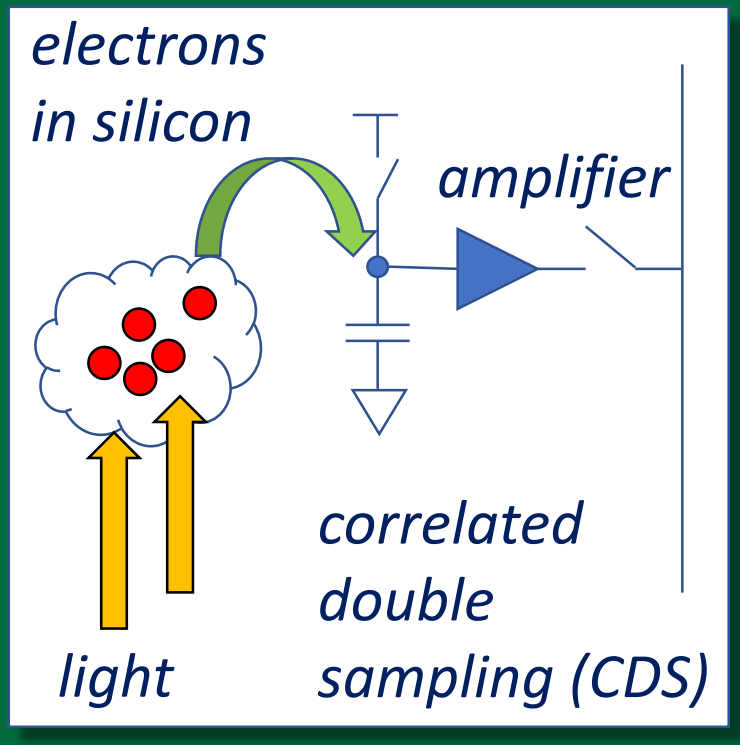
Our Approach

Use very low capacitance sense node

$\Delta V = \Delta Q / C$

1mV = 1.6e-19 / 0.16fF



One pixel

Voltage Output with No Electronics Noise

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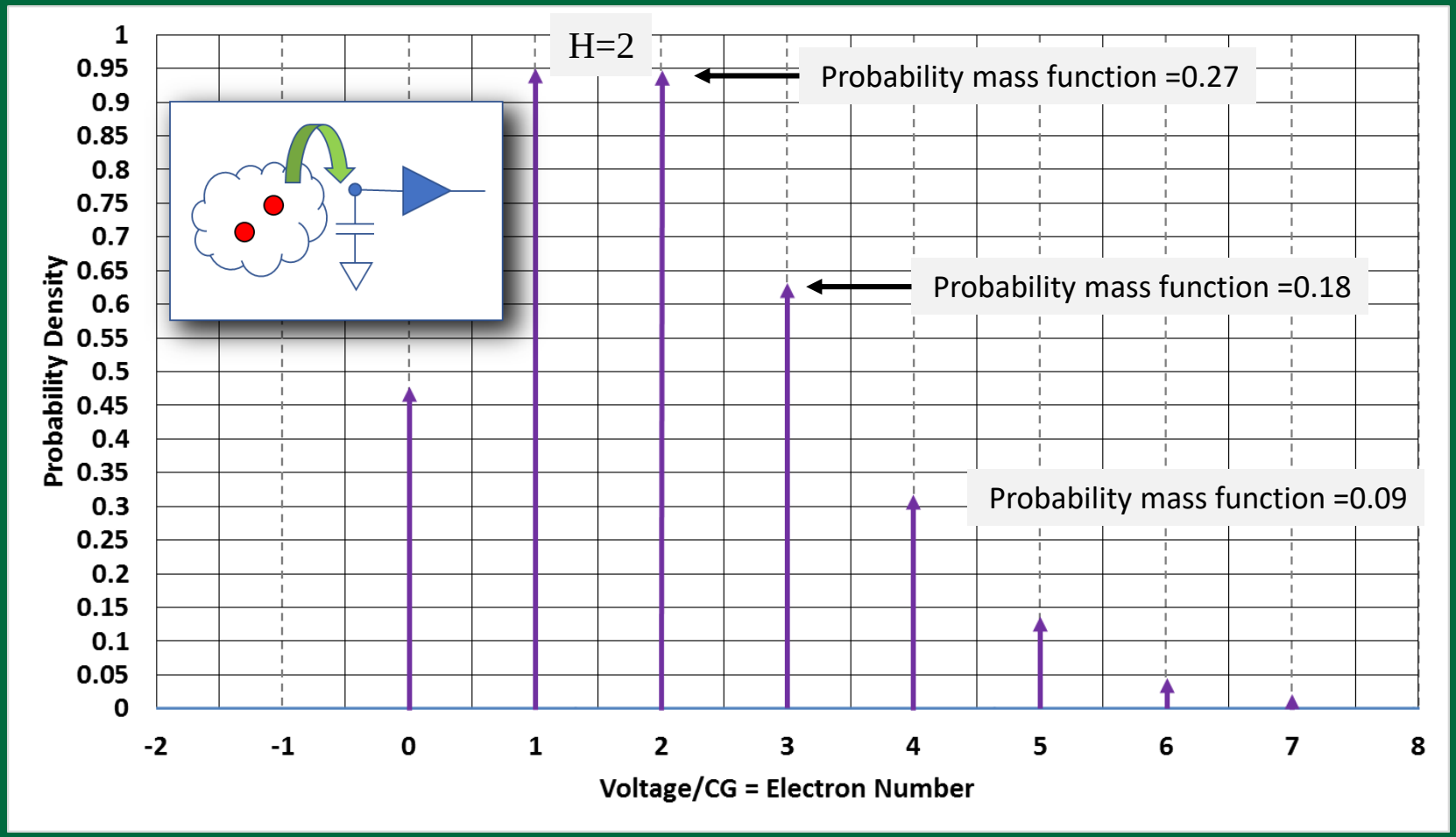
Poisson probability mass function $P[k] = \frac{e^{-H} H^k}{k!}, k = 0, 1, 2, 3 \ldots$



CG = conversion gain = q/C [V/e-]

Broadened by 0.12e- rms read noise

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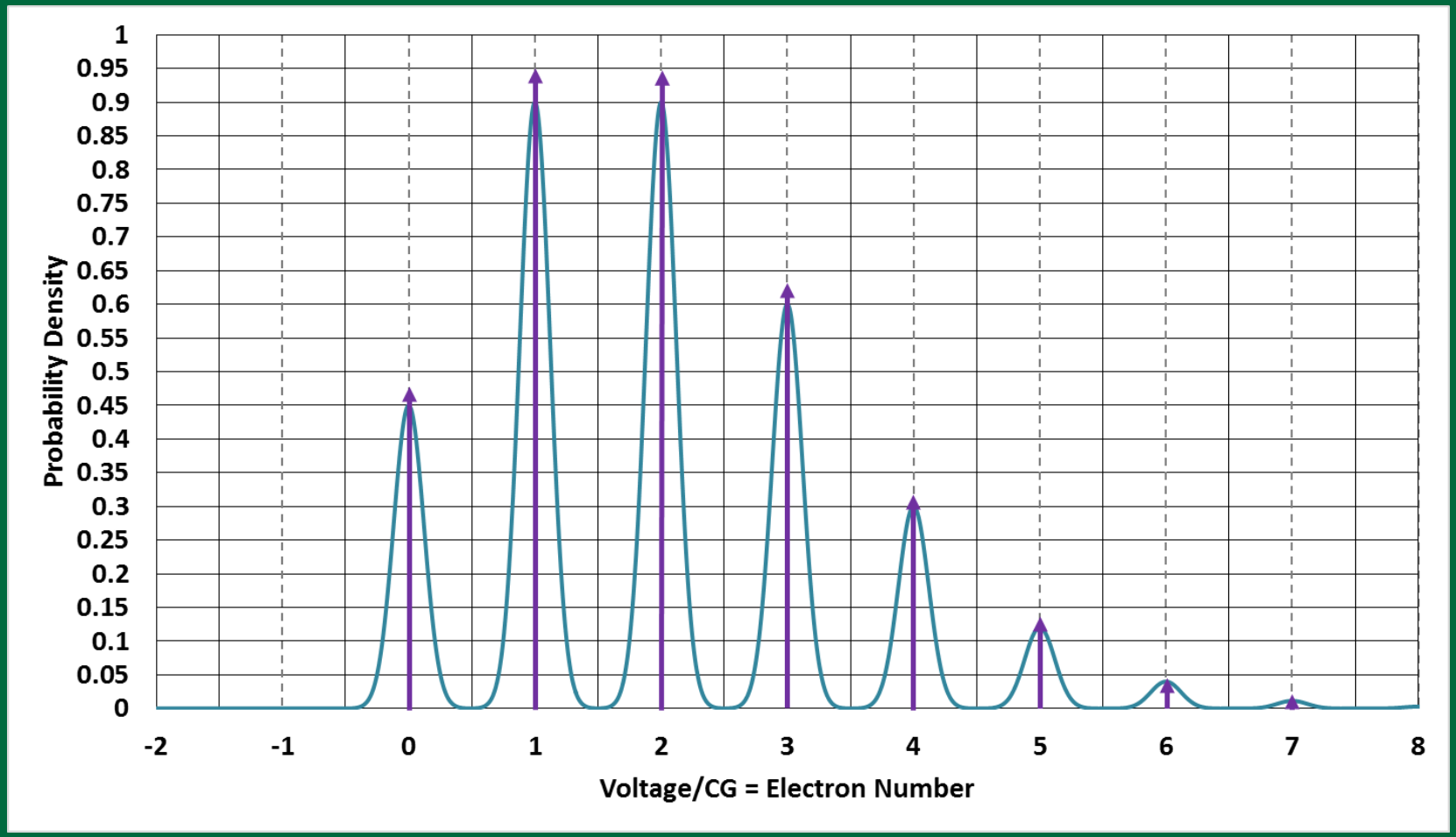
$U_n = V_n / CG$ [e- rms]



Broadened by 0.25e- rms read noise

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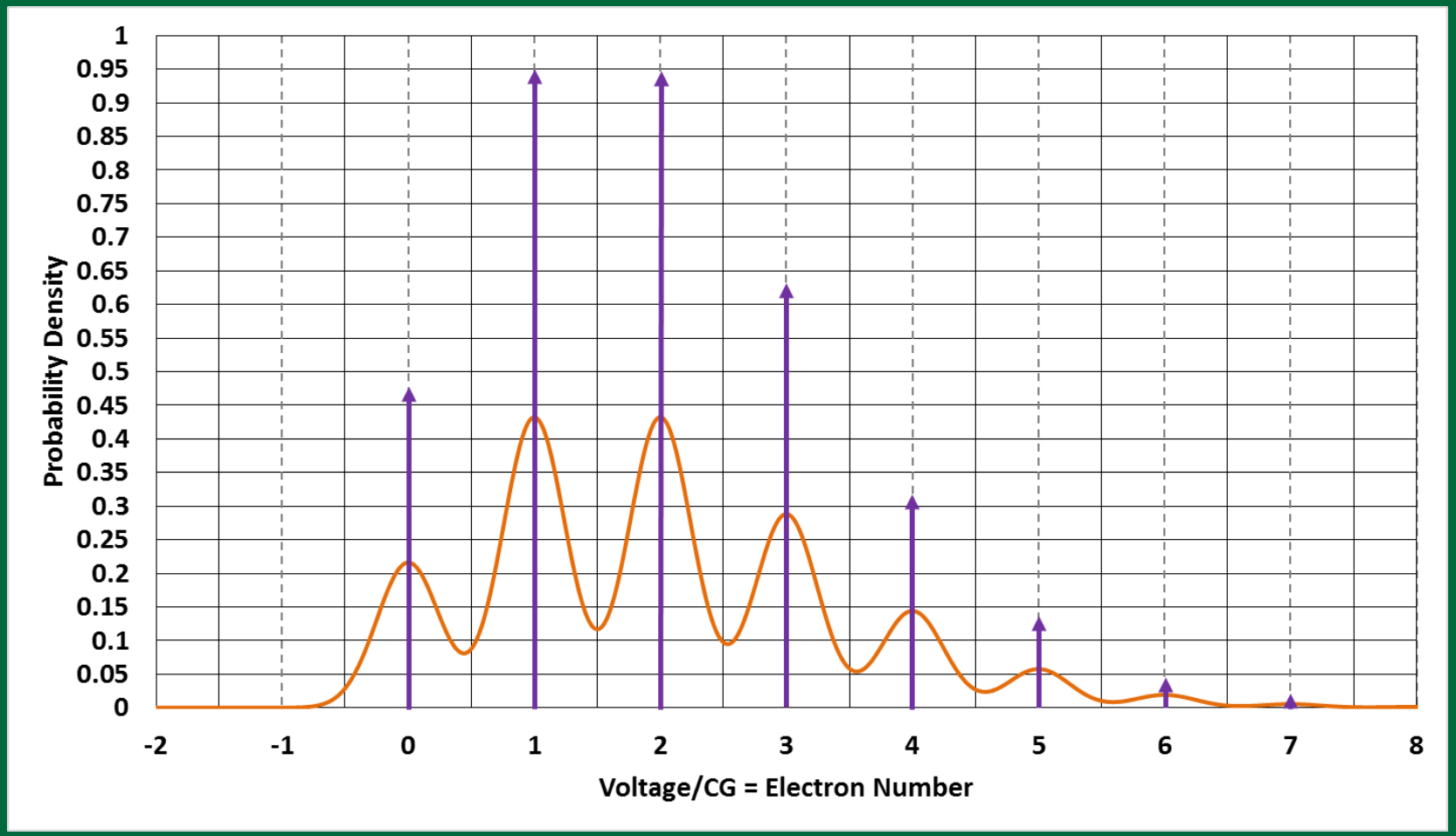

Model

Quantized Values Broadened by Readout Noise

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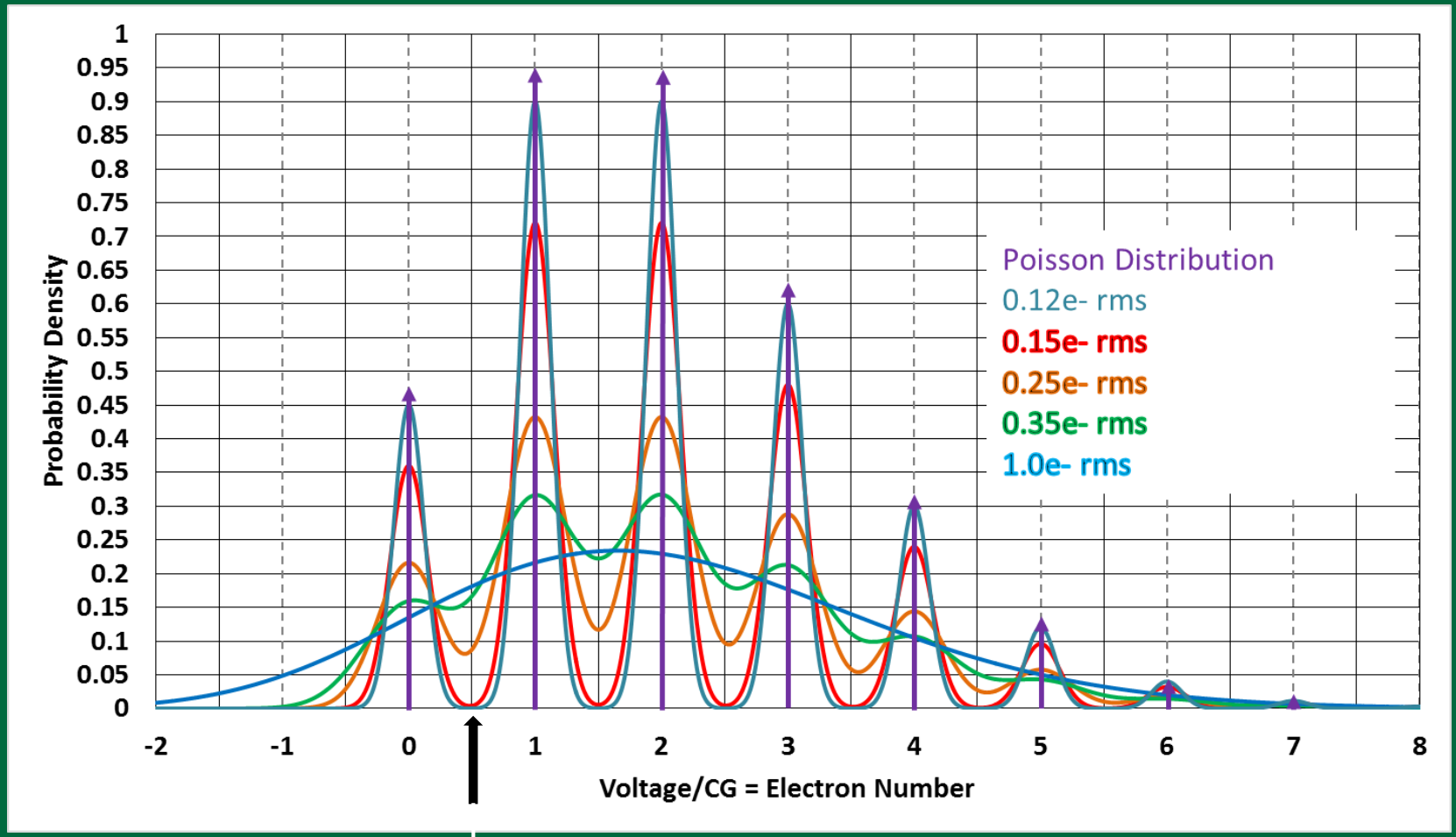

Single-bit QIS

"0" "1"

Pump-Gate Jot: Minimize TG-FD Overlap Capacitance

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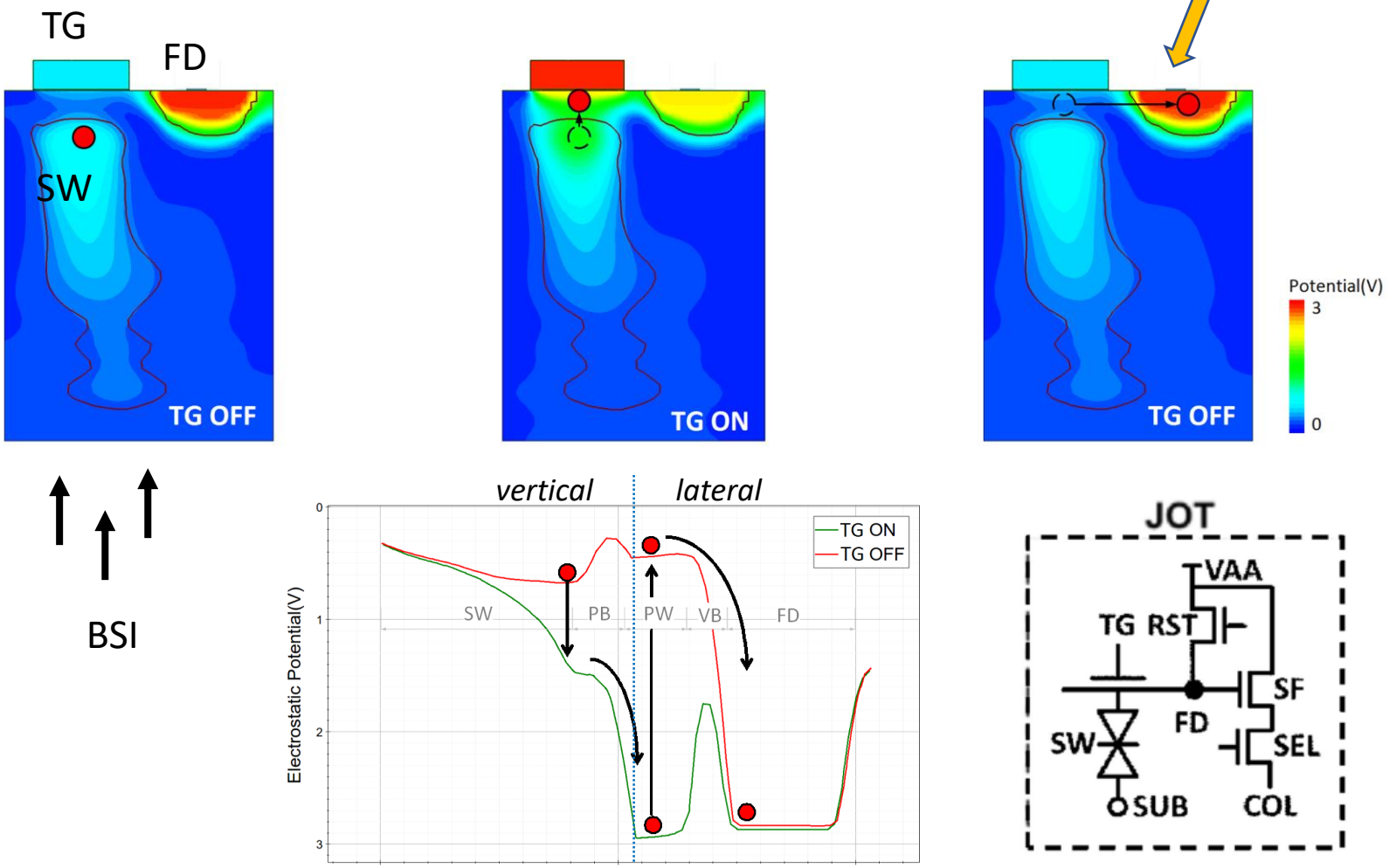
Highest possible CG
(Lowest possible cap.)



Experimental Data
Photon Counting Histograms

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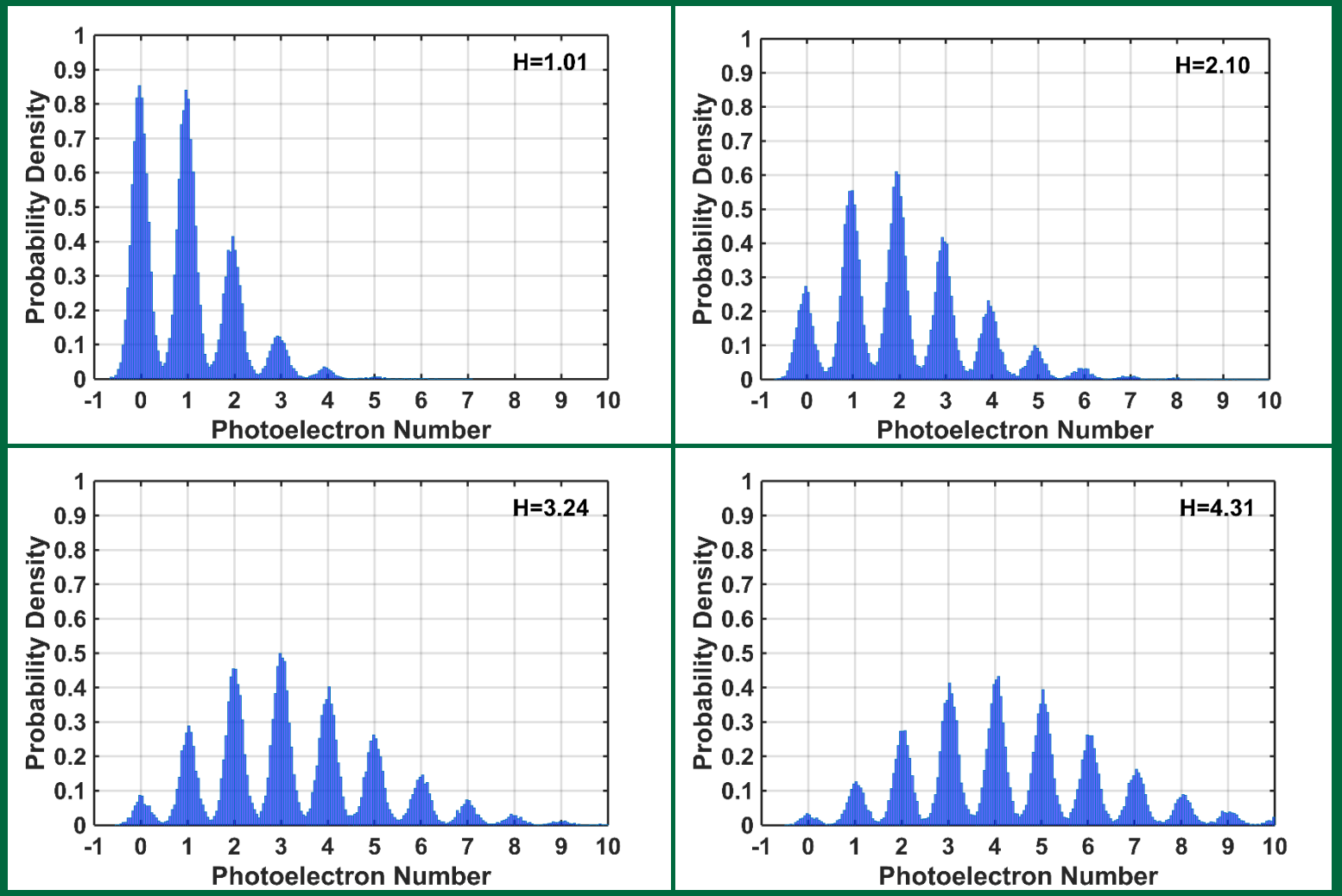
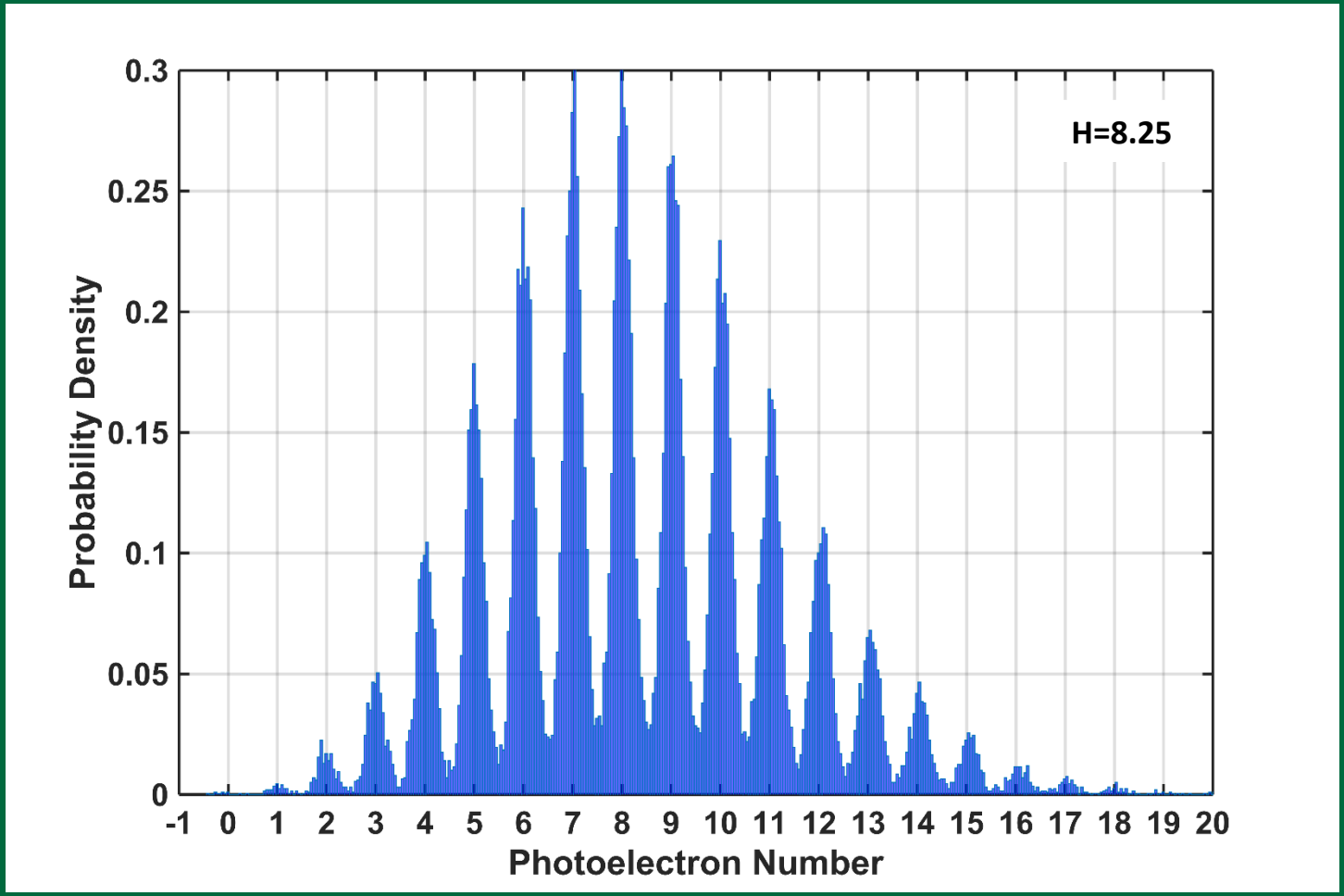
20k reads of same jot, 0.175e- rms read noise ~21DN/e- (61.2uV rms 350uV/e- or 0.45fF)
Room temperature, no avalanche, 20 CMS cycles, jot:TPG PTR BC



Experimental Data
Photon Counting Histograms

DARTMOUTH

20k reads of same jot, 0.2e- rms read noise ~21DN/e-
Room temperature, no avalanche, 20 CMS cycles, jot:TPG PTR BC



Ma, Masoodian, Wang, Fossum 2017

Read Noise and Photon-Counting Error

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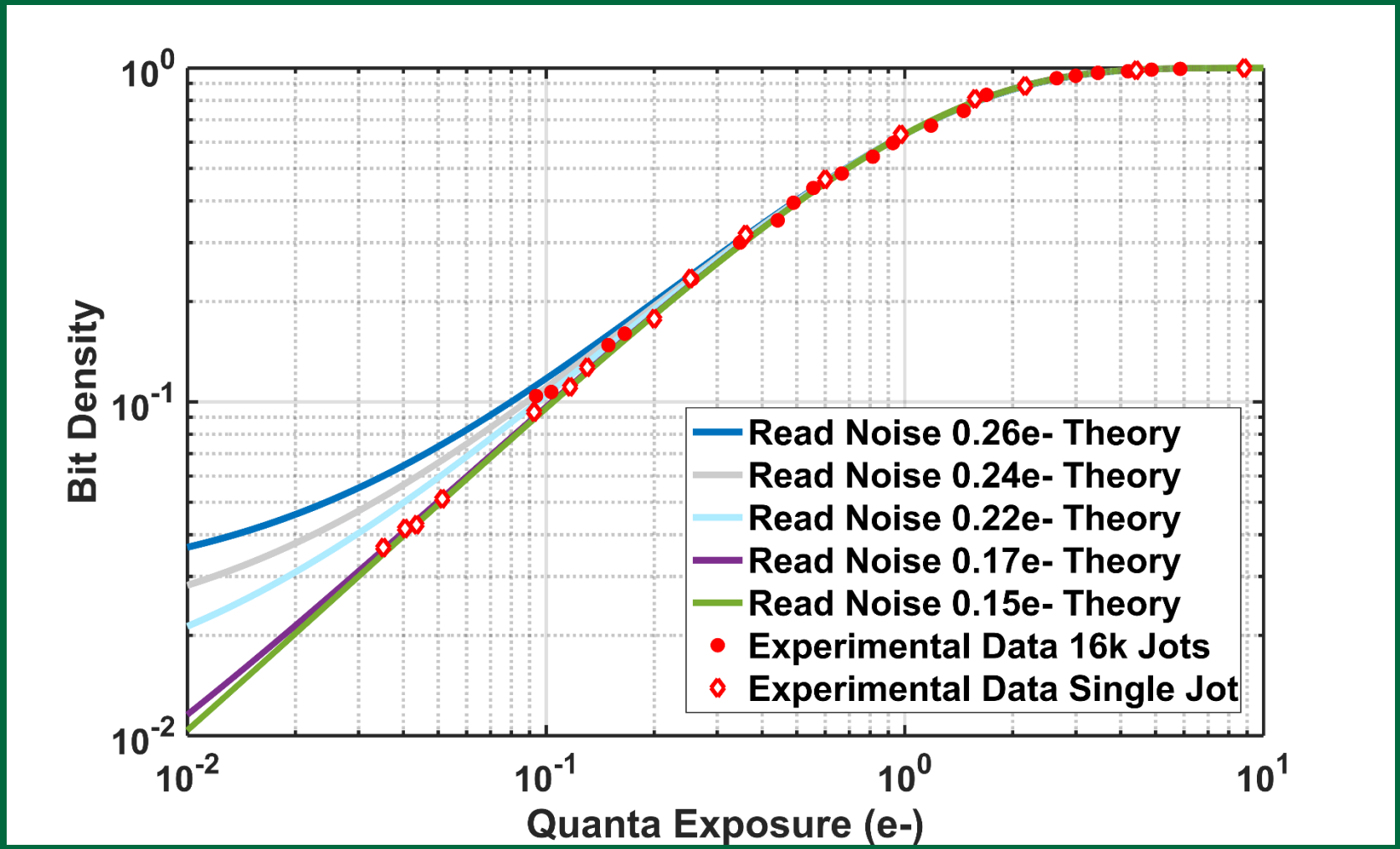

Dark Current

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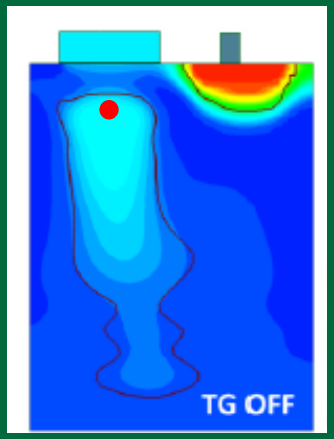
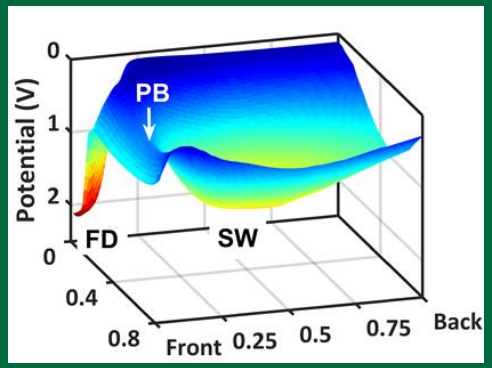
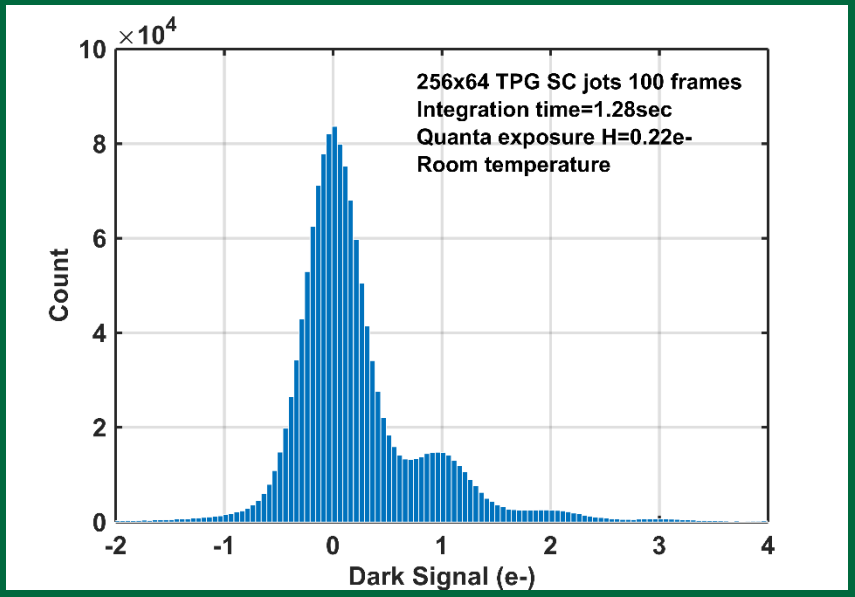
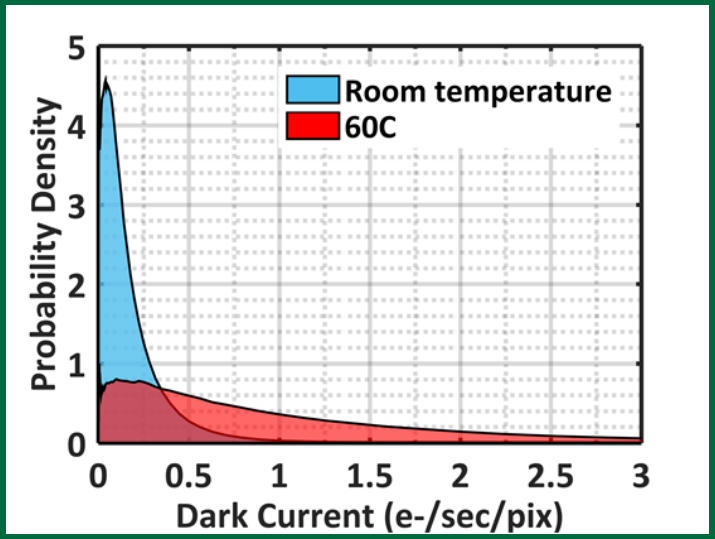
Room Temp: ~0.16e-/s avg. (~2pA/cm^2)
Previously measured ~2x every 10C



Storage well isolated from surface



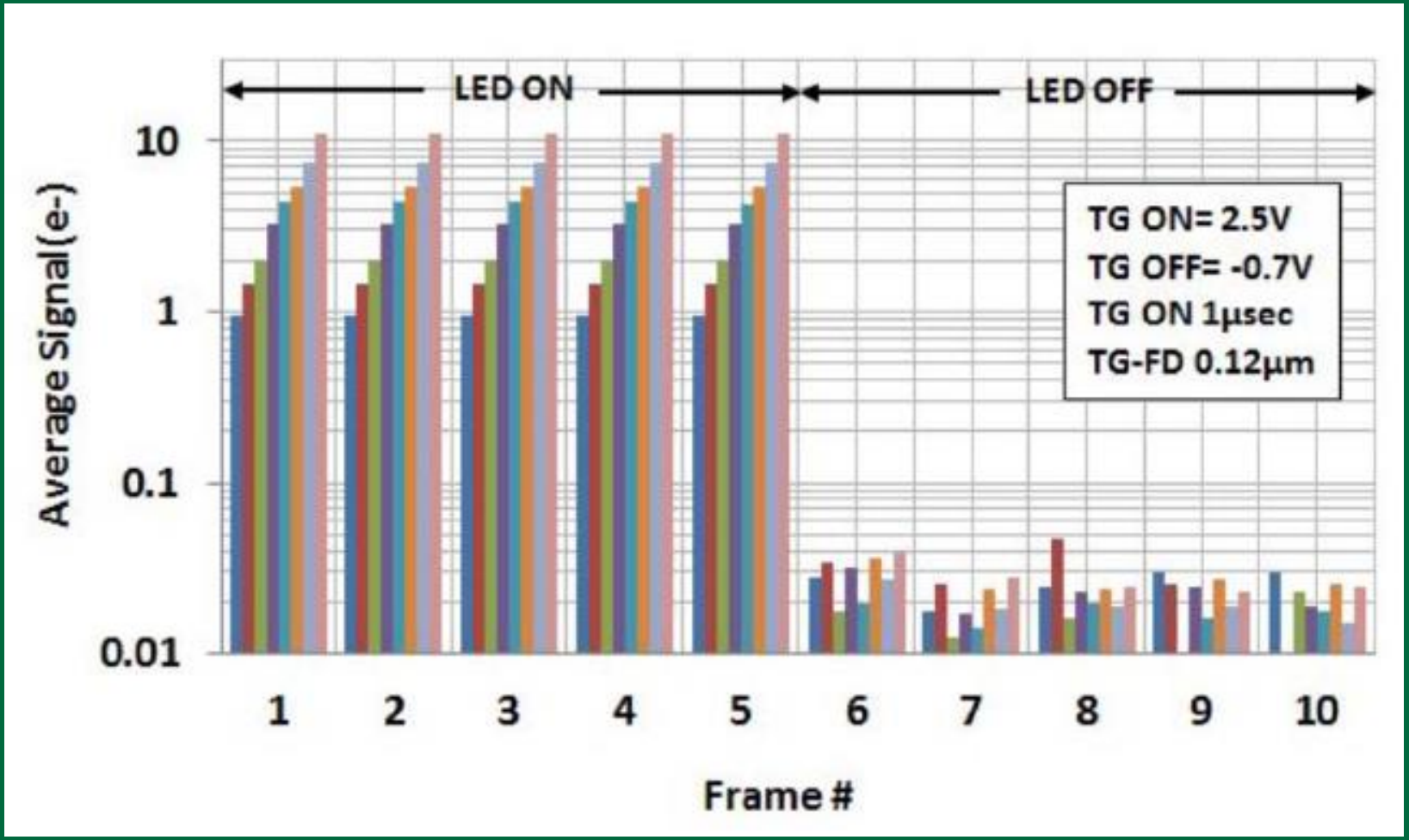




Ma, Masoodian, Wang, Fossum 2017

Lag

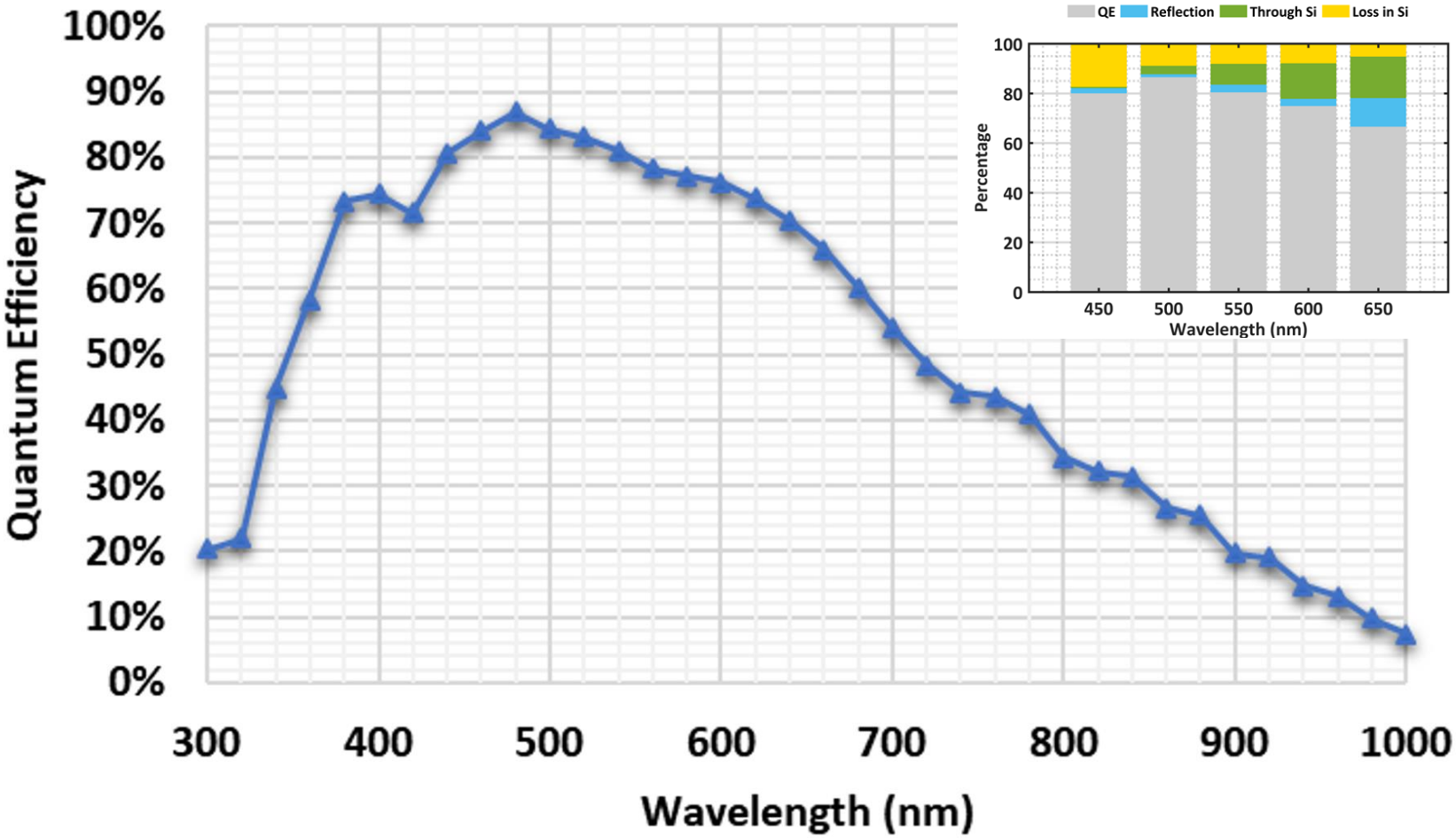
DARTMOUTH



Ma, Anzagira and Fossum IEEE JEDS 4(2) 2016

Quantum Efficiency

DARTMOUTH



QE data courtesy of Gigajot

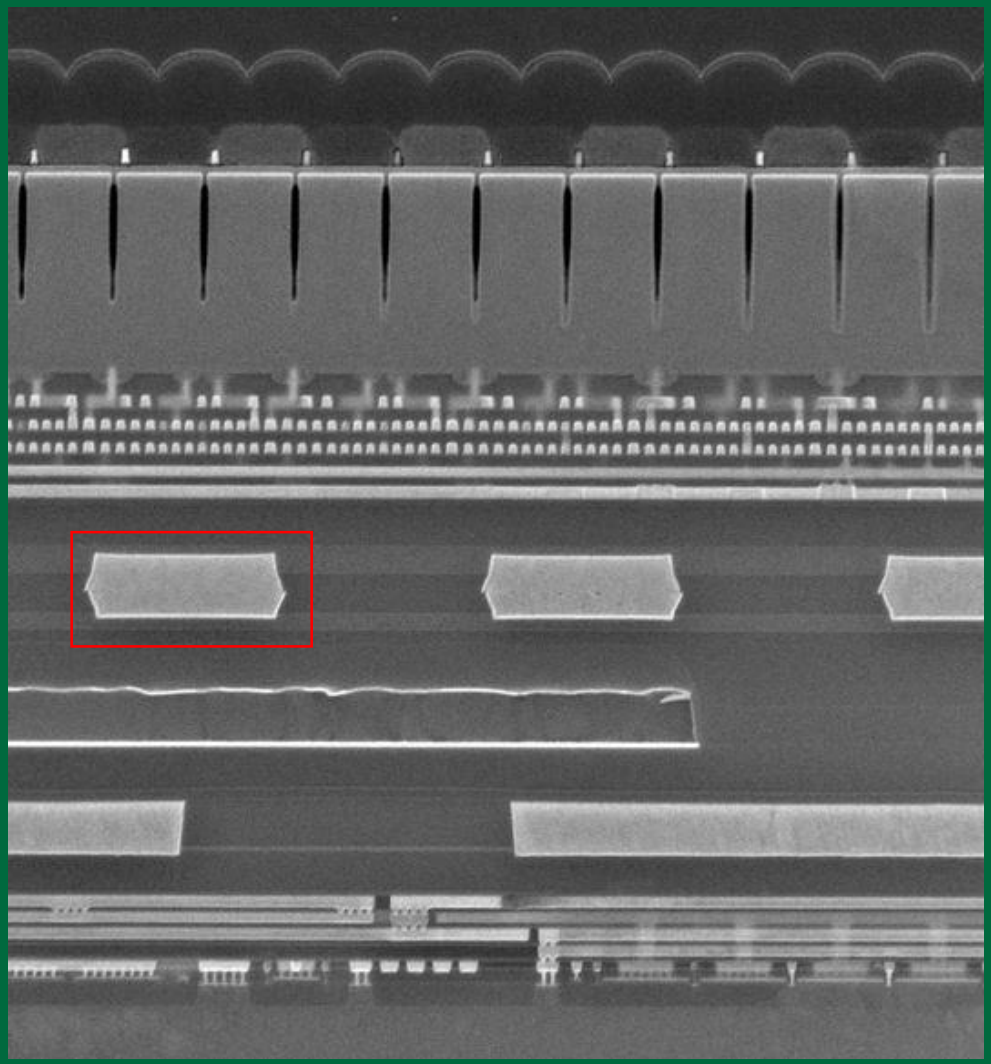
Stacked BSI CIS Using Wafer Bonding

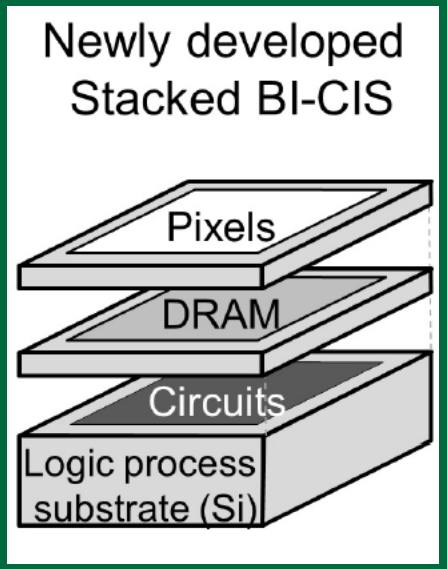
DARTMOUTH

Detector Layer

Wafer Bonding Connection

Circuit Layer





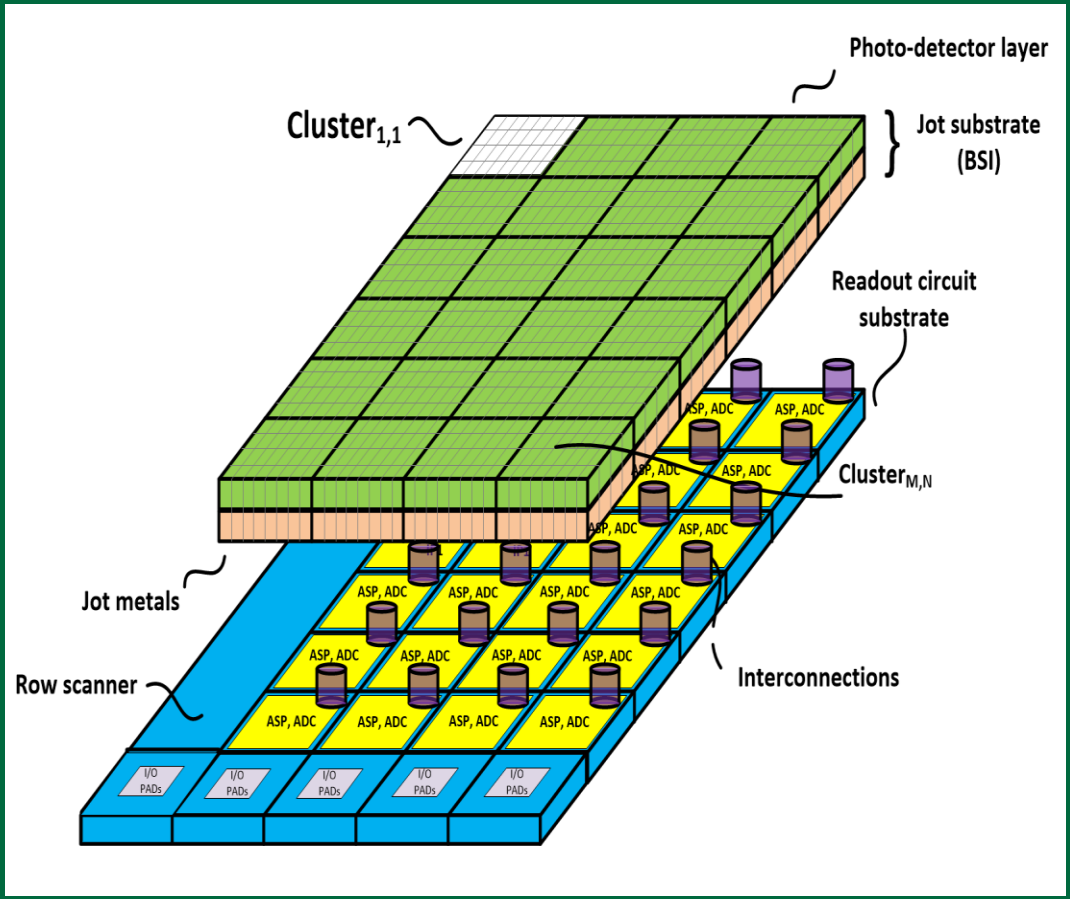
Sony 2017 ISSCC

Sony IMX260 dual pixel AF sensor from Samsung S7 teardown

3D Stacked Cluster-Parallel Readout to Increase Frame Rate and Reduce Power

DARTMOUTH

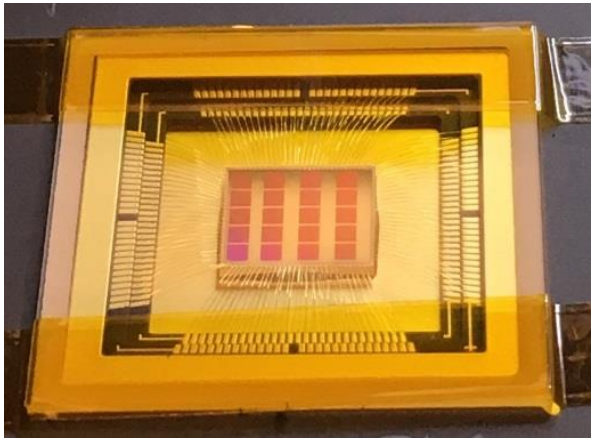
- Two or more stacked layers
- A group of jots form a cluster
- Readout circuits of a cluster of jots are located underneath cluster
- Clusters function in parallel
- Column line length is reduced, parasitics are reduced

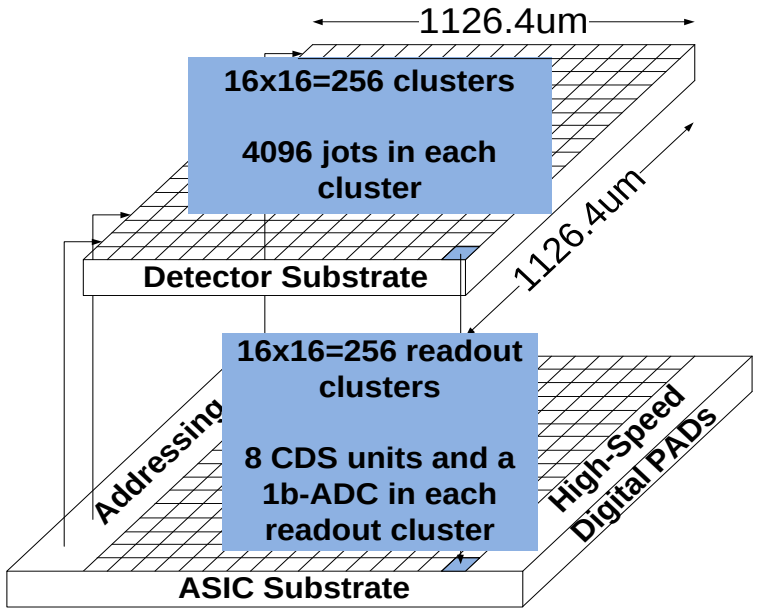


Prototype 1Mjot 1040fps QIS (1b Digital Output)

DARTMOUTH

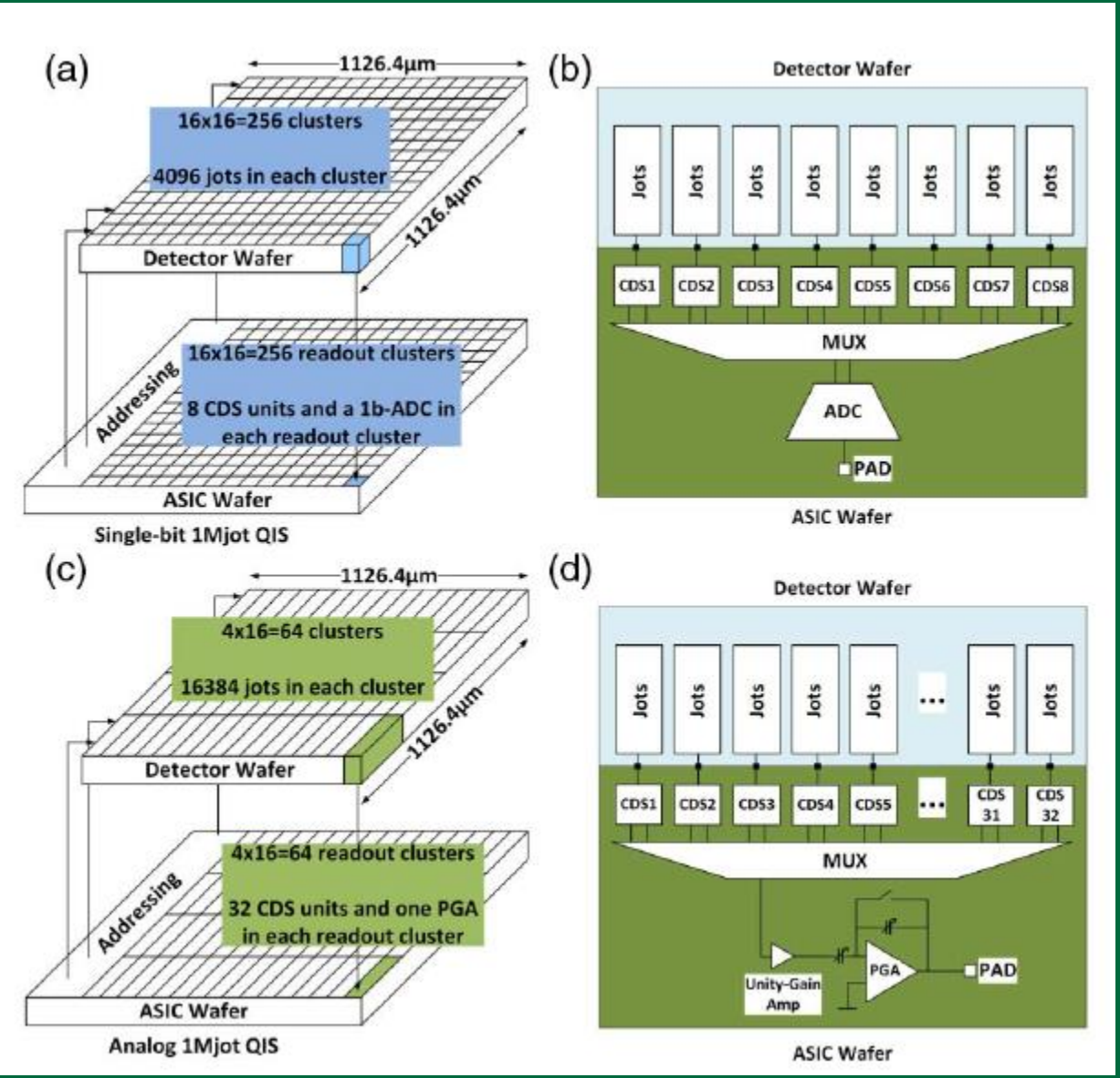
- Process technology: CMOS BSI 45nm/65nm 2-layer Stacking
- Cluster-Parallel Architecture
- Readout Variation:
  - Analog
  - Single-bit Digital
- Resolution: 1024x1024
- Jot pitch size: 1.1μm
- Jot types:
  - Tapered-reset Pump-Gate (TPG)
  - Punch-Through Reset (PTR)
  - JFET SF





Digital and Analog Readout Organization

DARTMOUTH

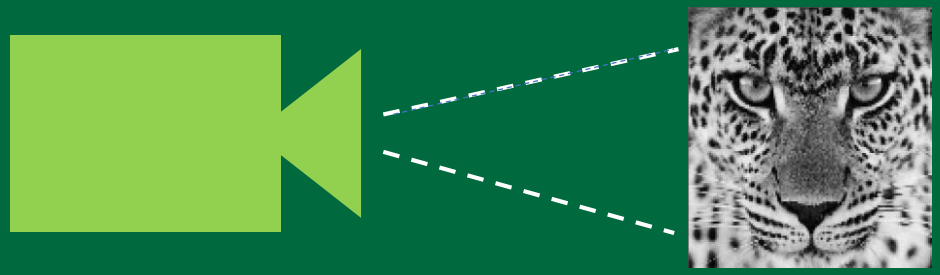


DIGITAL
High speed

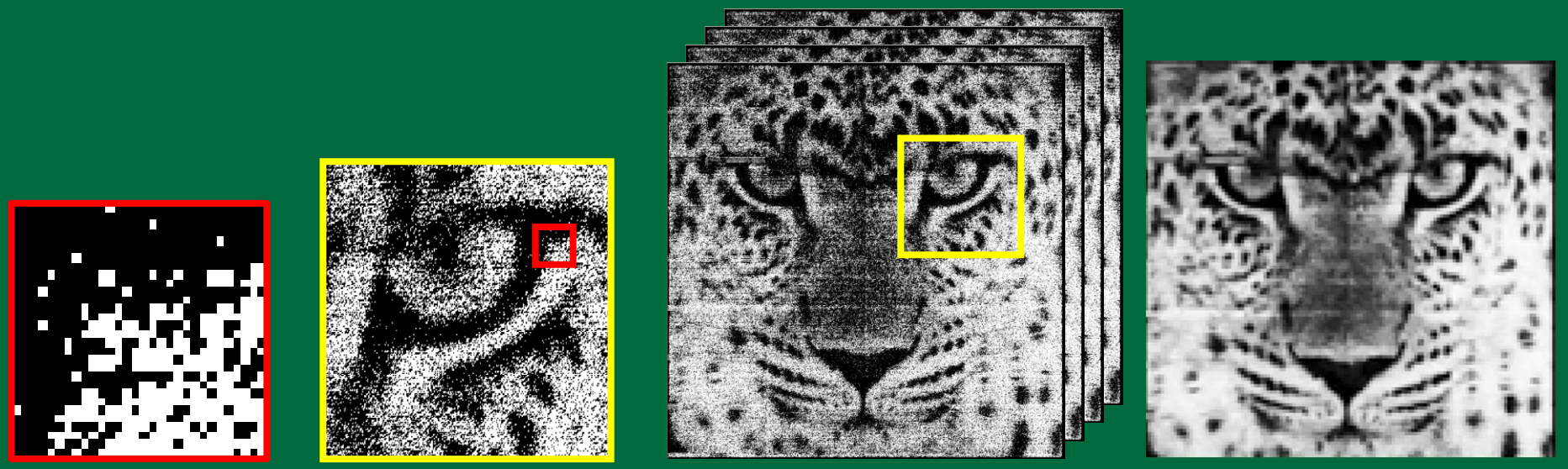
ANALOG
Low speed

1Mjot Prototype QIS Experimental Results

DARTMOUTH



Target scene



Purdue denoising

1Mpixel QIS photon-counting binary image sensor operating at 1040fps

Summary of Measured Results

Process	45nm (jot layer), 65nm (ASIC layer)
VDD	1.8V & 2.5V (Analog, digital and array), 3V & 2.2V (I/O pads)
Jot type	BSI Tapered Pump Gate 2-Way Shared RO
Jot pitch	1.1µm
BSI Fill Factor	~100%
Quantum Efficiency	79% @ 550nm
Conversion gain on column	345µV/e-
Input Referred Noise	0.22e- r.m.s.
Corresponding BER	~1%
Avg. Dark current (RT)	0.16e-/s
Equiv. Dark Count Rate (RT)	0.16Hz/jot

Equiv. PD Dead Time		<0.1%
Array		1024 (H) x 1024 (V)
Field rate		1040fps
ADC sampling rate		4MSa/s
ADC resolution		1 bit
Output data rate		32 (output pins) x 34Mb/s = 1090Mb/s
Package		PGA with 224 pins
Power	Array	2.3mW
	256 ADCs	7.5mW
	Addressing	4.1mW
	I/O pads	3.7mW
	Total	17.6mW
FOM ADC		6.9pJ/b

$$FOM = \frac{Power\ Consumption}{\#\ of\ pixels \times frame\ rate}\ [\frac{pJ}{b}]$$

Gigajot spinoff (2017)

DARTMOUTH

Dr. Saleh Masoodian

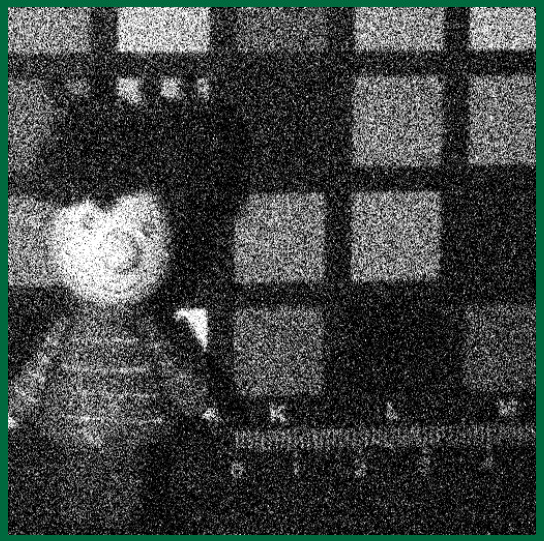
Dr. Jiaju Ma

Dr. Eric R. Fossum

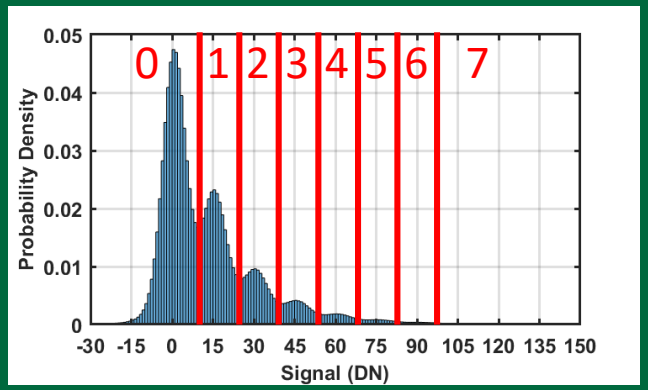
gigajot

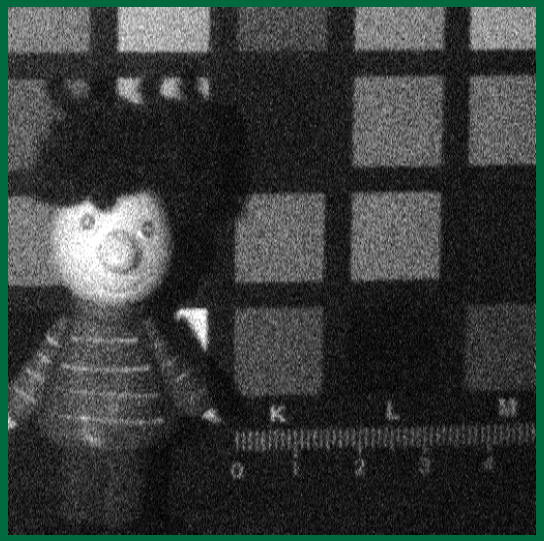
Where every photon counts®

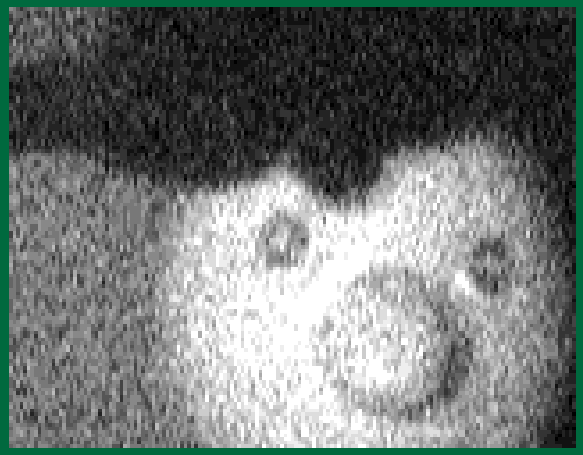
1Mpixel 3b QIS Image
Exposure of 0.87e-/pixel average



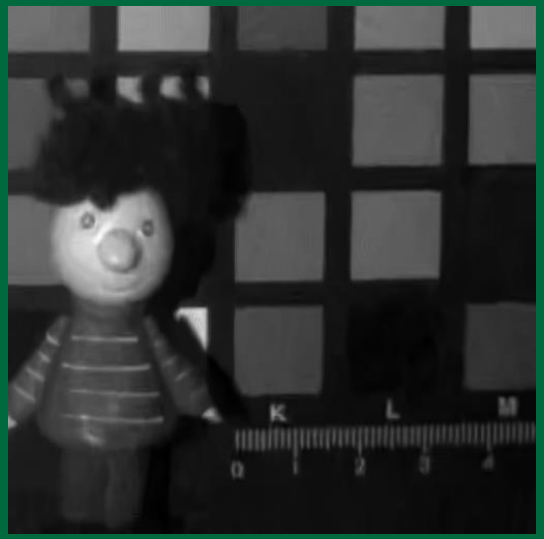
Raw image and Histogram







2x2x2 cubicle sum only



2x2x2 cubicle denoise

DARTMOUTH

Comments on VERY HIGH SPEED IMAGE SENSORS

DARTMOUTH

What is High Speed?

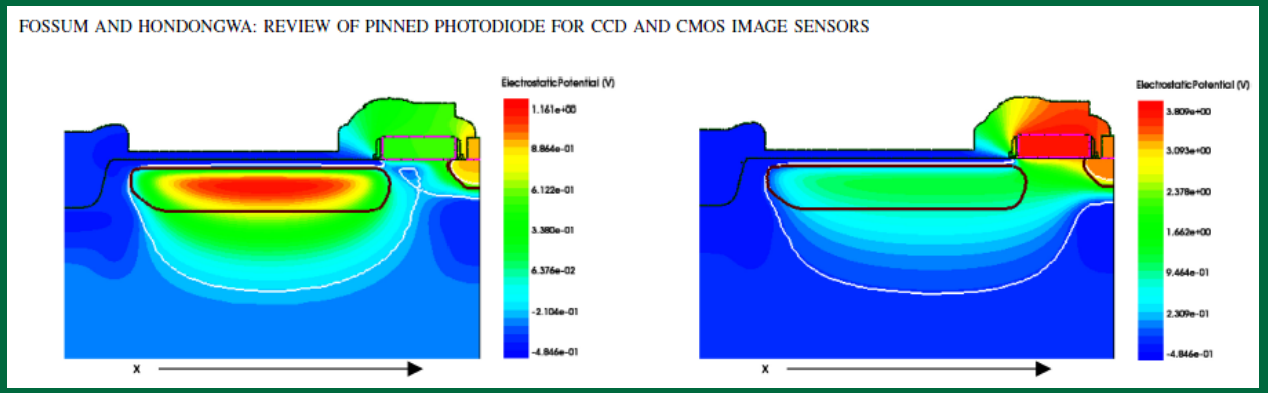
- Old Target circa 1995
- 1Mpix @ 1Kfps
- Continuous Readout
- 1Gpix/s @10b

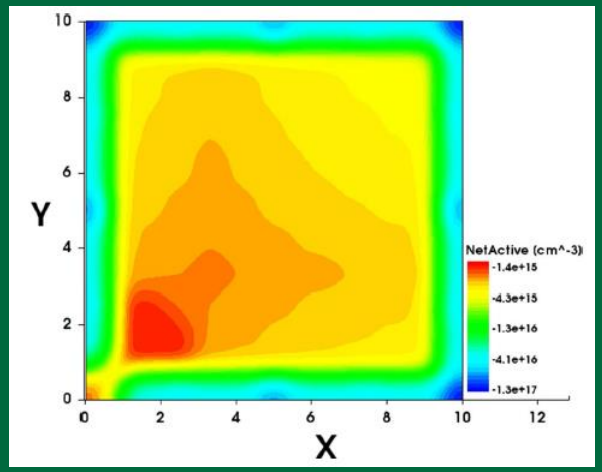
- New Target 2019 (?)
- 1Mpix @ 100K+fps
- Continuous Readout
- 100Gpix/s @ 10+b

DARTMOUTH

Issues

- Pixel Size, QE, and Charge Transport
  - Higher frame rate, fewer photons per frame
  - Thicker material, better QE, worse charge transport
  - Larger pixel, larger aperture, more photons
  - Larger pixel, longer charge transport distance
    - T ~ L^2 or at best L
  - Global Shutter vs. Rolling Shutter





DARTMOUTH

Issues

- On-chip Analog-to-Digital Conversion (ADC)
  - Chip area per ADC v. pixel pitch
  - 3D Stacking for Pixel-Parallel or Cluster-Parallel
  - How many bits? 1,2,3….16b
  - Conversion cycles – SA if resolution <= 6b
  - Power dissipation limits
    - 1Mpixel @ 1uW/pix = 1W
    - Energy/conversion related to ADC resolution

DARTMOUTH

Issues

- On-chip data reduction and off-chip readout
  - Mostly pertains to continuous mode readout
  - Power dissipation is critical, pad count is limited.
  - 1Mpixel @ 100Kframe/s = 0.1 Tpixel/sec = 1 Tb/sec for 10b ADC
  - For sparse illumination can reduce number of pixels read out.
  - Compressive sensing might help but not if data spans full space of values.
- Image data must be received, and stored at same data rate – also a problem.

DARTMOUTH

Issues

- Architecture
  - Continuous mode
    - 1Mpixel @ 100Kframe/s = 0.1Tpixel/s data rate (!)
  - Burst mode
    - 1Mpixel @ 1Gframes/s x *m* frames on-chip storage (ok)

DARTMOUTH

FA 11.3: 360x360-Element Very-High Frame-Rate Burst-Image Sensor

Walter F. Kosonocky, Guang Yang, Chao Ye, Rakesh K. Kabra, Liansheng Xie, John L. Lawrence[1], Vincent Mastrocolla[1], Frank V. Shallcross[2], Vipulkumar Patel[2]

1996 ISSCC

In-pixel transport

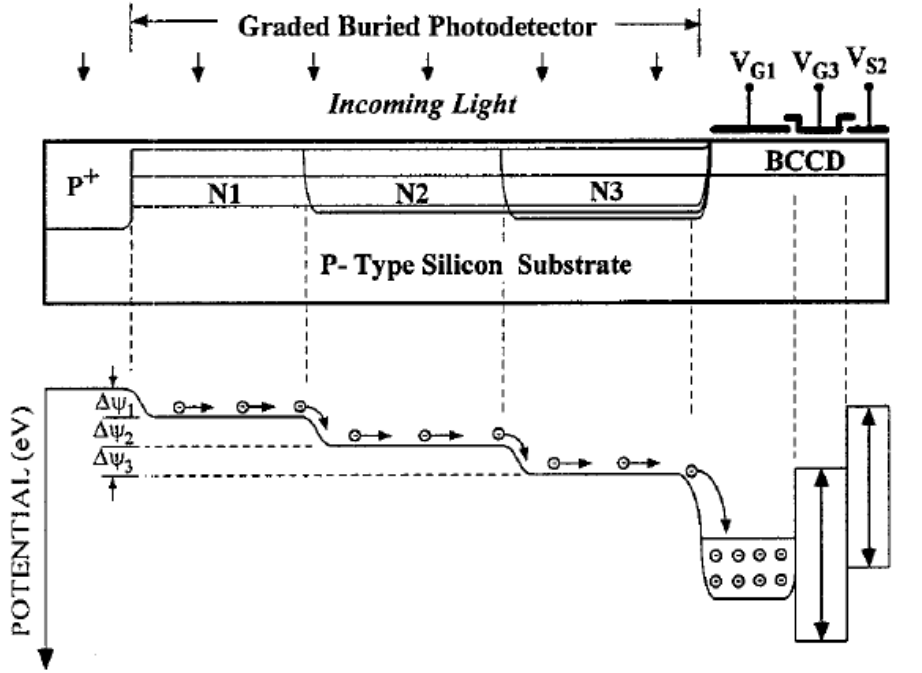


Figure 3: Photodetector construction and operation.

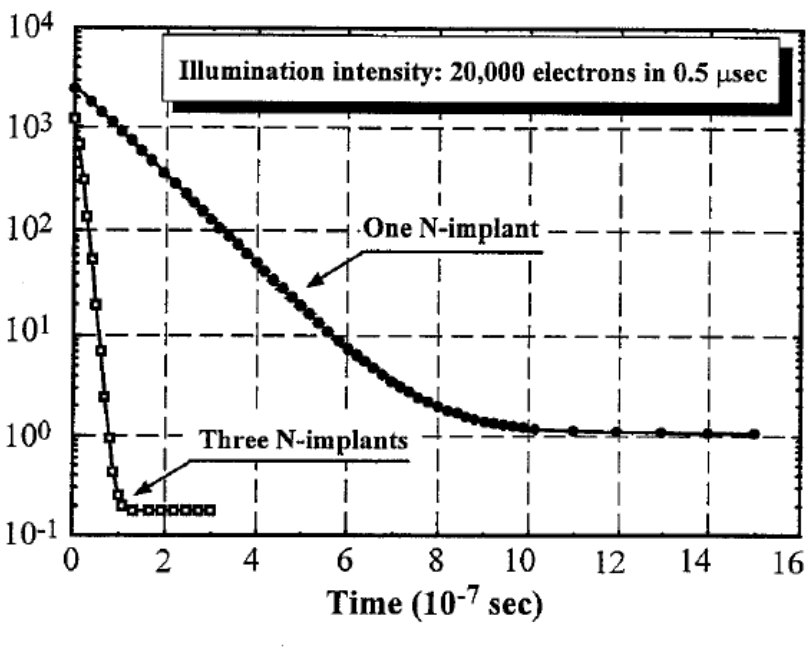


Figure 4: Charge decay in photodetector.

~18um

DARTMOUTH

FA 11.3: 360x360-Element Very-High Frame-Rate Burst-Image Sensor

Walter F. Kosonocky, Guang Yang, Chao Ye, Rakesh K. Kabra, Liansheng Xie, John L. Lawrence[1], Vincent Mastrocolla[1], Frank V. Shallcross[2], Vipulkumar Patel[2]

1996 ISSCC

Pixel data buffer storage

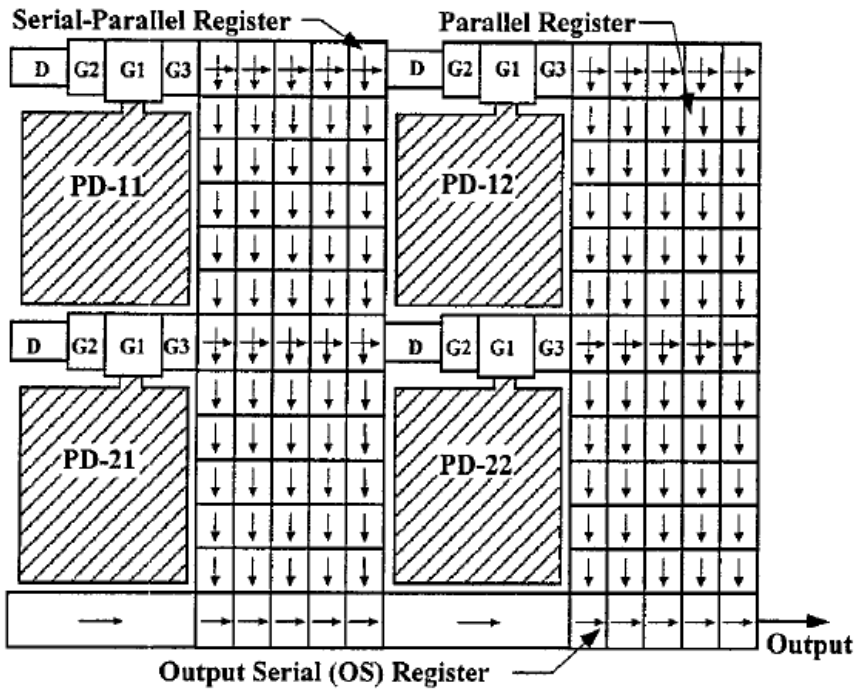


Figure 1: Architecture of 2x2 pixels.

100um

Off-chip readout architecture

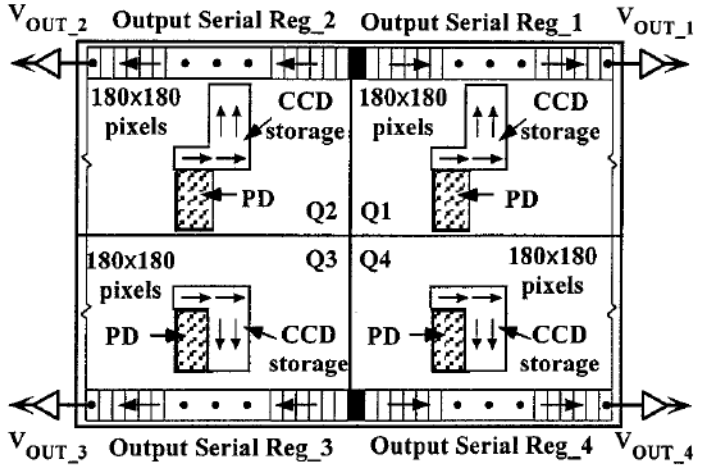
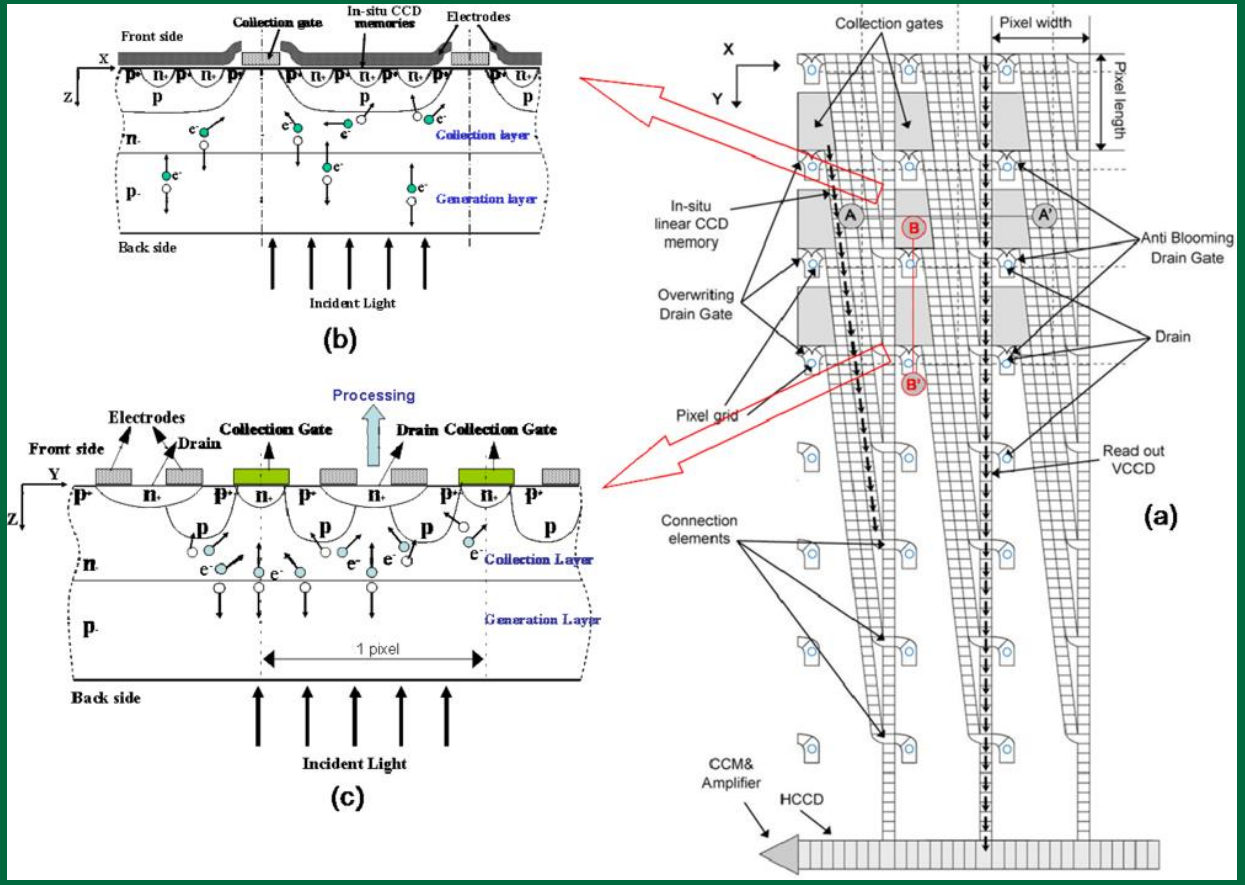


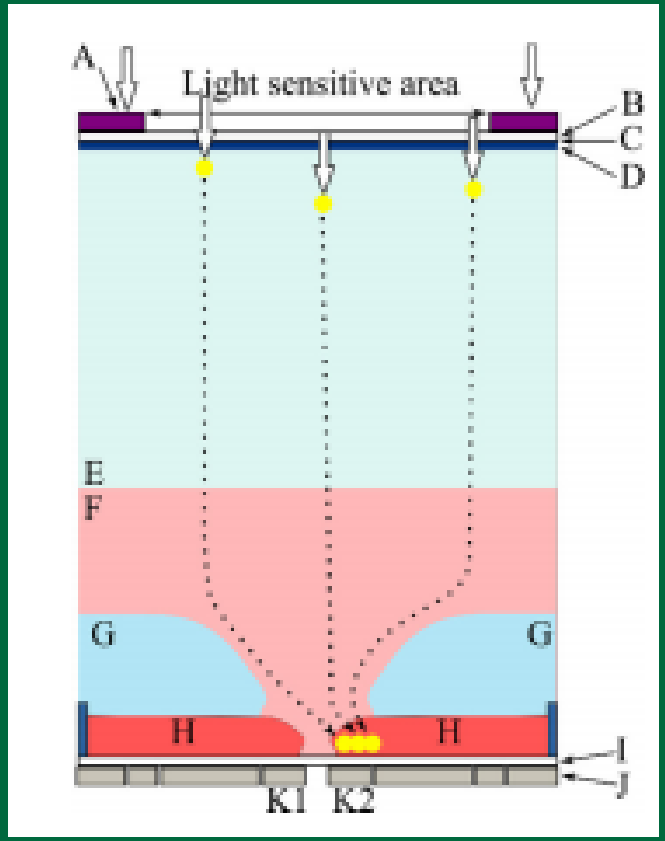
Figure 2: Imager block diagram.

Number of pixels	4x180x180
Pixel size	50x50μm²
Fill factor	13.5%
CCD elements per pixel	30
Saturation signal, Qmax	11,000e/p
Responsivity	2.2μV/e
Readout noise	9rms e/p
Dynamic range	1200:1
Maximum frame rate	8.33x10⁵ frames/s

Burst Mode
Work led by Etoh at Kinki Univ

DARTMOUTH





Continuous Readout circa 1998

DARTMOUTH

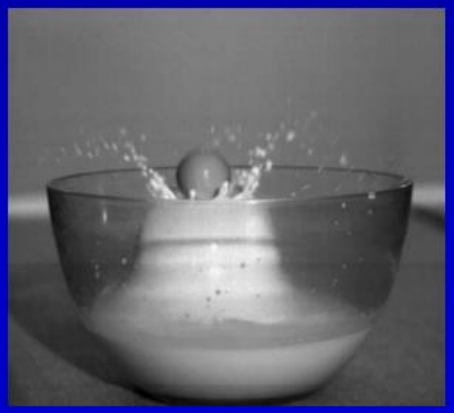
600Mpix/s

>1000Mpix/s

PB1024 HIGH SPEED SENSOR

Photobit

- 1024x1024 elements
- 10 μm x 10 μm pixel pitch
- 0.5 μm CMOS
- 1024 on-chip 8b ADCs
- 8 digital output ports (64 pins)
- Open architecture
- Power: 95 mW @ 60 fps
- Power: 270 mW @ 574 fps
- By far, world's pixel rate record of ALL image sensors (CCDs and CMOS)



Krymski, Van Blerkom, Bock, Anderson 1998

© 2000 E.R.Fossum, Photobit Corporation

Behind Every Great Digital Image

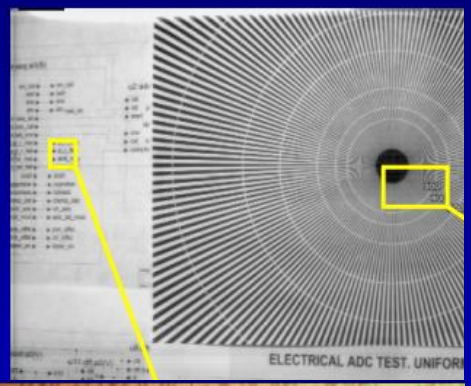
Continuous Readout circa 2000

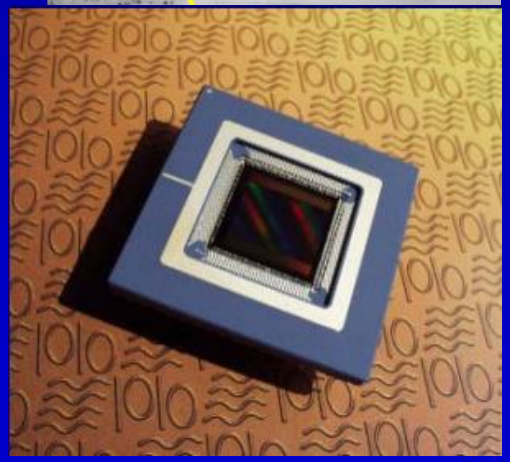
DARTMOUTH

820Mpix/s

4Mpixel, 200 fps SENSOR

Photobit





Technology	0.35um 2P3M CMOS
Format	2368x1728 (4.1Meg)
Frame rate	200 *F/s @50 MHz msclk*
Number of outputs	16x10bit
Data throughput	8.2 Gbit/s (820 Mpix/s)
Number of pins	273 (280PGA package)
Pixel pitch	7um
Shutter type	rolling
Conversion gain	>10 uV/e
Quantum Efficiency	30%
ADC , 2368 x1	10bit (9 bit accuracy)
Dark FPN, rms	2 mV
PRNU at 1/2 Sat	<2%
Temporal Noise	<100e
Power supply	3.3V
Power consumption	<800mW

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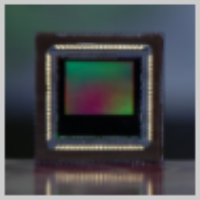
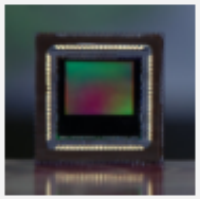
Behind Every Great Digital Image

Luxima 2018

DARTMOUTH

Alex Krymski, Lin Ping Ang

2000Mpix/s

	LUX2100	2.1 Megapixel 1952 x 1096	10.0um	4/3"	1920 x 1080 @ 1,000 FPS
	LUX1310	1.3 Megapixel 1280 X 1024	6.6um	2/3"	1280 x 1024 @ 1,070 FPS 640 x 512 @ 4,168 FPS
	LUX1310S	1.3 Megapixel 1280 X 1024	6.6um	2/3"	1280 x 1024 @ 267 FPS 640 x 512 @ 1,045 FPS

3600Mpix/s

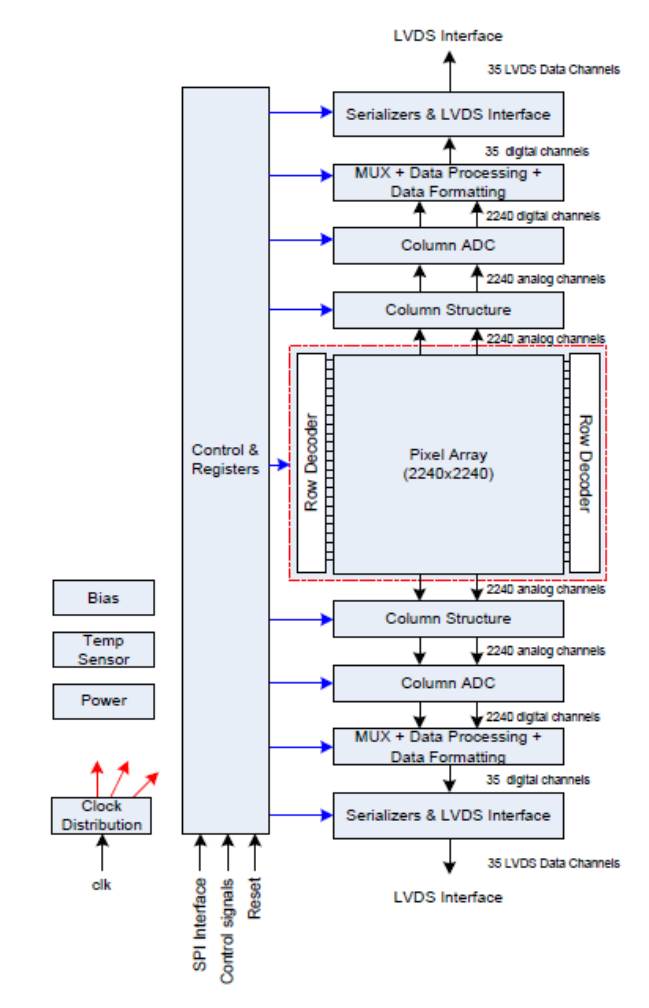
See also, CMOSIS (AMS)

CMV12000	12Mp High Speed Machine…	12.6	5.5	APS-like	Global	300	LVDS 64x 600Mbps

A 5 Megapixel, 1000fps CMOS Image Sensor with High Dynamic Range and 14-bit A/D Converters

DARTMOUTH

ON Semiconductor, Belgium



5000Mpix/s

YEAR PWR?

Table 1: key specifications

Parameter	Value	Remark
Pixel array	2240 x 2240	
Interface	Serial LVDS	
Frame Rate	1000fps	
Data Rate	70Gbps	
Main power supply	1.8 & 3.3 V	
Full well	20 ke$^-$	
Temporal noise	5 e-	
QE	>50%	@633nm
MTF	63%	@633nm
DR	72dB	Intra-scene
ADC resolution	14-bit	12-bit ENOB after rescaling

http://www.imagesensors.org/Past%20Workshops/2013%20Workshop/2013%20Papers/11-5_076-cremers.pdf

DARTMOUTH

Vision Research Phantom Camera

v2512

The Phantom v2512 is the maximum speed available with 25 Gpx of throughput. Our highly sensitive, proprietary CMOS sensor combines with easy data management to produce clear images when speed is critical.

- 25,700 fps at 1280 x 800
- Exposure Index Range:
  - Mono 32,000 – 160,000
  - Color 6,400 – 32,000
- 72, 144, or 288GB RAM
- 10Gb Ethernet and up to 8TB CineMag

~26,000Mpix/s 12b according to website

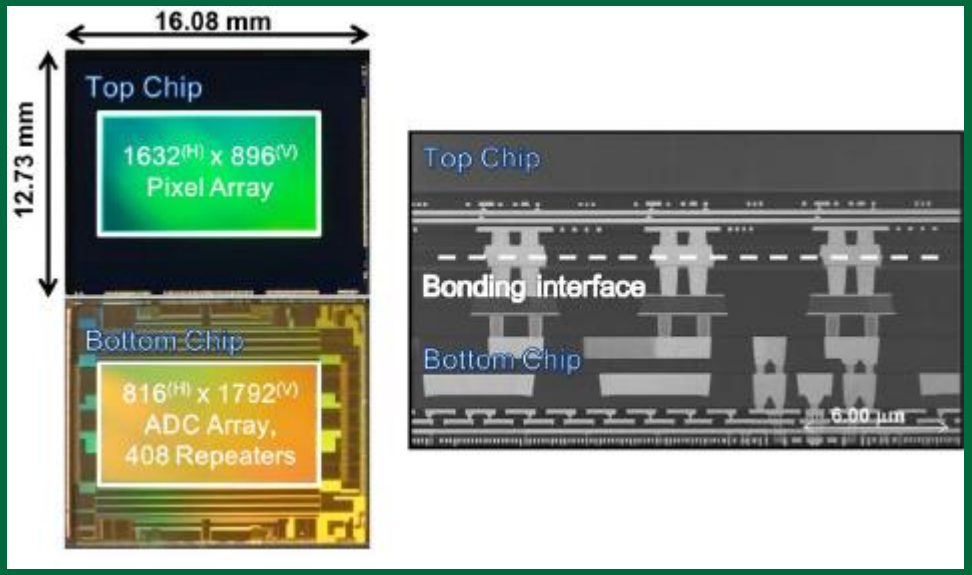
https://www.phantomhighspeed.com/products/cameras/ultrahighspeed/v2512

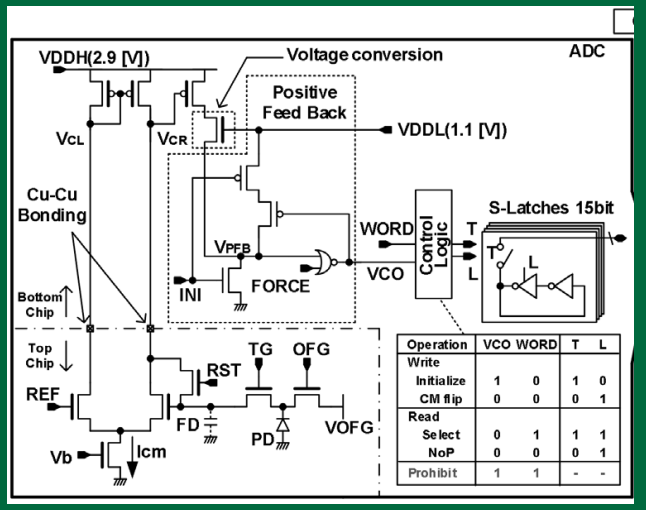
DARTMOUTH

ISSCC 2018 / SESSION 5 / IMAGE SENSORS / 5.1

5.1 A Back-Illuminated Global-Shutter CMOS Image Sensor with Pixel-Parallel 14b Subthreshold ADC

Sony





Process	CIS wafer: 90nm 1 Poly 4 Metal Layer
	Logic wafer: 65nm 1 Poly 7 Metal Layer
Supply Voltage	2.9 [V] / 1.1 [V]
Num. of pixels	$1632^{(H)}$ x $896^{(V)}$
Pixel size	6.9 [µm] x 6.9 [µm]
Output interface	16ch x 4.752 [Gbps/ch] SLVS-EC
Max frame rate	660 [fps]
Saturation signal	16.6k [e-]

~1000 Mpix/s, ~750mW, 14b

DARTMOUTH

Acknowledgments for QIS Part

- Dartmouth graduate students
  - Ma, Masoodian, Starkey, Deng, Zizza, Anzagira, Hondongwa, Song
- Faculty colleagues
  - Odame, Liu, Chan
- Rambus
  - Endsley, Stark, Guidash
- TSMC
  - Wei, Yamashita, Wang
- DARPA DETECT (a little bit)

The END